# N-Channel 30-V (D-S) MOSFET

# **Key Features:**

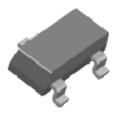
- Low r<sub>DS(on)</sub> trench technology
- · Low thermal impedance
- · Fast switching speed

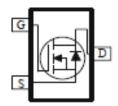
# **Typical Applications:**

- · White LED boost converters
- Automotive Systems
- Industrial DC/DC Conversion Circuits

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$r_{DS(on)}(m\Omega)$	I <sub>D</sub> (A)		
30	60 @ V <sub>GS</sub> = 4.5V	3.5		
	82 @ V <sub>GS</sub> = 2.5V	3.0		







ESD Protected

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage		$V_{DS}$	30	V	
Gate-Source Voltage		$V_{GS}$	±12	V	
Continuous Drain Coursent®	T <sub>A</sub> =25°C		3.5		
Continuous Drain Current <sup>a</sup>	T <sub>A</sub> =70°C	l <sub>D</sub>	2.8	Α	
ulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	16		
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	1.9	Α	
Device Discipation a	T <sub>A</sub> =25°C	D	1.3	W	
Power Dissipation <sup>a</sup>	T <sub>A</sub> =70°C	P <sub>D</sub>	0.8	VV	
Operating Junction and Storage Temperature Range	-	$T_J$ , $T_{stg}$	-55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Maximum	Units		
Maximum Junction-to-Ambient <sup>a</sup>	t <= 10 sec	$R_{\theta JA}$	100	°C/W		
Maximum Junction-to-Ambient	Steady State		166			

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### Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

### **Electrical Characteristics**

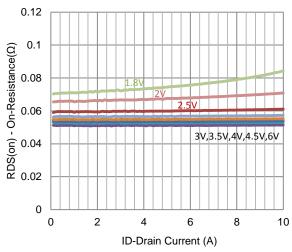
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \text{ uA}$	0.4			V
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			±10	uA
Zero Gate Voltage Drain Current		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
Zero Gate Voltage Brain Current	I <sub>DSS</sub>	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			25	
On-State Drain Current	I <sub>D(on)</sub>	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	6			Α
Drain-Source On-Resistance	r	$V_{GS} = 4.5 \text{ V}, I_D = 2.8 \text{ A}$			60	mΩ
	r <sub>DS(on)</sub>	$V_{GS} = 2.5 \text{ V}, I_D = 2.4 \text{ A}$			82	
Forward Transconductance	g <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_{D} = 2.8 \text{ A}$		10		S
Diode Forward Voltage	$V_{SD}$	$I_{S} = 1 \text{ A}, V_{GS} = 0 \text{ V}$		0.7		V
		Dynamic				
Total Gate Charge	$Q_g$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V},$		6.1		nC
Gate-Source Charge	$Q_{gs}$	$I_{DS} = 13 \text{ V}, \text{ V}_{GS} = 4.3 \text{ V},$ $I_{D} = 2.8 \text{ A}$		0.8		
Gate-Drain Charge	$Q_gd$	1D = 2.0 A		2		
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DS} = 15 \text{ V}, R_1 = 5.4 \Omega,$		6		
Rise Time	t <sub>r</sub>	$I_{DS} = 13 \text{ V}, K_L - 3.4 \Omega,$ $I_D = 2.8 \text{ A},$		17		ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{GEN} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$		49		
Fall Time	t <sub>f</sub>	V GEN - 4.5 V, T GEN - 0 12		22		
Input Capacitance	C <sub>iss</sub>			429		
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		51		pF
Reverse Transfer Capacitance	$C_{rss}$	1		47		

#### Notes

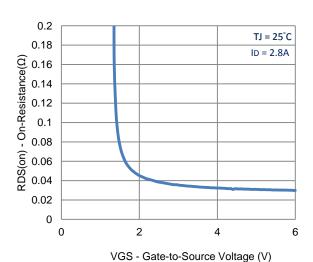
- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

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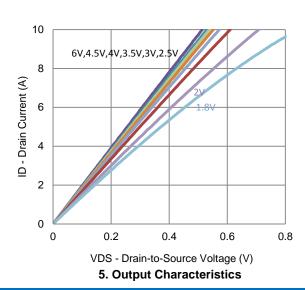
## **Typical Electrical Characteristics**



#### 1. On-Resistance vs. Drain Current



3. On-Resistance vs. Gate-to-Source Voltage



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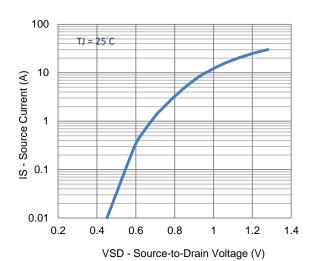
TJ = 25°C

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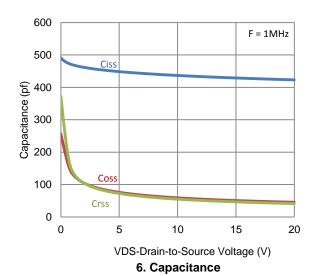
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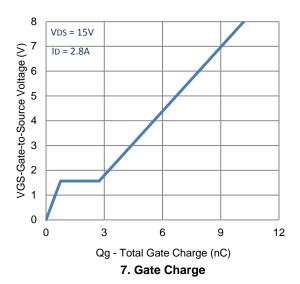
2. Transfer Characteristics

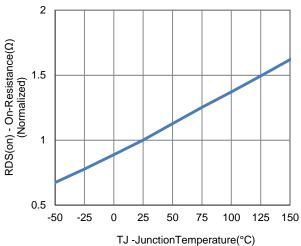


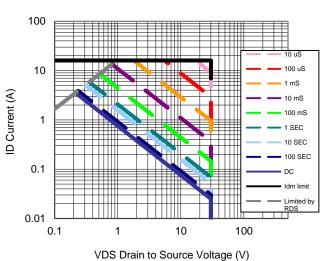
4. Drain-to-Source Forward Voltage

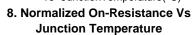


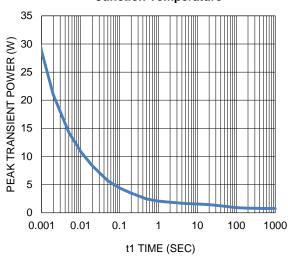
## **Typical Electrical Characteristics**





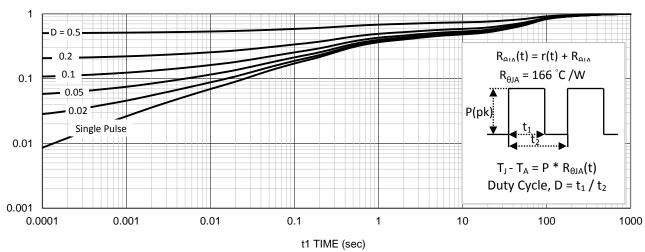






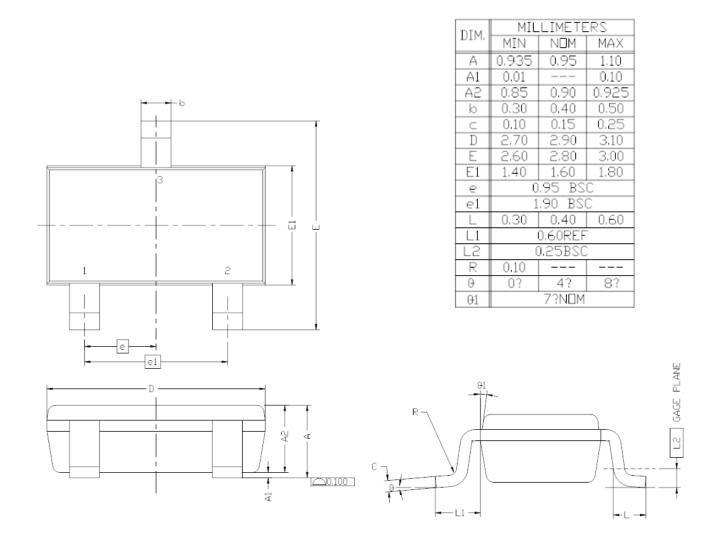
9. Safe Operating Area

10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient

### **Package Information**



#### Note:

- All Dimension Are In mm.
- Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- 5. Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.