



4GB, 8GB, 16GB, 32GB: e-MMC
Features

e-MMC™ Memory

N2M400FDB311A3C[E/F], N2M400GDB321A3C[E/F]

N2M400HDB321A3C[E/F], N2M400JDB341A3C[E/F]

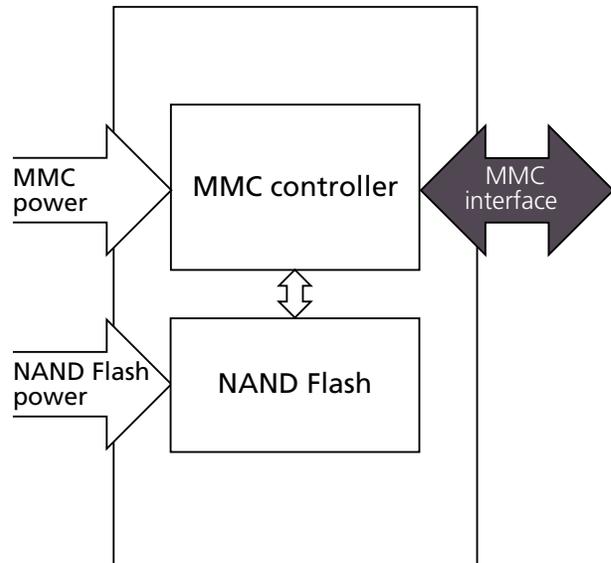
Features

- MultiMediaCard (MMC) controller and NAND Flash
- 100-ball LBGGA (RoHS 6/6-compliant)
- V_{CC} : 2.7–3.6V
- V_{CCQ} (dual voltage): 1.65–1.95V; 2.7–3.6V
- Temperature ranges
 - Industrial temperature: -40°C to $+85^{\circ}\text{C}$
 - Storage temperature: -40°C to $+85^{\circ}\text{C}$
- Typical current consumption
 - Standby current: $70\mu\text{A}$ (4GB, 8GB); $90\mu\text{A}$ (16GB, 32GB)
 - Active current (RMS): 70mA (4GB, 8GB); 90mA (16GB, 32GB)

MMC-Specific Features

- JEDEC/MMC standard version 4.41-compliant (JEDEC Standard No. 84-A441) – SPI mode not supported (see www.jedec.org/sites/default/files/docs/JESD84-A441.pdf)
 - Advanced 11-signal interface
 - x1, x4, and x8 I/Os, selectable by host
 - MMC mode operation
 - Command classes: class 0 (basic); class 2 (block read); class 4 (block write); class 5 (erase); class 6 (write protection); class 7 (lock card)
 - MMC*plus*™ and MMC*mobile*™ protocols
 - Temporary write protection
 - 52 MHz clock speed (MAX)
 - Boot operation (high-speed boot)
 - Sleep mode
 - Replay-protected memory block (RPMB)
 - Secure erase and trim
 - Hardware reset signal
 - Multiple partitions with enhanced attribute
 - Permanent and power-on write protection
 - Double data rate (DDR) function
 - High-priority interrupt (HPI)

Figure 1: Micron e-MMC Device



MMC-Specific Features (Continued)

- Enhanced reliable write
- Configurable reliability settings
- Background operation
- Fully enhanced configurable
- Backward-compatible with previous MMC modes
- ECC and block management implemented



4GB, 8GB, 16GB, 32GB: e-MMC Features

e-MMC Performance

Table 1: MLC Partition Performance

| Condition | Part Number | | Units |
|------------------|--|--|-------|
| | N2M400FDB311A3C[E/F] N2M400GDB321A3C[E/F] | N2M400HDB321A3C[E/F] N2M400JDB341A3C[E/F] | |
| Sequential write | 13.5 | 20 | MB/s |
| Sequential read | 44 | 44 | MB/s |

Note: 1. Sequential access of 1MB chunk. Additional performance data, such as power consumption or timing for different device modes, will be provided in a separate document upon customer request.

Ordering Information

Table 2: Ordering Information

| Base Part Number | Density | Package | NAND Flash Type | Shipping Media |
|----------------------|---------|--|---------------------|----------------|
| N2M400FDB311A3C[E/F] | 4GB | 100-ball LBGA 14.0mm x 18.0mm x 1.4mm | 1 x 32Gb, MLC, 25nm | Tray |
| | | | | Tape and reel |
| N2M400GDB321A3C[E/F] | 8GB | 100-ball LBGA 14.0mm x 18.0mm x 1.4mm | 2 x 32Gb, MLC, 25nm | Tray |
| | | | | Tape and reel |
| N2M400HDB321A3C[E/F] | 16GB | 100-ball LBGA 14.0mm x 18.0mm x 1.4mm | 2 x 64Gb, MLC, 25nm | Tray |
| | | | | Tape and reel |
| N2M400JDB341A3C[E/F] | 32GB | 100-ball LBGA 14.0mm x 18.0mm x 1.4mm | 4 x 64Gb, MLC, 25nm | Tray |
| | | | | Tape and reel |

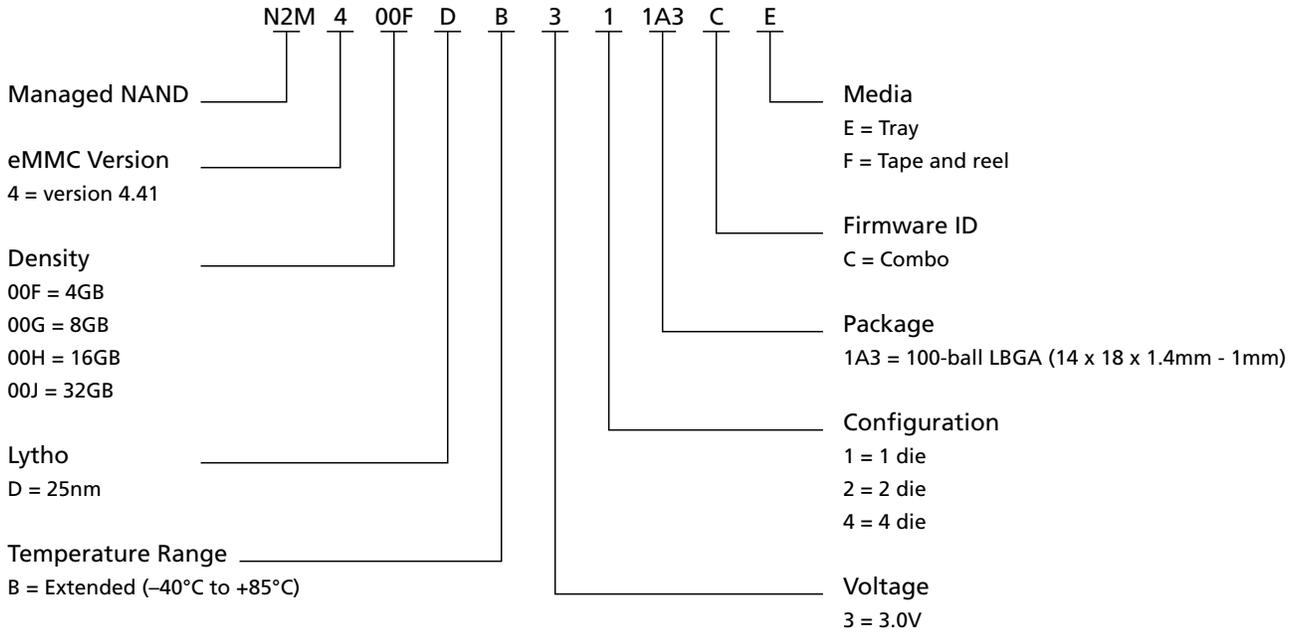


4GB, 8GB, 16GB, 32GB: e-MMC Features

Part Numbering Information

Micron® e-MMC memory devices are available in different configurations and densities. Verify valid part numbers by using Micron’s part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 2: Marketing Part Number Chart



Note: 1. Not all combinations are necessarily available. For a list of available devices or for further information on any aspect of these products, please contact your nearest Micron sales office.



4GB, 8GB, 16GB, 32GB: e-MMC General Description

General Description

Micron *e*-MMC is a communication and mass data storage device that includes a Multi-MediaCard (MMC) interface, a NAND Flash component, and a controller on an advanced 11-signal bus, which is compliant with the MMC system specification. Its cost per bit, small package sizes, and high reliability make it an ideal choice for industrial applications like infrastructure and networking equipment, PC and servers, a variety of other industrial products.

The nonvolatile *e*-MMC draws no power to maintain stored data, delivers high performance across a wide range of operating temperatures, and resists shock and vibration disruption.



Signal Descriptions

Table 3: Signal Descriptions

| Symbol | Type | Description |
|-------------------------------|--------|--|
| CLK | Input | Clock: Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency. |
| RST_n | Input | Reset: The RST_n signal is used by the host for resetting the device, moving the device to the pre-idle state. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it. |
| CMD | I/O | Command: This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode (see Operating Modes). Commands are sent from the MMC host to the device, and responses are sent from the device to the host. |
| DAT[7:0] | I/O | Data I/O: These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer either using DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode). e-MMC includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT[3:1] lines. Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines. |
| V _{CC} | Supply | V _{CC} : NAND interface (I/F) I/O and NAND Flash power supply. |
| V _{CCQ} | Supply | V _{CCQ} : e-MMC controller core and e-MMC I/F I/O power supply. |
| V _{SS} ¹ | Supply | V _{SS} : NAND I/F I/O and NAND Flash ground connection. |
| V _{SSQ} ¹ | Supply | V _{SSQ} : e-MMC controller core and e-MMC I/F ground connection. |
| V _{DDI} | | Internal voltage node: At least a 0.1µF capacitor is required to connect V _{DDI} to ground. A 1µF capacitor is recommended. Do not tie to supply voltage or ground. |
| NC | – | No connect: No internal connection is present. |
| RFU | – | Reserved for future use: No internal connection is present. Leave it floating externally. |

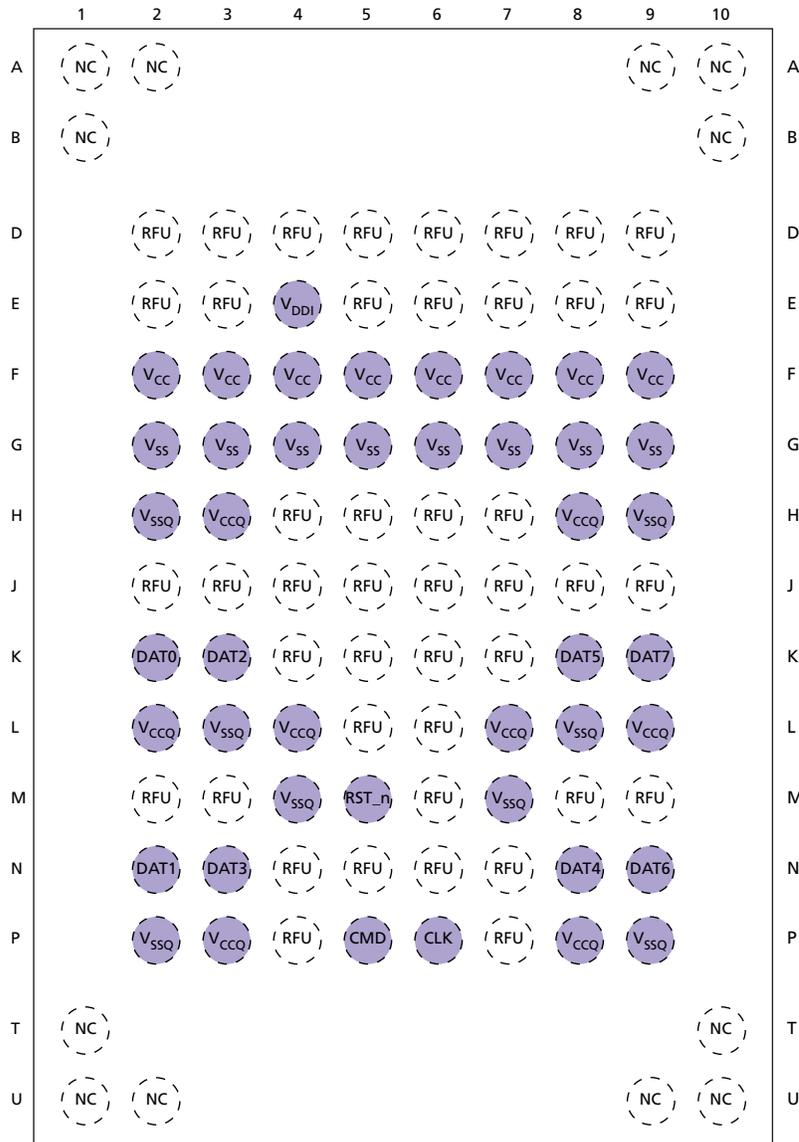
Note: 1. V_{SS} and V_{SSQ} are connected internally.



**4GB, 8GB, 16GB, 32GB: e-MMC
100-Ball Signal Assignments**

100-Ball Signal Assignments

Figure 3: 100-Ball LFBGA (Top View, Ball Down)



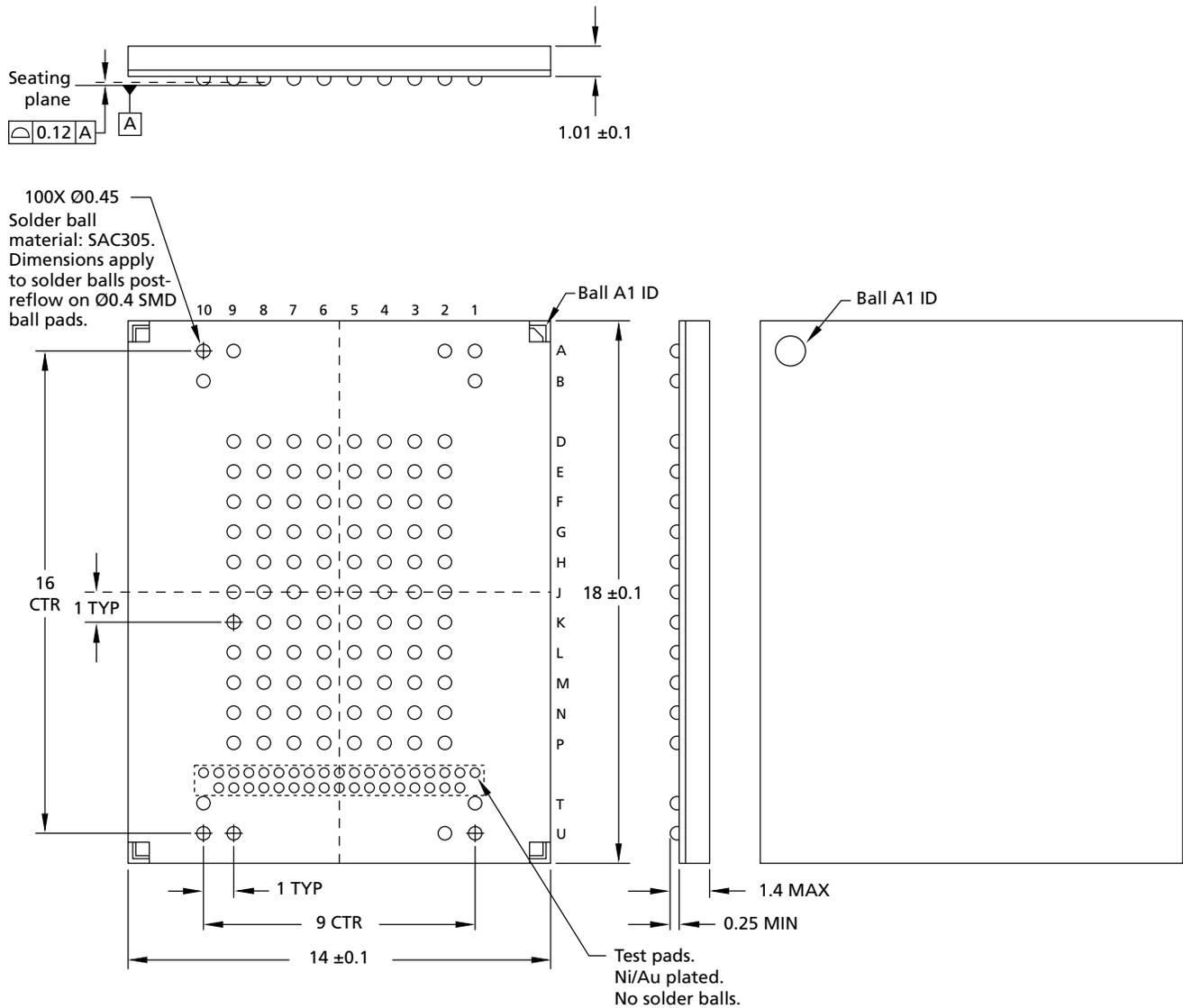
Note: 1. Connect a 1µF decoupling capacitor from V_{DD1} to ground.



**4GB, 8GB, 16GB, 32GB: e-MMC
Package Dimensions**

Package Dimensions

Figure 4: 100-Ball LPGA – 14.0mm x 18.00mm x 1.4mm (Package Code 1A3)

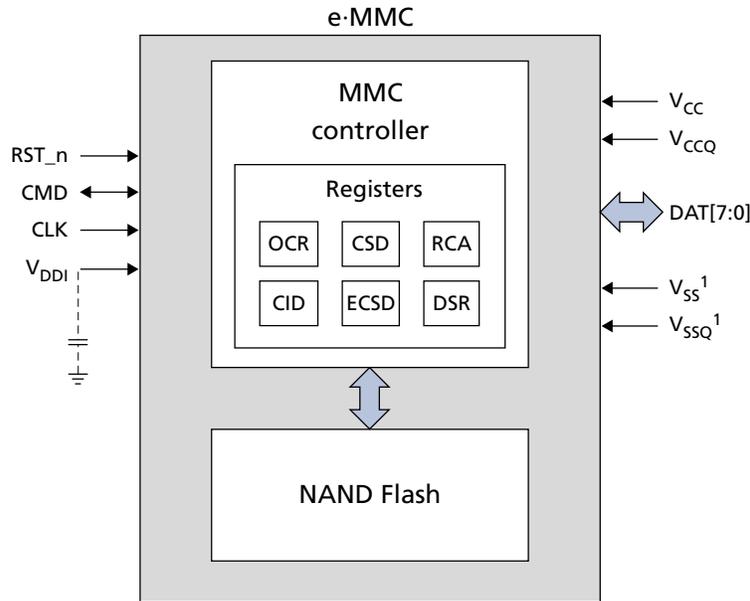


Note: 1. Dimensions are in millimeters.



Architecture

Figure 5: e-MMC Functional Block Diagram



Note: 1. V_{SS} and V_{SSQ} are internally connected.

MMC Protocol Independent of NAND Flash Technology

The MMC specification defines the communication protocol between a host and a device. The protocol is independent of the NAND Flash features included in the device. The device has an intelligent on-board controller that manages the MMC communication protocol.

The controller also handles block management functions such as logical block allocation and wear leveling. These management functions require complex algorithms and depend entirely on NAND Flash technology (generation or memory cell type).

The device handles these management functions internally, making them invisible to the host processor.

Defect and Error Management

Micron e-MMC incorporates advanced technology for defect and error management. If a defective block is identified, the device completely replaces the defective block with one of the spare blocks. This process is invisible to the host and does not affect data space allocated for the user.

The device also includes a built-in error correction code (ECC) algorithm to ensure that data integrity is maintained.

To make the best use of these advanced technologies and ensure proper data loading and storage over the life of the device, the host must exercise the following precautions:

- Check the status after WRITE, READ, and ERASE operations.
- Avoid power-down during WRITE and ERASE operations.



4GB, 8GB, 16GB, 32GB: e-MMC CID Register

CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by e-MMC protocol. Each device is created with a unique identification number.

Table 4: CID Register Field Parameters

| Name | Field | Width | CID Bits | CID Value |
|-----------------------|-------|-------|-----------|--------------------------------------|
| Manufacturer ID | MID | 8 | [127:120] | Fh |
| Reserved | – | 6 | [119:114] | – |
| Card/BGA | CBX | 2 | [113:112] | 01h |
| OEM/application ID | OID | 8 | [111:104] | – |
| Product name | PNM | 48 | [103:56] | MMC04G MMC08G MMC16G MMC32G |
| Product revision | PRV | 8 | [55:48] | – |
| Product serial number | PSN | 32 | [47:16] | – |
| Manufacturing date | MDT | 8 | [15:8] | – |
| CRC7 checksum | CRC | 7 | [7:1] | – |
| Not used; always 1 | – | 1 | 0 | – |


**4GB, 8GB, 16GB, 32GB: e-MMC
CSD Register**

CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

Table 5: CSD Register Field Parameters

| Name | Field | Width | Cell Type ¹ | CSD Bits | CSD Value |
|--|--------------------|----------------------|------------------------|-----------|-----------|
| CSD structure | CSD_STRUCTURE | 2 | R | [127:126] | 03h |
| System specification version | SPEC_VERS | 4 | R | [125:122] | 4h |
| Reserved ² | – | 2 | TBD | [121:120] | – |
| Data read access time 1 | TAAC | 8 | R | [119:112] | 4Fh |
| Data read access time 2 in CLK cycles (NSAC × 100) | NSAC | 8 | R | [111:104] | 01h |
| Maximum bus clock frequency | TRAN_SPEED | 8 | R | [103:96] | 32h |
| Card command classes | CCC | 12 | R | [95:84] | 0F5h |
| Maximum read data block length | READ_BL_LEN | 4 | R | [83:80] | 9h |
| Partial blocks for reads supported | READ_BL_PARTIAL | 1 | R | 79 | 0h |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | R | 78 | 0h |
| Read block misalignment | READ_BLK_MISALIGN | 77 | R | 77 | 0h |
| DS register implemented | DSR_IMP | 1 | R | 76 | 1h |
| Reserved | – | 2 | R | [75:74] | – |
| Device size | C_SIZE | 12 | R | [73:62] | FFFh |
| Maximum read current at V _{DD,min} | VDD_R_CURR_MIN | 3 | R | [61:59] | 7h |
| Maximum read current at V _{DD,max} | VDD_R_CURR_MAX | 3 | R | [58:56] | 7h |
| Maximum write current at V _{DD,min} | VDD_W_CURR_MIN | 3 | R | [55:53] | 7h |
| Maximum write current at V _{DD,max} | VDD_W_CURR_MAX | 3 | R | [52:50] | 7h |
| Device size multiplier | C_SIZE_MULT | 3 | R | [49:47] | 7h |
| Erase group size | ERASE_GRP_SIZE | 5 | R | [46:42] | 1Fh |
| Erase group size multiplier | ERASE_GRP_MULT | 5 | R | [41:37] | 1Fh |
| Write protect group size | WP_GRP_SIZE | N2M400FDB311A3C[E/F] | R | [36:32] | 07h |
| | | N2M400GDB321A3C[E/F] | | | 0Fh |
| | | N2M400HDB321A3C[E/F] | | | 1Fh |
| | | N2M400JDB341A3C[E/F] | | | |
| Write protect group enable | WP_GRP_ENABLE | 1 | R | 31 | 1h |
| Manufacturer default ECC | DEFAULT_ECC | 2 | R | [30:29] | 0h |
| rite-speed factor | R2W_FACTOR | 3 | R | [28:26] | 2h |


**4GB, 8GB, 16GB, 32GB: e-MMC
CSD Register**
Table 5: CSD Register Field Parameters (Continued)

| Name | Field | Width | Cell Type ¹ | CSD Bits | CSD Value |
|-------------------------------------|--------------------|-------|------------------------|----------|-----------|
| Maximum write data block length | WRITE_BL_LEN | 4 | R | [25:22] | 9h |
| Partial blocks for writes supported | WRITE_BL_PARTIAL | 1 | R | 21 | 0h |
| Reserved | – | 4 | R | [20:17] | – |
| Content protection application | CONTENT_PROT_APP | 1 | R | 16 | 0h |
| File-format group | FILE_FORMAT_GRP | 1 | R/W | 15 | 0h |
| Copy flag (OTP) | COPY | 1 | R/W | 14 | 0h |
| Permanent write protection | PERM_WRITE_PROTECT | 1 | R/W | 13 | 0h |
| Temporary write protection | TMP_WRITE_PROTECT | 1 | R/W/E | 12 | 0h |
| File format | FILE_FORMAT | 2 | R/W | [11:10] | 0h |
| ECC | ECC | 2 | R/W/E | [9:8] | 0h |
| CRC | CRC | 7 | R/W/E | [7:1] | – |
| Not used; always 1 | – | 1 | – | 0 | 1h |

Notes: 1. R = Read-only

R/W = One-time programmable and readable

R/W/E = Multiple writable with value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable

TBD = To be determined

2. Reserved bits should be read as 0.



4GB, 8GB, 16GB, 32GB: e-MMC ECSD Register

ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

Table 6: ECSD Register Field Parameters

| Name | Field | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECSD Value | |
|---|---------------------------|---|------------------------|------------|------------|-----|
| Properties Segment | | | | | | |
| Reserved ² | – | 7 | – | [511:505] | – | |
| Supported command sets | S_CMD_SET | 1 | R | 504 | 1h | |
| HPI features | HPI_FEATURES | 1 | R | 503 | 3h | |
| Background operations support | BKOPS_SUPPORT | 1 | R | 502 | 1h | |
| Reserved | – | 255 | – | [501:247] | – | |
| Background operations status | BKOPS_STATUS | 1 | R | 246 | 0h | |
| Number of correctly programmed sectors | CORRECTLY_PRG_SECTORS_NUM | 4 | R | [245:242] | – | |
| First initialization time after partitioning (first CMD1 to device ready) | INI_TIMEOUT_PA | N2M400FDB311A3C[E/F] | 1 | R | 241 | 78h |
| | | N2M400HDB321A3C[E/F] | | | | F4h |
| | | N2M400GDB321A3C[E/F] | | | | F6h |
| | | N2M400JDB341A3C[E/F] | | | | FFh |
| Reserved | – | 1 | – | 240 | – | |
| Power class for 52 MHz, DDR at 3.6V ³ | PWR_CL_DDR_52_360 | 1 | R | 239 | 0h | |
| Power class for 52 MHz, DDR at 1.95V ³ | PWR_CL_DDR_52_195 | 1 | R | 238 | 0h | |
| Reserved | – | 2 | – | [237:236] | – | |
| Minimum write performance for 8-bit at 52 MHz in DDR mode | MIN_PERF_DDR_W_8_52 | 1 | R | 235 | 0h | |
| Minimum read performance for 8-bit at 52 MHz in DDR mode | MIN_PERF_DDR_R_8_52 | 1 | R | 234 | 0h | |
| Reserved | – | 1 | – | 233 | – | |
| TRIM multiplier | TRIM_MULT | N2M400FDB311A3C[E/F], N2M400GDB321A3C[E/F] | 1 | R | 232 | 06h |
| | | N2M400HDB321A3C[E/F], N2M400JDB341A3C[E/F] | | | | 0Fh |
| Secure feature support | SEC_FEATURE_SUPPORT | 1 | R | 231 | 15h | |


**4GB, 8GB, 16GB, 32GB: e-MMC
ECSD Register**
Table 6: ECSD Register Field Parameters (Continued)

| Name | Field | | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECSD Value |
|---|--------------------|---|--------------|------------------------|------------|------------|
| SECURE ERASE multiplier | SEC_ERASE_MULT | N2M400FDB311A3C[E/F], N2M400GDB321A3C[E/F] | 1 | R | 230 | 02h |
| | | N2M400HDB321A3C[E/F], N2M400JDB341A3C[E/F] | | | | 06h |
| SECURE TRIM multiplier | SEC_TRIM_MULT | N2M400FDB311A3C[E/F], N2M400GDB321A3C[E/F] | 1 | R | 229 | 03h |
| | | N2M400HDB321A3C[E/F], N2M400JDB341A3C[E/F] | | | | 09h |
| Boot information | BOOT_INFO | | 1 | R | 228 | 7h |
| Reserved | - | | 1 | - | 227 | - |
| Boot partition size | BOOT_SIZE_MULT | | 1 | R | 226 | 80h |
| Access size | ACC_SIZE | N2M400FDB311A3C[E/F], N2M400GDB321A3C[E/F] | 1 | R | 225 | 06h |
| | | N2M400HDB321A3C[E/F], N2M400JDB341A3C[E/F] | | | | 07h |
| High-capacity erase unit size | HC_ERASE_GRP_SIZE | N2M400FDB311A3C[E/F], N2M400GDB321A3C[E/F] | 1 | R | 224 | 08h |
| | | N2M400HDB321A3C[E/F], N2M400JDB341A3C[E/F] | | | | 10h |
| High-capacity erase timeout | ERASE_TIMEOUT_MULT | | 1 | R | 223 | 01h |
| Reliable write-sector count | REL_WR_SEC_C | | 1 | R | 222 | 01h |
| High-capacity write protect group size | HC_WP_GRP_SIZE | N2M400FDB311A3C[E/F] | 1 | R | 221 | 01h |
| | | N2M400GDB321A3C[E/F], N2M400HDB321A3C[E/F] | | | | 02h |
| | | N2M400JDB341A3C[E/F] | | | | 04h |
| Sleep current (V _{CC}) | S_C_VCC | | 1 | R | 220 | 08h |
| Sleep current (V _{CCQ}) | S_C_VCCQ | | 1 | R | 219 | 08h |
| Reserved | - | | 1 | - | 218 | - |
| Sleep/awake timeout | S_A_TIMEOUT | | 1 | R | 217 | 10h |
| Reserved | - | | 1 | - | 216 | - |
| Sector count | SEC_COUNT | N2M400FDB311A3C[E/F] | 4 | R | [215:212] | 0070C000h |
| | | N2M400HDB321A3C[E/F] | | | | 00E88000h |
| | | N2M400GDB321A3C[E/F] | | | | 01D30000h |
| | | N2M400JDB341A3C[E/F] | | | | 03B20000h |
| Reserved | - | | 1 | - | 211 | - |
| Minimum write performance for 8-bit at 52 MHz | MIN_PERF_W_8_52 | | 1 | R | 210 | 08h |


**4GB, 8GB, 16GB, 32GB: e-MMC
ECSD Register**
Table 6: ECSD Register Field Parameters (Continued)

| Name | Field | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECSD Value |
|---|-----------------------|--------------|------------------------|------------|------------|
| Minimum read performance for 8-bit at 52 MHz | MIN_PERF_R_8_52 | 1 | R | 209 | 08h |
| Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz | MIN_PERF_W_8_26_4_52 | 1 | R | 208 | 08h |
| Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz | MIN_PERF_R_8_26_4_52 | 1 | R | 207 | 08h |
| Minimum write performance for 4-bit at 26 MHz | MIN_PERF_W_4_26 | 1 | R | 206 | 08h |
| Minimum read performance for 4-bit at 26 MHz | MIN_PERF_R_4_26 | 1 | R | 205 | 08h |
| Reserved | – | 1 | – | 204 | – |
| Power class for 26 MHz at 3.6V ³ | PWR_CL_26_360 | 1 | R | 203 | 00h |
| Power class for 52 MHz at 3.6V ³ | PWR_CL_52_360 | 1 | R | 202 | 00h |
| Power class for 26 MHz at 1.95V ³ | PWR_CL_26_195 | 1 | R | 201 | 00h |
| Power class for 52 MHz at 1.95V ³ | PWR_CL_52_195 | 1 | R | 200 | 00h |
| Partition switching timing | PARTITION_SWITCH_TIME | 1 | R | 199 | 1h |
| Out-of-interrupt busy timing | OUT_OF_INTERRUPT_TIME | 1 | R | 198 | 02h |
| Reserved | – | 1 | – | 197 | – |
| Card type | CARD_TYPE | 1 | R | 196 | 07h |
| Reserved | – | 1 | – | 195 | – |
| CSD structure version | CSD_STRUCTURE | 1 | R | 194 | 2h |
| Reserved | – | 1 | – | 193 | – |
| Extended CSD revision | EXT_CSD_REV | 1 | R | 192 | 5h |
| Modes Segment | | | | | |
| Command set | CMD_SET | 1 | R/W/E_P | 191 | 0h |
| Reserved | – | 1 | – | 190 | – |
| Command set revision | CMD_SET_REV | 1 | R | 189 | 0h |
| Reserved | – | 1 | – | 188 | – |
| Power class | POWER_CLASS | 1 | R/W/E_P | 187 | 0h |
| Reserved | – | 1 | – | 186 | – |


**4GB, 8GB, 16GB, 32GB: e-MMC
ECSD Register**
Table 6: ECSD Register Field Parameters (Continued)

| Name | Field | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECSD Value |
|---|------------------|--------------|------------------------|------------|------------------|
| High-speed interface timing | HS_TIMING | 1 | R/W/E_P | 185 | 0h |
| Reserved | – | 1 | – | 184 | – |
| Bus width mode | BUS_WIDTH | 1 | W/E_P | 183 | 0h |
| Reserved | – | 1 | – | 182 | – |
| Erased memory content | ERASED_MEM_CONT | 1 | R | 181 | 0h |
| Reserved | – | 1 | – | 180 | – |
| Partition configuration | PARTITION_CONFIG | 1 | R/W/E, R/W/E_P | 179 | 0h |
| Boot configuration protection | BOOT_CONFIG_PROT | 1 | R/W, R/W/C_P | 178 | 0h |
| Boot bus width | BOOT_BUS_WIDTH | 1 | R/W/E | 177 | 0h |
| Reserved | – | 1 | – | 176 | – |
| High-density erase group definition | ERASE_GROUP_DEF | 1 | R/W/E_P | 175 | 00h |
| Reserved | – | 1 | – | 174 | – |
| Boot area write protection register | BOOT_WP | 1 | R/W, R/W/C_P | 173 | 0h |
| Reserved | – | 1 | – | 172 | – |
| User write protection register | USER_WP | 1 | R/W, R/W/C_P, R/W/E_P | 171 | 0h |
| Reserved | – | 1 | – | 170 | – |
| Firmware configuration | FW_CONFIG | 1 | R/W | 169 | 0h |
| RPMB size | RPMB_SIZE_MULT | 1 | R | 168 | 1h |
| Write reliability setting register ³ | WR_REL_SET | 1 | R/W | 167 | 00h ⁴ |
| Write reliability parameter register | WR_REL_PARAM | 1 | R | 166 | 05h |
| Reserved | – | 1 | – | 165 | – |
| Manually start background operations | BKOPS_START | 1 | W/E_P | 164 | – |
| Enable background operations handshake | BKOPS_EN | 1 | R/W | 163 | 0h |
| Hardware reset function | RST_n_FUNCTION | 1 | R/W | 162 | 0h |


Table 6: ECSD Register Field Parameters (Continued)

| Name | Field | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECSD Value |
|----------------------------------|-----------------------------|--------------|------------------------|------------|----------------------|
| HPI management | HPI_MGMT | 1 | R/W/E_P | 161 | 0h |
| Partitioning support | PARTITIONING_SUPPORT | 1 | R | 160 | 3h |
| Maximum enhanced area size | MAX_ENH_SIZE_MULT | 3 | R | [159:157] | N2M400FDB311A3C[E/F] |
| | | | | | N2M400HDB321A3C[E/F] |
| | | | | | N2M400GDB321A3C[E/F] |
| | | | | | N2M400JDB341A3C[E/F] |
| Partitions attribute | PARTITIONS_ATTRIBUTE | 1 | R/W | 156 | 0h |
| Partitioning setting | PARTITION_SETTING_COMPLETED | 1 | R/W | 155 | 0h |
| General-purpose partition size | GP_SIZE_MULT | 12 | R/W | [154:143] | 0h |
| Enhanced user data area size | ENH_SIZE_MULT | 3 | R/W | [142:140] | 0h |
| Enhanced user data start address | ENH_START_ADDR | 4 | R/W | [139:136] | 0h |
| Reserved | – | 1 | – | 135 | – |
| Bad block management mode | SEC_BAD_BLK_MGMNT | 1 | R/W | 134 | 0h |
| Reserved | – | 134 | – | [133:0] | – |

Notes: 1. R = Read-only

R/W = One-time programmable and readable

R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable

R/W/C_P = Writable after the value is cleared by a power cycle and assertion of the RST_n signal (the value not cleared by CMD0 reset) and readable

R/W/E_P = Multiple writable with the value reset after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable

W/E_P = Multiple writable with the value reset after power cycle, assertion of the RST_n signal, and any CMD0 reset, and not readable

TBD = To be determined

- Reserved bits should be read as 0.
- Micron has tested power failure under best application knowledge conditions with positive results. Customers may request a dedicated test for their specific application condition.
- Set at 00h when shipped for optimized write performance; can be set to 1Fh to enable protection on previously written data if power failure occurs during a WRITE operation. This byte is one-time programmable.



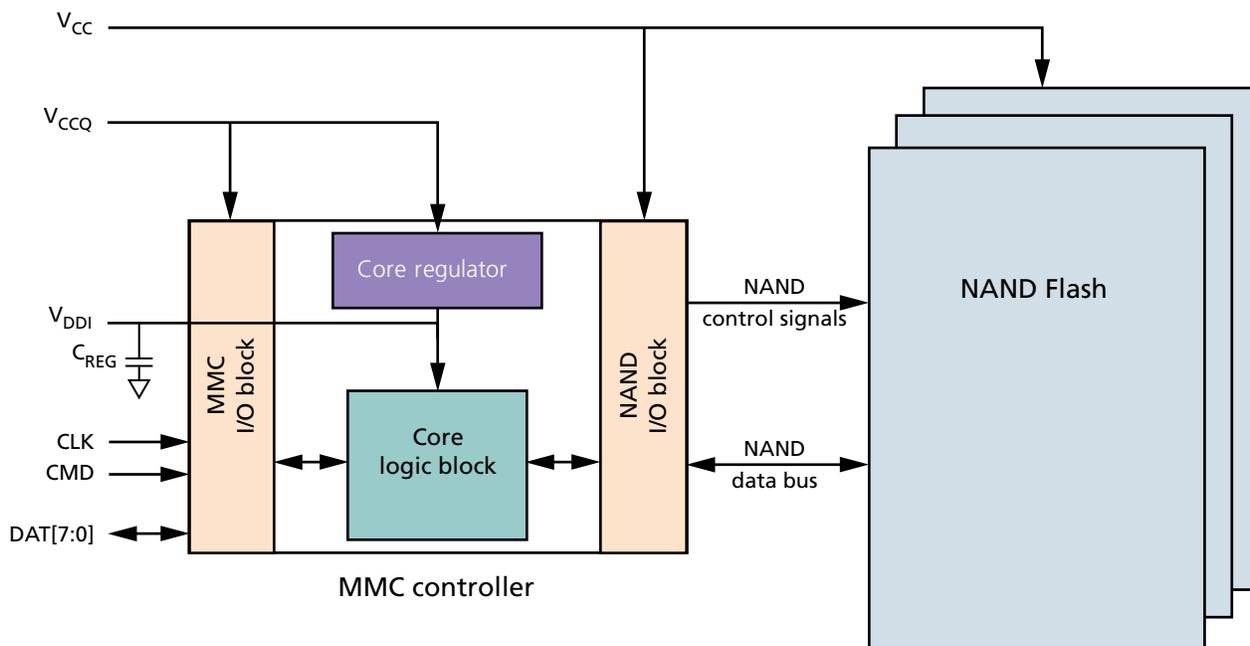
**4GB, 8GB, 16GB, 32GB: e-MMC
DC Electrical Specifications – Device Power**

DC Electrical Specifications – Device Power

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is used for the NAND Flash device and its interface voltage; V_{CCQ} is used for the controller and the e-MMC interface voltage. A C_{REG} capacitor must be connected to the V_{DDI} terminal to stabilize regulator output on the system.

Figure 6: Device Power Diagram



Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

| Parameters | Symbol | Min | Max | Unit |
|---------------------|-----------|------|-----|------|
| Voltage input | V_{IN} | -0.6 | 4.6 | V |
| V_{CC} supply | V_{CC} | -0.6 | 4.6 | V |
| V_{CCQ} supply | V_{CCQ} | -0.6 | 4.6 | V |
| Storage temperature | T_{STG} | -40 | 85 | °C |

Note: 1. Voltage on any pin relative to V_{SS} .



4GB, 8GB, 16GB, 32GB: e-MMC DC Electrical Specifications – Device Power

Table 8: Operating Conditions

| Parameters | Symbol | Min | Typ | Max | Unit |
|-------------------------------------|-------------|------|-----|------|--------------------|
| Supply voltage (controller and I/O) | V_{CCQ} | 1.65 | – | 1.95 | V |
| | | 2.70 | – | 3.6 | |
| Supply voltage (NAND) | V_{CC} | 2.70 | – | 3.6 | V |
| Supply power-on for 3.3V | t_{PRUH} | – | – | 35 | ms |
| Supply power-on for 1.8V | t_{PRUL} | – | – | 25 | ms |
| V_{DDI} capacitance value | C_{REG}^1 | 0.1 | – | – | μF |
| Operating temperature | T_A | –40 | – | 85 | $^{\circ}\text{C}$ |

- Note: 1. C_{REG} is used to stabilize the internal regulator output to controller core logic voltages. Micron recommends using the following capacitor values:
 C_{VCC} (capacitor for V_{CC}) = 4.3 μF .
 C_{VCCQ} (capacitor for V_{CCQ}) = 4.3 μF .
 C_{REG} = 1.0 μF .



Revision History

Rev. C – 7/12

- Updated MMC-Specific Features
- Updated Ordering Information table
- Updated 160-ball LPGA package dimension drawing (package code 1A3)
- Added part numbering information
- Corrected typos in CID and ECSD Register tables
- Added Note 4 to ECSD Register table
- Updated CSD[36:32] and ECSD[bytes 241, 222, 215:212, 175, 167, 166, 159:157] Register tables

Rev. B – 2/12

- Changed the part numbers and the minimum operating temperature from -25 to -40 degrees C

Rev. A – 1/12

- Initial release

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This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.