

#### GENERAL DESCRIPTION

The SX9300 is the world's first dual channel capacitive Specific Absorption Rate (SAR) controller that accurately discriminates between an inanimate object and human body proximity. The resulting detection is used in portable electronic devices to reduce and control radio-frequency (RF) emission power in the presence of a human body, enabling significant performance advantages for manufacturers of electronic devices with EMF radiation sources to meet stringent emission regulations' criteria and Specific Absorption Rate (SAR) standards. Operating directly from an input supply voltage of 2.7 to 5.5V, the SX9300 outputs its data via a 1.65 – 5.5V host compatible I2C serial bus.

The I2C serial communication bus port is compatible with 1.8V host control to report body detection/proximity and to facilitate parameter settings adjustment. Upon proximity detection, the NIRQ output asserts, enabling the user to either determine the relative proximity distance, or simply obtain an indication of detection. The serial bus can also serve to overwrite detection thresholds and operational settings in the event the user wants to change them from their factory presets.

The SX9300 includes an on-chip auto-calibration controller that regularly performs sensitivity adjustments to maintain peak performance over a wide variation of temperature, humidity and noise environments, providing simplified product development and enhanced performance. A dedicated transmit enable (TXEN) pin is available to synchronize proximity measurements to RF transmission, enabling very low supply current and high noise immunity by only measuring proximity when requested.

#### KEY PRODUCT FEATURES

- ◆ **2.7 – 5.5V Input Supply Voltage**
- ◆ **Dual SAR Capacitive Sensor Inputs**
  - ❖ On-Chip SAR Engine For Body versus Inanimate Object Detection
  - ❖ Stable Proximity Sensing With Temperature
  - ❖ 20mm detection distance
  - ❖ Capacitance Offset Compensation to 30pF
- ◆ **Active Sensor Guarding**
- ◆ **Automatic Calibration**
- ◆ **Ultra Low Power Consumption:**
  - ❖ Active Mode: 170  $\mu$ A
  - ❖ Doze Mode: 18  $\mu$ A
  - ❖ Sleep Mode: 2.5  $\mu$ A
- ◆ **400KHz I2C Serial Interface**
  - ❖ Four programmable I2C Sub-Addresses
  - ❖ Input Levels Compatible with 1.8V Host Processors
- ◆ **Open Drain NIRQ Interrupt pin**
- ◆ **Three (3) Reset Sources: POR, NRST pin, Soft Reset**
- ◆ **-40°C to +85°C Operation**
- ◆ **Compact Size: 3 x 3mm Thin QFN package**
- ◆ **Pb & Halogen Free, RoHS/WEEE compliant**

#### APPLICATIONS

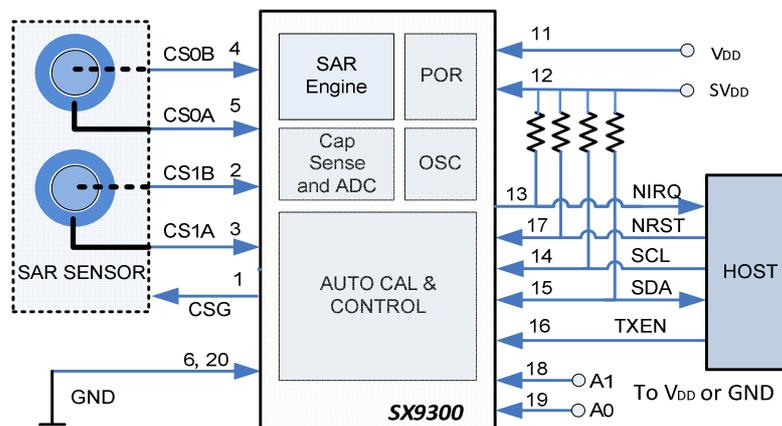
- SAR Compliant Systems
- Notebooks
- Tablets
- Mobile Phones
- Mobile Hot Spots

#### ORDERING INFORMATION

Semtech P/N	Package	Marking
SX9300IULTRT <sup>Note1</sup>	QFN-20	ZM5C
SX9300EVK	Eval. Kit	

Note 1: Quantities are ordered in 3K units per Reel

#### TYPICAL APPLICATION CIRCUIT



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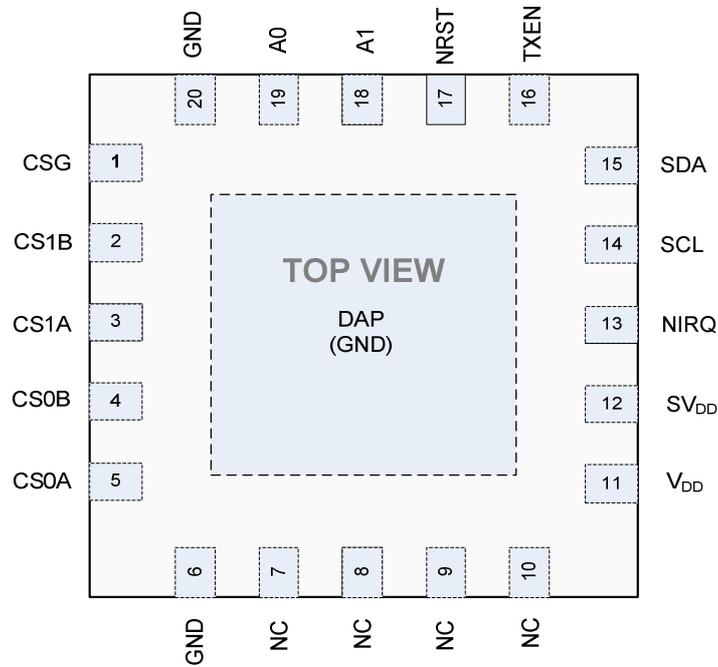
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**1 GENERAL DESCRIPTION**

**1.1 Pin Diagram**



**Figure 1: Pin Diagram**

**1.2 Marking information**



yyww = Date Code  
xxxx = Lot Number

**Figure 2: QFN Marking Information**

### 1.3 Pin Identification

Pin Number	Name	Type	Description
1	CSG	Analog	Capacitive Sensor Guard
2	CS1B	Analog	Capacitive Sensor, 1B
3	CS1A	Analog	Capacitive Sensor, 1A
4	CS0B	Analog	Capacitive Sensor, 0B
5	CS0A	Analog	Capacitive Sensor, 0A
6	GND	Ground	Ground
7	NC	Not Used	Do Not Connect
8	NC	Not Used	Do Not Connect
9	NC	Not Used	Do Not Connect
10	NC	Not Used	Do Not Connect
11	V <sub>DD</sub>	Power	SX9300 Core Power
12	SV <sub>DD</sub>	Power	Host serial port supply voltage. Must be less than or equal to V <sub>DD</sub> . NOTE: During power-up or power-down, SV <sub>DD</sub> must be less than or equal to V <sub>DD</sub>
13	NIRQ	Digital Output	Interrupt request, active LOW, requires pull-up resistor to SV <sub>DD</sub>
14	SCL	Digital Input	I2C Clock, requires pull up resistor to SV <sub>DD</sub>
15	SDA	Digital I/O	I2C Data, requires pull up resistor to SV <sub>DD</sub>
16	TXEN	Input	Transmit Enable, active HIGH (Tie to SV <sub>DD</sub> if not used).
17	NRST	Input	External reset, active LOW, requires pull up resistor to SV <sub>DD</sub>
18	A1	Digital Input	I2C Sub-Address, connect to GND or V <sub>DD</sub>
19	A0	Digital Input	I2C Sub-Address, connect to GND or V <sub>DD</sub>
20	GND	Ground	Ground
DAP	GND	Ground	Exposed Pad. Connect to Ground

**Table 1: Pin Description**

### 1.4 Acronyms

DAP            Die Attach Paddle  
 SAR            Specific Absorption Rate

## 2 ELECTRICAL CHARACTERISTICS

### 2.1 Absolute Maximum Ratings

Stresses above the values listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions beyond the "Recommended Operating Conditions", is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability and proper functionality.

Parameter	Symbol	MIN	MAX	UNIT
Supply Voltage	V <sub>DD</sub>	-0.5	6.0	V
	SV <sub>DD</sub>	-0.5	6.0	
Input voltage (non-supply pins)	V <sub>IN</sub>	-0.5	V <sub>DD</sub> +0.3	
Input current (non-supply pins)	I <sub>IN</sub>	-10	10	mA
Operating Junction Temperature	T <sub>JCT</sub>	-40	125	°C
Reflow temperature	T <sub>RE</sub>		260	
Storage temperature	T <sub>STOR</sub>	-50	150	
ESD HBM (Human Body model, to JESD22-A114)	ESD <sub>HBM</sub>	8		kV

**Table 2: Absolute Maximum Ratings**

### 2.2 Recommended Operating Conditions

Parameter	Symbol	MIN	MAX	UNIT
Supply Voltage	V <sub>DD</sub>	2.7	5.5	V
	SV <sub>DD</sub>	1.65	V <sub>DD</sub>	
Ambient Temperature Range	T <sub>A</sub>	-40	85	°C

**Table 3: Recommended Operating Conditions**

**NOTE:** During power-up or power-down, SV<sub>DD</sub> must be less than or equal to V<sub>DD</sub>

### 2.3 Thermal Characteristics

Parameter	Symbol	MIN	Typical	MAX	UNIT
Thermal Resistance – Junction to Air (Static Airflow)	θ <sub>JA</sub>		34		°C/W

**Table 4: Thermal Characteristics**

**Note:** Theta JA is calculated from a package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under exposed pad per JESD51 standards.

**Electrical Specifications**
*All values are valid within the operating conditions unless otherwise specified.*

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
<b>Current consumption</b>						
Sleep Mode	I <sub>SLEEP</sub>	Power down, all analog circuits shut down. (I2C listening)		2.5		uA
Doze	I <sub>DOZE</sub>	CPS_PERIOD = 200mS DozePeriod = 2xCps_Period CPS_FS = 167KHz CPS_RES = Medium VDD = 5 volt		18		
Active (See Note i)	I <sub>ACTIVE</sub>	CPS_PERIOD = 30mS CPS_FS = 167KHz CPS_RES = Medium. VDD = 5 volt		170		
<b>Outputs: SDA, NIRQ</b>						
Output Current at Output Low Voltage	I <sub>OL</sub>	VOL = 0.4V	6			mA
Maximum Output LOW Voltage	V <sub>OL(Max)</sub>	SV <sub>DD</sub> > 2V			0.4	V
		SV <sub>DD</sub> ≤ 2V			0.2 x SV <sub>DD</sub>	
<b>Inputs: SCL, SDA, TXEN</b>						
Input logic high	V <sub>IH</sub>		0.8 x SV <sub>DD</sub>		SV <sub>DD</sub> + 0.3	V
Input logic low	V <sub>IL</sub>		-0.3		0.25 x SV <sub>DD</sub>	
Input leakage current	I <sub>L</sub>	CMOS input	-1		1	uA
Hysteresis	V <sub>HYS</sub>	SV <sub>DD</sub> > 2V		0.05x SV <sub>DD</sub>		V
		SV <sub>DD</sub> ≤ 2V		0.1x SV <sub>DD</sub>		
TXEN measurements	TXEN <sub>ACTDLY</sub>	Delay to when the SX9300 actually begins measurements from when TXEN becomes active		100		μS
<b>Input: A0, A1</b>						
Input logic high	V <sub>IH</sub>		0.7 x V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
Input logic low	V <sub>IL</sub>		-0.3		0.3 x V <sub>DD</sub>	

Input: NRST						
Input logic high	$V_{IH}$	$SV_{DD} > 2V$	$0.7 \times SV_{DD}$		$SV_{DD} + 0.3$	V
		$SV_{DD} \leq 2V$	$0.75 \times SV_{DD}$			
Input logic low	$V_{IL}$	$SV_{DD} > 2V$			0.6	
		$SV_{DD} \leq 2V$			$0.3 \times SV_{DD}$	
Start-up						
Power-up time	$T_{POR}$			1		mS
NRST						
NRST minimum pulse width	$T_{RESETPW}$			20		nS

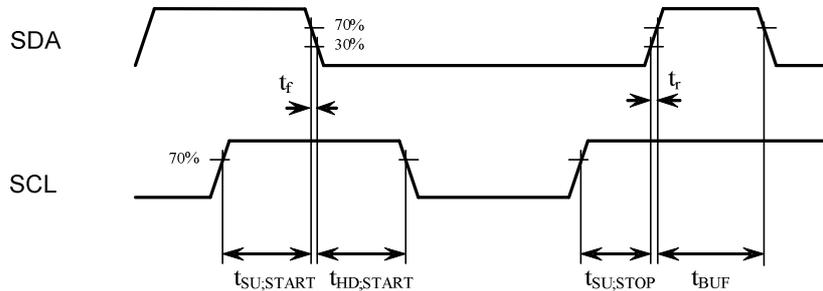
**Table 5: Electrical Characteristics**

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
<b>I2C Timing Specifications</b>						
SCL clock frequency	$f_{SCL}$				400	kHz
SCL low period	$t_{LOW}$		1.3			uS
SCL high period	$t_{HIGH}$		0.6			
Data setup time	$t_{SU;DAT}$		100			
Data hold time	$t_{HD;DAT}$		0			
Repeated start setup time	$t_{SU;STA}$		0.6			
Start condition hold time	$t_{HD;STA}$		0.6			
Stop condition setup time	$t_{SU;STO}$		0.6			
Bus free time between stop and start	$t_{BUF}$		1.3			
Input glitch suppression	$t_{SP}$	Note (1)			50	nS

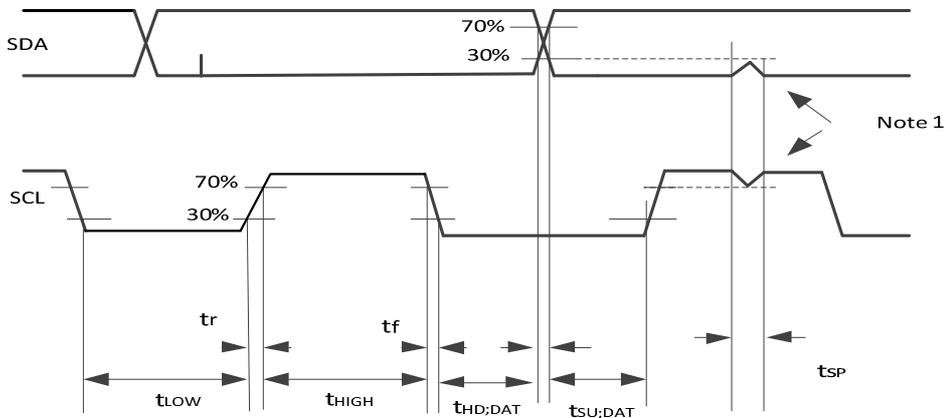
Note (1) -- Minimum glitch amplitude is  $0.7V_{DD}$  at High level and Maximum  $0.3V_{DD}$  at Low level.

**Table 6: I2C Timing Specification**

Note: All timing specifications, refer to Figure 3, Figure 4, and Table 6



**Figure 3: I2C Start and Stop timing**



**Figure 4: I2C Data timing**

### 3 FUNCTIONAL DESCRIPTION

#### 3.1 Introduction

##### 3.1.1 General

The SX9300 is the world's first SAR controller that is designed to detect proximity, differentiating between a human body and an inanimate object. The resulting detection is used in portable electronic devices to reduce and control radio-frequency (RF) emission power in the presence of a human body, enabling significant performance advantages for manufacturers of electronic devices with EMF radiation sources to meet stringent emission regulations' criteria and Specific Absorption Rate (SAR) standards.

##### 3.1.2 Parameters and Configuration

The SX9300 allows the user full parameter customization for Sensor sensitivity, hysteresis, and detection thresholds. If custom parameters are used by the customer, these parameters must be uploaded by the host immediately following boot-up or after a reset.

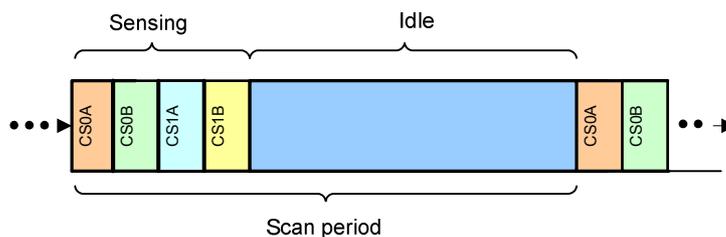
##### 3.1.3 Sensor Proximity Adjustment

Capacitive proximity detection is directly proportional to the SX9300 internal gain and threshold settings, and external sensor area to optimize proximity detection distance. A longer Proximity detection range can be accomplished without changing the capacitive sensor size, by using a high sensitivity setting and/or lower signal threshold setting for proximity detection.

#### 3.2 Scan Period

The Scan period determines the minimum SAR detection reaction time of the SX9300 and can be varied by the host from 30ms to approximately 400ms. SAR detection reaction time is proportional to the Scan period and inversely proportional to power consumption, so longer Scan periods corresponds to lower power, but also to longer detection reaction times.

The Scan period of the SX9300 is defined by two periods: Sensing and Idle. During the Sensing period, all enabled CS inputs, from CS0A to CS1B are sampled and any detection reported via the I2C bus (via I2C register polling or NIRQ). The Sensing period is variable and is proportional to the Scan Frequency and Resolution settings in the Cap Sensing Control Registers. During the Idle period, the SX9300 the analog circuits are placed in standby and the idle timer is initiated. Upon expiry of the idle timer, a new Scan period cycle begins.



**Figure 5 Scan Period**

### 3.3 Operational Modes

The SX9300 has four (4) operational modes: Active, Doze, Sleep, and Commanded. These modes enable tradeoffs between SAR detection reaction time and power consumption.

**Active:** Active mode has the shortest scan periods, with a typical SAR detection reaction time of 30ms. In this mode, all enabled sensors are scanned and information data is processed within this interval. The Active scan period is user configurable and can be extended to a maximum period of 400ms. See CPS\_PERIOD register in Section 7.3, (I2C Register Overview) below.

**Doze:** Doze mode is by default, enabled in the SX9300. The Doze mode period is user configurable (see Section 7.3, I2C Register Overview) and can be used to extend the scan period out to 6.4 seconds for very low power consumption applications at the expense of very long SAR detection reaction times (6.4 seconds).

In some applications, the SAR detection reaction time needs to be fast, when a human body is present, but can be slow when SAR detection has not been active for a while. When the SX9300 has not detected an object for a specific time, it will automatically change modes from Active to Doze reducing power. This time-out period is determined by the CPS\_DOZEPERIOD which can be configured by the user or turned OFF (CPS\_DOZEEN) if not required.

Proximity detection on any sensor will cause the SX9300 to leave Doze mode and re-enter Active mode.

**Sleep:** Sleep mode places the SX9300 in its lowest power mode, disabling all sensor scanning and setting the idle period to continuous. In this mode, only the I2C serial bus is active.

**Commanded:** The commanded mode is perhaps the SX9300's most useful feature. The TXEN input enables the measurement of the SAR channels when HIGH, likewise when the TXEN input is LOW, the SX9300 is in the Sleep mode. Specifically, on the rising edge of TXEN the SX9300 will begin measuring the SAR channels beginning with the lowest enabled channel repeating the measurement cycle at programmed rates (CPS\_PERIOD) so long as TXEN remains HIGH. When TXEN goes LOW the current measurement sequence will complete and then measurement will cease until the next rising edge of TXEN.

### 3.4 I2C interface

The I2C serial interface is configured as a slave device, operates at speeds up to 400 kHz and serves as the Host interface to the SX9300.

The SX9300 has two I/O pins (A0 and A1) that provides for four possible, user selectable I2C addresses:

A1	A0	Address
0	0	0x28
0	1	0x29
1	0	0x2A
1	1	0x2B

**Table 7: I2C Sub-Address Selection**

### 3.5 Configuration

If the application requires customization, the SX9300 configuration registers can be changed over the I2C bus. Some I2C addressable registers are used to read sensor status and information, while other (configuration) registers allow the host to take control of the SX9300. Via the configuration registers, the host can command an operational mode change or modify the active sensors. These user programmable configuration registers are volatile, therefore during a power-down or reset event, they lose all user programmed content, requiring the host to re-write the I2C registers after the event.

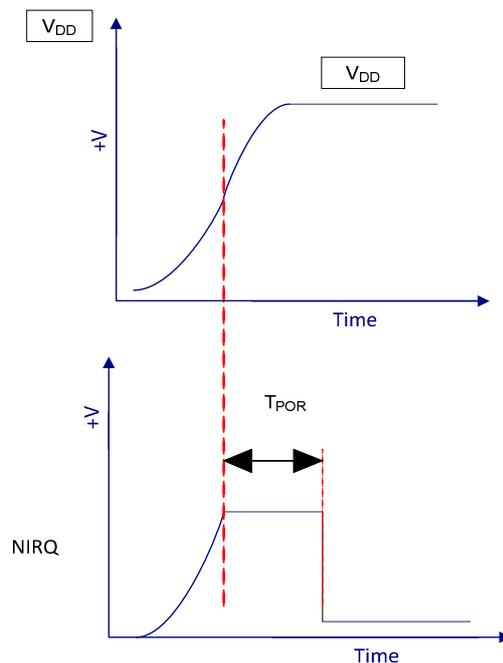
### 3.6 Reset

A Reset to the SX9300 is performed by any one of the following methods:

- Power-up
- NRST pin
- Software reset

#### 3.6.1 Power-up

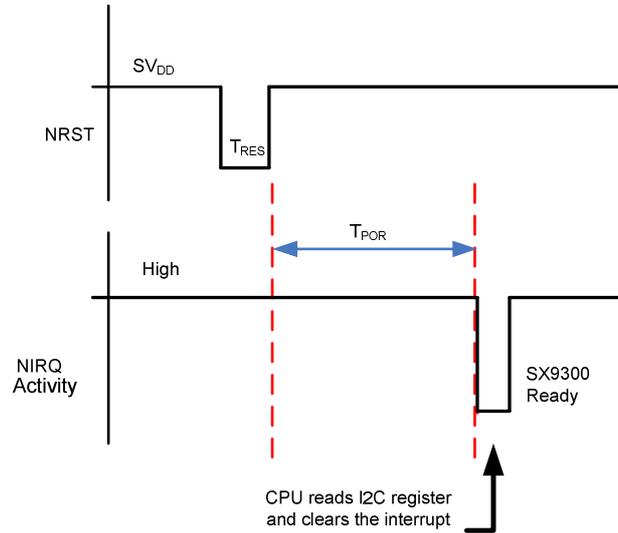
During a power-up condition, the NIRQ output is HIGH until  $V_{DD}$  has met the minimum input voltage requirements and a  $T_{POR}$  time has expired upon which, NIRQ asserts to a LOW condition indicating the SX9300 is initialized. The Host is required to perform an I2C read to clear this NIRQ status. The SX9300 is then ready for normal I2C communication and is operational.



**Figure 6: Power-up vs. NIRQ**

### 3.6.2 NRST

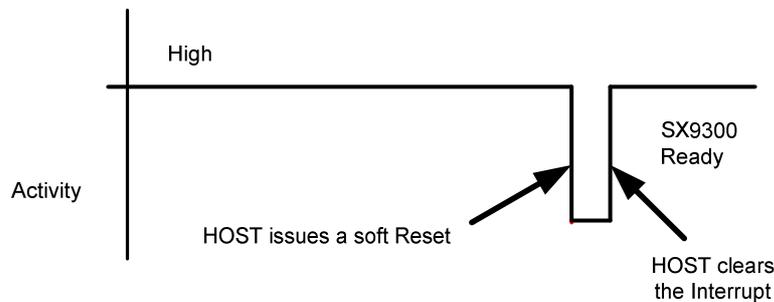
When NRST is asserted LOW and then HIGH, the SX9300 will reset its internal registers and will become active after period,  $T_{POR}$ . If a hardware reset control output is not available to drive NRST, then this pin must be pulled high to  $SV_{DD}$ .



**Figure 7: Hardware Reset**

### 3.6.3 Software Reset

The host can perform software resets by writing to the I2CSoftReset register (see Section 7.3 for additional information). The NIRQ output will be asserted LOW and the Host is required to perform an I2C read to clear this NIRQ status.



**Figure 8: Software Reset**

### **3.7 Interrupt**

Interrupt sources are disabled by default upon power-up and resets, and thus must be enabled by the host (apart from RESET IRQ). Any or all of the following interrupts can be enabled by writing a “1” into the appropriate locations within the IRQ\_Enable register (see Section 7.3 for details):

- Body detected
- Completed Compensation
- Completed Conversion

The interrupt status can be read from register IRQStat for each of these interrupt sources (see Section 7.3 for details).

#### **3.7.1 Power-up**

During initial power-up, the NIRQ output is HIGH. Once the SX9300 internal power-up sequence has completed, NIRQ is asserted LOW, signaling that the SX9300 is ready. The host must perform a read to IRQStat to acknowledge that the status is read and the SX9300 will clear the interrupt and release the NIRQ line.

#### **3.7.2 NIRQ Clearing**

The NIRQ can be asserted in either the Active or Doze mode during a scan period. The NIRQ will be automatically cleared after the Host performs a read of the IRQStat I2C register.

**4 PIN DESCRIPTIONS**

**4.1 Introduction**

This section describes the SX9300 pin functionality, pin protection, whether or not the pins are analog or digital, and if they require pull-up resistors. There is ESD protection on all SX9300 I/O.

**4.2 V<sub>DD</sub> and SV<sub>DD</sub>**

These are the device supply voltages. V<sub>DD</sub> is the supply voltage for the internal core and I/O. SV<sub>DD</sub> is the supply voltage for the I2C serial interface. NOTE: SV<sub>DD</sub> MUST be equal or lower than V<sub>DD</sub>.

**4.3 TXEN**

This signal can be used in many applications if a conversion trigger/enable is needed. This input pin synchronizes the Capacitance Sensing inputs in systems that need to (for example) transmit RF signals. When this signal is active, SX9300 immediately performs capacitive measurements. If this input becomes inactive during the middle of a measurement, the SX9300 will complete all remaining measurements and will enter sleep mode until TXEN goes active again.

**4.4 Capacitor Sensing Interface (CS0A, CS0B, CS1A, CS1B, CSG)**

The Capacitance Sensor input pins CS0A, CS0B, CS1A and CS1B are connected directly to the Capacitor Sensing Interface circuitry which converts the sensed capacitance into digital values. The Capacitive Sensor Guard (CSG) output provides a guard reference to minimize the parasitic sensor pin capacitances to ground. Capacitance sensor pins which are not used must be left open-circuited. Additionally, CS pins must be connected directly to the capacitive sensors using a minimum length circuit trace to minimize external “noise” pick-up.

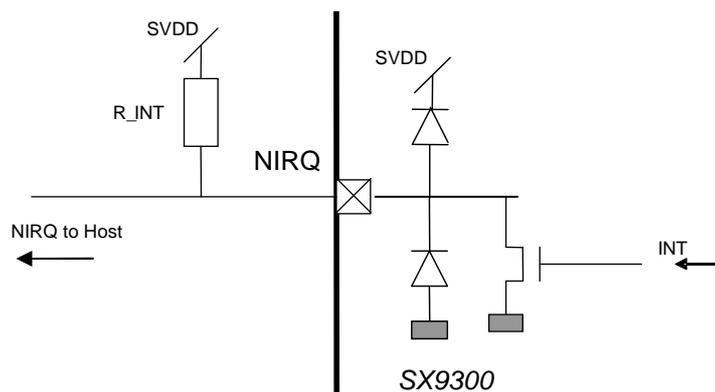
The capacitance sensor and capacitive sensor guard pins are protected from ESD events to V<sub>DD</sub> and GROUND.

**4.5 Host Interface**

The Host Interface consists of: NIRQ, NRST, SCL, SDA, and TXEN. These signals are discussed below.

**4.5.1 NIRQ**

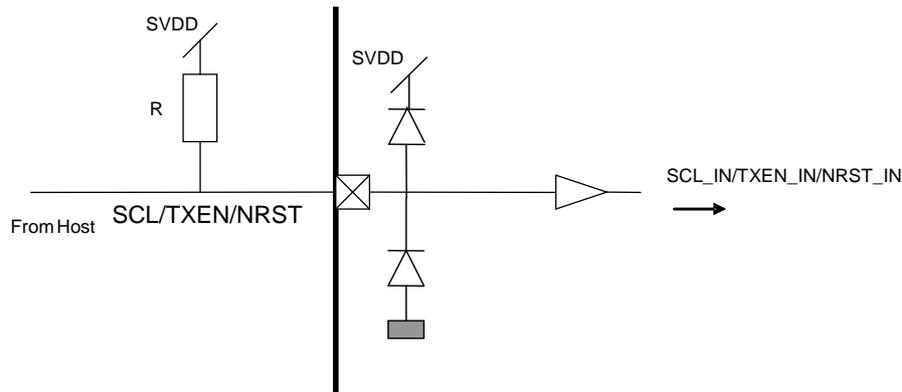
The NIRQ pin is an open drain output that requires an external pull-up resistor (1..10 KOhm). The NIRQ pin is protected from ESD events to SV<sub>DD</sub> and GROUND.



**Figure 9: NIRQ Output Simplified Diagram**

#### 4.5.2 SCL, NRST and TXEN

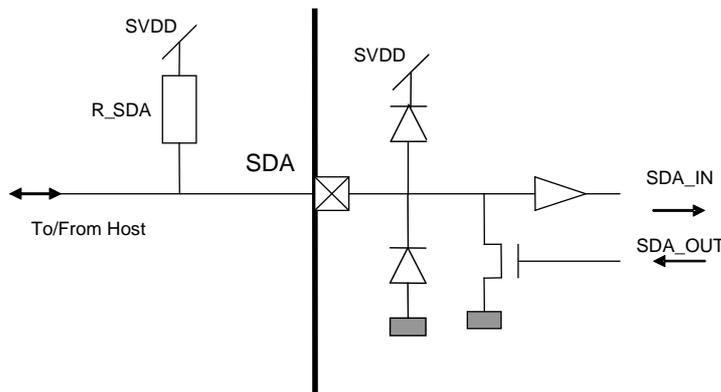
The SCL, NRST and TXEN pins are high impedance input pins that require an external pull-up resistor (1..10 kOhm). It is possible to connect NRST and TXEN Host output drivers directly without the requirement for a pull-up resistor if driven from a push-pull host output. These pins are protected from ESD events to SVDD and GROUND.



**Figure 10: SCL/TXEN/NRST**

#### 4.5.3 SDA

SDA is an I/O pin that requires an external pull-up resistor (1..10 KOhm). The SDA I/O pin is protected to SV<sub>DD</sub> and GROUND.



**Figure 11: SDA Simplified Diagram**

**5 DIFFERENTIAL DETECTION AND SAR COMPLIANCE**
**5.1 Specific Absorption Rate (SAR) Basics**

SAR is a measure of the rate at which energy is absorbed by the body when exposed to a radio frequency (RF) electromagnetic field; although, it can also refer to absorption of other forms of energy by tissue, including ultrasound. It is defined as the power absorbed per mass of tissue and has units of watts per kilogram (W/kg). SAR is usually averaged either over the whole body, or over a small sample volume (typically 1g or 10g of tissue). The value cited is then the maximum level measured in the body part studied over the stated volume or mass.

The FCC requires that cell phone manufacturers conduct their SAR testing to include the *most severe, worst-case (and highest power) operating conditions for all the frequency bands* used in the USA for that cell phone. The SAR values recorded on the FCC's authorization and in the cell phone manual to demonstrate compliance with Commission rules indicate only the highest single measurement taken for each frequency range that the particular model uses. FCC approval means that the device will never exceed the maximum levels of consumer RF exposure permitted by federal guidelines, but it does not indicate the amount of RF exposure consumers experience during normal use of the device. While only the maximum SAR values are used for FCC approval, all test reports submitted by the manufacturer are available *in full* for public inspection on the Commission's website.

**5.2 SAR Solution**

A SAR measurement consists of taking two sets of capacitive sensor data. In this case, each sensor must have recognized proximity detection. The two sets of data are then combined within the SX9300 as both a "ratio" of the data and a difference or "delta" of the data. The measured capacitance data can represent a very low level of capacitance. Therefore insuring that the signal is detected for a number of samples will minimize false triggers. The SX9300 includes the ability to "debounce" the detected data for up to 8 samples.

**5.2.1 Set CPS\_DEB [5:4] (Debounce)**

The register for the SAR debounce control: Bits [5:4] set the number of debounce samples.

BITS		DEBOUNCE SAMPLES
5	4	
0	0	None
0	1	2
1	0	4
1	1	8

**Table 8: Detection Debounce Control**

**5.2.2 Set CPS\_DELTATRS [3:0] (SAR Delta Detection Threshold)**

The register for the SAR Delta Threshold Control is at: Bits [3:0] and is used to set Delta Detection Threshold. The Delta measurement is the capacitive difference measurement between the two SAR Sensing Capacitors (Sensor B – Sensor A).

Reg value	Threshold Value	Reg value	Threshold Value
0000	0	1000	30
0001	1	1001	35
0010	3	1010	40
0011	5	1011	45
0100	10	1100	50
0101	15	1101	55
0110	20	1110	60
0111	25	1111	70

**Table 9: Delta Threshold Selection**

**5.2.3 Set CPS\_RATIOTRS [7:0] (SAR Ratio Detection Threshold)**

The register for the SAR Ratio Threshold Control is at: 0x10. Bits [7:0] are used to set the SAR RATIO Threshold for the SX9300. The determination of the SAR Ratio Detection Threshold must be determined experimentally, but will be stable for a given design

**5.2.4 Setting Up The SX9300 To Discriminate Between A Human Body & Inanimate Object**

An accurate discrimination between a human body and inanimate object can be obtained using the SX9300. It is important that the sensor pair areas are identical (in area, not necessarily in shape, see Section 7.4 for information as to how to design a successful SAR capacitive sensor). This involves a careful set-up between the following two registers: Delta and Ratio Thresholds. The set-up of these two registers is as follows:

With the customer's system set onto a table, bring a hand to the desired detection distance from the sensor.

Set the Delta threshold limit until a "detection" is reported by the SX9300

Set the Ratio threshold limit until a "detection" is reported by the SX9300

Remove the hand and test with a number of inanimate objects to determine if the SX9300 successfully rejects them from reporting. If the SX9300 reports any of them as a "detection", then raise the Delta threshold limit until it stops being reported and confirm that the human body is still reported (note: you will lose a bit of detection range when you raise threshold limits).

If you cannot determine a successful setting that simultaneously rejects inanimate objects and detects a human body, then you must raise the Ratio threshold limit. Repeat 4) until a solution is determined.

**6 DETAILED CONFIGURATION DESCRIPTIONS**
**6.1 Introduction**

The SX9300 is the first Smart Proximity SAR Compliant sensor that solves the human body versus inanimate object problem that designers of mobile appliances face every day. It requires only small external sensors plus some minor set-up commands to provide a robust SAR solution. The SX9300 comes with factory default settings that are appropriate for most general applications, however a full complement of registers are accessible to the user to enable application customization and optimization.

**6.2 Capacitive Sensor (CS0A, CS0B, CS1A, CS1B) Parameters**

The SX9300 sensor has default parameters for the Capacitive Sensors that provides a quick and initial starting point to achieve SAR compliance. However, because of unique sensor sizes and sensor locations, it is possible to achieve higher and more robust performance with minor changes to these default parameters. In general only a few registers require changes to their default parameters to achieve improved performance. These registers are:

**6.2.1 Set CPS\_Digital\_GAIN [6:5] (Cap Sensor Gain)**

The address for the (capacitive) sensor gain is: Bits [6:5] provide for four (4) gain settings as shown below:

Bits		Gain
6	5	
0	0	x 1
0	1	x 2
1	0	x 4
1	1	x 8

**Table 10: CPS\_Digital\_GAIN**

**6.2.2 Set CPS\_C<sub>INR</sub> [1:0] (Input Capacitance Range and Resolution)**

The register for the input capacitance full scale range and resolution is: Bits [1:0] provide set ability over the expected maximum sensed capacitance. A setting of 00 on these bits provides for the largest capacitance measurement range, but is not as sensitive for the longest proximity distance, while the setting of 11 provides for the smallest capacitive measurement range, and provides the longest proximity distance. The table for this register is shown below:

Bits		C <sub>INPUT</sub> Range and Resolution
1	0	
0	0	Large
0	1	Medium-Large
1	0	Medium-Small
1	1	Small

**Table 11: C<sub>INPUT</sub> Range and Resolution Register**

**6.2.3 Set CPS\_TRS [4:0] (Detection threshold)**

This register defines the detection threshold for all sensors and the details are shown below. Lower thresholds provide longer proximity detection distances but are more susceptible to noise, while higher threshold values provide immunity to noise, but results in shorter proximity detection range. The default value for this register is [00000].

BITS					THRESHOLD VALUE
4	3	2	1	0	
0	0	0	0	0	0
0	0	0	0	1	20
0	0	0	1	0	40
0	0	0	1	1	60
0	0	1	0	0	80
0	0	1	0	1	100
0	0	1	1	0	120
0	0	1	1	1	140
0	1	0	0	0	160
0	1	0	0	1	180
0	1	0	1	0	200
0	1	0	1	1	220
0	1	1	0	0	240
0	1	1	0	1	260
0	1	1	1	0	280
0	1	1	1	1	300
1	0	0	0	0	350
1	0	0	0	1	400
1	0	0	1	0	450
1	0	0	1	1	500
1	0	1	0	0	600
1	0	1	0	1	700
1	0	1	1	0	800
1	0	1	1	1	900
1	1	0	0	0	1000
1	1	0	0	1	1100
1	1	0	1	0	1200
1	1	0	1	1	1300
1	1	1	0	0	1400
1	1	1	0	1	1500
1	1	1	1	0	1600
1	1	1	1	1	1700

**Table 12: Cap Sensor Threshold**

**6.2.4 Set CPS\_HYST [5:4] (Detection Hysteresis)**

This register defines the detection hysteresis for all sensors. Hysteresis for the SAR sensors provides an important function in that it keeps the SX9300 from providing “oscillating” results when detection levels are close to threshold. The register details are shown below.

Bits		
5	4	DETECTION HYSTERESIS
0	0	32
0	1	64
1	0	128
1	1	256

*Table 13: CPS\_HYST*

**6.2.5 Set CPS\_AVGDEB[7:6] (Average Pos/Neg Debouncing)**

Use of debounce in the SX9300 is recommended as it will reduce the effects of extraneous noise for reported detection. The SX9300 includes several conditions for debounce: Close, Far, and Data Detection.

Bits		
7	6	AVERAGE POS/NEG DEBOUNCING
0	0	OFF
0	1	2 Samples
1	0	4 Samples
1	1	8 Samples

*Table 14: CPS\_AVGDEB*

**6.2.6 Set CPS\_AVGNEGFILT[5:3] & CPS\_AVGPOSFILT[2:0] (Average Neg/Pos Filters)**

The SX9300 includes circuitry to average out the detected signals. These detected signals can be both positive and negative, and so there are registers to control both the positive and negative averaging filter coefficients. There are eight (8) settings possible in each of these filters ranging from OFF up to highest filtering. Use of these filters is recommended for noisy environment and represents a tradeoff detection response versus false triggering. See CPS\_AVGNEGFILT and CPS\_AVGPOSFILT for register and bit locations.

**6.2.7 Set CPS\_FS[4:3] (Sampling Frequency)**

The capacitance sampling frequency can be changed in CPS\_CTRL2 if the environment is particularly noisy. Changing this frequency affects the Capacitance Sensing period. It is recommended to use the 167 kHz sampling frequency.

Bits		SAMPLING FREQUENCY
4	3	
0	0	83 kHz
0	1	125 kHz
1	0	167 kHz
1	1	Reserved, do not use

**Table 15: Sampling Frequency Control**

**6.2.8 Set CPS\_RES[2:0] (Resolution Factor)**

The CPS Resolution factor has 8 possible settings that range from coarsest to very fine that controls the total number of measurements per sensor in a Scan Period. Along with the CPS Sampling Frequency, changing this register affects the SX9300 Sensing Period. This register is located in CPS\_CTRL2.

Bits			RESOLUTION
2	1	0	
0	0	0	Coarsest
0	0	1	Very Coarse
0	1	0	Coarse
0	1	1	Medium Coarse
1	0	0	Medium
1	0	1	Fine
1	1	0	Very Fine
1	1	1	Finest

**Table 16: CPS Resolution Factor**

**6.2.9 Set CPS\_AVGTRS[7:0] (Averaging Threshold)**

The SX9300 performs averaging on all capacitive measurements to determine when to perform a calibration cycle. The CPS\_AVGTRS register is used to set an 8-bit positive and negative threshold that determines when a calibration is internally requested. Typically the user would set this register to be between 1000000 [7:0] to 11000000 [7:0] which corresponds to  $\frac{1}{2}$  to  $\frac{3}{4}$  of the system dynamic range.

### 6.3 Additional Parameter Settings

Further application customization is possible to control scan period, enabled sensors and individual sensor interrupts are also possible. Scan period affects both power dissipation and detection reaction time.

#### 6.3.1 Set CPS\_PERIOD[6:4] (Scan Period)

This register controls the scan period of the SX9300 over a range of 30ms to 400ms.

Bits			Scan PERIOD (ms)
6	5	4	
0	0	0	30
0	0	1	60
0	1	0	90
0	1	1	120
1	0	0	150
1	0	1	200
1	1	0	300
1	1	1	400

**Table 17: Scan Period**

#### 6.3.2 Set CPS\_EN [3:0] (Enable Capacitive Sensor Inputs)

If one set of SAR capacitive sensors is not required, they can be disabled in this register. Each bit in this register corresponds to a specific sensor input. A logic “1” enables the capacitive sensor input, while a logic “0” disables a capacitive input. INPUTS MUST BE DISABLED IN PAIRS.

CS0A & CS0B = Bits [1:0]

CS1A & CS1B = Bits [3:2]

#### 6.3.3 Set IRQ\_Enable [6:3] (Enable Interrupt Sources)

There are a number of interrupt sources that the SX9300 can report. A logic “1” in the specific location will enable the specific interrupt as shown below.

SARIRQEN [6]: Enables the SAR Proximity Detection IRQ

SARRLSIRQEN [5]: Enables the SAR Proximity No Detect IRQ

COMPDONEIRQEN [4]: Enables the Compensation Done Notification IRQ

CONVIRQEN [3]: Enables the Conversion Completion Done Notification IRQ

## 7 I2C INTERFACE

The I2C implemented on the SX9300 is compliant with:

- Standard (100kb/s) and fast mode (400kb/s)
- I2C standard slave mode
- 7 bit address (default is 0x28 assuming A1=A0=0).

The host can use the I2C to read and write data at any time, and these changes are effective immediately. Therefore the user should ideally disable the sensor before changing settings, or discard the results while changing (Section 3.2).

There are four types of I2C registers:

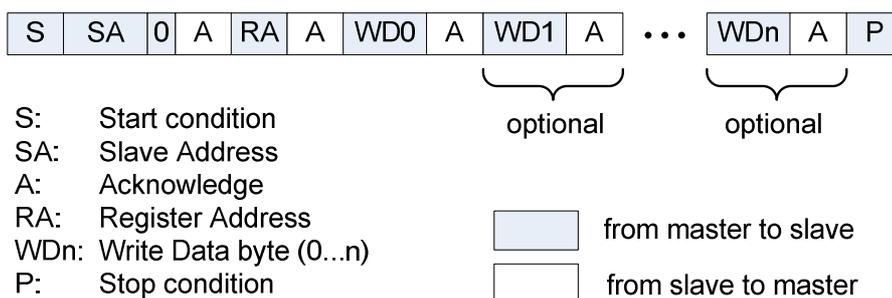
- Control and Status (read). These registers give information about the status of the capacitive sensors
- Operation Control (read/write). These registers control Operating Modes.
- Cap Sensor Control and Parameters (read/write)
- Cap Sensor Data Read Back (read)

The I2C can be used to read and write from a start address and then perform read or writes sequentially, and the address increments automatically.

Supported I2C access formats are described in the next sections.

### 7.1 I2C Write

The format of the I2C write is given in Figure 12. After the start condition [S], the slave address (SA) is sent, followed by an eighth bit ('0') indicating a Write. The SX9300 then Acknowledges [A] that it is being addressed, and the Master sends an 8 bit Data Byte consisting of the SX9300 Register Address (RA). The Slave Acknowledges [A] and the master sends the appropriate 8 bit Data Byte (WD0). Again the Slave Acknowledges [A]. In case the master needs to write more data, a succeeding 8 bit Data Byte will follow (WD1), acknowledged by the slave [A]. This sequence will be repeated until the master terminates the transfer with the Stop condition [P].

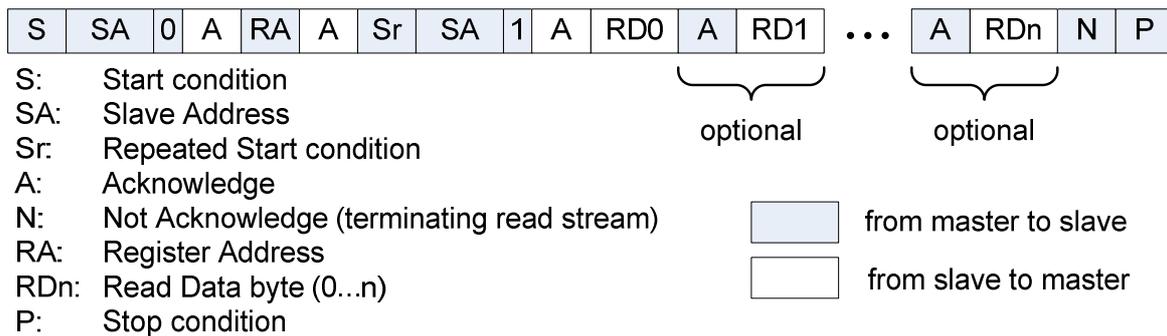


**Figure 12: I2C Write**

The register address is incremented automatically when successive register data (WD1...WDn) is supplied by the master.

## 7.2 I2C Read

The format of the I2C read is given in Figure 13. After the start condition [S], the slave address (SA) is sent, followed by an eighth bit ('0') indicating a Write. The SX9300 then Acknowledges [A] that it is being addressed, and the Master responds with an 8-bit Data consisting of the Register Address (RA). The Slave Acknowledges [A] and the master sends the Repeated Start Condition [Sr]. Once again, the slave address (SA) is sent, followed by an eighth bit ('1') indicating a Read. The SX9300 responds with an Acknowledge [A] and the read Data byte (RD0). If the master needs to read more data it will acknowledge [A] and the SX9300 will send the next read byte (RD1). This sequence can be repeated until the master terminates with a NACK [N] followed by a stop [P].



**Figure 13: I2C Read**

**7.3 Register Overview**

Add	Reg	Acc	Bits	Field	Reset	Function
<b>General Control &amp; Status</b>						
0x00	IRQStat	R	7	RESETIRQ	1	Reset event occurred
			6	TCHIRQ	0	Sensor proximity detected
			5	RLSIRQ	0	Sensor detection release condition interrupt
		R/W	4	COMPDONE	0	Compensation complete. Writing a one in this bit trigs a compensation on all channels
		R	3	CONVIRQ	0	Conversion cycle complete
			2:1	Not Used	00	Not Used
			0	TXENSTAT	0	Report TXEN pad status
0x01	TchCmpStat	R	7	SARSTAT3	0	Determines if proximity has been detected for the pair CS1A/CS1B
			6	SARSTAT2	0	Determines if a human body has been detected for the pair CS1A/CS1B
			5	SARSTAT1	0	Determines if a proximity has been detected for the pair CS0A/CS0B
			4	SARSTAT0	0	Determines if a human body has been detected for the pair CS0A/CS0B
			3:0	COMPSTAT	1111	Specifies which capacitive sensor(s) has a compensation pending
<b>General Operations Control</b>						
0x03	IRQ_Enable	R	7	Not Used	0	Not Used
		R/W	6	SARIRQEN	0	Enables the detection irq
			5	SARRLSIRQEN	0	Enables the release irq
			4	COMPDONEIRQEN	0	Enables the compensation irq
			3	CONVIRQEN	0	Enables the conversion irq
		R	2:0	Not Used	000	Not Used
<b>Cap Sensing Control</b>						
0x06	CPS_CTRL0	R/W	7	Not Used	0	Not Used
			6:4	CPS_PERIOD	000	Scan period : 000: 30 ms 001: 60 ms 010: 90 ms 011: 120 ms 100: 150 ms 101: 200 ms 110: 300 ms 111 : 400 ms
			3:0	CPS_EN	1111	Enables CS0A through CS1B
0x07	CPS_CTRL1	R/W	7:6	CPS_SH	01	CG bias/shield usage. 00 : Off, CG high-Z (off) 01: On(def.) 10: Reserved 11: Reserved
					0000	Not used
		R/W	1:0	CPS_CINR	00	Capacitance Range: 00: Large

						01: Medium Large 10: Medium Small 11: Small
0x08	CPS_CTRL2	R/W	7	Not Used	0	Not Used
			6:5	CPS_Digital_GAIN	00	Set Digital gain factor 00: Gain = 1 01: Gain = 2 10: Gain = 4 11: Gain = 8
			4:3	CPS_FS	01	Sampling frequency 00: 83 kHz 01: 125 kHz 10: 167 kHz (Typical) 11: Reserved
			2:0	CPS_RES	000	Resolution Control 000: Coarsest .... 100: Medium .... 111: Finest
0x09	CPS_CTRL3	R/W	7	Not Used	0	Not Used
			6	CPS_DOZEEN	1	Enables doze mode
			5:4	CPS_DOZEPERIOD	00	When doze is enabled, the cap sensing period moves from CPS_PERIOD to CPS_PERIOD * : 00: 2*CPS_PERIOD 01: 4* CPS_PERIOD 10: 8*CPS_PERIOD 11: 16*CPS_PERIOD
			3:2	Reserved	00	Must be 00
			1:0	CPS_RAWFILT	00	Raw filter coefficient 00: off 01: Low 10: Medium 11: High (Max Filtering)
0x0A	CPS_CTRL4	R/W	7:0	CPS_AVGTRS	00000000	Average pos/neg threshold = 8 x reg
0x0B	CPS_CTRL5	R/W	7:6	CPS_AVGDEB	00	Average pos/neg debouncer: 00: off 01: 2 samples 10: 4 samples 11: 8 samples
			5:3	CPS_AVGNEGFILT	000	Average negative filter coefficient : 000: off 001: Lowest .... .... 111: Highest (Max. Filter)
			2:0	CPS_AVGPOSFILT	000	Average positive filter coefficient : 000: off 001: Lowest .... .... 111: Highest (Max. Filter)
0x0C	CPS_CTRL6	R/W	7:5	Not Used	000	Not Used

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			4:0	CPS_TRS	00000	Defines the touch/prox detection threshold for all sensors. See Table 12
0x0D	CPS_CTRL7	R/W	7	CPS_CMPAUTOOFF	0	Disables the automatic compensation triggered by average
			6	CPS_CMPTRG	0	0: compensate channels independently 1: compensate all channels when triggered
			5:4	CPS_HYST	00	Detection hysteresis 00: 32 01: 64 10: 128 11: 256
			3:2	CPS_CLSDEB	00	Close debouncer 00: off 01: 2 samples 10: 4 samples 11: 8 samples
			1:0	CPS_FARDEB	00	Far debouncer 00: off 01: 2 samples 10: 4 samples 11: 8 samples
0x0E	CPS_CTRL8	R/W	7:4	CPS_STUCK	0000	Stuck at timeout timer : 0000 : off 00XX: increment every CPS_STUCK x 64 active frames 01XX: increment every CPS_STUCK x 128 active frames 1XXX: increment every CPS_STUCK x 256 active frames
			3:0	CPS_CMPPRD	0000	Periodic compensation 0: off else : increment every CPS_COMPPRD x 128 active frames
<b>Sensor Readback</b>						
0x20	CPSRD	R	7:2	Not Used	000000	Not Used
		R	1:0	CPSRD	00	Determines which sensor data will be available in the next Reg read.
0x21	UseMSB	R	7:0	SENSUSEMSB	00000000	Provides the useful information for monitoring purposes. Signed, 2's complement format
0x22	UseLSB	R	7:0	SENSUSELSB	00000000	
0x23	AvgMSB	R	7:0	SENSAVGMSB	00000000	Provides the average information for monitoring purposes. Signed, 2's complement format
0x24	AvgLSB	R	7:0	SENSAVGLSB	00000000	
0x25	DiffMSB	R	7:0	SENSDIFFMSB	00000000	Provides the Diff information for monitoring purposes. Signed, 2's complement format
0x26	DiffLSB	R	7:0	SENSDIFFLSB	00000000	
0x27	OffMSB	R/W	7:0	SENSOFFMSB	00000000	Offset compensation DAC

**WIRELESS & SENSING PRODUCTS**
**Datasheet**

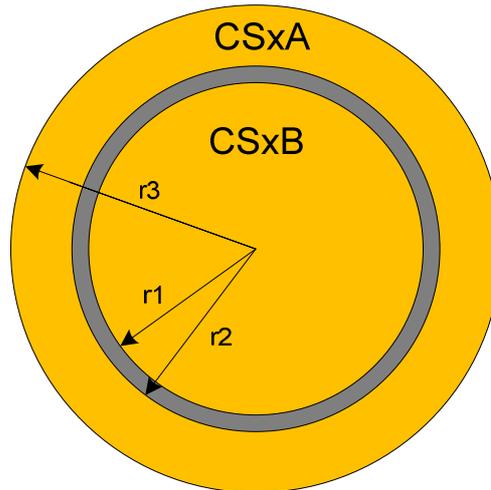
0x28	OffLSB	R/W	7:0	SENSOFFLSB	00000000	code. This is writable to allow forcing some DAC codes. When written, the internal DAC code is updated after the write of the LSB reg. MSB and LSB regs should be written in sequence.
0x29	Delta	R	3:0	SENDELTA	0000	SAR Value Delta (Difference) reading. Signed, 2's complement format (See Register 0x20)
0x2A	Ratio	R	7:0	SENSERATIO	00000000	Ratio of the SAR values. Unsigned. (See Register 0x20)
0x7F	I2CSoftReset	W	7:0	SOFTRESET	00000000	Write 0xDE and Reset the chip
<b>SAR Mode Registers</b>						
0x0F	Deb_DeltaTrs	R/W	7:6	Not Used	00	Not Used
			5:4	CPS_DEB	00	Data Debouncing associated with detection/release (Useful in a noisy environment): 00: off 01: 2 samples 10: 4 samples 11: 8 samples
			3:0	CPS_DELTATRS	0000	Defines the delta detection threshold that's applied to all sensors. See <b>Table 9</b>
0x10	CPS_RatioTrs	R/W	7:0	CPS_RATIOTRS	00000000	Defines the ratio detection threshold applied to all sensors

**Table 18: Register Overview**

### 7.4 SAR Sensor Design

This section describes how to properly design SAR sensors. The SAR sensors for the SX9300 can be designed in a variety of shapes depending on the physical requirements of the system.

In the drawing below, the yellow areas represent copper (conductor) and the gray area represents a non-conductor and is the distance  $r_2 - r_1$  (spacing between the two copper areas).



**Figure 14: Typical SAR Capacitive Sensor**

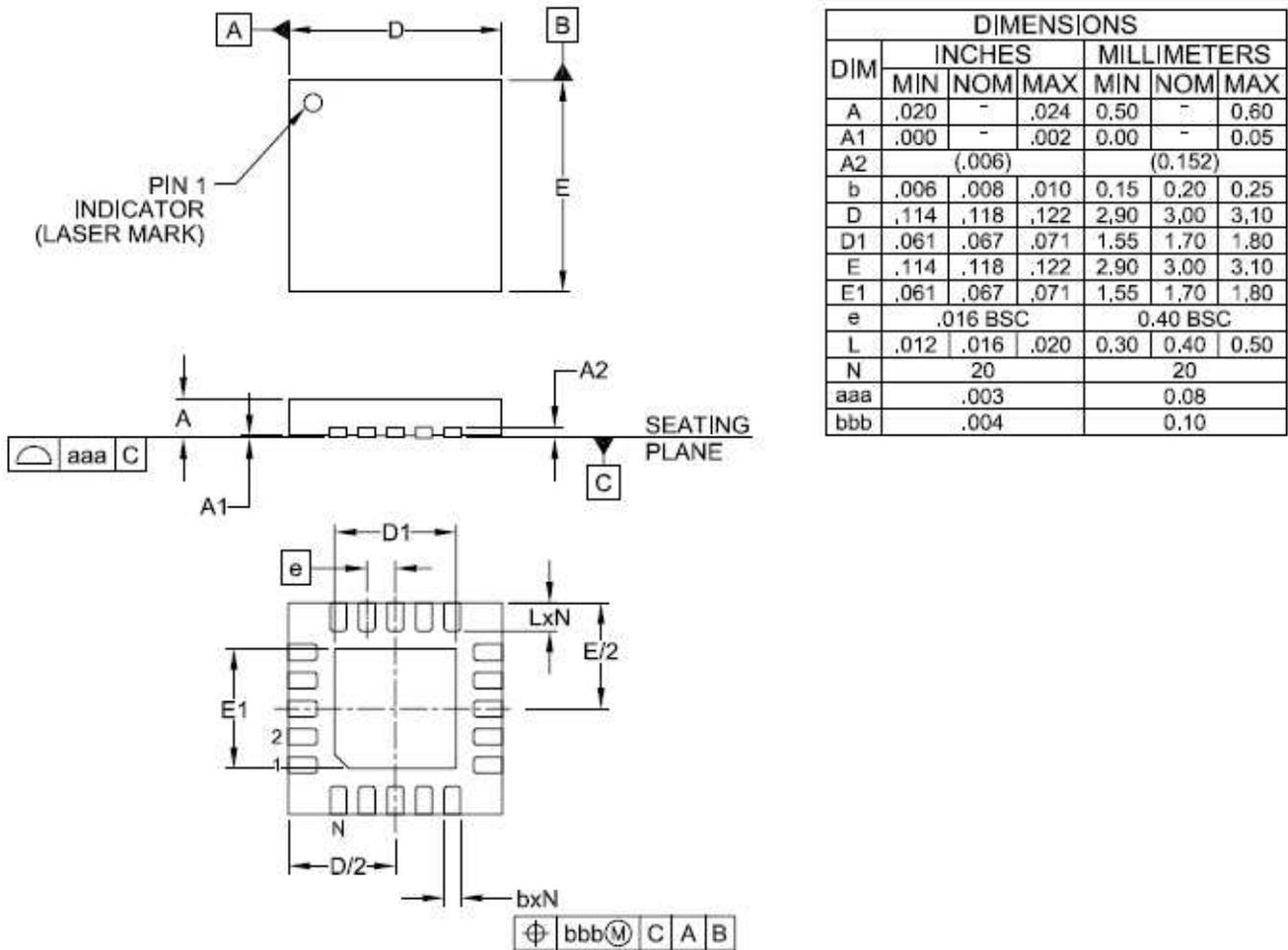
“CSxA” and “CSxB” copper areas refer to the SX9300 sensor inputs.

**IMPORTANT NOTE: The “A” and “B” sensors cannot be swapped on the SX9300.** The outer copper area is always the “A” sensor, and the inner copper area is always the “B” sensor. Also, the area of a CSxB sensor and CSxA sensor must be designed to be nearly equal.

The radius “r1” sets the area of SAR sensor CSxB, while the radius “ $r_3 - r_2$ ” sets the area of SAR sensor CSxA. For circular capacitive sensors shown above where “r1” is very nearly equal to “r2”, then the area of CSxA is defined by

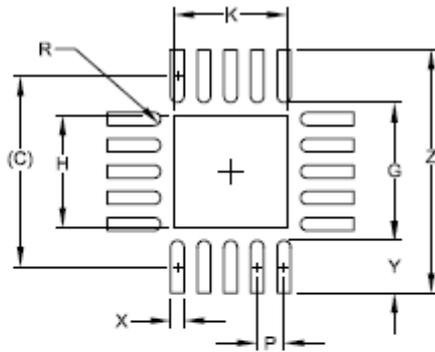
$$r_3 = \sqrt{2} \times r_1$$

This approximation is also true for square type sensors

**8 PACKAGING INFORMATION**
**8.1 Package Outline Drawing**

**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

**Figure 15: Package Outline Drawing**

**8.2 Land Pattern**


DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.031	0.80
Z	.146	3.70

**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY, CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE, FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

**Figure 16: Package Land Pattern**

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