1 Kbit, 2 Kbit, 4 Kbit, 8 Kbit, and 16 Kbit (x8 or x16) MicroWire Serial EEPROM

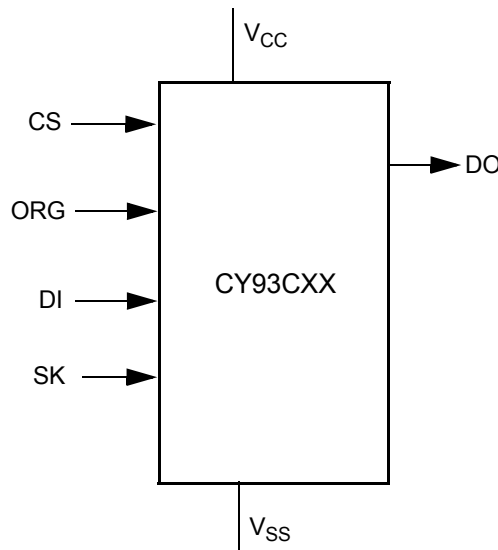## Features

■ Continuous voltage operation
   ❏ V_{CC} = 1.65V to 5.5V

■ Internally organized as x8 or x16

■ Industry standard three wire serial interface

■ Schmitt trigger, filtered inputs for noise suppression

■ Programming instructions that work on byte, word, or entire memory

■ Sequential read operation

■ 4 MHz clock rate (5V) compatibility

■ Self timed write cycle (5 ms max)

■ Ready/$\overline{Busy}$ signal during programming

■ Industrial temperature range

■ High reliability
   ❏ Endurance: 1 million write cycles
   ❏ Data retention: 100 years

■ RoHS compliant 8-Pin SOIC and 8-Pin TSSOP packages

■ Pb-free and RoHS compliant

Functional Description

The CY93C01/02/04/08/16 provides 1K, 2K, 4K, 8K, and 16K bits of serial Electrically Erasable and Programmable Read Only Memory (EEPROM). The memory is organized as x16 when the ORG pin is connected to V_{CC} and as x8 when it is tied to ground. The device is optimized for use in many industrial applications, where low power and low voltage operations are essential. The CY93C01/02/04/08/16 is available in space saving 8-Pin SOIC, and 8-Pin TSSOP packages. The CY93C01/02/04/08/16 is enabled through the Chip Select pin (CS), and accessed through a three wire serial interface consisting of Data Input (DI), Data Output (DO), and Serial Clock (SK). On receiving a read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The write cycle is completely self timed and no separate erase cycle is required before write. The write cycle is enabled only when the part is in the erase or write enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/$\overline{Busy}$ status of the part. The CY93C01/02/04/08/16 is available in a 1.65V to 5.5V version.

Logic Block Diagram

Cypress Semiconductor Corporation   •   198 Champion Court   •   San Jose, CA 95134-1709   •   408-943-2600
Document #: 001-15635 Rev. *C   Revised February 05, 2009

[+] Feedback

Pinouts

Figure 1. Pin Diagram: 8-Pin SOIC/TSSOP Package
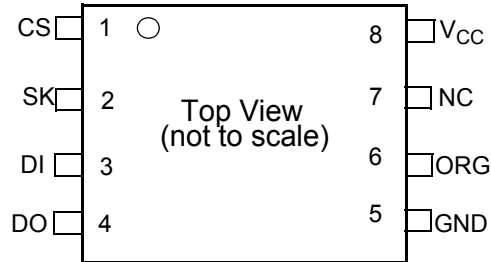
Table 1. Pin Definition – 8-SOIC/TSSOP

Pin Name	8-SOIC Pin Number	8-TSSOP Pin Number	I/O Type	Description
CS	1	1	Input	Chip Select
SK	2	2	Input	Serial Clock
DI	3	3	Input	Serial Data Input
DO	4	4	Output	Serial Data Output
GND	5	5	Input	Ground
ORG	6	6	Input	Internal Organization[1]
NC	7	7	NA	No Connect[2]
V_{CC}	8	8	Input	Power Supply

Notes
1. When the ORG is connected to Vcc, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1Meg ohm pull up, then the x16 organization is selected.
2. The NC pin does not contribute to the normal operation of the device. The pin may be left unconnected or may be connected to Vcc or GND. Direct connection of NC to GND is recommended for lowest standby power consumption.

Device Operating Features

Internal Device Reset

To prevent inadvertent write operations during power up, a Power On Reset (POR) circuit is included.

During power up and power down, the device must not be selected (that is, the Chip Select Input (CS) must be driven low) until the supply voltage reaches the operating voltage V_{CC}.

During power up (the phase during which V_{CC} is lower than the minimum V_{CC}, but increases continuously), the device does not respond to any instruction until V_{CC} has reached the POR threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in DC Electrical Characteristics on page 9). After V_{CC} has passed the POR threshold, the device is reset.

Before selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage is applied. This voltage must remain stable and valid until the end of transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_{WC}).

During power down (the phase during which V_{CC} decreases continuously), as soon as V_{CC} drops from the normal operating voltage below the POR threshold voltage, the device stops responding to any instruction sent to it.

Active and Standby Power Modes

When Chip Select (CS) is high, the device is selected and in the active power mode. It consumes I_{CC}, as specified in DC Electrical Characteristics on page 9. When Chip Select (CS) is low, the device is deselected.

If no erase or write cycle is in progress when Chip Select goes low, the device enters the standby power mode and the power consumption drops to I_{SB1}.

Device Operations

The CY93C02 is accessed through a simple and versatile three wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a Start Bit (logic '1') followed by the appropriate op-code and the desired memory address location.

Read

The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. Note that a dummy bit (logic '0') precedes the 8-bit or 16-bit data output string. The CY93C02 supports sequential read operations. The device automatically increments the internal address pointer and clocks out the next memory location as long as CS is held high. In this case, the dummy bit (logic '0') is not clocked out between memory locations, therefore enabling a continuous stream of data to be read.

Write

The Write (WRITE) instruction contains 8 or 16 bits of data to be written into the specified memory location. The self timed programming cycle t_{WC} starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 100 ns (t_{CE}). A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address is written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status is not obtained if the CS is brought high after the end of the self timed programming cycle t_{WC}.

An internal power on data protection mechanism in the CY93C02 inhibits the device when the supply is too low.

Erase

The Erase (ERASE) instruction programs all bits in the specified memory location to the logical '1' state. The self timed erase cycle starts after the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 100 ns (t_{CE}). A logic '1' at pin DO indicates that the selected memory location is erased, and the part is ready for another instruction.

Erase/Write Enable (EWEN)

To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instruction is carried out. Note that in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the part.

Erase All (ERAL)

The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 100 ns (t_{CE}).

Write All (WRAL)

The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 100 ns (t_{CE}).

Erase/Write Disable (EWDS)

To protect against accidental data disturbance, the Erase/Write Disable (EWDS) instruction disables all programming modes and is executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and is executed at any time.

Table 2. Instruction Set for CY93C01 [3]

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	11	A6–A0	A5–A0			Clear Address AN–A0
WRITE	1	01	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	00	11XXXXX	11XXXX			Write Enable
EWDS	1	00	00XXXXX	00XXXX			Write Disable
ERAL	1	00	10XXXXX	10XXXX			Clear All Address
WRAL	1	00	01XXXXX	01XXXX	D7–D0	D15–D0	Write All Address

Table 3. Instruction Set for CY93C02 and CY93C04 [3]

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A8[4]–A0	A7[5]–A0			Read Address AN–A0
ERASE	1	11	A8[4]–A0	A7[5]–A0			Clear Address AN–A0
WRITE	1	01	A8[4]–A0	A7[5]–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	00	11XXXXXXX	11XXXXXX			Write Enable
EWDS	1	00	00XXXXXXX	00XXXXXX			Write Disable
ERAL	1	00	10XXXXXXX	10XXXXXX			Clear All Address
WRAL	1	00	01XXXXXXX	01XXXXXX	D7–D0	D15–D0	Write All Address

Table 4. Instruction Set for CY93C08 and CY93C16 [3]

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A10[6]–A0	A9[7]–A0			Read Address AN–A0
ERASE	1	11	A10[6]–A0	A9[7]–A0			Clear Address AN–A0
WRITE	1	01	A10[6]–A0	A9[7]–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	00	11XXXXXXXXX	11XXXXXXXX			Write Enable
EWDS	1	00	00XXXXXXXXX	00XXXXXXXX			Write Disable
ERAL	1	00	10XXXXXXXXX	10XXXXXXXX			Clear All Address
WRAL	1	00	01XXXXXXXXX	01XXXXXXXX	D7–D0	D15–D0	Write All Address

Notes
3. X = Do not care bit.
4. Address bit A8 is not decoded by CY93C02.
5. Address bit A7 is not decoded by CY93C02.
6. Address bit A10 is not decoded by CY93C08.
7. Address bit A9 is not decoded by CY93C08.

Ready/Busy Status

While the Write or Erase cycle is underway, for a WRITE, ERASE, WRAL or ERAL instruction, the Busy signal (DO=0) is returned whenever Chip Select input (CS) is driven high. In this state, the CY93C02 ignores any data on the bus. When the write cycle is completed, and Chip Select input (CS) is driven high, the Ready signal (DO=1) indicates that the CY93C02 is ready to receive the next instruction. Serial Data Output (DO) remains set to 1 until the Chip Select Input (CS) is brought low or until a new start bit is decoded.

Common I/O Operation

Serial Data Output (DO) and Serial Data Input (DI) are connected together, through a current limiting resistor, to form a common, single wire data bus. Some precautions must be taken when operating the memory in this way, mostly to prevent a short

circuit current from flowing when the last address bit (A0) clashes with the first data bit on Serial Data Output (DO).

Clock Pulse Counter

In a noisy environment, the number of pulses received on Serial Clock (SK) may be greater than the number delivered by the master (the microcontroller). This leads to a misalignment of the instruction of one or more bits, as shown in Figure 8 on page 8, and may lead to the writing of erroneous data at an erroneous address. To combat this problem, the CY93C02 has an on-chip counter that counts the clock pulses from the start bit until the falling edge of the Chip Select input (CS). If the number of clock pulses received is not the number expected, the WRITE, ERASE, ERAL, or WRAL instruction is aborted and the contents of the memory are not modified.
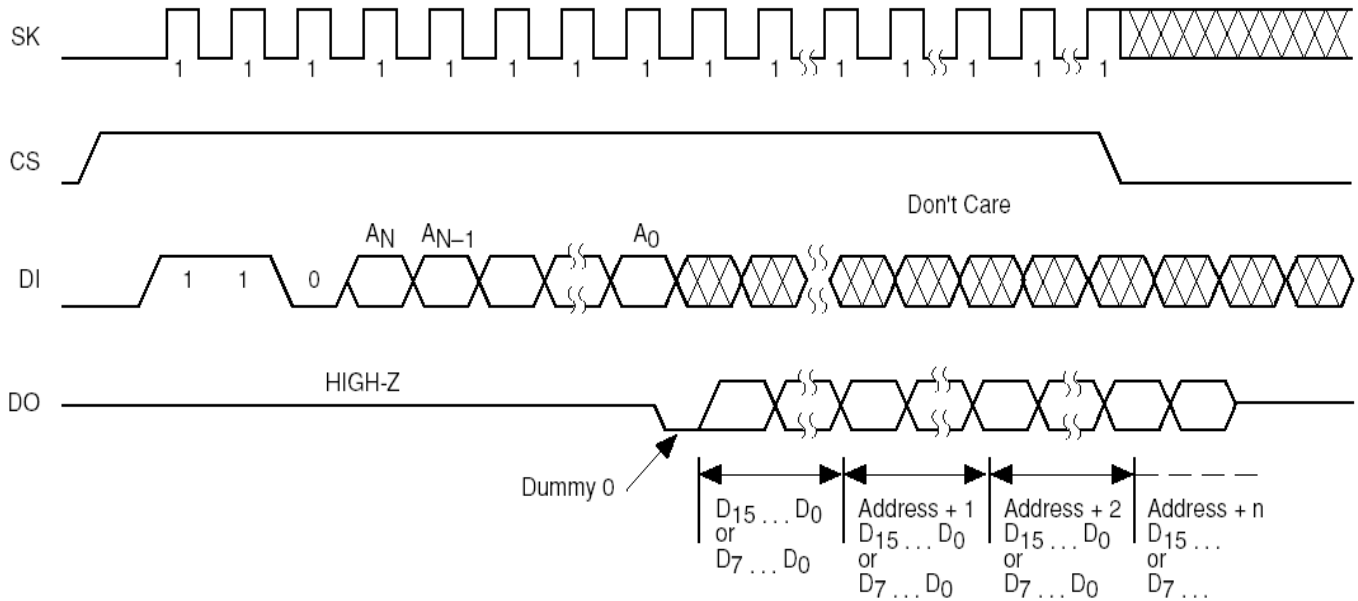
Figure 2. Read Instruction Timing

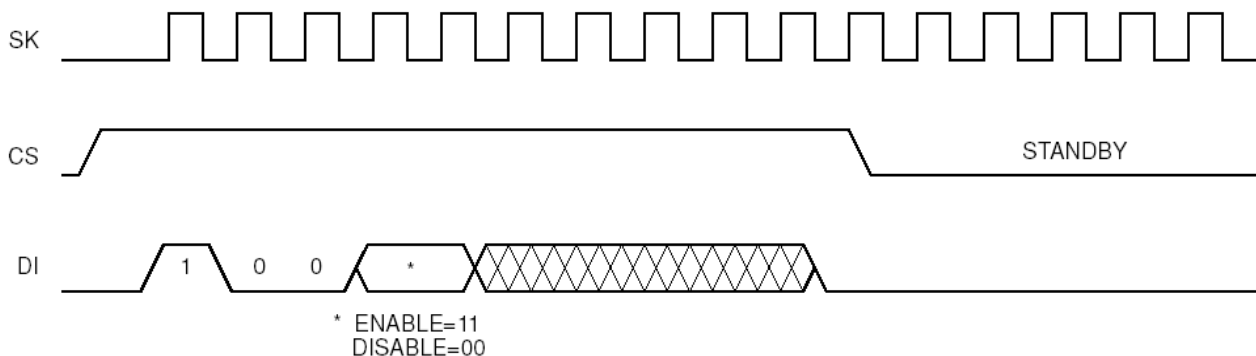**Figure 3. Erase Enable/Disable Instruction Timing**
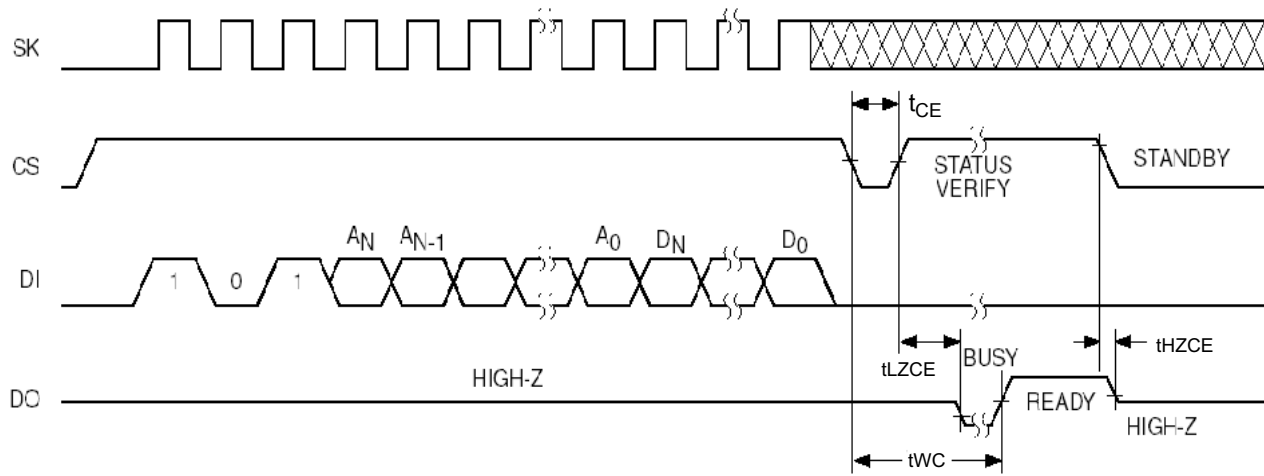
Figure 4. Write Instruction Timing
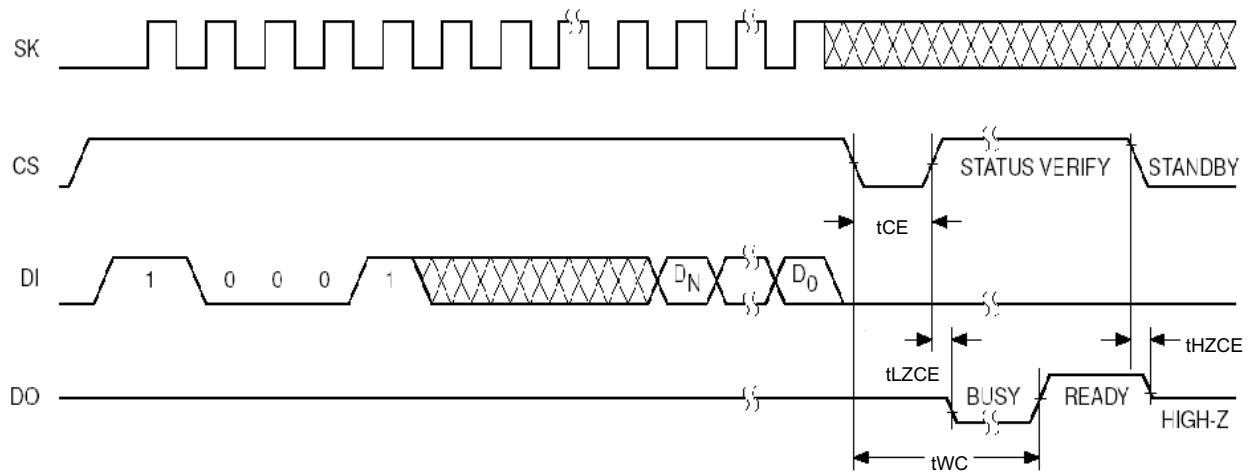

Figure 5. Write All Instruction Timing

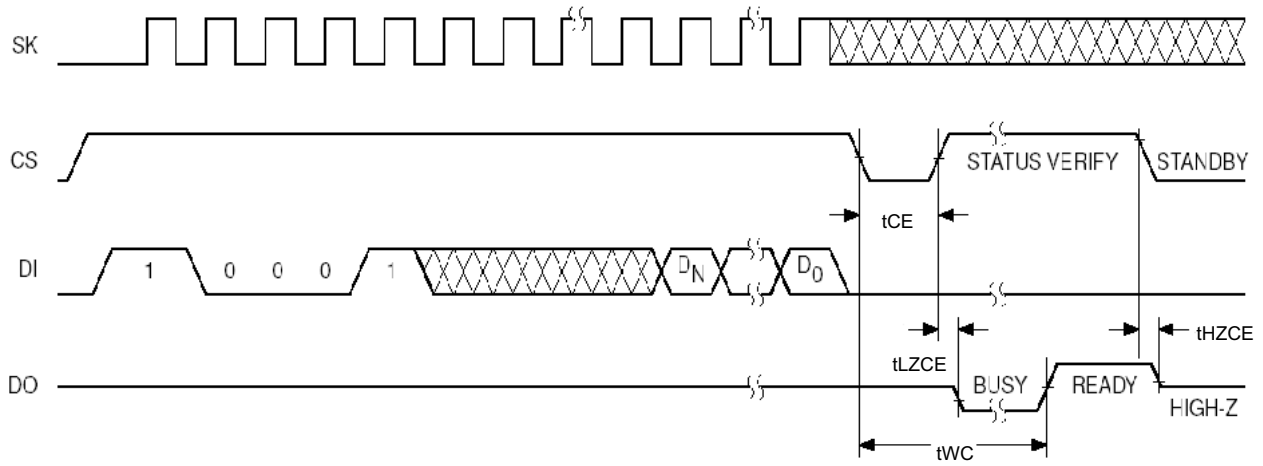**Figure 6. Erase Instruction Timing**

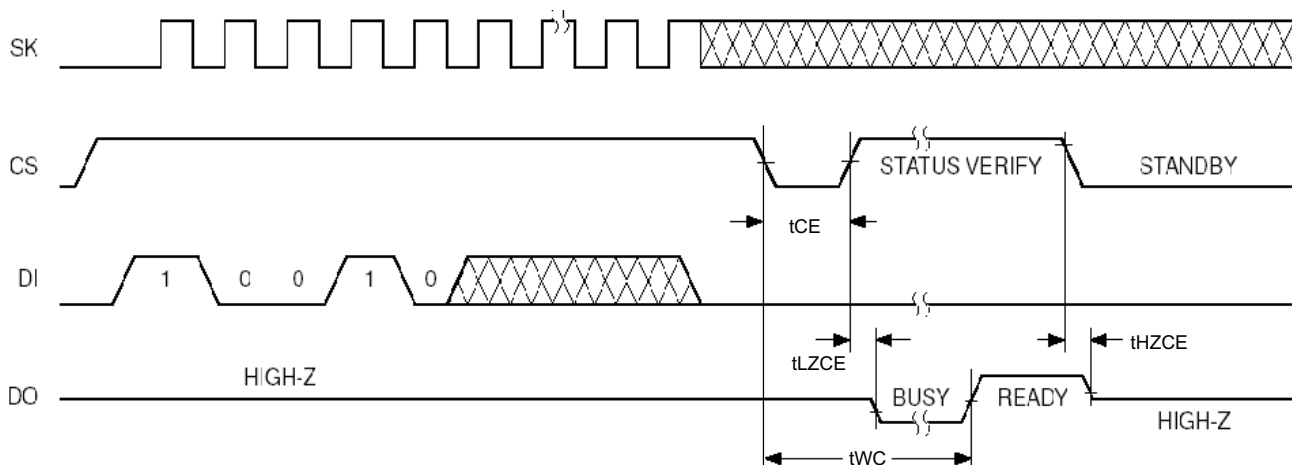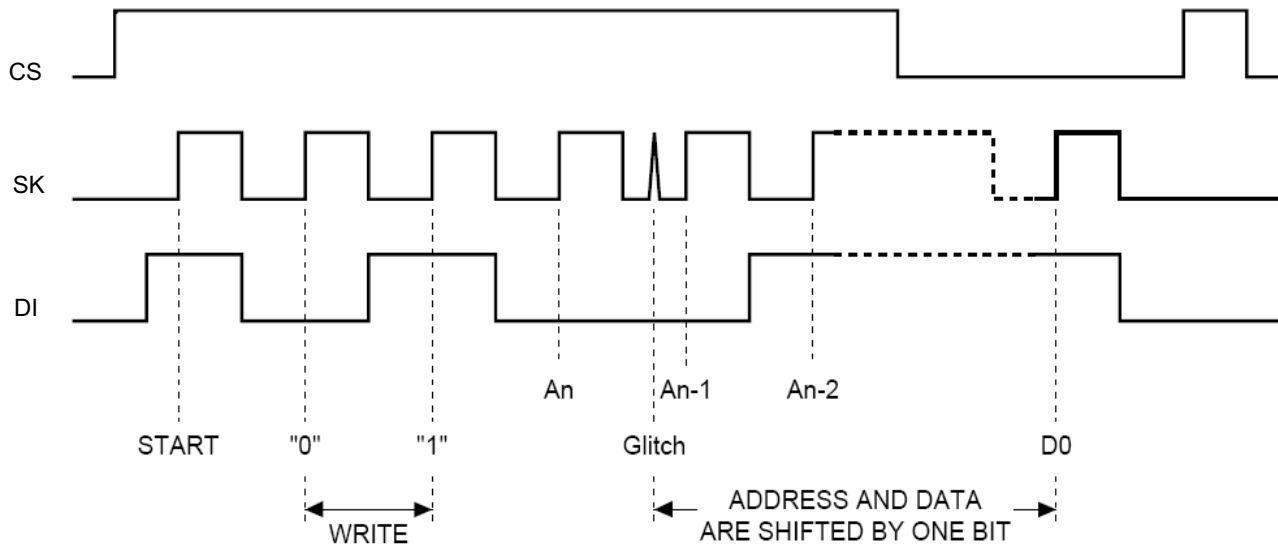

Figure 7. Erase All Instruction Timing

Figure 8. Write Sequence with One Clock Glitch

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65°C to +150°C

Ambient temperature with
power applied .... –55°C to +125°C

Supply voltage on V_{CC} relative to GND..........–1.0V to +6.0V

DC voltage applied to outputs
in high-Z state.. –0.5V to V_{CC} + 1.0V

Input voltage .... –0.5V to V_{CC} + 0.5V

Transient voltage (<20 ns) on
any pin to ground potential .... –1.0V to V_{CC} + 2.0V

Package power dissipation
capability (T_A = 25°C) 1.0W

Surface mount lead soldering
Temperature (3 Seconds).................. +260°C for 10 seconds

Output short circuit current[8] .... 50 mA

Static discharge voltage.. > 2001V
(per MIL-STD-883, Method 3015)

Latch up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	1.65V to 5.5V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 1.65V to 5.5V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{CC1}	Supply Voltage		1.65	5.5	V
I_{SB1}	Standby Current	V_{CC} = 1.65V, $\overline{CS}$ = V_{CC}		1	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}		1.1	µA
I_{SB3}	Standby Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{CC}		1.2	µA
I_{CC1}	Supply Current (Read)	V_{CC} = 5.5V at 4 MHz		2	mA
I_{CC2}	Supply Current (Write)	V_{CC} = 5.5V		2	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		1	µA
I_{LO}	Output Leakage Current	V_{IN} = V_{CC} or V_{SS}		1	µA
V_{IL}	Input LOW Voltage	1.65V ≤ V_{CC} ≤ 2.7V	–0.6 [9]	0.3 V_{CC}	V
		2.7V ≤ V_{CC} ≤ 5.5V	–0.6 [9]	0.8	
V_{IH}	Input HIGH Voltage	1.65V ≤ V_{CC} ≤ 5.5V	0.7 V_{CC}	V_{CC} + 0.5 [9]	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA, 2.7 ≤ V_{CC} ≤ 5.5V		0.4	V
		I_{OL} = 0.15 mA, 1.65 ≤ V_{CC} ≤ 2.7V		0.2	
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA, 1.65 ≤ V_{CC} ≤ 2.7V	V_{CC} – 0.2		V
		I_{OH} = -0.4 mA, 2.7 ≤ V_{CC} ≤ 5.5V	2.4		

Capacitance

In the following table, the capacitance parameters are listed. [10]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 1.65V	5	pF
C_{OUT}	Output Pin Capacitance		5	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed. [10]

| Parameter	Description	Test Conditions	8-SOIC	8-TSSOP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	120.83	119.31	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		90.31	82.77	°C/W

Notes
8. Outputs shorted for only one second. Only one output shorted at a time.
9. This parameter is characterized but not tested.
10. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[+] Feedback

Reliability Characteristics

In the following table, the reliability characteristics parameters are listed. [10]

Parameter	Description	Test Method	Min	Unit
N_{END}	Endurance	JEDEC Standard A117	1 Million	Cycles
T_{DR}	Data Rentention	JEDEC Standard A103	100	Years
I_{LTH}	Latch Up	JEDEC Standard 78	$100 + I_{CC}$	mA

Figure 9. AC Test Loads and Waveforms
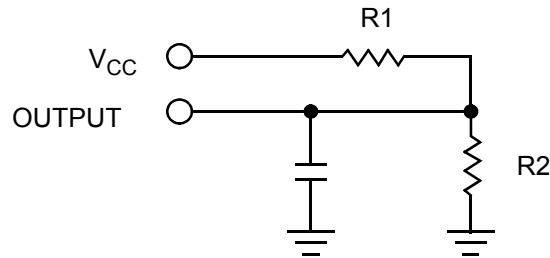
Parameters	1.65V - 2.7V	2.7V - 5.5V	Unit
R1	1.8K	1.8K	ohm
R2	1.3K	1.3K	ohm
C_L	30	100	pF

Figure 10. AC Input/Output Reference Waveforms
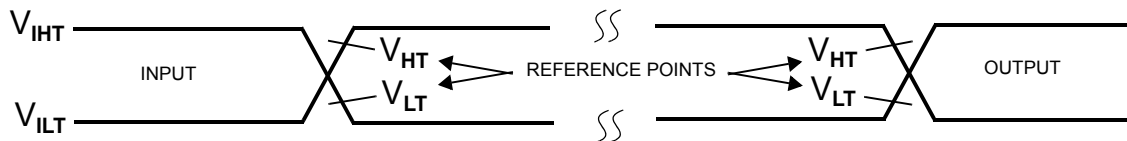
AC test inputs are driven at V_{IHT} ($0.9V_{CC}$) for a logic '1' and V_{ILT} ($0.1V_{CC}$) for a logic '0'. Measurement reference points for inputs and outputs are V_{LT} ($V_{CC}/2 - 0.1V$) and V_{HT} ($V_{CC}/2 + 0.1V$). Input rise and fall times (10%–90%) are <3.3 ns.

[+] Feedback

AC Switching Characteristics

Over the Operating Range (V_{CC}= 1.65V–5.5V)

Cypress Parameter	Alt Parameter	Description	4 MHz		3 Mhz		2 Mhz		1 Mhz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{SK}	f_{SK}	Clock Frequency		4		3		2		1	MHz
t_{CL}	t_{SKLO}	Clock Pulse Width Low	100		130		200		400		ns
t_{CH}	t_{SKHI}	Clock Pulse Width High	100		130		200		400		ns
t_{CE}	t_{CS}	Minimum CS Low Time	100		130		200		400		ns
t_{LZCE}	t_{SV}	Output Valid		100		130		200		400	ns
t_{CES}	t_{CSS}	CS Setup Time	60		50		50		50		ns
t_{CEH}	t_{CSH}	CS Hold Time	0		0		0		0		ns
t_{SD}	t_{DIS}	Data In Setup Time	60		50		100		100		ns
t_{HD}	t_{DIH}	Data In Hold Time	60		50		100		100		ns
t_{CO2}	t_{PD1}	Output Delay to 1		100		130		200		400	ns
t_{CO1}	t_{PD0}	Output Delay to 0		100		130		200		400	ns
t_{HZCE}	t_{HZ}	CS to Data Out in High Impedance		60		150		150		150	ns
t_{WC}	t_{WP}	Write Cycle Time		5		5		5		5	ms
t_F	t_F	Input Fall Time		20		28		45		95	ns
t_R	t_R	Input Rise Time		20		28		45		95	ns

Figure 11. Synchronous Data Timing
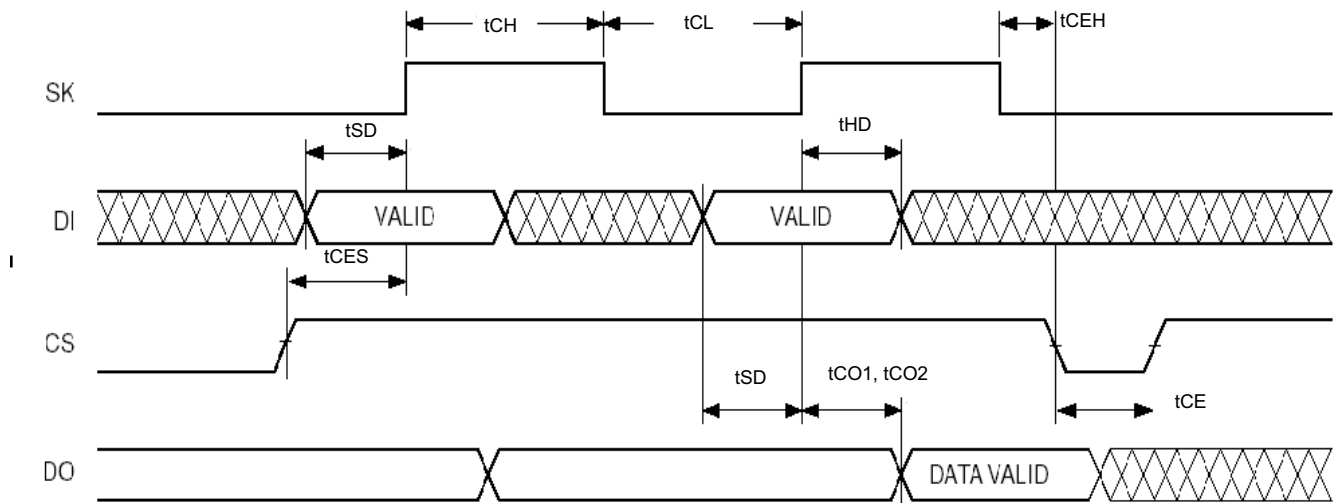
Part Numbering Nomenclature

CY93 C 01 - SX I T

Option:
T = Tape & Reel
Blank = Std.

Temperature:
I = Industrial (–40 to 85°C)

X = Pb-Free

Package:
S = SOIC
Z = TSSOP

Density:
01 = 1 Kb
02 = 2 Kb
04 = 4 Kb
08 = 8 Kb
16 = 16 Kb

Voltage:
C = 1.65V - 5.5V

93 =MicroWire Interface

Cypress
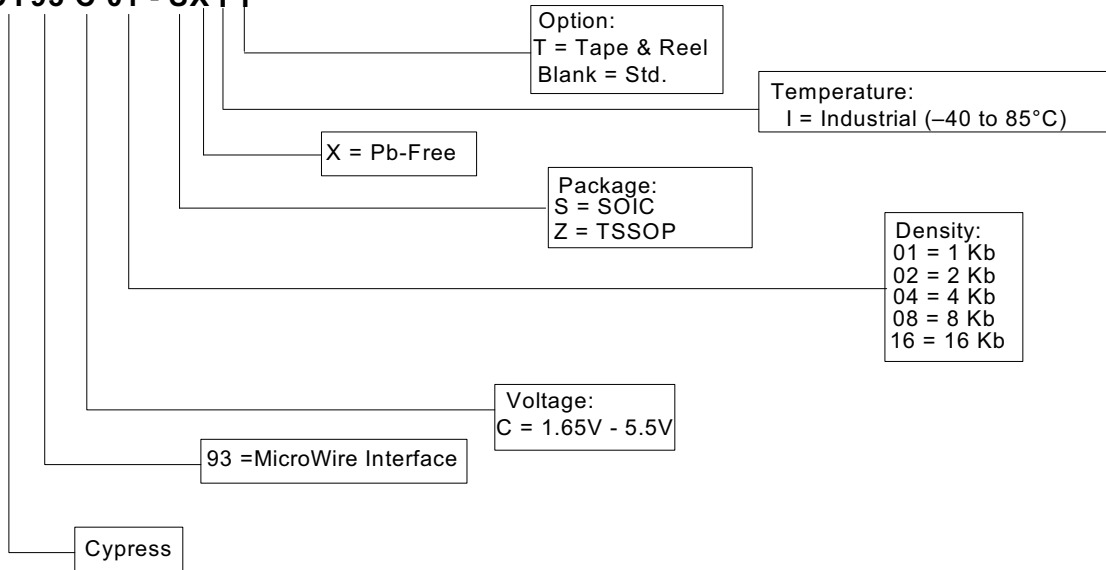
Ordering Information

Density	Ordering Code	Package Diagram	Package Type	Operating Range
1 Kbit	CY93C01-SXI	51-85066	8-Pin SOIC	Industrial
	CY93C01-SXIT		8-Pin SOIC (Tape & Reel)	
	CY93C01-ZXI	51-85093	8-Pin TSSOP	
	CY93C01-ZXIT		8-Pin TSSOP (Tape & Reel)	
2 Kbit	CY93C02-SXI	51-85066	8-Pin SOIC	Industrial
	CY93C02-SXIT		8-Pin SOIC (Tape & Reel)	
	CY93C02-ZXI	51-85093	8-Pin TSSOP	
	CY93C02-ZXIT		8-Pin TSSOP (Tape & Reel)	
4 Kbit	CY93C04-SXI	51-85066	8-Pin SOIC	Industrial
	CY93C04-SXIT		8-Pin SOIC (Tape & Reel)	
	CY93C04-ZXI	51-85093	8-Pin TSSOP	
	CY93C04-ZXIT		8-Pin TSSOP (Tape & Reel)	
8 Kbit	CY93C08-SXI	51-85066	8-Pin SOIC	Industrial
	CY93C08-SXIT		8-Pin SOIC (Tape & Reel)	
	CY93C08-ZXI	51-85093	8-Pin TSSOP	
	CY93C08-ZXIT		8-Pin TSSOP (Tape & Reel)	
16 Kbit	CY93C16-SXI	51-85066	8-Pin SOIC	Industrial
	CY93C16-SXIT		8-Pin SOIC (Tape & Reel)	
	CY93C16-ZXI	51-85093	8-Pin TSSOP	
	CY93C16-ZXIT		8-Pin TSSOP (Tape & Reel)	

Above table contains Preliminary information. Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

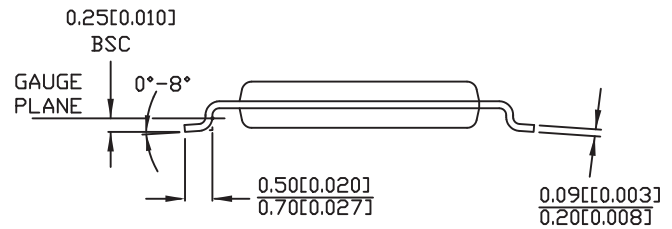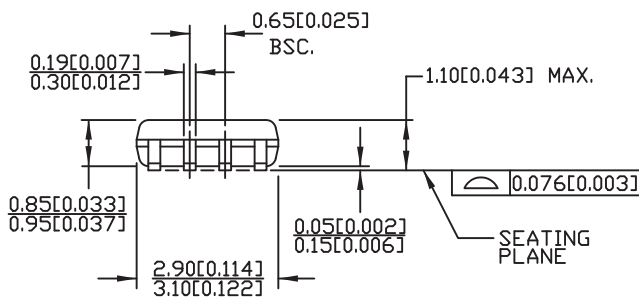### Figure 12. 8-Pin (150-Mil) SOIC, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.
                                                    MAX.

2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME

3. REFERENCE JEDEC MS-012

4. PACKAGE WEIGHT 0.07gms

PART #
S08.15 STANDARD PKG.
SZ08.15 LEAD FREE PKG.

51-85066-*C

[+] Feedback
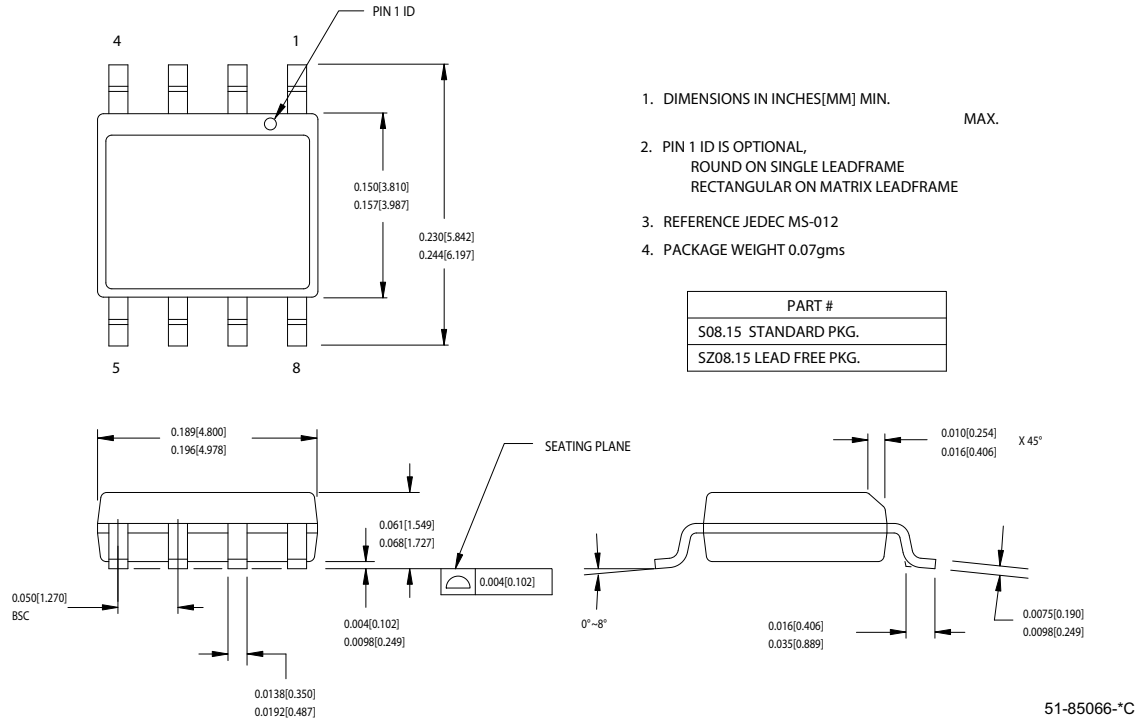
Package Diagrams (continued)

Figure 13. 8-Pin (4.4 mm) TSSOP, 51-85093
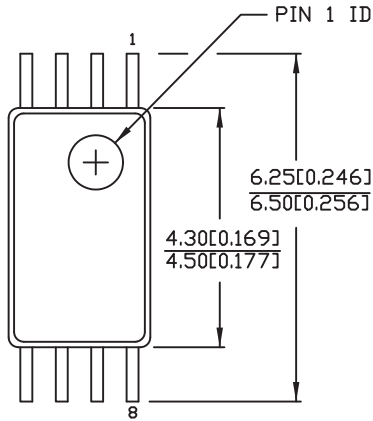
DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PART #	
Z08.173	STANDARD PKG.
ZZ08.173	LEAD FREE PKG.

PIN 1 ID

6.25[0.246]
6.50[0.256]

4.30[0.169]
4.50[0.177]

0.65[0.025]
BSC.

0.19[0.007]
0.30[0.012]

1.10[0.043] MAX.

0.076[0.003]

0.85[0.033]
0.95[0.037]

0.05[0.002]
0.15[0.006]

SEATING
PLANE

2.90[0.114]
3.10[0.122]

0.25[0.010]
BSC

GAUGE
PLANE

0°-8°

0.50[0.020]
0.70[0.027]

0.09[[0.003]
0.20[0.008]

51-85093-*A

Document History Page

Document Title: CY93C01/02/04/08/16, 1 Kbit, 2 Kbit, 4 Kbit, 8 Kbit, and 16 Kbit (x8 or x16) MicroWire Serial EEPROM Document Number: 001-15635				
Revision	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1069220	UHA	See ECN	New Data Sheet
*A	2522135	GVCH/PYRS	06/27/08	Added Pb-Free and RoHS Compliant information in Features Removed PDIP package Removed Automotive Temperature range Changed Supply voltage on V_{CC} relative to GND max value from 5.0V to 6.0V Corrected Typo of Vcc max value from 5.0V to 5.5V Added AC test load values for different parameters Table 10: Updated AC Switching Characteristics Table 8: Added Thermal Resistance values for 8-TSSOP packages Table 9: Changed T_{DR} value from 20 to 100 years Updated Part Numbering Nomenclature and Ordering Information
*B	2611873	VKN/PYRS	11/24/08	Updated Part numbering nomenclature Updated Ordering information table
*C	2656511	VKN/AESA	02/09/09	Changed part# from CY93C46/56/66/76/86 to CY93C01/02/04/08/16 Converted from preliminary to final Included V_{IL} spec of 0.8V for the V_{CC} range between 2.7V to 5.5V Updated V_{IH} test conditions Added footnote #9 Updated V_{OL} and V_{OH} test conditions On page 10, Specified V_{CC} range for AC test load conditions On page 10, corrected AC measurement reference points from V_{IT} and V_{OT} to V_{LT} and V_{HT} respectively Changed V_{LT} level from $0.3V_{CC}$ to $V_{CC}/2 - 0.1V$ Changed V_{HT} level from $0.7V_{CC}$ to $V_{CC}/2 + 0.1V$

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