FAIRCHILD
A Schlumberger Company

F9444
Memory Management and Protection Unit

Advance Product Information

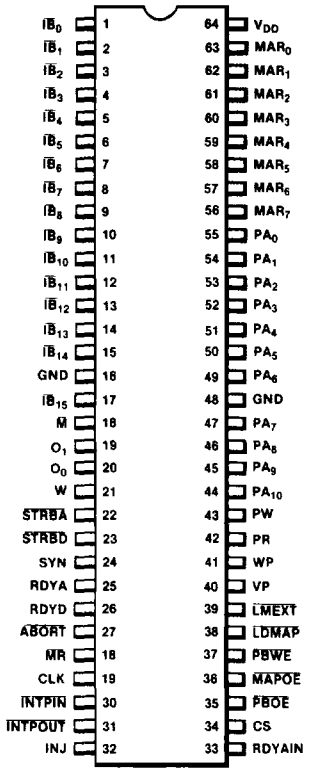
Microprocessor Product

Description

The Fairchild F9444 programmable Memory Management and Protection Unit (MMPU) is designed to support complex multi-user and large single-user environments. With four F93422 bipolar static random-access memories (RAMs) serving as map memory, the F9444 expands the physical address space of the F9445 16-bit microprocessor to 2M words by performing logical-to-physical address translation. That is, the six most significant bits (MSBs) of the logical address are translated into 11 physical address bits, leaving the 10 least significant bits (LSBs) of the logical address unchanged. The memory thus consists of 21 bits (10 LSB and 11 MSB), or 4 megabytes. System integrity is maintained by access protection bits associated with each page. Any violation causes non-maskable interrupt to the F9445 central processing unit. Page-written (PW) and page-referenced (PR) bits permit the implementation of demand-paging algorithms. Figure 1 is a functional diagram of the MMPU.

- **Standard Input/Output (I/O) Instruction Format**
- **Ability to Implement Demand-Paged Virtual Memory System**
- **Ability to Access Up to 2M Words of Memory**
- **2K Pages, With 1K Words for Each Page**
- **Memory Expansion Through Mapping and Demand Paging**
- **Controls for Memory Mapping**
- **Separate RAMs for Storing Maps**
- **Access and I/O Protection to Maintain System Integrity**
- **Special Status Bits for Read/Write Protection, Demand Paging, and I/O Protection**
- **Support for Two User and Two Data Channel Maps**
- **Low-Power Schottky-Compatible I/O**
- **Single +5 V Power Supply**
- **64 Pin Dual-In-Line Package (DIP)**
- **I^3L® Technology**

Connection Diagram



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Maps

The MMPU allows two user maps and two data channel maps to reside in map memory. Each data channel map contains 32 1K-word pages and each user map either 32 or 64 1K-word pages that can be relocated anywhere in memory. The two user maps and two data channel maps function independently. Only one user map can be enabled at a time, but both data channel maps are enabled at the same time. The supervisor determines whether the mapping of program address and data channel address are to be enabled at the same time. If either user mapping or data channel mapping is disabled, the physical address space for that function is equal to the logical address space and only the lowest 64K words can be accessed.

Signal Functions

Figure 1 F9444 Functional Diagram