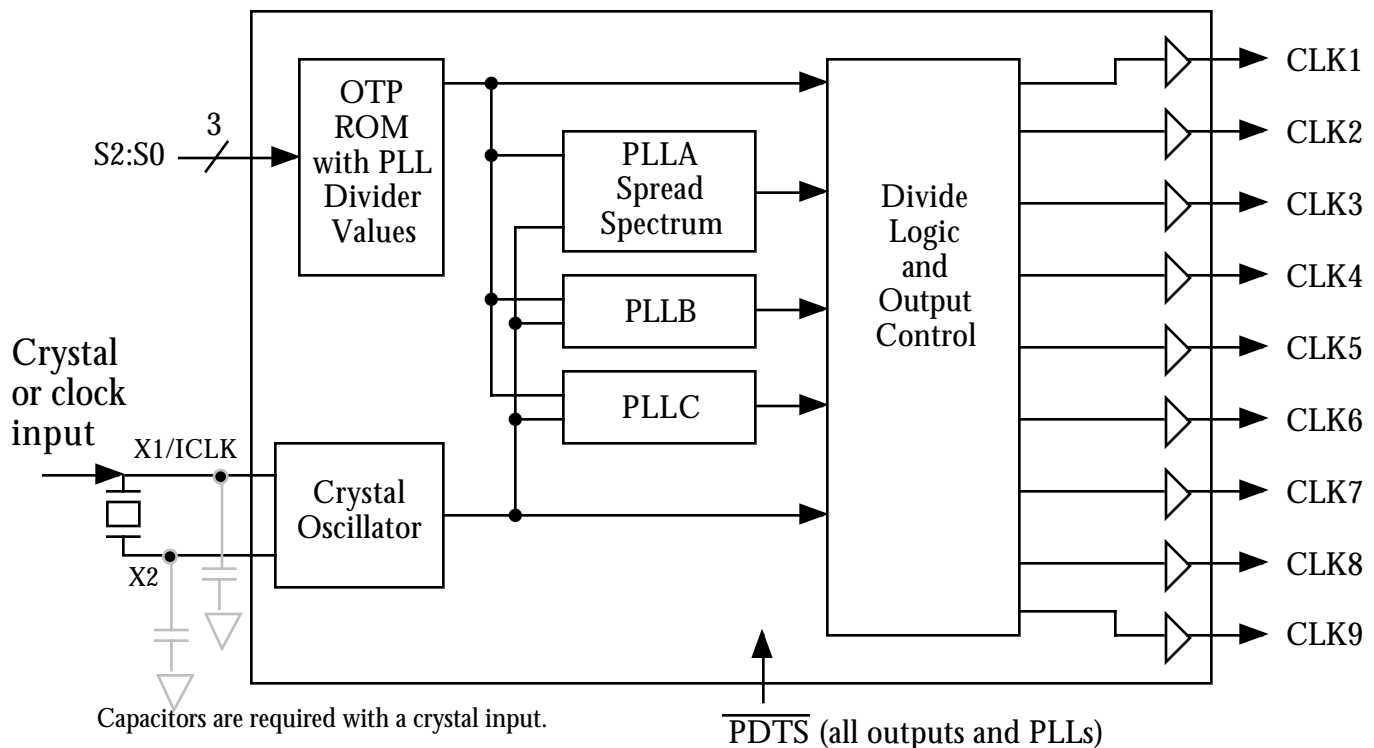# Triple PLL Quick Turn Clock Synthesizer

Description

The ICS355 QTClock™ generates up to 9 high quality, high frequency clock outputs including a reference from a low frequency crystal or clock input. It is designed to replace crystals and crystal oscillators in most electronic systems. The ICS355 contains a One Time Programmable (OTP) ROM which is factory programmed with PLL divider values to output a broad range of frequencies up to 200 MHz, allowing customer requests for different frequencies to be shipped in 1-3 days. Programming features include a selectable frequency table, up to 4 low-skew outputs, and optional Spread Spectrum on PLLA.
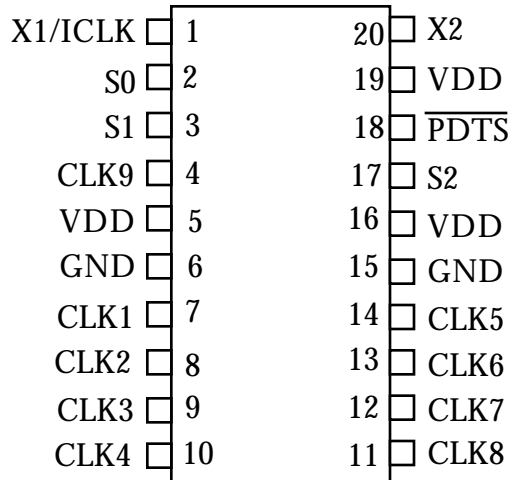
Using Phase-Locked-Loop (PLL) techniques, the device runs from a standard fundamental mode, inexpensive crystal, or clock. It can replace multiple crystals and oscillators, saving board space and cost.

Features

- Packaged as 20 pin SSOP (QSOP)
- Quick turn frequency programming allows samples as quickly as one day
- Up to 4 outputs can be low-skew
- Spread-Spectrum capability included
- Can include 8 selectable output frequencies
- Up to 5 reference outputs
- Replaces multiple crystals and oscillators
- Output frequencies up to 200 MHz at 3.3V
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Duty cycle of 45/55
- Operating voltages of 3.3 V or 5 V
- Advanced, low power CMOS process

Block Diagram

Capacitors are required with a crystal input.

$\overline{PDTS}$ (all outputs and PLLs)

Pin Assignments

```
        X1/ICLK  □  1        20  □  X2
             S0  □  2        19  □  VDD
             S1  □  3        18  □  PDTS
           CLK9  □  4        17  □  S2
            VDD  □  5        16  □  VDD
            GND  □  6        15  □  GND
           CLK1  □  7        14  □  CLK5
           CLK2  □  8        13  □  CLK6
           CLK3  □  9        12  □  CLK7
           CLK4  □ 10        11  □  CLK8
```

20 pin (150 mil) SSOP

Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	XI	Crystal connection. Connect to fundamental mode crystal or clock input.
2	S0	I	Select pin 0 for frequency table/chip control. Internal pull-up resistor.
3	S1	I	Select pin 1 for frequency table/chip control. Internal pull-up resistor.
4	CLK9	O	Clock output.
5	VDD	P	Connect to +3.3V or +5V. Must be same voltage as pins 16 and 19.
6	GND	P	Connect to ground.
7	CLK1	O	Clock output.
8	CLK2	O	Clock output.
9	CLK3	O	Clock output.
10	CLK4	O	Clock output.
11	CLK8	O	Clock output.
12	CLK7	O	Clock output.
13	CLK6	O	Clock output.
14	CLK5	O	Clock output.
15	GND	P	Connect to ground.
16	VDD	P	Connect to +3.3V or +5V. Must be same voltage as pins 5 and 19.
17	S2	I	Select pin 2 for frequency table/chip control. Internal pull-up resistor.
18	$\overline{PDTS}$	I	All-chip Power Down when low. Note 1.
19	VDD	P	Connect to +3.3V or +5V. Must be same voltage as pins 5 and 16.
20	X2	XO	Crystal connection. Leave unconnected for clock input.

Key: XI, XO = crystal connections, I = Input, O = output, P = power supply connection
Note 1: All outputs are internally high impedance with a weak internal pull-down resistor. When $\overline{PDTS}$ is active, it is possible to overdrive the output pins for board-level testing.

Device Configuration

The ICS355 QTClock provides the facility for up to 9 clock outputs. The outputs are derived from either the reference input or from one of the 3 PLLs. All chip functions are controlled from an OTP ROM which has 3 input control lines (S2, S1, S0), giving a total of 8 address locations. Each address location gives control of the following:

1) Each output can be turned off individually
2) The internal dividers for each PLL are controlled to generate any required frequency.
3) Each PLL can be turned off (powered down) individually.
4) The spread spectrum function available on PLLA can be enabled or disabled
5) The output divide and control logic can be configured to bring the appropriate clock to the correct pin.
6) Up to four low skew copies of the same clock can be enabled.

This chip architecture provides the user with unrivaled flexibility. For example, one of the input pins could be dedicated to enabling/disabling spread spectrum, a second could be used to control the power of the chip by shutting down PLLs and outputs when not used. The third could be used to change the output clock frequencies.

The specification is complete when the ICS355 QTClock Order Form accompanies this data sheet. The order form lists the input and CLK actual frequencies, as well as any other available options. This unique configuration is given a two character alphanumeric programming code (ICS355-xx), which must be specified when referring to samples.

Frequency Select Table

The ICS355 can be configured so that one PLL provides up to 8 frequency selections. For example, CPU frequencies of 66.7 MHz, 100.0 MHz, 133.3 MHz, and 166.7 MHz could be included. This information should be indicated on the Order Form when the ICS355 is initially defined.

External Components / Crystal Selection

The ICS355 requires a 0.01µF decoupling capacitor to be connected between VDD and GND on pins 5 and 6, and another between pins 16 and 15. These must be connected close to the ICS355 to minimize lead inductance. No external power supply filtering is required for this device. A 33 series terminating resistor can be used next to each CLK pin. For a crystal input, a parallel resonant, fundamental mode crystal should be used. Crystal capacitors must be connected from each of the pins X1 and X2 to Ground. The value (in pF) of these crystal caps should equal $(C_L\text{-}6pf)*2$, where C_L is the crystal load capacitance in pF. As an example, for a crystal with 16 pF load capacitance, each crystal capacitor would be XX pF $[(16 - 6pf)*2 = 20]$.

For a clock input, connect to X1/ICLK and leave X2 unconnected (no capacitors on either X1 or X2).

Triple PLL Quick Turn Clock Synthesizer

Electrical Specifications

| Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature	Commercial version	0		70	°C
Ambient Operating Temperature	Industrial version	-40		85	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V unless otherwise noted)					
Operating Voltage, VDD		3.13		5.5	V
Input High Voltage, VIH, ICLK only	ICLK (Pin 1)	(VDD/2)+1			V
Input Low Voltage, VIL, ICLK only	ICLK (Pin 1)			(VDD/2)-1	V
Input High Voltage, VIH	$\overline{PDTS}$, S0, S1, S2	2			V
Input Low Voltage, VIL	$\overline{PDTS}$, S0, S1, S2			0.8	V
Output High Voltage, VOH	IOH=-4mA	VDD-0.4			V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
IDD Operating Supply Current, 20 MHz crystal	No Load, 100MHz		20		mA
Short Circuit Current	CLK output		±70		mA
On-Chip Pull-up Resistor, inputs			TBD		k
On-Chip Pull-down Resistor, outputs			TBD		
Input Capacitance, inputs			4		pF
AC CHARACTERISTICS (VDD = 3.3V unless otherwise noted)					
Input Frequency, crystal input		5		27	MHz
Input Frequency, clock input		2		50	MHz
Output Frequency		2		200	MHz
Output Clock Rise Time	0.8 to 2.0V		1		ns
Output Clock Fall Time	2.0 to 0.8V		1		ns
Output Clock Duty Cycle (Note 1)	at VDD/2	45	49 to 51	55	%
Absolute Clock Period Jitter	Deviation from mean		±TBD		ps
One Sigma Clock Period Jitter			TBD		ps
Pin to Pin Skew	Low skew outputs	-250		250	ps
Power-up time, $\overline{PDTS}$ goes high until CLK out			8	20	ms

Note 1:   These are typical values. The actual minimum and maximum duty cycle limits are shown on the
ICS355 QTClock Order Form for each programmed version.

Package Outline and Package Dimensions
(For current dimensional specifications, see JEDEC Publication No. 95.)

20 pin SSOP
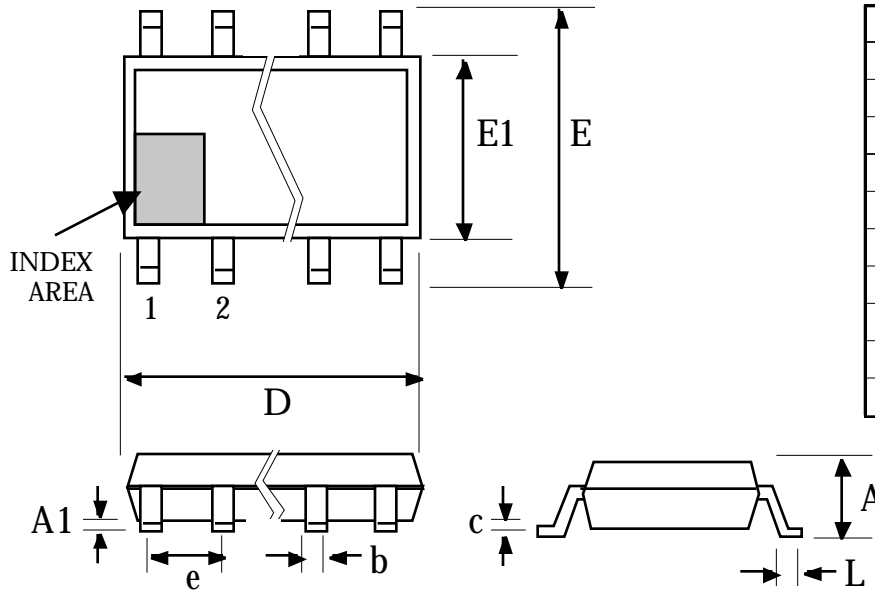
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
D	0.337	0.344	8.55	8.75
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.80	6.20
E1	0.150	0.157	3.80	4.00
L	0.016	0.050	0.40	1.27

Ordering Information

Part/Order Number	Marking	Package	Shipping	Temperature
ICS355R-xx	ICS355R-xx	20 pin SSOP	Tubes	0 to 70 °C
ICS355R-xxT	ICS355R-xx	20 pin SSOP	Tape and Reel	0 to 70 °C
ICS355R-xxI	ICS355R-xxI	20 pin SSOP	Tubes	-40 to 85 °C
ICS355R-xxIT	ICS355R-xxI	20 pin SSOP	Tape and Reel	-40 to 85 °C

xx represents a 2 character alphanumeric programming code assigned by the factory, which indicates the output frequencies on all CLKs and other features. All samples are shipped with an ICS355 order form describing the characteristics of the device.

QTClock is a trademark of ICS