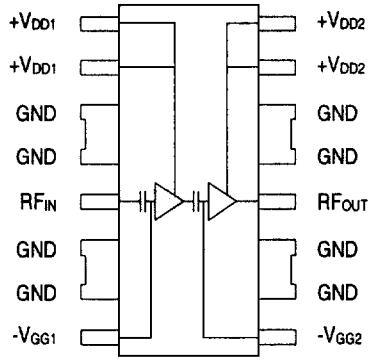
4.6V 1.0W RF Power Amplifier IC for ISM900
ITT333103BD

Applications

900 MHz ISM
Cordless Telephones
Wireless Modems
N-PCS

Features

- Class AB Bias
- 850 to 1000 MHz Operation
- 50 Ω Input Impedance
- Simple 2 Element Output Match
- Small Size — 16 Pin Narrow Body SOIC Plastic Package
- Self-Aligned MSAG®-Lite MESFET Process
- Guaranteed Stability and Ruggedness



16 pin narrow body SOIC

Typical 4.6 Volt Performance

30 dBm Power Output
25 dB Power Gain
57% Power Added Efficiency
-35 dBc 2nd Harmonic
-45 dBc 3rd Harmonic

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 1, 2, 15, 16)	V_{DD}	10	Vdc
DC Gate Bias Voltage (Pins 8,9)	V_{GG}	-5	Vdc
RF Input Power	P_{IN}	-15	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-40 to +150	°C

ELECTRICAL CHARACTERISTICS V_{DD}=4.6 V, P_{IN}=+5 dBm, T_S=30 °C (See Note 1), Output externally matched to 50 Ω System

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	—	900	—	942	MHz
Load Power (V_{GG} adjusted for desired output power)	P_{OUT}	1.0	—	—	W
Power Gain (P_{OUT} = 30 dBm)	G_P	25	—	—	dB
Drain Current (P_{OUT} = 30 dBm)	I_{DD}	—	379	417	mA
Harmonics (P_{OUT} = 30 dBm)	$2f_o$	—	-35	-30	dBc
	$3f_o$	—	-45	-40	dBc
Input VSWR (P_{OUT} = 30 dBm), 50 Ω Ref.	—	—	1.5:1	2.0:1	—
Thermal Resistance (Junction of 2nd stage FET to solder point of pin 11)	$R_{TH\ J\text{-}S}$	—	—	24	°C/W
Load Mismatch (V_{DD} = 8.5 V, VSWR = 10:1)	—	No Degradation in Power Output			
Stability (P_{IN}=-3 to +12 dBm, V_{DD}=0-8.5 V, 0 mW < P_{OUT} < 1.0 W, T_S=-40 to +100 °C, Load VSWR = 10:1)	—	All non-harmonically related outputs more than 60 dB below desired signal			

Note 1: T_s is the temperature measured at the soldering point of pin 11, mounted on 60 mil GETEK evaluation board in a free air condition with ambient room temperature T_A=25°C. The electrical data presented herein was taken with the evaluation board shown in Figures 1 & 13, under room temperature conditions , operating at 1.0 W of load power (V_{DD} = 4.6 V), unless otherwise specified.

APPLICATION INFORMATION

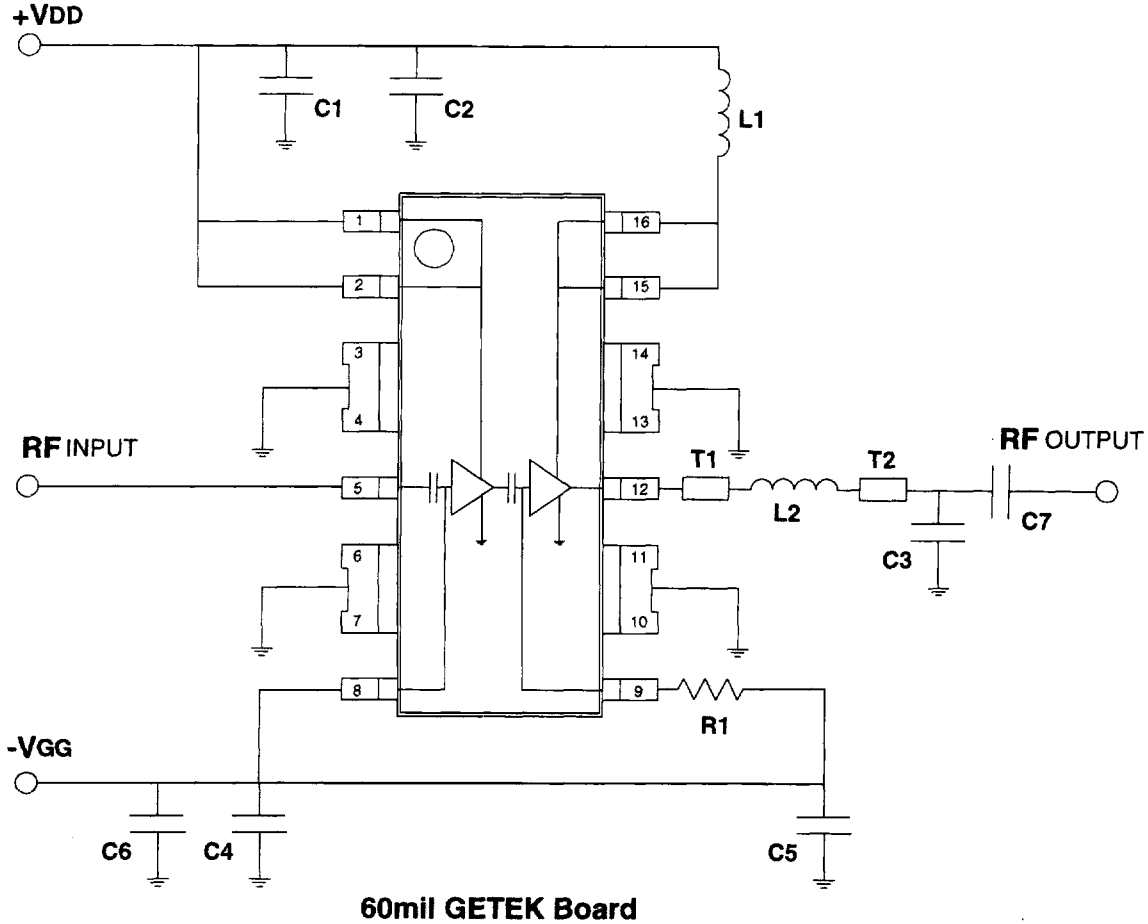


Figure 1. Evaluation Board Schematic

List of components:

C1 = C4 = C5 = 4700 pF Kemet multilayer ceramic chip capacitor (C0805C472K5RAC)
C2 = C6 = 0.1µF Kemet multilayer ceramic chip capacitor (C1206C104K5RAC)
C3 = 5.6 pF DLI multilayer ceramic chip capacitor (C11AH5R6B5TXL)
C7 = 100 pF DLI multilayer ceramic chip capacitor (DC Block; C11AH101K5TXL)
L1 = 39 nH Coilcraft chip inductor (1008CS.390XMBB)
L2 = 2.2 nH Toko chip inductor (TKS2361CTND)
R1 = 100 Ω chip resistor
T1 = 0.10" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)
T2 = 0.05" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)

Component layout and printed circuit board drawing for RF IC evaluation board are shown in Figure 13.

Biasing: Gate bias voltage (V_{GG}) must be applied prior to RF input power and drain bias voltage (V_{DD}). Reverse the sequence when turning the part off — remove the RF input and drain bias before removing gate bias.

TYPICAL CHARACTERISTICS

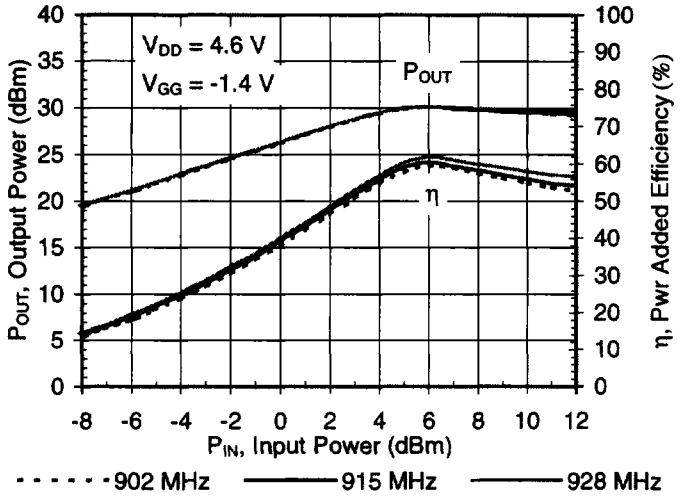


Figure 2. Output power and efficiency vs. input power for a fixed gate bias

Conditions for Figure 2:
Gate bias (V_{GG}) is set for 1.0 W of output power when P_{IN} = 5 dBm.

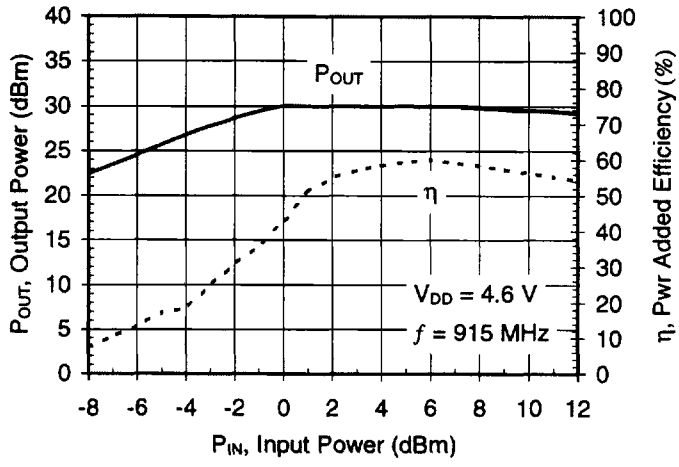


Figure 3. 1.2 Watt output power capability and efficiency vs. input power

Conditions for Figure 3:
Control voltage (V_{GG}) is adjusted at each input power level in an attempt to maintain 1.0 W output power.

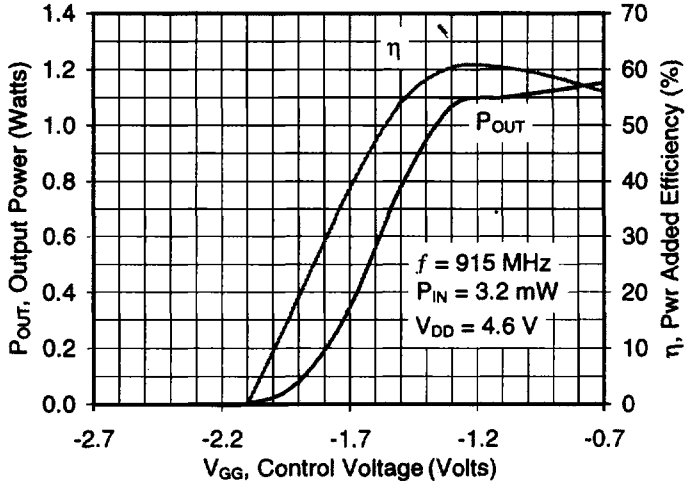


Figure 4. Output power and efficiency vs. control voltage

Conditions for Figure 4:
While keeping supply voltage constant (V_{DD} = 4.6 V), the output power is controlled by adjusting DC gate bias (V_{GG}).

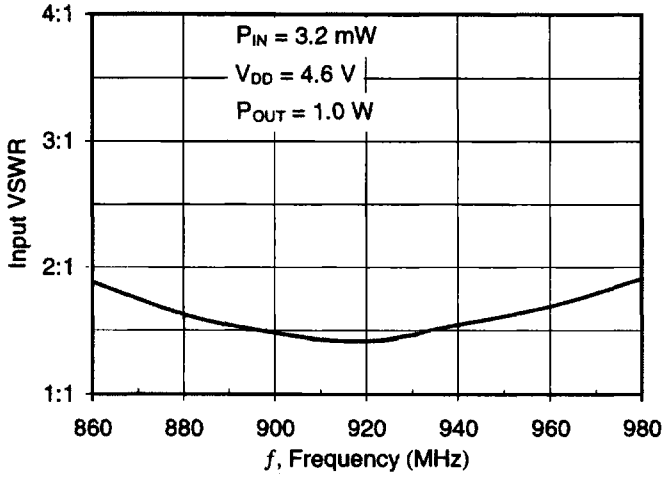


Figure 5. Input VSWR vs . frequency

Conditions for Figure 5:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.0 W output power.

TYPICAL CHARACTERISTICS

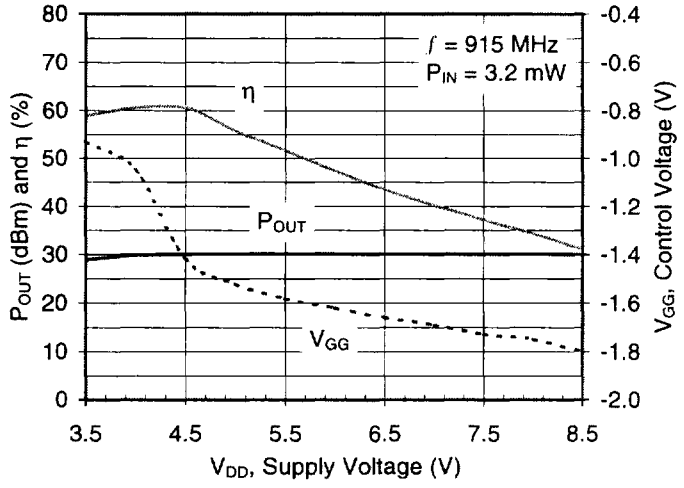


Figure 6. Output power, efficiency, and control voltage vs. supply voltage

Conditions for Figure 6:
Control voltage (V_{GG}) is adjusted for each supply voltage in an attempt to maintain 1.0 W output power.

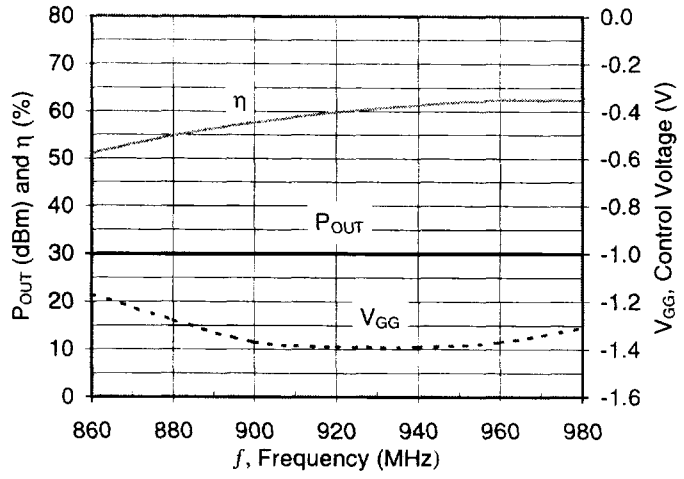


Figure 7. Output power, efficiency, and control voltage vs. frequency

Conditions for Figure 7:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.0 W output power. V_{DD}=4.6 V, P_{IN}=5 dBm.

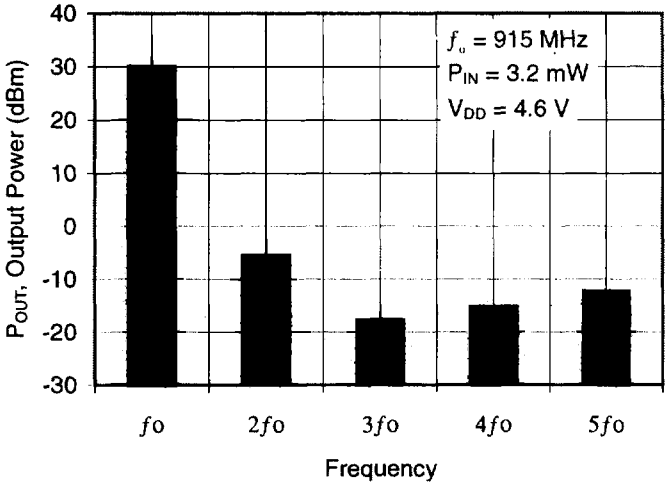


Figure 8. Harmonics

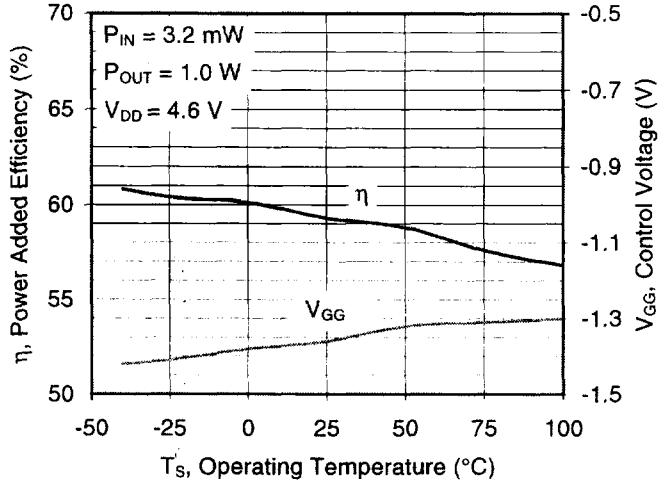


Figure 9. Power added efficiency and control voltage vs. temperature

Conditions for Figure 9:
Control voltage is adjusted for each temperature to maintain 1.0 W output power. Data was taken at f = 900 MHz.

TYPICAL CHARACTERISTICS

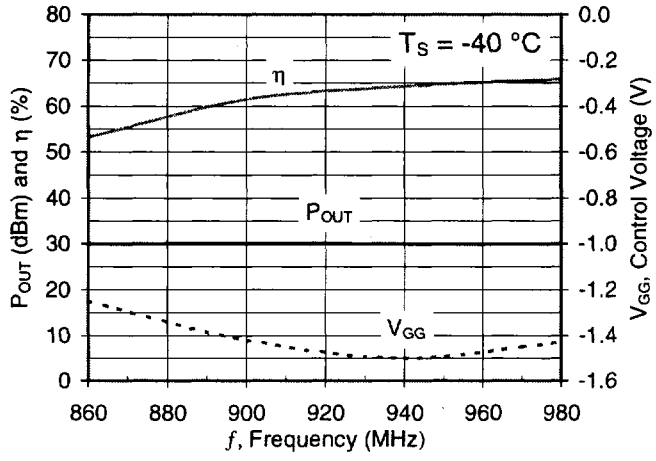


Figure 10. Output power, efficiency, and control voltage vs. frequency for T_S = -40°C

Conditions for Figure 10:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.0 W output power. V_{DD}=4.6 V, P_{IN}=5 dBm.

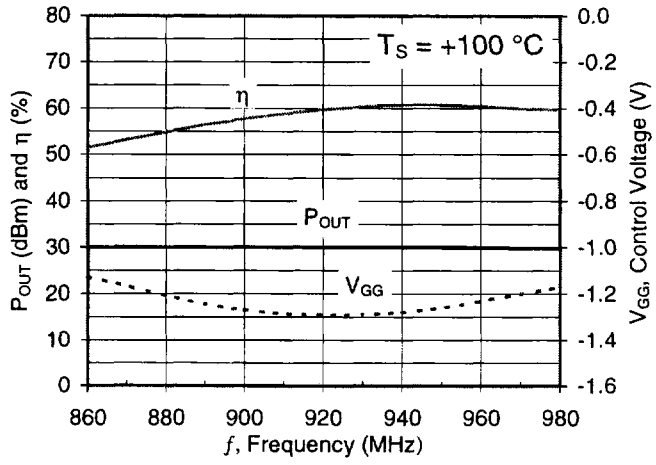


Figure 11. Output power, efficiency, and control voltage vs. frequency for T_S = +100°C

Conditions for Figure 11:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.0 W output power. V_{DD}=4.6 V, P_{IN}=5 dBm.

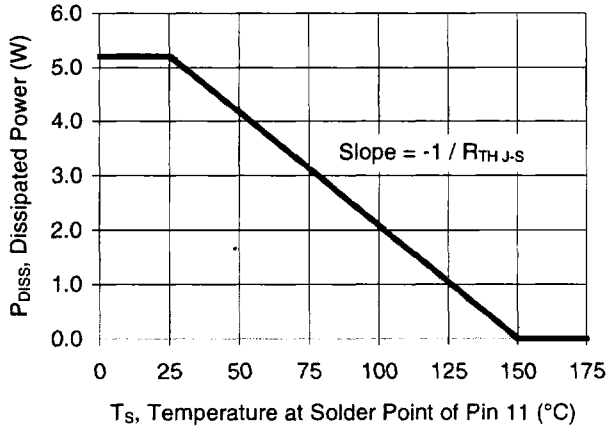
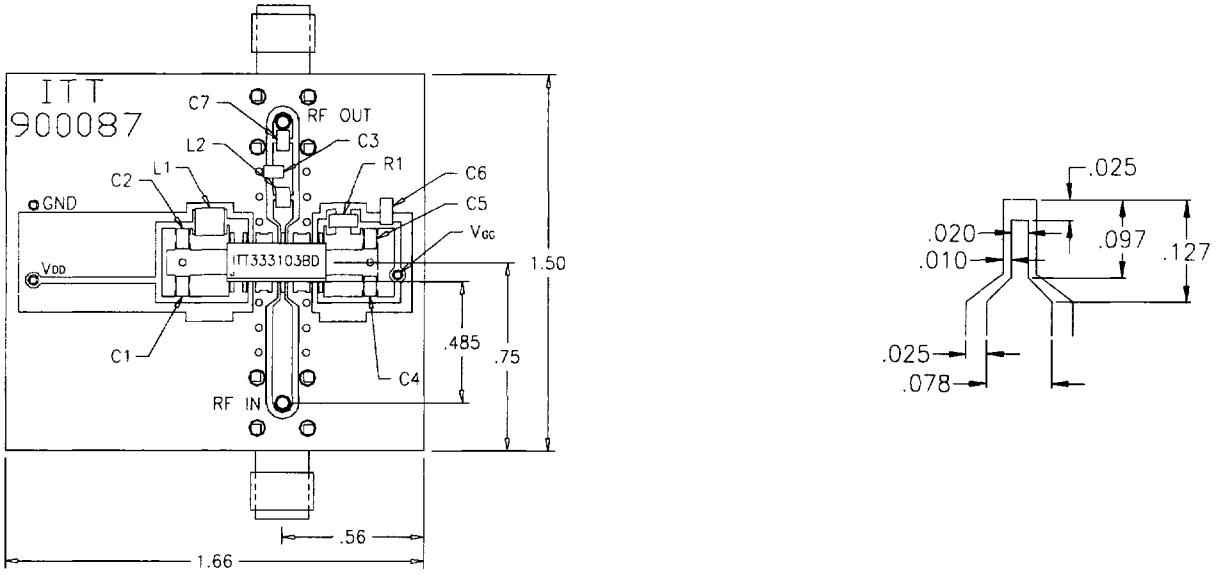


Figure 12. Maximum operating temperature chart

Conditions for Figure 12:

- $P_{DISS} = I_{DD2} * V_{DD} - P_{OUT}$, which refers to the dissipated power in the hottest area of the IC (Stage 2 FET). Stage 1 power dissipation and Stage 2 input power have negligible effect on IC maximum temperature located in Stage 2.
- I_{DD2} is typically 85% of I_{DD}.

MECHANICAL DATA



Top view **50Ω lead transition**

Figure 13. Component layout and printed circuit drawing for evaluation board.

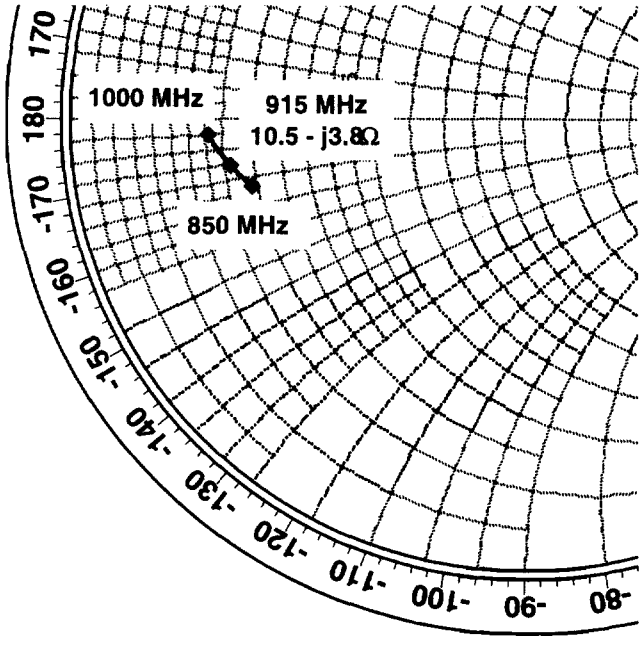


Figure 14. Output match impedance (as seen from pin 12)