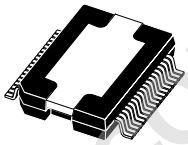
# STA506

## 40V 4A QUAD POWER HALF BRIDGE

- MINIMUM INPUT OUTPUT PULSE WIDTH DISTORTION
- 200mΩ $R_{dsON}$ COMPLEMENTARY DMOS OUTPUT STAGE
- CMOS COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- THERMAL WARNING OUTPUT
- UNDER VOLTAGE PROTECTION

**MULTIPOWER BCD TECHNOLOGY**



**PowerSO36**

**ORDERING NUMBER: STA506**

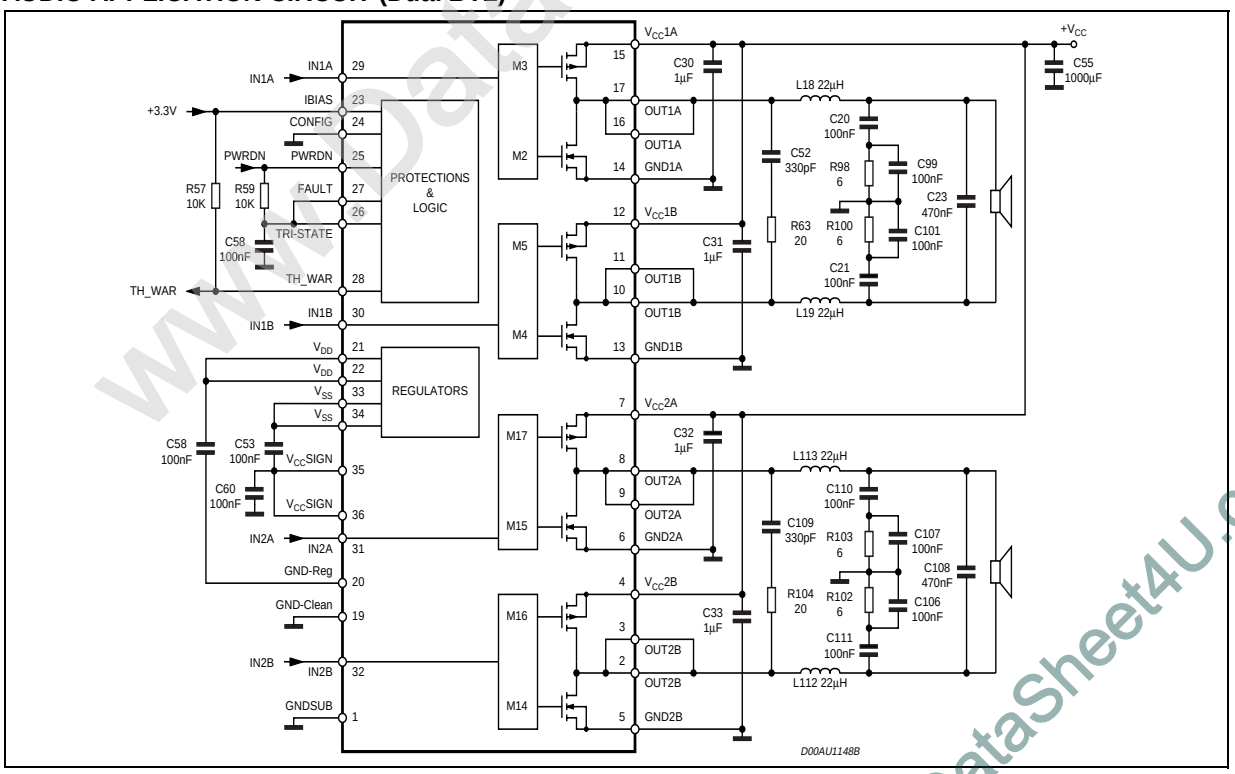
### DESCRIPTION

STA506 is a monolithic quad half bridge stage in Multipower BCD Technology. The device can be used as dual bridge or reconfigured, by connecting CONFIG pin to Vdd pin, as single bridge with double current capability, and as half bridge (Binary mode) with half current capability.

The device is particularly designed to make the output stage of a stereo All-Digital High Efficiency (DDX™) amplifier capable to deliver 60 + 60W @ THD = 10% at $V_{cc}$ 32V output power on 8Ω load and 80W @ THD = 10% at $V_{CC}$ 36V on 8Ω load in single BTL configuration. In single BTL configuration is also capable to deliver a peak of 120W @THD = 10% at $V_{CC}$ = 32V on 4Ω load (t ≤1sec)

The input pins have threshold proportional to Ibias pin voltage.

### AUDIO APPLICATION CIRCUIT (Dual BTL)






www.DataSheet4U.com

**PIN FUNCTION**

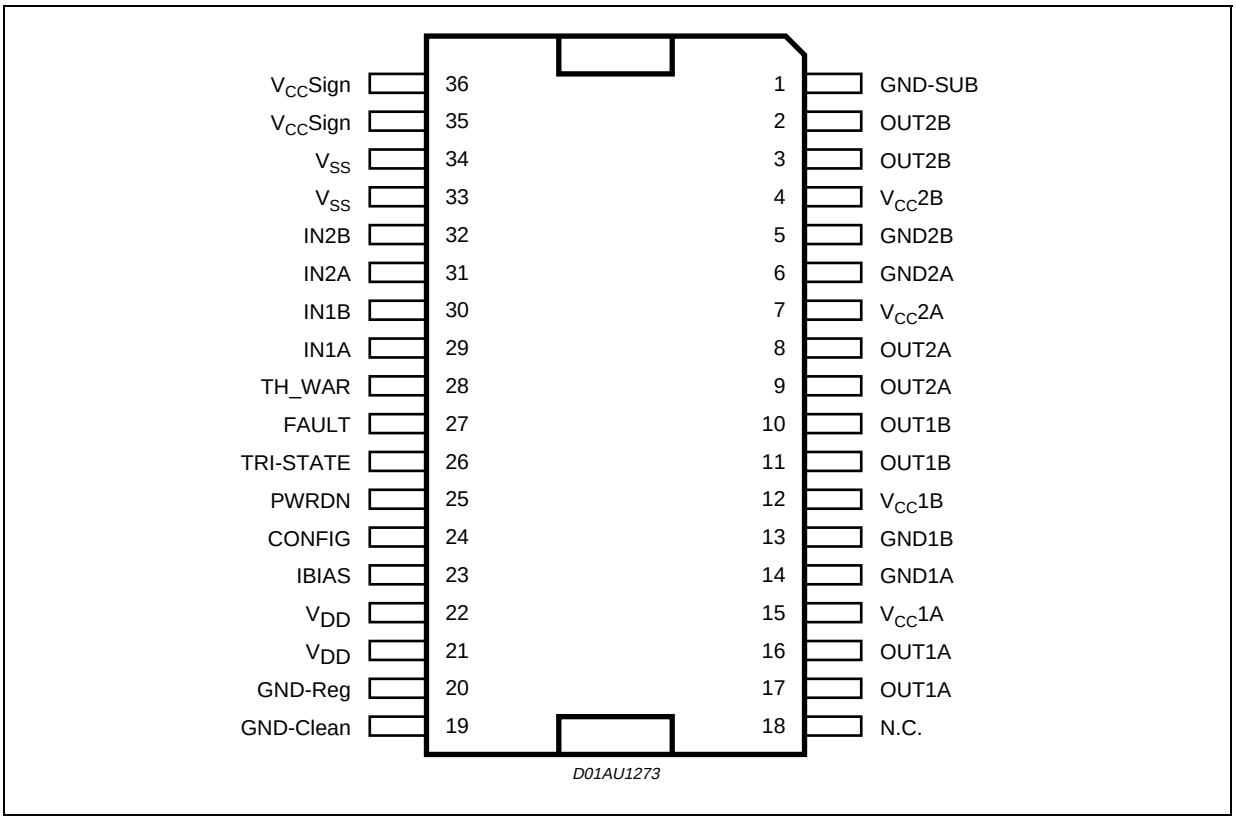
| N° | Pin | Description |
|---|---|---|
| 1 | GND-SUB | Substrate Ground |
| 35 ; 36 | $V_{CC}$ Sign | Signal Positive Supply |
| 15 | $V_{CC}$1A | Positive Supply |
| 12 | $V_{CC}$1B | Positive Supply |
| 7 | $V_{CC}$ 2A | Positive Supply |
| 4 | $V_{CC}$ 2B | Positive Supply |
| 14 | GND1A | Negative Supply |
| 13 | GND1B | Negative Supply |
| 6 | GND2A | Negative Supply |
| 5 | GND2B | Negative Supply |
| 16 ; 17 | OUT1A | Output Half Bridge 1A |
| 10 ; 11 | OUT1B | Output Half Bridge 1B |
| 8 ; 9 | OUT2A | Output Half Bridge 2A |
| 2 ; 3 | OUT2B | Output Half Bridge 2B |
| 29 | IN1A | Input of Half Bridge 1A |
| 30 | IN1B | Input of Half Bridge 1B |
| 31 | IN2A | Input of Half Bridge 2A |
| 32 | IN2B | Input of Half Bridge 2B |
| 21 ; 22 | $V_{dd}$ | 5V Regulator Referred to Ground |
| 33 ; 34 | $V_{SS}$ | 5V Regulator Referred to +$V_{CC}$ |
| 25 | PWRDN | Stand-by pin |
| 26 | TRI-STATE | Hi-Z pin |
| 27 | FAULT | Fault pin Advisor |
| 24 | CONFIG | Configuration pin |
| 28 | TH-WAR | Thermal Warning Advisor |
| 19 | GND-clean | Logical Ground |
| 23 | IBIAS | High Logical State Setting Voltage |
| 18 | NC | Not Connected |
| 20 | GND-Reg | Ground for Regulator $V_{dd}$ |

## FUNCTIONAL PIN STATUS

| PIN NAME | Logical value | IC -STATUS |
|---|---|---|
| FAULT | 0 | Fault detected (Short circuit, or Thermal ..) |
| FAULT (*) | 1 | Normal Operation |
| TRI-STATE | 0 | All powers in Hi-Z state |
| TRI-STATE | 1 | Normal operation |
| PWRDN | 0 | Low absorpion |
| PWRDN | 1 | Normal operation |
| THWAR | 0 | Temperature of the IC =130°C |
| THWAR(*) | 1 | Normal operation |
| CONFIG | 0 | Normal Operation |
| CONFIG(**) | 1 | OUT1A = OUT1B ; OUT2A=OUT2B<br>(IF IN1A = IN1B; IN2A = IN2B) |

(*) : The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.
(**): To put CONFIG = 1 means connect Pin 24 (CONFIG) to Pins 21, 22 (Vdd)

## PIN CONNECTION




## THERMAL DATA

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal Resistance Junction-case | max 1.5 | °C/W |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CE}$ | DC Supply Voltage (Pin 4,7,12,15) | 40 | V |
| $V_{max}$ | Maximum Voltage on pins 23 to 32 | 5.5 | V |
| $P_{tot}$ | Power Dissipation ($T_{case}$ = 70°C) | 50 | W |
| $T_{op}$ | Operating Temperature Range | 0 to 70 | °C |
| $T_{stg}$, $T_j$ | Storage and Junction Temperature | -40 to 150 | °C |

## THERMAL DATA

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{j\text{-}case}$ | Thermal Resistance Junction to Case (thermal pad) | | | 2.5 | °C/W |
| $T_{jSD}$ | Thermal shut-down junction temperature | | 150 | | °C |
| $T_{warn}$ | Thermal warning temperature | | 130 | | °C |
| $t_{hSD}$ | Thermal shut-down hysteresis | | 25 | | °C |

## ELECTRICAL CHARACTERISTCS ($I_{bias}$ = 3.3V; $V_{CC}$ = 30V; $T_{amb}$ = 25°C unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_{dsON}$ | Power Pchannel/Nchannel MOSFET RdsON | Id=1A | | 200 | 270 | mΩ |
| $I_{dss}$ | Power Pchannel/Nchannel leakage Idss | $V_{CC}$ =35V | | | 50 | µA |
| $g_N$ | Power Pchannel RdsON Matching | Id=1A | 95 | | | % |
| $g_P$ | Power Nchannel RdsON Matching | Id=1A | 95 | | | % |
| Dt_s | Low current Dead Time (static) | see test circuit no.1; see fig. 1 | | 10 | 20 | ns |
| Dt_d | High current Dead Time (dinamic) | L=22µH; C = 470nF; $R_L$ = 8 Ω Id=3.5A; see fig. 3 | | | 50 | ns |
| $t_{d\ ON}$ | Turn-on delay time | Resistive load | | | 100 | ns |
| $t_{d\ OFF}$ | Turn-off delay time | Resistive load | | | 100 | ns |
| $t_r$ | Rise time | Resistive load; as fig.1 | | | 25 | ns |
| $t_f$ | Fall time | Resistive load; as fig. 1 | | | 25 | ns |
| $V_{CC}$ | Supply voltage operating voltage | | 9 | | 36 | V |
| $V_{IN\text{-}H}$ | High level input voltage | | | | Ibias/2 +300mV | V |
| $V_{IN\text{-}L}$ | Low level input voltage | | Ibias/2 -300mV | | | V |
| $I_{IN\text{-}H}$ | Hi level Input current | Pin Voltage = Ibias | | 1 | | µA |

**ELECTRICAL CHARACTERISTCS** (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IN-L}$ | Low level input current | Pin Voltage = 0.3V | | 1 | | µA |
| $I_{PWRDN-H}$ | Hi level PWRDN pin input current | Ibias = 3.3V | | 35 | | µA |
| $V_L$ | Low logical state voltage VL (pin PWRDN, TRISTATE) (note 1) | Ibias = 3.3V | 0.8 | | | V |
| $V_H$ | High logical state voltage VH (pin PWRDN, TRISTATE) (note 1) | Ibias = 3.3V | | | 1.7 | V |
| $I_{VCC-PWRDN}$ | Supply CURRENT from Vcc in Power Down | PWRDN = 0 | | | 3 | mA |
| $I_{FAULT}$ | Output Current pins FAULT -TH-WARN when FAULT CONDITIONS | Vpin = 3.3V | | 1 | | mA |
| $I_{VCC-hiz}$ | Supply Current from Vcc in Tri-state | $V_{CC}$ = 30V; Tri-state = 0 | | 22 | | mA |
| $I_{VCC}$ | Supply Current from Vcc in operation both channel switching) | $V_{CC}$ =30V; Input Pulse width = 50% Duty; Switching Frequency = 384KHz; No LC filters; | | 80 | | mA |
| $I_{VCC-q}$ | Isc (short circuit current limit) (note 2) | | 4 | 6 | 8 | A |
| $V_{OUT-SH}$ | Undervoltage protection threshold | | | 7 | | V |
| $V_{OV}$ | Output minimum pulse width | No Load | 70 | | 150 | ns |

Notes: 1. The following table explains the VL, VH variation with Ibias

| Ibias | VLmin | VHmax | Unit |
|---|---|---|---|
| 2.7 | 0.7 | 1.5 | V |
| 3.3 | 0.8 | 1.7 | V |
| 5 | 0.85 | 1.85 | V |

Note 2: If used in single BTL configuration, the device may be not short circuit protected

**LOGIC TRUTH TABLE** (see fig. 2)

| TRI-STATE | INxA | INxB | Q1 | Q2 | Q3 | Q4 | OUTPUT MODE |
|---|---|---|---|---|---|---|---|
| 0 | x | x | OFF | OFF | OFF | OFF | Hi-Z |
| 1 | 0 | 0 | OFF | OFF | ON | ON | DUMP |
| 1 | 0 | 1 | OFF | ON | ON | OFF | NEGATIVE |
| 1 | 1 | 0 | ON | OFF | OFF | ON | POSITIVE |
| 1 | 1 | 1 | ON | ON | OFF | OFF | Not used |

**Figure 1. Test Circuit.**

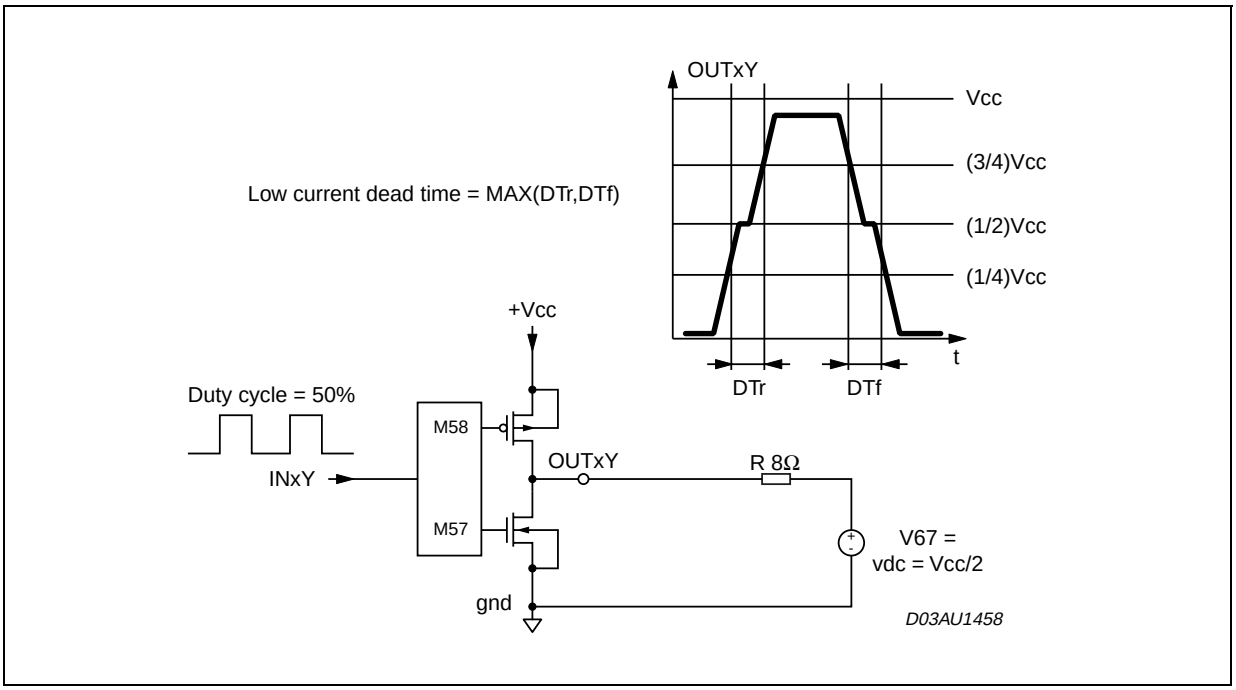



**Figure 2.**

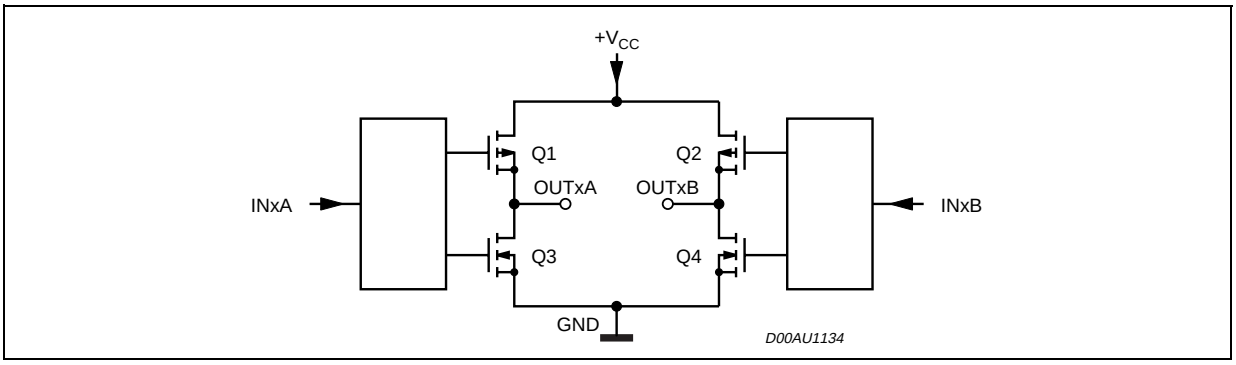



**Figure 3.**

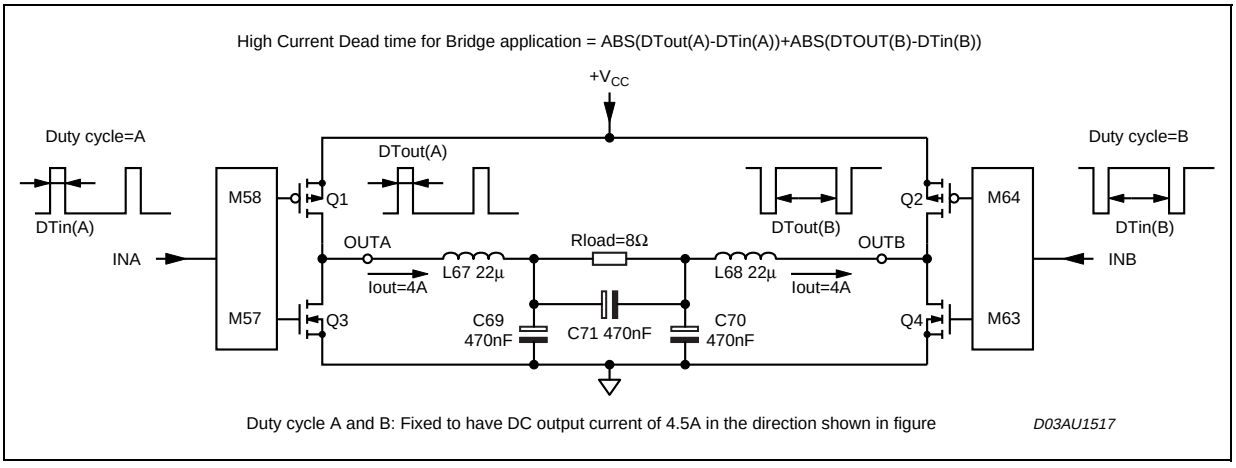
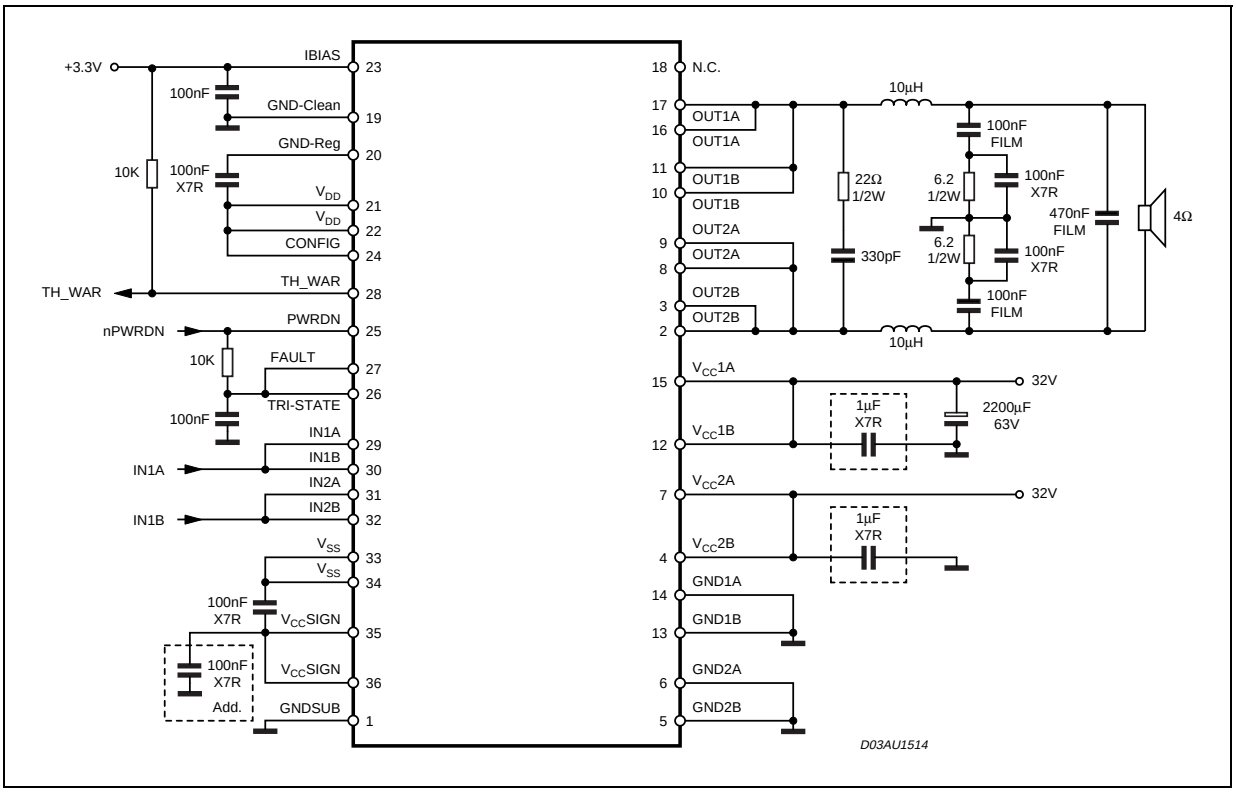
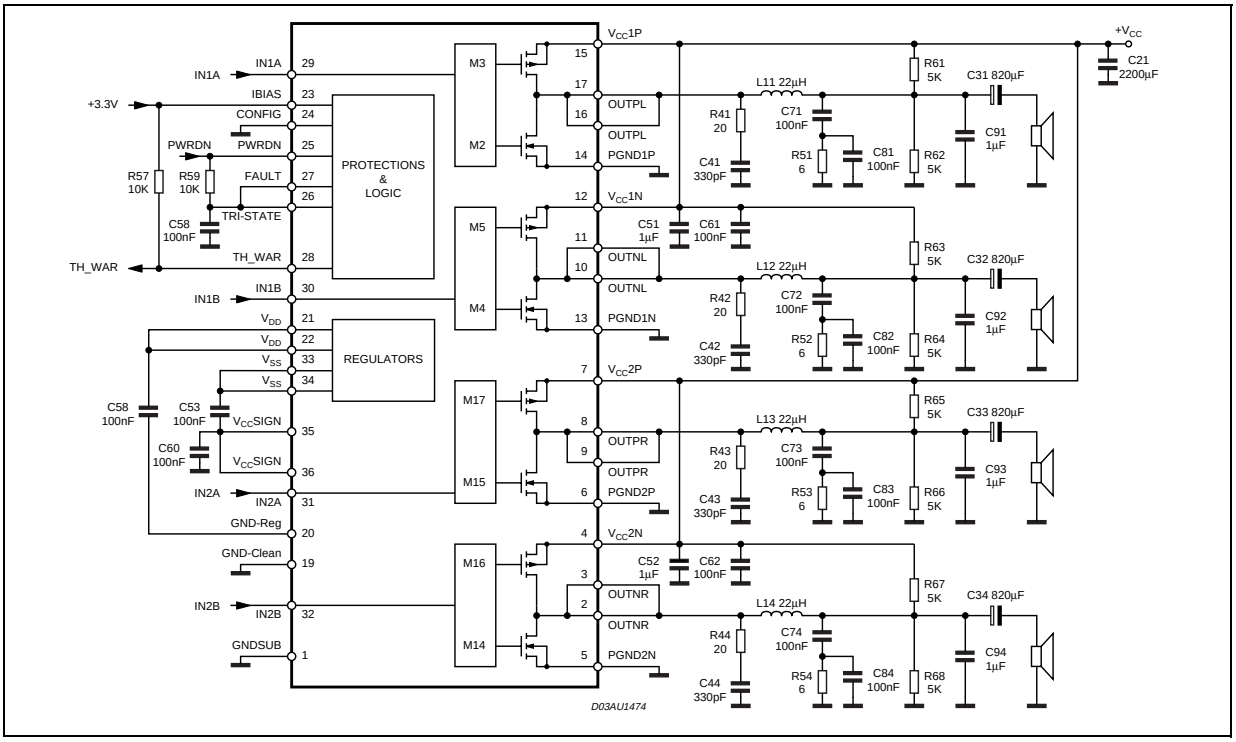


**Figure 4. Typical Single BTL Configurationto obtain 120W @ THD 10%, $R_L$ = 4Ω, $V_{CC}$ = 32V** (note 1))




Note: 1. "A PWM modulator as driver is needed . In particular, this result is performed using the STA30X+STA50X demo board". Peak Power for t ≤1sec

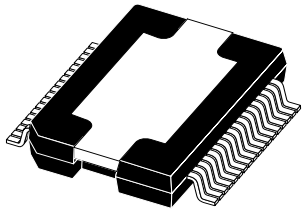
**Figure 5. Typical Quad Half Bridge Configuration**



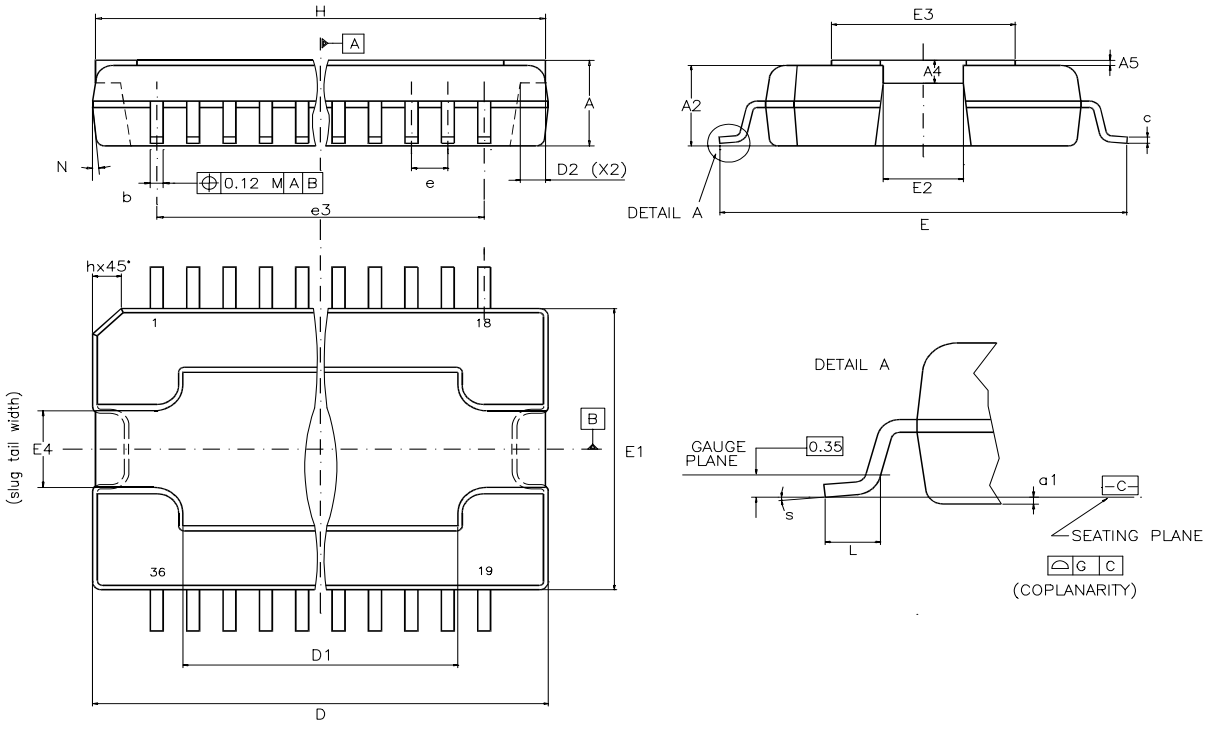
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 3.25 | | 3.5 | 0.128 | | 0.138 |
| A2 | | | 3.3 | | | 0.13 |
| A4 | 0.8 | | 1 | 0.031 | | 0.039 |
| A5 | | 0.2 | | | 0.008 | |
| a1 | 0 | | 0.075 | 0 | | 0.003 |
| b | 0.22 | | 0.38 | 0.008 | | 0.015 |
| c | 0.23 | | 0.32 | 0.009 | | 0.012 |
| D | 15.8 | | 16 | 0.622 | | 0.630 |
| D1 | 9.4 | | 9.8 | 0.37 | | 0.38 |
| D2 | | 1 | | | 0.039 | |
| E | 13.9 | | 14.5 | 0.547 | | 0.57 |
| E1 | 10.9 | | 11.1 | 0.429 | | 0.437 |
| E2 | | | 2.9 | | | 0.114 |
| E3 | 5.8 | | 6.2 | 0.228 | | 0.244 |
| E4 | 2.9 | | 3.2 | 0.114 | | 1.259 |
| e | | 0.65 | | | 0.026 | |
| e3 | | 11.05 | | | 0.435 | |
| G | 0 | | 0.075 | 0 | | 0.003 |
| H | 15.5 | | 15.9 | 0.61 | | 0.625 |
| h | | | 1.1 | | | 0.043 |
| L | 0.8 | | 1.1 | 0.031 | | 0.043 |
| N | 10° (max) | | | | | |
| s | 8° (max) | | | | | |

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
(2) No intrusion allowed inwards the leads.

## OUTLINE AND MECHANICAL DATA



## PowerSO36 (SLUG UP)



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.
All other names are the property of their respective owners

© 2003 STMicroelectronics - All rights reserved

**STMicroelectronics GROUP OF COMPANIES**
Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States
**www.st.com**