RADIATION HARDENED
CONVOLUTIONAL ENCODER
VITERBI DECODER
STEL-5269RH

ASIC
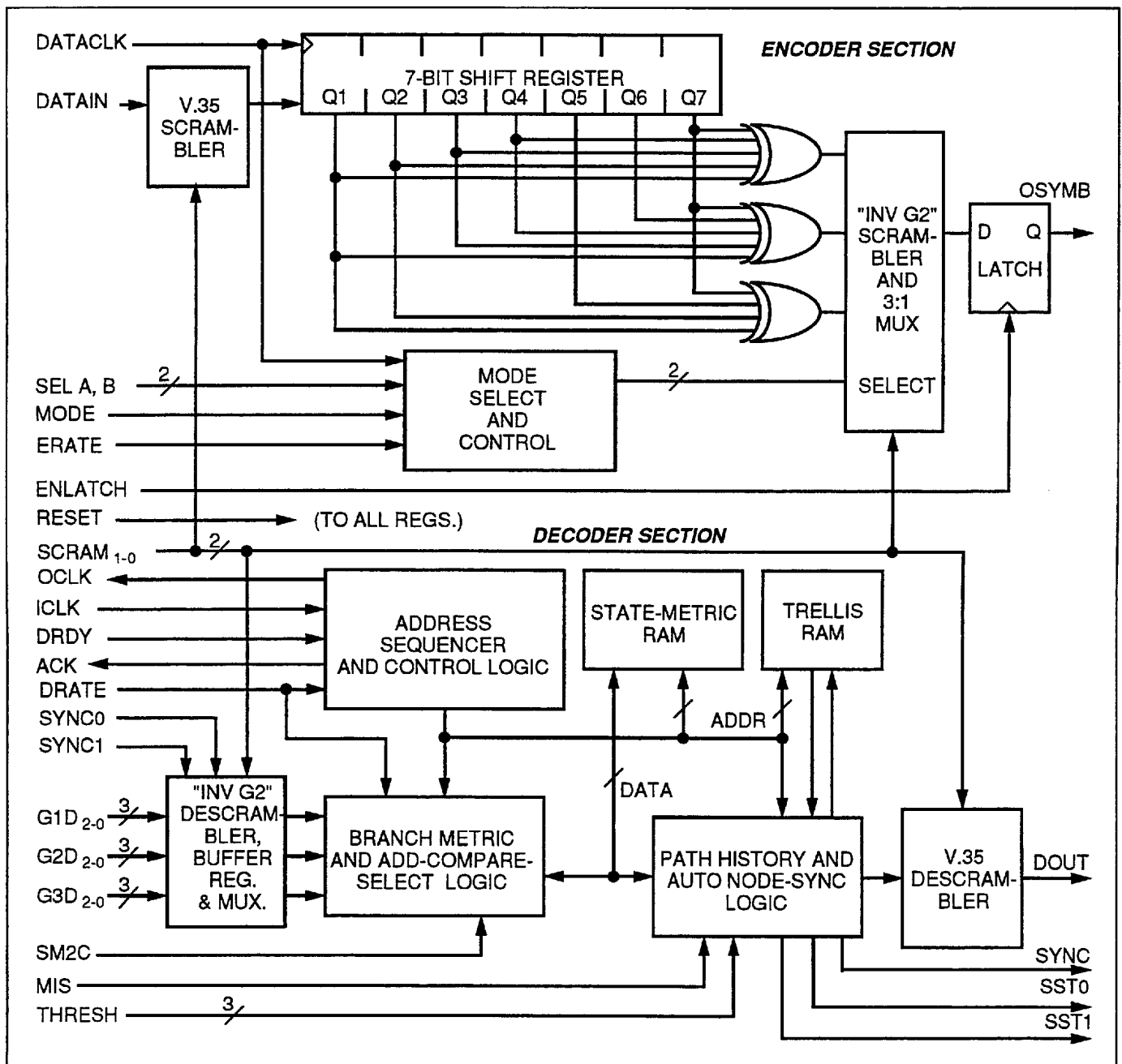Custom
Products
Division

STANFORD
TELECOM®

FEATURES

- **Constraint length 7**
- **RATES $1/3$ AND $1/2$**
- **Up to 256 kbps data rate**
- **Programmable scrambler:**
  V.35 (CCITT or IESS) or "Invert G2"
- **Three bit soft decision in signed magnitude or 2's complement formats**
- **Coding gain of 5.2 dB (at 10^{-5} BER, Rate $1/2$)**
- **Industry standard polynomials**
  $G1=171_8$, $G2=133_8$, $G3=145_8$,
- **Low power consumption CMOS**

- **84-pin flat package**
- **Commercial and military temperature ranges available**
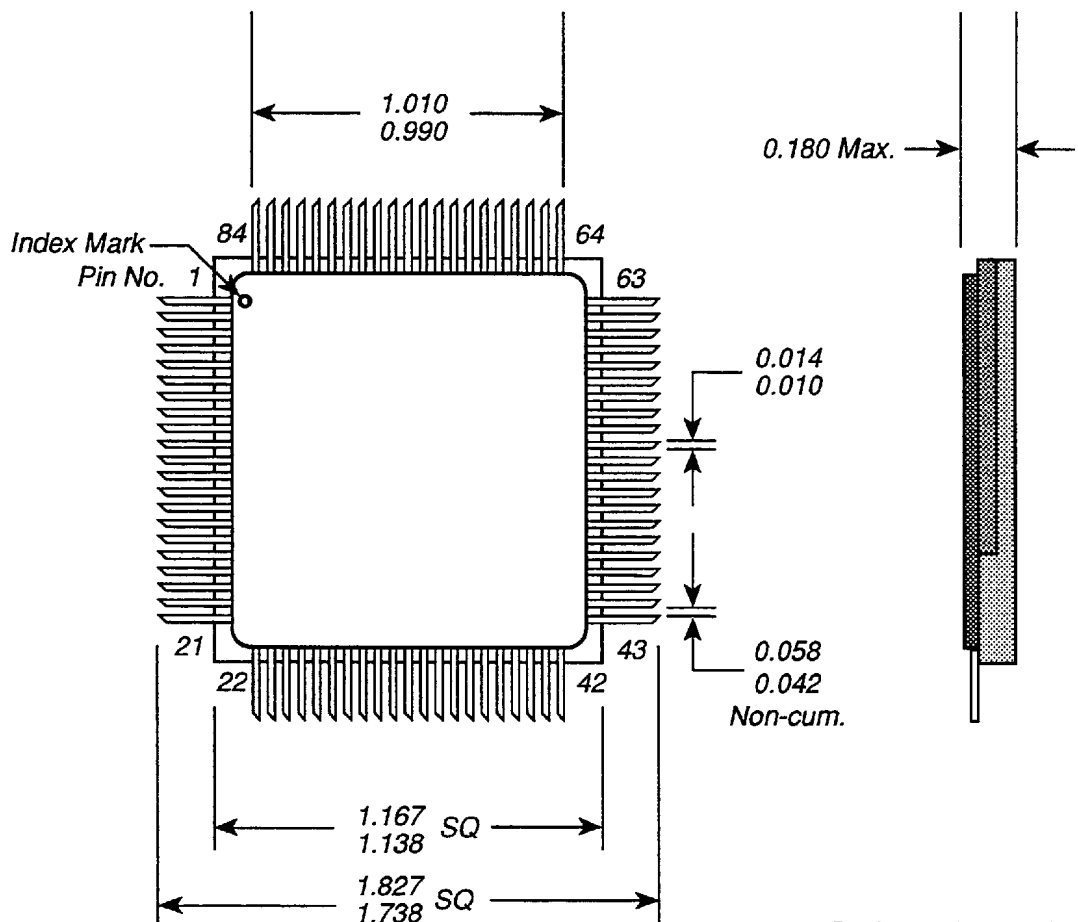- **Available to MIL-STD 883C Class 'S'**

RAD HARDNESS CAPABILITIES

- **Total dose – 1 MRad (Si)**
- **Dose rate**
  - **Upset > 109 Rads (Si)/sec.**
  - **Latchup > 2x1011 Rads (Si)/sec.**
- **Projected neutron fluence > 10^{14} N/cm2**

BLOCK DIAGRAM

STEL-5269RH

2

PIN CONFIGURATION

Index Mark
Pin No. 1

84

64

63

21

22

43

42

1.010
0.990

0.180 Max.

0.014
0.010

0.058
0.042
Non-cum.

1.167
1.138 SQ

1.827
1.738 SQ

Package: 84 pin Flat Pack
Thermal coefficient, θ_{ja} = 37°C/W

PIN CONNECTIONS

1	V_{DD}	18	$THRESH_0$	34	OSYMB	51	I.C.	68	SST1
2	$G1D_0$	19	$THRESH_1$	35	I.C.	52	I.C.	69	SST0
3	$G1D_1$	20	$THRESH_2$	36	I.C.	53	V_{SS}	70	SYNC
4	$G1D_2$	21	V_{DD}	37	I.C.	54	I.C.	71	V_{SS}
5	$G2D_0$	22	V_{DD}	38	I.C.	55	I.C.	72	OCLK
6	$G2D_1$	23	SCRAM1	39	I.C.	56	I.C.	73	ICLK
7	$G2D_2$	24	SCRAM0	40	I.C.	57	I.C.	74	V_{SS}
8	$G3D_0$	25	MODE	41	I.C.	58	I.C.	75	DOUT
9	$G3D_1$	26	ERATE	42	V_{DD}	59	I.C.	76	V_{SS}
10	$G3D_2$	27	ENLATCH	43	V_{DD}	60	I.C.	77	ACK
11	V_{SS}	28	SEL B	44	I.C.	61	I.C.	78	I.C.
12	DRDY	29	SEL A	45	I.C.	62	I.C.	79	I.C.
13	SM2C	30	DATA IN	46	I.C.	63	V_{DD}	80	I.C.
14	DRATE	31	DATA	47	I.C.	64	V_{DD}	81	I.C.
15	$SYNC_0$		CLK	48	I.C.	65	I.C.	82	V_{SS}
16	$SYNC_1$	32	V_{SS}	49	I.C.	66	I.C.	83	V_{SS}
17	MIS	33	RESET	50	I.C.	67	I.C.	84	V_{DD}

Note: I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.

STEL-5269RH

FUNCTIONAL DESCRIPTION

Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited, FEC techniques can reduce the required transmission power. The STEL-5269RH is a specialized product designed to perform this specific communications related function and is especially designed for use in high radiation environments, e.g., in spaceborne applications.

The encoder creates a stream of symbols which are transmitted at 2 (Rate $^1/2$) or 3 (Rate $^1/3$) times the information rate. This encoding introduces a high degree of redundancy which enables accurate decoding of information despite a high symbol error rate resulting from a noisy link.

The STEL-5269RH incorporates all the memories required to perform these functions. In addition, the STEL-5269RH incorporates 3 different scrambling algorithms and a microprocessor interface. The STEL-5269RH is available in an 84-pin Ceramic Flat Pack and is radiation hardened to 1 MRad (Si) total dose.

FUNCTION BLOCK DESCRIPTION

ENCODER

The convolutional coder is functionally independent of the decoder. A single data bit is clocked into the 7-bit shift register on the rising edge of **DATA CLK**. There are two modes of operation, controlled by the **MODE** input. When **MODE** is low the timing of the **SEL A, SEL B** and **ENLATCH** signals determine whether 2 or 3 symbol bits are generated for every data bit. When **MODE** is high the symbols are automatically generated sequentially every clock cycle. In this case, the state of **ERATE** determines whether the device generates symbols for Rate $^1/2$ or Rate $^1/3$ operation. The symbols G1, G2, and G3 are generated from the modulo-2 sum (exclusive-OR) of the inputs to the 3 generators from the taps on the shift register. The 3 polynomials are 171_8 (G1), 133_8 (G2), and 145_8 (G3). Example inputs are shown in the timing diagram for both rate $^1/2$ and rate $^1/3$ operation.

DECODER

The STEL-5269RH is designed to accept symbols either synchronously or in a handshake mode. Symbols are latched into the decoder input registers on the falling edge of the DRDY input. ACK is returned by the decoder to indicate that the symbols have been accepted.

The **RATE** input determines whether the decoder will operate in Rate $^1/2$ or Rate $^1/3$ mode. When operating at Rate $^1/2$ the G3 symbol is ignored by the decoder.

For hard decision binary symbols the G1, G2, G3 symbol bits should be connected to pins $G1D_2$, $G2D_2$ and $G3D_2$ respectively, and the other symbol input pins should be tied high (V_{DD}). Three-bit soft decision symbols may be input in Signed Magnitude or Inverted Two's Complement code, according to the setting of the code control pin, SM2C. The code should be set to Signed Magnitude when using hard decision data.

A single decoded data bit is output for every set of input symbols. The data bit corresponding to a particular symbol set will be output after a delay of 42 symbols. Therefore, when using the STEL-5269RH to decode blocks of data 42 additional dummy symbols and 42 DRDY signals need to be added to the data stream to flush the last 42 decoded data bits out of the decoder.

Node synchronization (correctly grouping incoming symbols into G1, G2, and G3 sets) is inherent with many communication techniques such as TDMA and some spread spectrum systems. If node synchronization is not an inherent property of the communications link the internal auto node sync circuit can be used to do this. This is accomplished by connecting the node sync outputs (SST0 and SST1) to the node sync inputs (SYNC0 and SYNC1). The threshold for determining the out of sync condition is user selectable by means of the $THRESH_{2-0}$ inputs. Alternatively, the SYNC0 and SYNC1 pins can be used with an external algorithm to achieve the same result.

Further information on the theory of operation of Viterbi decoders may be obtained from textbooks such as "Error-Correcting Codes", by Peterson and Weldon (MIT Press), or "Error Control Coding", by Lin and Costello (Prentice-Hall). An alternative source of information is the many papers on this subject that have appeared in the IEEE transactions, such as "Convolutional Codes and their Performance in Communication Systems", by Dr. A. J. Viterbi, IEEE Trans. on Communications Technology, October 1971.

INPUT SIGNALS

RESET

Asynchronous master **Reset**. A logic low on this pin will clear all registers on the STEL-5269RH in both the encoder and decoder sections of the chip. **RESET** should remain low for at least 3 cycles of **ICLK**.

DATACLK

This is the encoder Shift Register Clock. A rising edge on this clock latches **DATAIN** into the encoder shift register. This signal should nominally be a square wave with a maximum frequency of 256 KHz.

DATAIN

This is the encoder input. The data present at this pin is latched into the encoder shift register on the rising edge of **DATACLK**. This signal should be stable at the rising edge of **DATACLK**.

MODE

The state of the **MODE** input determines the method of symbol sequencing in the encoder. When **MODE** is set low the sequencing is generated externally under the control of the **SEL A** and **SEL B** inputs, and when **MODE** is set high it is generated automatically.

SEL A, SEL B

When **MODE** is set low **SEL A** and **SEL B** select the encoded symbol, G1, G2 or G3, which will appear on the **OSYMB** pin on the next rising edge of **ENLATCH** according to the table:

SEL A	SEL B	SYMBOL	POLYNOMIAL
0	1	G1	171_8 (1111001_2)
1	0	G2	133_8 (1011011_2)
0	0	G3	145_8 (1100101_2)

When **MODE** is set high the symbol sequence is generated automatically and the **SEL A** and **SEL B** inputs are inactive.

ERATE

When **MODE** is high the Encoder **Rate** input determines whether symbols for Rate $1/2$ (**ERATE** = 1) or Rate $1/3$ (**ERATE** = 0) operation are generated. When **MODE** is low this input is inactive.

SCRAM0, SCRAM1

The Scramble inputs are used to enable the three different scrambler functions included in th STEL-5269RH, as shown in the following table:

SCRAM0	SCRAM1	FUNCTION
0	0	Scrambler disabled
1	0	Invert G2
0	1	V.35 (CCITT compatible)
1	1	V.35 (IESS compatible)

The "Invert G2" scrambler simply inverts the G2 symbols generated in the encoder. The decoder then re-inverts the received G2 symbols before decoding. Two different "V.35" scrambler formats are provided since there are two versions of this standard in existence: the true, CCITT version of the standard, and the IESS version, which has become a de facto standard through widespread use. In each case, the scrambling function is provided at the encoder and the descrambler is provided at the decoder.

ENLATCH

This is the encoder Output Latch Enable. The new symbol is clocked into the output latch and appears on the **OSYMB** pin on the rising edge of **ENLATCH**. When **MODE** is low the symbol selected will depend on the states of the **SEL A** and **SEL B** lines, which should be stable on the rising edge of **ENLATCH**. When **MODE** is high the symbol selection is internal, and the frequency of the **ENLATCH** signal should be 2 or 3 times the frequency of the **DATACLK**, depending on the rate selected.

ICLK, OCLK

System Clock. A crystal may be connected between **ICLK** and **OCLK** or a CMOS level clock may be fed into **ICLK** only. The clock frequency should be at least 70 times the data rate but no more than 18 MHz.

DRATE

The Decoder **Rate** input selects whether the decoder will read two symbols (**DRATE** set high) or three symbols (**DRATE** set low)) for every data bit decoded. During Rate $1/2$ operation the symbol G3 on inputs $G3D_{2-0}$ is completely ignored by the decoder.

$G1D_{2-0}$, $G2D_{2-0}$, $G3D_{2-0}$

The three 3-bit soft decision symbols are connected to these inputs and loaded into the input registers on the falling edge of **DRDY**. The order in which the symbols are entered into the decoder from the registers depends on the state of the **SYNC0** and **SYNC1** inputs. The decoder can make use of soft decision information, which includes both polarity information and a confidence measure, to improve the decoder performance. If hard decision (single bit) symbols are used the signals are connected to pins $G1D_2$, $G2D_2$ and

STEL-5269RH

G3D$_2$ and the other inputs are connected to V$_{DD}$. See SM2C for a description of the input data codes.

SM2C

The state of the Signed Magnitude/2's Complement input determines the format of the incoming soft-decision symbols into the decoder. When SM2C is high the input code is Signed Magnitude, and when it is low the code is Two's Complement. The codes are shown in the following table:

CODE CONTROL: SYMBOL INPUT:	SM2C=1 GXD$_{2-0}$	SM2C=0 GXD$_{2-0}$
Most Confident '+' level (Data = 0)	0 1 1	0 1 1
	0 1 0	0 1 0
	0 0 1	0 0 1
Least Confident '+' level	0 0 0	0 0 0
Least Confident '–' level (Data = 1)	1 0 0	1 1 1
	1 0 1	1 1 0
	1 1 0	1 0 1
Most Confident '–' level	1 1 1	1 0 0

SM2C should be set high when using hard decision data.

DRDY

The Data Ready signal is used to load symbols into the decoder. A new set of symbols is latched into the input registers on each falling edge of the DRDY input.

SYNC0, SYNC1

The Symbol Sync0 and Symbol Sync1 inputs are used for auto node sync operation. When using the internal auto node sync mode these two pins are connected to SST0 and SST1, respectively. The operation of the decoder is affected in the following way by the SYNC0 and SYNC1 inputs:

RATE	SYNC0	SYNC1	G1	G2	G3
1	0	0	G1$_N$	G2$_N$	–
1	1	0	G2$_{N-1}$	G1$_N$	–
1	0	1	G2$_N$	G1$_N$	–
1	1	1	Invalid state		
0	0	0	G1$_N$	G2$_N$	G3$_N$
0	1	0	G3$_{N-1}$	G1$_N$	G2$_N$
0	0	1	G2$_{N-1}$	G3$_{N-1}$	G1$_N$
0	1	1	Invalid state		

Note that whenever the states of the SYNC0 and SYNC1 inputs are changed there will be a delay of 42 bit periods before valid data starts appearing at DOUT.

MIS

Two algorithms for auto node-sync are incorporated into the STEL-5269RH. When MIS is set high the Traceback Mismatch algorithm is selected, and when MIS is set low the Metric Renormalization algorithm is selected.

THRESH$_{2-0}$

A counter is used to determine the number of either traceback mismatches or metric renormalizations per 256 bits in the auto node-sync circuit, and the threshold at which the counter triggers the SST0 and SST1 outputs to change states is set with the data on the THRESH$_{2-0}$ inputs. The threshold values will be as shown in the table below.

THRESH$_{2-0}$	Threshold value
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

Since the actual error rate obtained will depend on the signal to noise ratio (E$_b$/N$_o$) in the signal, the optimum value of the threshold will also depend on E$_b$/N$_o$ and should be set accordingly.

OUTPUT SIGNALS

OSYMB

Output Symbol from the Encoder. This output depends on the seven most recent data bits (DATAIN) clocked into the encoder shift register and on the select lines SEL A and SEL B. The individual symbols are formed by the modulo-2 sum of the inputs to the generators from the 7-bit shift register.

ACK

A low level pulse on the Acknowledge pin indicates that the decoder has input the current set of two or three symbols. The signal will pulse low between 68 and 69 clock cycles after the falling edge of DRDY.

DOUT

Decoded Data Out. The signal is latched into the output register on the falling edge of DRDY. There is a delay of 42 data bits from the time a set of symbols is input to the time the corresponding data bit is output. Consequently, in order to flush the last 42 bits of data out of the system at the end of a burst it is necessary to continue pulsing the DRDY line for 42 symbol periods after the last valid symbol has been entered.

SST0, SST1

The Sync State 0 and Sync State 1 signals are the outputs of the internal auto node sync circuit. They should be connected to SYNC0 and SYNC1 respectively to use the internal auto node sync capability. They may also be used in conjunction with an external node sync algorithm implementation which can use the SST0 and SST1 outputs.

SYNC

The Sync output provides an indication of the status of the internal auto node sync circuit. When it is low it indicates that the system is assumed to be in sync, as determined by the error rate estimate. When node sync has not been established or has been lost SYNC will pule high for one cycle of DRDY as soon as the threshold value has been exceeded by the mismatch/renormalization counter.

APPLICATION INFORMATION -

USING AUTOMATIC NODE SYNC

The automatic node sync circuit built into the STEL-5269RH can be used to provide node sync in applications where this is not intrinsic to the nature of the operation. The automatic node sync is enabled by connecting the SST1 and SST0 outputs to the SYNC1 and SYNC0 inputs, as shown below. The threshold should be set according to the expected signal to noise ratio of the input signal for optimum operation of the system.

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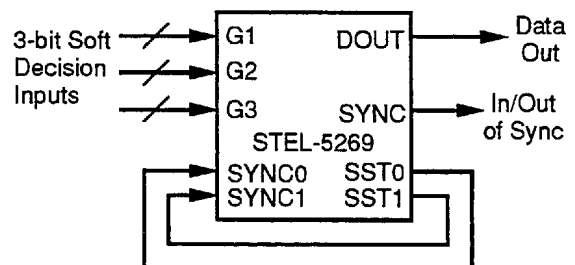
ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{SS}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–65 to +150	°C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD} + 0.3	volts
I_i	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 5%	Volts (Commercial)
		+5 ± 10%	Volts (Military)
T_a	Operating Temperature (Ambient)	0 to +70	°C (Commercial)
		–55 to +125	°C (Military)

D.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 V ±5%, V_{SS} = 0 V, T_a = 0° to 70° C, Commercial
V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, Ta = –55° to 125° C, Military)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			5.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	0.7 x V_{DD}			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.3 x V_{DD}	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current			10	μA	$V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current	–15	–45	–130	μA	$V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5	V_{DD}	volts	I_O = –4.0 mA
$V_{OL(max)}$	Low Level Output Voltage	V_{SS}	0.2	0.4	volts	I_O = +4.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2	15	pF	All inputs
C_{OUT}	Output Capacitance		4	20	pF	All outputs

ENCODER TIMING. MODE = 1
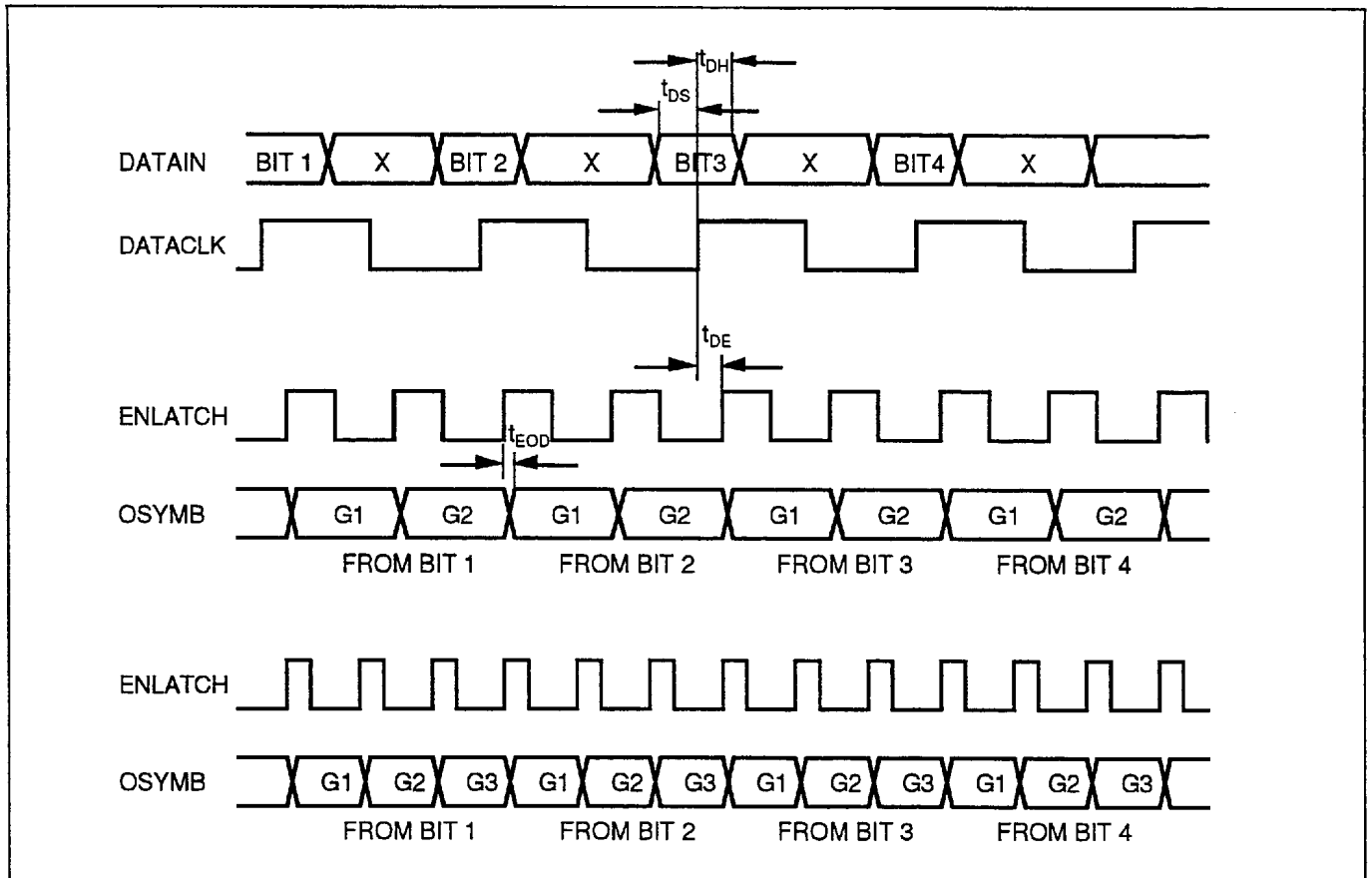
ENCODER ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 V ±5%, V_{SS} = 0 V, T_a = 0° to 70° C, Commercial

V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, Ta = –55° to 125° C, Military)

Symbol	Parameter	Commercial		Military		Units	Conditions
		Min.	Max.	Min.	Max.		
t_{RS}	RESET pulse width	$3*t_{CLK}$		$3*t_{CLK}$		nsec.	
t_{SR}	RESET to ICLK setup	7		10		nsec.	
t_{DS}	DATAIN to DATACLK setup	7		10		nsec.	
t_{DH}	DATAIN to DATACLK hold	7		10		nsec.	
t_{SS}	SEL A or SEL B to ENLATCH setup	7		10		nsec.	
t_{SH}	SEL A or SEL B to ENLATCH hold	7		10		nsec.	
t_{DE}	DATACLK to ENLATCH delay	10			12	nsec.	
t_{EOD}	ENLATCH to OSYMB stable delay		12		15	nsec.	

Notes: t_{CLK} = Period of ICLK =(1/ f_{CLK}).
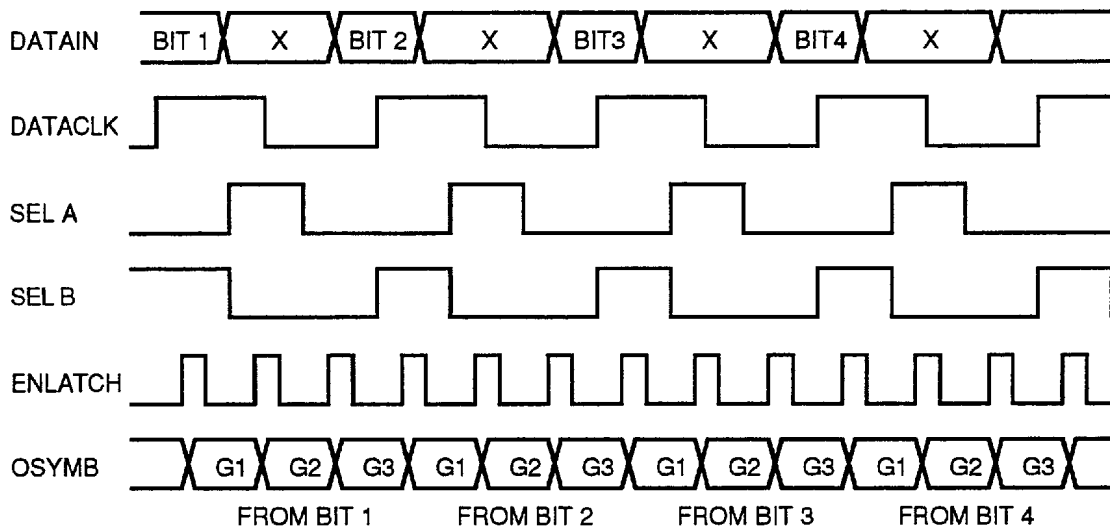
t_{SR} is only relevant if operation is to commence during the first clock cycle after RESET goes high.
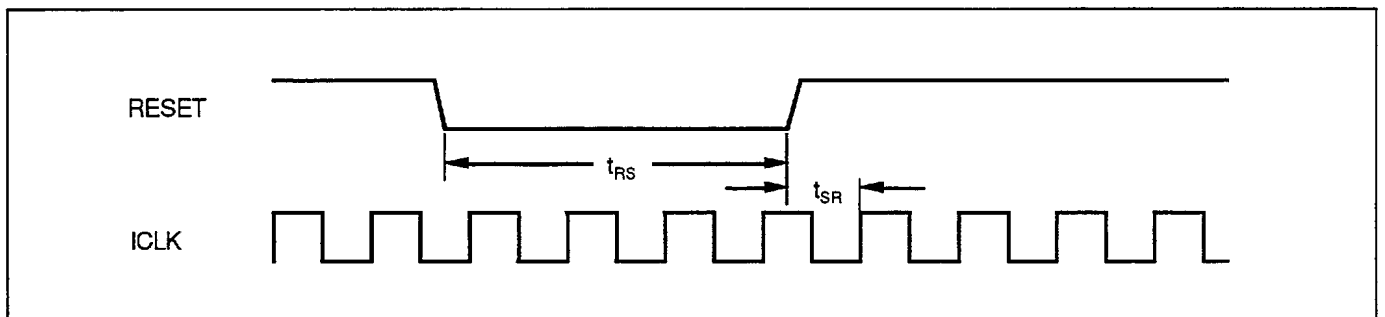
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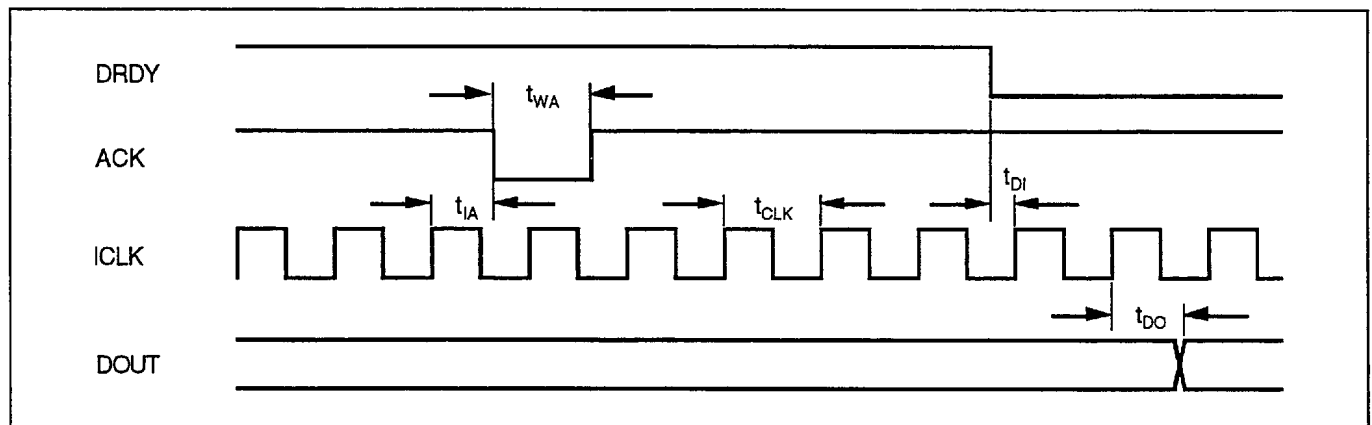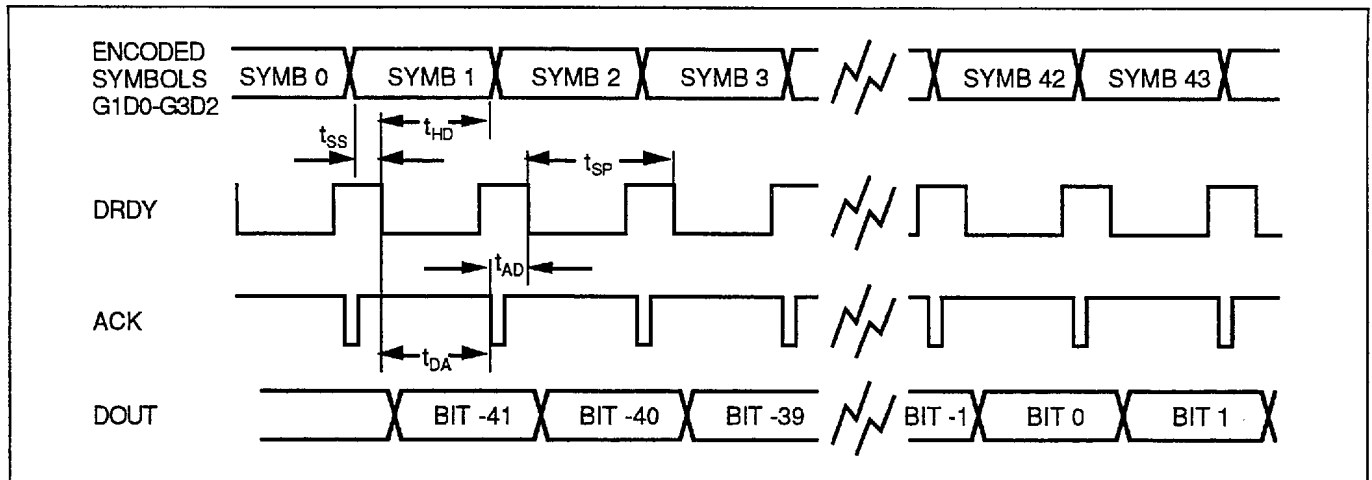## ENCODER TIMING. MODE = 0

RATE ½ OPERATION
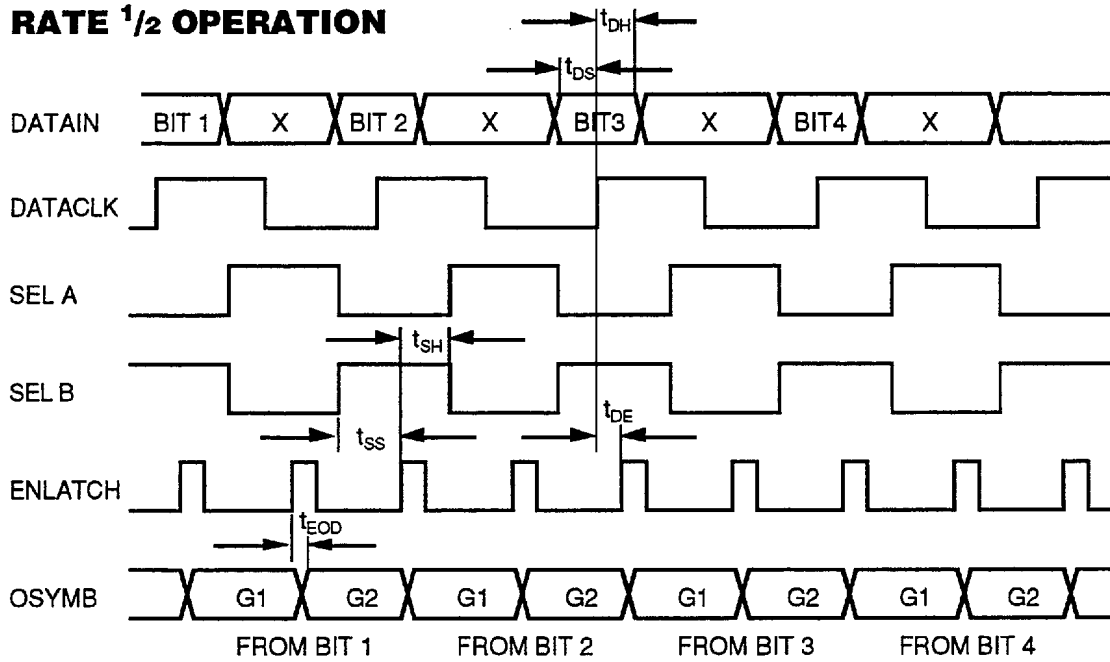
RATE ⅓ OPERATION (Timing parameters as for Rate ½ operation)

RESET TIMING

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DECODER TIMING

DECODER ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 V ±5%, V_{SS} = 0 V, T_a = 0° to 70° C, Commercial

V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, Ta = –55° to 125° C, Military)

Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
f_{CLK}	ICLK Frequency	$70*f_{DRDY}$	18	$70*f_{DRDY}$	14	MHz
t_{SS}	SYMBOL to DRDY setup	25		35		nsec.
t_{HD}	SYMBOL to DRDY hold	11		15		nsec.
t_{SP}	SYMBOL Period	3.9		5		μsec.
t_{DA}	DRDY to ACK	$15 + 68*t_{CLK}$	$18 + 69*t_{CLK}$	$12 + 68*t_{CLK}$	$25 + 69*t_{CLK}$	nsec.
t_{AD}	ACK to DRDY	$2*t_{CLK}$		$2*t_{CLK}$		nsec.
t_{WA}	ACK pulse width	t_{CLK}		t_{CLK}		nsec.
t_{DI}	DRDY to ICLK setup	8		12		nsec.
t_{IA}	ICLK to ACK		45		60	nsec.
t_{DO}	ICLK to DOUT		65		90	nsec.
t_{SR}	RESET to ICLK setup	8		12		nsec.

Notes: f_{DRDY} = Frequency of DRDY, t_{CLK} = Period of ICLK =(1/f_{CLK}).

t_{SR} is only relevant if operation is to commence during the first clock cycle after RESET goes high.

STEL-5269RH