16Mb ZBT® SRAM

MT55L256Y72P, MT55V256V72P

3.3V VDD, 3.3V or 2.5V I/O; 2.5V VDD 2.5V I/O

FEATURES

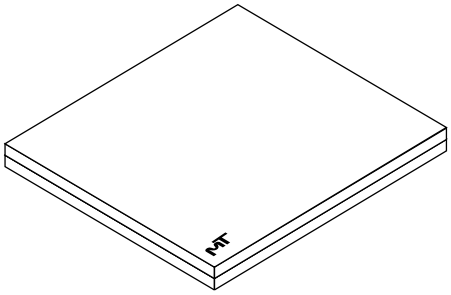
- High frequency and 100 percent bus utilization
- Fast cycle times: 6ns, 7.5ns, and 10ns
- Single +3.3V ±5% or +2.5V ±5% power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs to eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)

OPTIONS	MARKING*
• Timing (Access/Cycle/MHz)	
3.5ns/6ns/166 MHz	-6
4.2ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10
• Configurations	
3.3V VDD, 3.3V or 2.5V I/O	
256K x 72	MT55L256Y72P
2.5V VDD, 2.5V I/O	
256K x 72	MT55V256V72P
• Package	
221-pin FBGA	G
209-pin PBGA	H

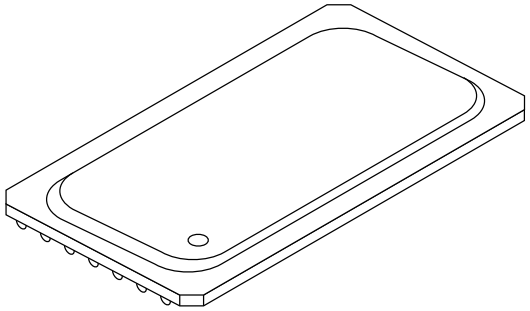
Part Number Example:
MT55L256Y72PT-7.5

*Part Marking for the FBGA device may be found on Micron's web site at http://www.micron.com/support.

221-PIN FBGA



209-PIN PBGA



GENERAL DESCRIPTION

The Micron® Zero Bus Turnaround™ (ZBT®) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

Micron's 16Mb ZBT SRAMs integrate a 256K x 72 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles for READ to WRITE, or WRITE to READ, transitions. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc#, BWd#, BWe#, BWf#, BWg#, and BWh#) and read/write (R/W#).

Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal mini-

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GENERAL DESCRIPTION (continued)

mization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The data-out (Q), enabled by OE#, is registered by the rising edge of CLK. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

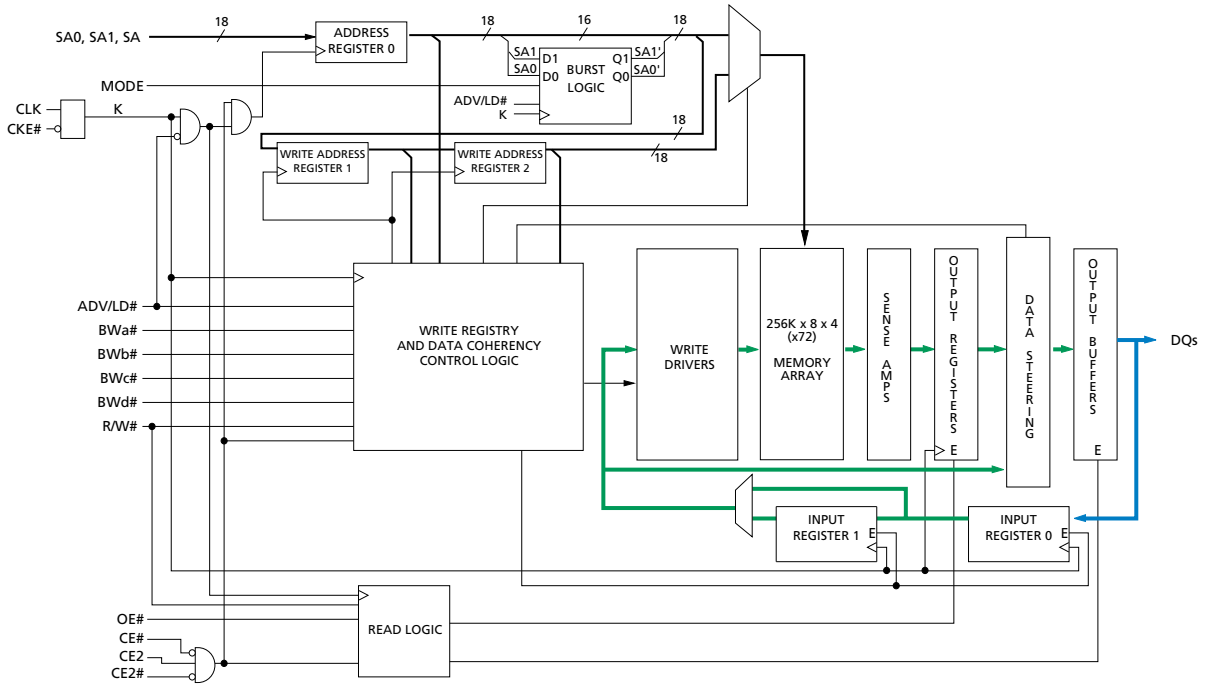
To allow for continuous, 100 percent use of the data bus, the pipelined ZBT SRAM uses a LATE LATE WRITE cycle. For example, if a WRITE cycle begins in clock cycle one, the address is present on rising edge one. BYTE WRITEs need to be asserted on the same cycle as the address. The data associated with the address is required two cycles later, or on the rising edge of clock cycle three.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins; BWe# controls DQe pins; BWf# controls DQf pins; BWg# controls DQg pins; and BWh# controls DQh pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are only available on the x36 versions.

Micron's 16Mb ZBT SRAMs operate from a +3.3V or +2.5V V_{DD} power supply, and all 3.3V V_{DD} inputs and outputs are LVTTL-compatible. Users can implement either a 3.3V or 2.5V I/O for the +3.3V V_{DD} or a 2.5V I/O for the +2.5V V_{DD}. The device is ideally suited for systems requiring high bandwidth and zero bus turn-around delays.

Please refer to Micron's Web site (www.micron.com/sram) for the latest data sheet.

FUNCTIONAL BLOCK DIAGRAM
256K x 72



NOTE: Functional block diagrams illustrate simplified device operation. See truth table, pin descriptions and timing diagrams for detailed information.

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PIN LAYOUT (TOP VIEW)
221-PIN FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	DQa	DQa	V_{SS}	SA	CE2	SA	ADV/ LD#	SA	CE2#	SA	V_{SS}	DQe	DQe
B	DQa	DQa	$V_{DD}Q$	BWb#	BWa#	NC	BWE#	SA	BWe#	BWf#	V_{DD}	DQe	DQe
C	DQa	DQa	V_{SS}	BWc#	BWd#	NC	CE#	NC	BWh#	BWg#	V_{SS}	DQe	DQe
D	DQa	DQa	DQa	V_{DD}	NC	NC	OE#/G#	NC	NC	$V_{DD}Q$	DQe	DQe	DQe
E	DQb	DQb	DQb	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQf	DQf	DQf
F	DQb	DQb	$V_{DD}Q$	V_{DD}	V_{DD}	V_{DD}	NC	V_{DD}	V_{DD}	V_{DD}	$V_{DD}Q$	DQf	DQf
G	DQb	DQb	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
H	DQb	DQb	$V_{DD}Q$	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	$V_{DD}Q$	DQf	DQf
J	NC	NC	CLK	NC	V_{SS}	V_{SS}	CKE#	V_{SS}	V_{SS}	NC	NC	NC	NC
K	DQc	DQc	$V_{DD}Q$	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	DQg	DQg
L	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	DQg	DQg
M	DQc	DQc	$V_{DD}Q$	V_{DD}	V_{DD}	V_{DD}	NC	V_{DD}	V_{DD}	V_{DD}	V_{DD}	DQg	DQg
N	DQc	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQg	DQg	DQg
P	DQd	DQd	DQd	V_{DD}	NC	NC	MODE/ LBO#	NC	NC	V_{DD}	DQh	DQh	DQh
R	DQd	DQd	V_{SS}	NC	SA	NC	SA	NC	SA	NC	V_{SS}	DQh	DQh
T	DQd	DQd	$V_{DD}Q$	SA	SA	SA	SA1	SA	SA	SA	$V_{DD}Q$	DQh	DQh
U	DQd	DQd	V_{SS}	TMS	TDI	SA	SA0	SA	TDO	TCK	V_{SS}	DQh	DQh

NOTE: Pins 11B and 3B reserved for address expansion; 32Mb and 64Mb respectively.

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FBGA PIN DESCRIPTIONS

x72	SYMBOL	TYPE	DESCRIPTION
7R 7P 3A, 4A, 10A, 11A, 4B, 5B, 9B, 10B, 4P, 5P, 9P, 10P, 4R, 5R, 9R, 10R	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
3F 3G 3J 3K 11F 11G 11J 11K	BWa# BWb# BWc# BWd# BWe# BWf# BWg# BWh#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins; BWe# controls DQe pins; BWf# controls DQf pins; BWg# controls DQg pins; BWh# controls DQh pins.
7B	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
6C	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
6B	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
6A	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
9A	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
8A	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
8B	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
7A	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
5A	MODE	Input (LBO#)	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.

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FBGA PIN DESCRIPTIONS (continued)

x72	SYMBOL	TYPE	DESCRIPTION
8R 8P 6R	TMS DI TCK	Input	IEEE 1149.1 Test Inputs: JEDEC-standard 2.5V I/O levels. These pins may be left Not Connected if the JTAG function is not used in the circuit.
(a) 1A, 2A, 1B, 2B, 1C, 2C, 3C, 1D, 2D (b) 3D, 1E, 2E, 3E, 1F, 2F, 1G, 2G, 1H (c) 2H, 1J, 2J, 1K, 2K, 1L, 2L, 3L, 1M (d) 2M, 3M 1N, 2N, 3N, 1P, 2P, 1R, 2R (e) 12A, 13A, 12B, 13B, 11C, 12C, 13C, 11D, 12D (f) 13D, 11E, 12E, 13E, 12F, 13F, 12G, 13G, 12H (g) 13H, 12J, 13J, 12K, 13K, 11L, 12L, 13L, 11M (h) 12M, 13M, 11N, 12N, 13N, 12P, 13P, 12R, 13R	DQa DQb DQc DQd DQe DQf DQg DQh	Input/ Output	SRAM Data I/Os: Byte "a" is associated with DQa pins; Byte "b" is associated with DQb pins; Byte "c" is associated with DQc pins; Byte "d" is associated with DQd pins; Byte "e" is associated with DQe pins; Byte "f" is associated with DQf pins; Byte "g" is associated with DQg pins; Byte "h" is associated with DQh pins. Input data must meet setup and hold times around the rising edge CLK.
6P	TDO	Output	IEEE 1149.1 Test Output: JEDEC-standard 2.5V I/O level.
7C, 7D, 7E, 7F, 7G, 5H, 6H, 7H, 8H, 9H, 7J, 7K, 7L, 7M, 7N	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4C, 5C, 9C, 10C, 4D, 10D, 4E, 10E, 4F, 10F, 4G, 10G, 4H, 10H, 4J, 10J, 4K, 10K, 4L, 10L, 4M, 10M, 4N, 5N, 9N, 10N	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5D, 6D, 8D, 9D, 5E, 6E, 8E, 9E, 5F, 6F, 8F, 9F, 5G, 6G, 8G, 9G, 5J, 6J, 8J, 9J, 5K, 6K, 8K, 9K, 5L, 6L, 8L, 9L, 5M, 6M, 8M, 9M	V_{SS}	Supply	Ground: GND.
3B, 11B, 8C, 3H, 11H, 11P, 3R, 11R	NC	–	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance. Pins 11B and 3B are reserved for future address expansion; 32Mb and 64Mb respectively.

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PIN LAYOUT (TOP VIEW)
209-PIN BGA

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	SA	CE2	SA	ADV/LD#	SA	CE2#	SA	DQb	DQb
B	DQg	DQg	BWc#	BWg#	NC	R/W#	SA	BWb#	BWf#	DQb	DQb
C	DQg	DQg	BWh#	BWd#	NC	CE#	NC	BWe#	BWa#	DQb	DQb
D	DQg	DQg	V_{SS}	NC	NC	G#/OE#	GW#	NC	V_{SS}	DQb	DQb
E	DQPg	DQPc	$V_{DD}Q$	$V_{DD}Q$	V_{DD}	V_{DD}	V_{DD}	$V_{DD}Q$	$V_{DD}Q$	DQPf	DQPb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
G	DQc	DQc	$V_{DD}Q$	$V_{DD}Q$	V_{DD}	V_{DD}	V_{DD}	$V_{DD}Q$	$V_{DD}Q$	DQf	DQf
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
J	DQc	DQc	$V_{DD}Q$	$V_{DD}Q$	V_{DD}	V_{DD}	V_{DD}	$V_{DD}Q$	$V_{DD}Q$	DQf	DQf
K	NC	NC	CLK	NC	V_{SS}	CKE#	V_{SS}	NC	NC	NC	NC
L	DQh	DQh	$V_{DD}Q$	$V_{DD}Q$	V_{DD}	V_{DD}	V_{DD}	$V_{DD}Q$	$V_{DD}Q$	DQa	DQa
M	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	DQh	DQh	$V_{DD}Q$	$V_{DD}Q$	V_{DD}	V_{DD}	V_{DD}	$V_{DD}Q$	$V_{DD}Q$	DQa	DQa
P	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQPd	DQPh	$V_{DD}Q$	$V_{DD}Q$	V_{DD}	V_{DD}	V_{DD}	$V_{DD}Q$	$V_{DD}Q$	DQPa	DQPe
T	DQd	DQd	V_{SS}	NC	NC	MODE#/ LBO	NC	NC	V_{SS}	DQe	DQe
U	DQd	DQd	NC	SA	NC	SA	NC	SA	NC	DQe	DQe
V	DQd	DQd	SA	SA	SA	SA1	SA	SA	SA	DQe	DQe
W	DQd	DQd	TMS	TDI	SA	SA0	SA	TDO	TCK	DQe	DQe

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PBGA PIN DESCRIPTIONS

x72	SYMBOL	TYPE	DESCRIPTION
6W 6V 3A, 5A, 7A, 9A, 7B, 4U, 6U, 8U, 3V, 9V, 5W, 7W	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
9C 8B 3B 4C 8C 9B 4B 3C	BWa# BWb# BWc# BWd# BWe# BWf# BWg# BWh#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins.
3K	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
6C	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
8A	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
4A	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
6D	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
6A	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
6K	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
6P	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. This pin has an internal pull-down and can be floating.
3W 4W 9W	TMS TDI TCK	Input	IEEE 1149.1 Test Inputs: JEDEC-standard 2.5V I/O levels. These pins may be left Not Connected if the JTAG function is not used in the circuit.

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PBGA PIN DESCRIPTIONS (continued)

x72	SYMBOL	TYPE	DESCRIPTION
6B	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
6T	MODE	Input (LBO#)	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
10L, 11L, 10M, 11M, 10N, 11N, 10P, 11P, 10A, 11A, 10B, 11B, 10C, 11C, 10D, 11D 1F, 2F, 1G, 2G, 1H, 2H, 1J, 2J 1T, 2T, 1U, 2U, 1V, 2V, 1W, 2W 10T, 11T, 10U, 11U, 10V, 11V, 10W, 11W 10F, 11F, 10G, 11G, 10H, 11H, 10J, 11J 1A, 2A, 1B, 2B, 1C, 2C, 1D, 2D, 1L, 2L, 1M, 2M, 1N, 2N, 1P, 2P	DQa DQb DQc DQd DQe DQf DQg DQh	Input/ Output	SRAM Data I/Os: Byte "a" is associated with DQa pins; Byte "b" is associated with DQb pins; Byte "c" is associated with DQc pins; Byte "d" is associated with DQd pins. Input data must meet setup and hold times around the rising edge CLK.
10R 11E 2E 1R 11R 10E 1E 2R	DQPa DQPb DQPc DQPd DQPe DQPf DQPh DQPh	NC/ I/O	These are parity pins which hold the parity bit information but have no parity logic.
5E, 6E, 7E, 5G, 6G, 7G, 5J, 6J, 7J, 5L, 6L, 7L, 5N, 6N, 7N, 5R, 6R, 7R	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
3E, 4E, 8E, 9E, 3G, 4G, 8G, 9G, 3J, 4J, 8J, 9J, 3L, 4L, 8L, 9L, 3N, 4N, 8N, 9N, 3R, 4R, 8R, 9R	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
8W	TDO	Output	IEEE 1149.1 Test Output: JEDEC-standard 2.5V I/O level.

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PBGA PIN DESCRIPTIONS (continued)

x72	SYMBOL	TYPE	DESCRIPTION
3D, 9D, 3F, 4F, 5F, 6F, 7F, 8F, 9F, 3H, 4H, 5H, 6H, 7H, 8H, 9H, 5K, 7K, 3M, 4M, 5M, 7M , 8M, 9M, 3P, 4P, 5P, 7P, 8P, 9P, 3T, 9T	Vss	Supply	Ground: GND.
5B, 5C, 7C, 4D, 5D, 8D, 1K, 2K, 4K, 8K, 9K, 10K, 11K, 4T, 5T, 7T, 8T, 3U, 5U, 7U, 9U	NC	–	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance.

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INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR READ/WRITE COMMANDS (x72)

FUNCTION	R/W#	BWa#	BWb#	BWc#	BWd#	BWe#	BWf#	BWg#	BWh#
READ	H	X	X	X	X	X	X	X	X
WRITE Byte “a”	L	L	H	H	H	H	H	H	H
WRITE Byte “b”	L	H	L	H	H	H	H	H	H
WRITE Byte “c”	L	H	H	L	H	H	H	H	H
WRITE Byte “d”	L	H	H	H	L	H	H	H	H
WRITE Byte “e”	L	H	H	H	H	L	H	H	H
WRITE Byte “f”	L	H	H	H	H	H	L	H	H
WRITE Byte “g”	L	H	H	H	H	H	H	L	H
WRITE Byte “h”	L	H	H	H	H	H	H	H	L

NOTE: Pins 11B and 3B reserved for address expansion; 32Mb and 64Mb respectively.

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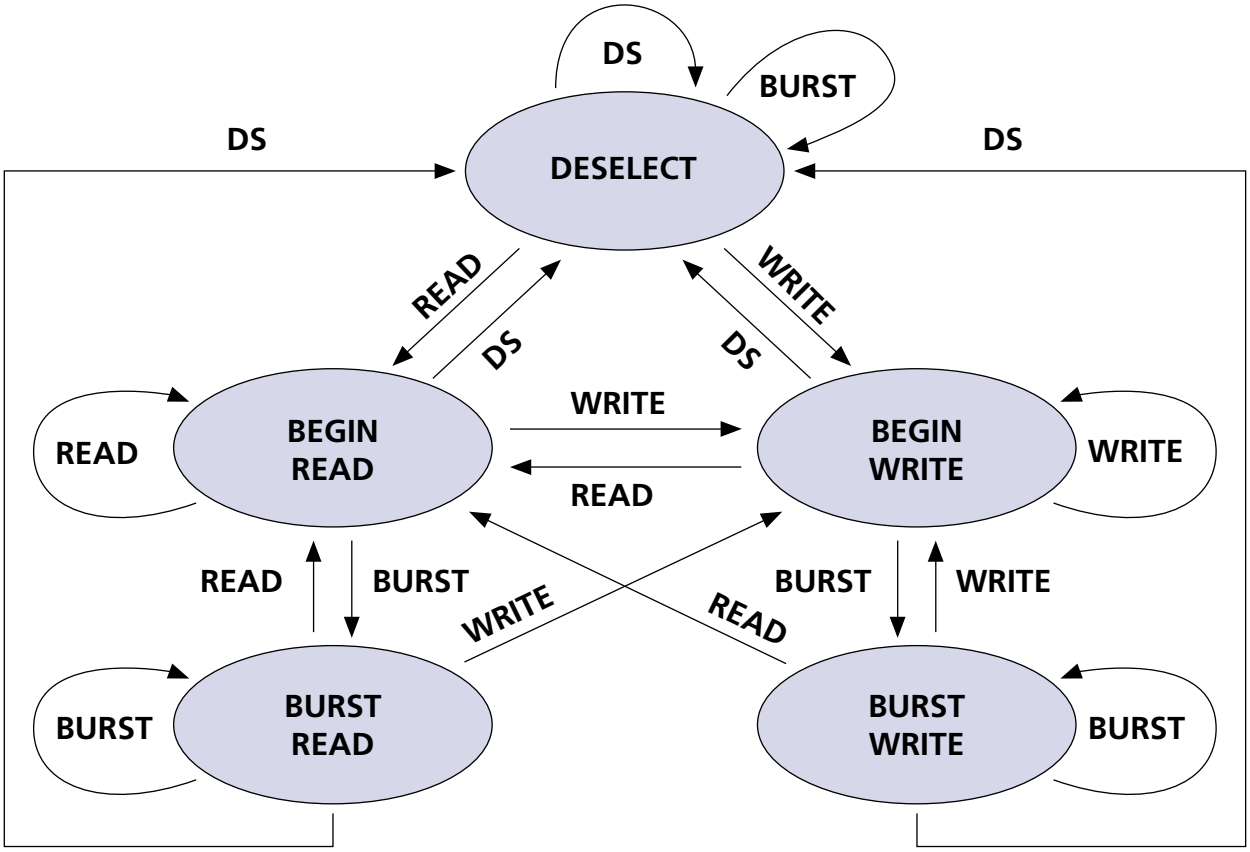
STATE DIAGRAM FOR ZBT SRAM



KEY:

COMMAND	OPERATION
DS	DESELECT
READ	New READ
WRITE	New WRITE
BURST	BURST READ, BURST WRITE or CONTINUE DESELECT

NOTE: 1. A STALL or IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE# HIGH only blocks the clock (CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock (CLK).

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TRUTH TABLE

(Notes 5-10)

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADV/ LD#	R/W#	BWx	OE#	CKE#	CLK	DQ	NOTES
DESELECT Cycle	None	H	X	X	L	L	X	X	X	L	L→H	High-Z	
DESELECT Cycle	None	X	H	X	L	L	X	X	X	L	L→H	High-Z	
DESELECT Cycle	None	X	X	L	L	L	X	X	X	L	L→H	High-Z	
CONTINUE DESELECT Cycle	None	X	X	X	L	H	X	X	X	L	L→H	High-Z	1
READ Cycle (Begin Burst)	External	L	L	H	L	L	H	X	L	L	L→H	Q	
READ Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L→H	Q	1, 11
NOP/DUMMY READ (Begin Burst)	External	L	L	H	L	L	H	X	H	L	L→H	High-Z	2
DUMMY READ (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L→H	High-Z	1, 2, 11
WRITE Cycle (Begin Burst)	External	L	L	H	L	L	L	L	X	L	L→H	D	3
WRITE Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L→H	D	1, 3, 11
NOP/WRITE ABORT (Begin Burst)	None	L	L	H	L	L	L	H	X	L	L→H	High-Z	2, 3
WRITE ABORT (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L→H	High-Z	1, 2, 3, 11
IGNORE CLOCK EDGE (Stall)	Current	X	X	X	L	X	X	X	X	H	L→H	–	4
SNOOZE MODE	None	X	X	X	H	X	X	X	X	X	X	High-Z	

NOTE:
1. CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chosen in the initial BEGIN BURST cycle. A CONTINUE DESELECT cycle can only be entered if a DESELECT cycle is executed first.
2. DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.
3. OE# may be wired LOW to minimize the number of control signals to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. OE# may be used when the bus turn-on and turn-off times do not meet an application's requirements.
4. If an IGNORE CLOCK EDGE command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the IGNORE CLOCK EDGE cycle.
5. X means "Don't Care." H means logic HIGH. L means logic LOW. BWx = H means all byte write signals (BWa#, BWb#, BWc#, BWd#, BWe#, BWf#, BWg#, and BWh#) are HIGH. BWx = L means one or more byte write signals are LOW.
6. BWa# enables WRITEs to Byte "a" (DQa pins); BWb# enables WRITEs to Byte "b" (DQb pins); BWc# enables WRITEs to Byte "c" (DQc pins); BWd# enables WRITEs to Byte "d" (DQd pins); BWe# enables WRITEs to Byte "e" (DQe pins); BWf# enables WRITEs to Byte "f" (DQf pins); BWg# enables WRITEs to Byte "g" (DQg pins); BWh# enables WRITEs to Byte "h" (DQh pins).
7. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
8. Wait states are inserted by setting CKE# HIGH.
9. This device contains circuitry that will ensure that the outputs will be in High-Z during power-up.
10. The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth burst cycle.
11. The address counter is incremented for all CONTINUE BURST cycles.

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3.3V VDD, ABSOLUTE MAXIMUM RATINGS*

Voltage on VDD Supply Relative to VSS ..... -0.5V to +4.6V
Voltage on VDDQ Supply Relative to VSS ..... -0.5V to VDD
VIN ..... -0.5V to VDDQ + 0.5V
Storage Temperature (plastic) ..... -55°C to +150°C
Junction Temperature** ..... +150°C
Short Circuit Output Current 100mA

2.5V VDD, ABSOLUTE MAXIMUM RATINGS*

Voltage on VDD Supply Relative to VSS ..... -0.3V to +3.6V
Voltage on VDDQ Supply Relative to VSS ..... -0.3V to +3.6V
VIN ..... -0.3V to VDDQ + 0.3V
Storage Temperature (plastic) ..... -55°C to +150°C
Junction Temperature** ..... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

3.3V VDD, 3.3V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; VDD = +3.3V ±0.165V, VDDQ = +3.3V ±0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.0	VDD + 0.3	V	1, 2
Input High (Logic 1) Voltage	DQ pins	VIH	2.0	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-1.0	1.0	µA	3, 6
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDD	ILO	-1.0	1.0	µA	
Output High Voltage	IOH = -4.0mA	VOH	2.4	–	V	1, 4
Output Low Voltage	IOL = 8.0mA	VOL	–	0.4	V	1, 4
Supply Voltage		VDD	3.135	3.465	V	1
Isolated Output Buffer Supply		VDDQ	3.135	VDD	V	1, 5

NOTE:
1. All voltages referenced to VSS (GND).
2. For 3.3V VDD:
   Overshoot: VIH ≤ +4.6V for t ≤ ^{t}KC/2 for I ≤ 20mA
   Undershoot: VIL ≥ -0.7V for t ≤ ^{t}KC/2 for I ≤ 20mA
   Power-up: VIH ≤ +3.6V and VDD ≤ 3.135V for t ≤ 200ms
   For 2.5V VDD:
   Overshoot: VIH ≤ +3.6V for t ≤ ^{t}KC/2 for I ≤ 20mA
   Undershoot: VIL ≥ -0.5V for t ≤ ^{t}KC/2 for I ≤ 20mA
   Power-up: VIH ≤ +2.65V and VDD ≤ 2.375V for t ≤ 200ms
3. MODE pin has an internal pull-up, and input leakage = ±10µA.
4. The load used for VOH, VOL testing is shown in Figure 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
5. VDDQ should never exceed VDD. VDD and VDDQ can be externally wired together to the same power supply.
6. Ms# pin has an internal pull-down , and input leakage = ±10µA.

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3.3V V_{DD}, 2.5V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V ±0.165V; $V_{DD}Q$ = ±0.125V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	$V_{IH}Q$	1.7	$V_{DD}Q$ + 0.3	V	1, 2
	Inputs	V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-1.0	1.0	µA	3, 4
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (DQx)	I_{LO}	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	1.7	–	V	1
	I_{OH} = -1.0mA	V_{OH}	2.0	–	V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}	–	0.7	V	1
	I_{OL} = 1.0mA	V_{OL}	–	0.4	V	1
Supply Voltage		V_{DD}	3.135	3.465	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	2.375	2.625	V	1

2.5V V_{DD}, 2.5V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V ±0.165V; $V_{DD}Q$ = +2.5V ±0.125V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	$V_{IH}Q$	1.7	$V_{DD}Q$ + 0.3	V	1, 2
	Inputs	V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-1.0	1.0	µA	3, 4
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (DQx)	I_{LO}	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	1.7	–	V	1
	I_{OH} = -1.0mA	V_{OH}	2.0	–	V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}	–	0.7	V	1
	I_{OL} = 1.0mA	V_{OL}	–	0.4	V	1
Supply Voltage		V_{DD}	2.375	3.625	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	2.375	3.625	V	1

NOTE: 1. All voltages referenced to V_{SS} (GND).
2. For 3.3V V_{DD}:
   Overshoot: V_{IH} ≤ +4.6V for t ≤ $^tKC/2$ for I ≤ 20mA
   Undershoot: V_{IL} ≥ -0.7V for t ≤ $^tKC/2$ for I ≤ 20mA
   Power-up: V_{IH} ≤ +3.6V and V_{DD} ≤ 3.135V for t ≤ 200ms
   For 2.5V V_{DD}:
   Overshoot: V_{IH} ≤ +3.6V for t ≤ $^tKC/2$ for I ≤ 20mA
   Undershoot: V_{IL} ≥ -0.5V for t ≤ $^tKC/2$ for I ≤ 20mA
   Power-up: V_{IH} ≤ +2.65V and V_{DD} ≤ 2.375V for t ≤ 200ms
3. MODE pin has an internal pull-up, and input leakage = ±10µA.
4. Ms# pin has an internal pull-down , and input leakage = ±10µA.

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FBGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	TBD	TBD	pF	1
Input/Output Capacitance (DQ)	V_{DD} = 3.3V	C_O	TBD	TBD	pF	1
Address Capacitance		C_A	TBD	TBD	pF	1
Clock Capacitance		C_{CK}	TBD	TBD	pF	1

PBGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	TBD	TBD	pF	1
Input/Output Capacitance (DQ)	V_{DD} = 3.3V	C_O	TBD	TBD	pF	1
Address Capacitance		C_A	TBD	TBD	pF	1
Clock Capacitance		C_{CK}	TBD	TBD	pF	1

FBGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	TBD	°C/W	1
Thermal Resistance (Junction to Top of Case)		θ_{JC}	TBD	°C/W	1

PBGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	TBD	°C/W	1
Thermal Resistance (Junction to Top of Case)		θ_{JC}	TBD	°C/W	1
Thermal Resistance (Junction to Pins)		θ_{JC}	TBD	°C/W	1

NOTE: 1. This parameter is sampled.

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I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Note 1) (0°C ≤ T_A ≤ +70°C)

				MAX				
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-6**	**-7.5**	**-10**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKC (MIN); V_{DD} = MAX; Outputs open	I_{DD}	TBD	475	425	325	mA	2, 3, 4
Power Supply Current: Idle	Device selected; V_{DD} = MAX; CKE# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{DD1}	TBD	32	29	24	mA	2, 3, 4
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; All inputs static; CLK frequency = 0	I_{SB2}	TBD	10	10	10	mA	3, 4
TTL Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or ≥ V_{IH}; All inputs static; CLK frequency = 0	I_{SB3}	TBD	25	25	25	mA	3, 4
Clock Running	Device deselected; V_{DD} = MAX; ADV/LD# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{SB4}	TBD	120	105	75	mA	3, 4
Snooze Mode	ZZ ≥ V_{IH}	I_{SB2Z}	TBD	10	10	10	mA	4

NOTE:
1. If V_{DD} = +3.3V, then $V_{DD}Q$ = +3.3V or +2.5V. If V_{DD} = +2.5V, then $V_{DD}Q$ = +2.5V. Voltage tolerances: +3.3V ±0.165 or +2.5V ±0.125V for all values of V_{DD} and $V_{DD}Q$.
2. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in a deselected cycle as defined in the truth table. "Device selected" means device is active (not in deselected mode).
4. Typical values are measured at 3.3V, 25°C and 10ns cycle time.

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AC ELECTRICAL CHARACTERISTICS

(Notes 6, 8, 9, 10) (0°C ≤ T_A ≤ +70°C)(Original ZBT MODE: MS# = HIGH)

DESCRIPTION	SYMBOL	-6		-7.5		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Clock									
Clock cycle time	^{t}KHKH	6.0		7.5		10		ns	
Clock frequency	^{f}KF		166		133		100	MHz	
Clock HIGH time	^{t}KHKL	1.8		2.2		3.2		ns	1
Clock LOW time	^{t}KLKH	1.8		2.2		3.2		ns	1
Output Times									
Clock to output valid	^{t}KHQV		3.5		4.2		5.0	ns	
Clock to output invalid	^{t}KHQX	1.5		1.5		1.5		ns	2
Clock to output in Low-Z	^{t}KHQX1	1.5		1.5		1.5		ns	2, 3, 4, 5
Clock to output in High-Z	^{t}KHQZ	1.5	3.0	1.5	3.0	1.5	3.3	ns	2, 3, 4, 5
OE# to output valid	^{t}GLQV		3.5		4.2		5.0	ns	6
OE# to output in Low-Z	^{t}GLQX	0		0		0		ns	2, 3, 4, 5
OE# to output in High-Z	^{t}GHQZ		3.5		4.2		5.0	ns	2, 3, 4, 5
Setup Times									
Address	^{t}AVKH	1.5		1.7		2.0		ns	7
Clock enable (CKE#)	^{t}EVKH	1.5		1.7		2.0		ns	7
Control signals	^{t}CVKH	1.5		1.7		2.0		ns	7
Data-in	^{t}DVKH	1.5		1.7		2.0		ns	7
Hold Times									
Address	^{t}KHAX	0.5		0.5		0.5		ns	7
Clock enable (CKE#)	^{t}KHEX	0.5		0.5		0.5		ns	7
Control signals	^{t}KHCX	0.5		0.5		0.5		ns	7
Data-in	^{t}KHDX	0.5		0.5		0.5		ns	7

NOTE:
1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Refer to Technical Note TN-55-01, "Designing with ZBT SRAMs," for a more thorough discussion of these parameters.
3. This parameter is sampled.
4. This parameter is measured with output loading as shown in Figure 2 for 3.3V I/O and Figure 4 for 2.5V I/O.
5. Transition is measured ±200mV from steady state voltage.
6. OE# can be considered a "Don't Care" during WRITEs; however, controlling OE# can help fine-tune a system for turnaround timing.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when they are being registered into the device. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when ADV/LD# is LOW to remain enabled.
8. Test conditions as specified with output loading as shown in Figure 1 for 3.3V I/O ($V_{DD}Q$ = +3.3V ±0.165V) and Figure 3 for 2.5V I/O ($V_{DD}Q$ = +2.5V +0.4V/-0.125V).
9. A WRITE cycle is defined by R/W# LOW having been registered into the device at ADV/LD# LOW. A READ cycle is defined by R/W# HIGH with ADV/LD# LOW. Both cases must meet setup and hold times.
10. If V_{DD} = +3.3V, then $V_{DD}Q$ = +3.3V or +2.5V. If V_{DD} = +2.5V, then $V_{DD}Q$ = +2.5V. Voltage tolerances: +3.3V ±0.165 or +2.5V ±0.125V for all values of V_{DD} and $V_{DD}Q$.

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3.3V V_{DD}, 3.3V I/O AC TEST CONDITIONS

Input pulse levels	V_{IH} = (V_{DD}/2.2) + 1.5V
	V_{IL} = (V_{DD}/2.2) - 1.5V
Input rise and fall times	1ns
Input timing reference levels	V_{DD}/2.2
Output reference levels	$V_{DD}Q$/2.2
Output load	See Figures 1 and 2

3.3V I/O Output Load Equivalents

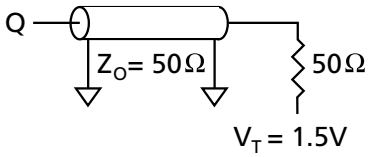

Figure 1

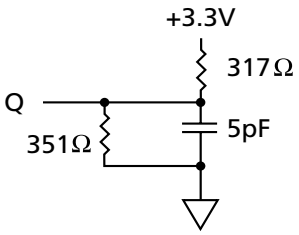

Figure 2

3.3V V_{DD}, 2.5V I/O AC TEST CONDITIONS

Input pulse levels	V_{IH} = (V_{DD}/2.64) + 1.25V
	V_{IL} = (V_{DD}/2.64) - 1.25V
Input rise and fall times	1ns
Input timing reference levels	V_{DD}/2.64
Output reference levels	$V_{DD}Q$/2
Output load	See Figures 3 and 4

2.5V V_{DD}, 2.5V I/O AC TEST CONDITIONS

Input pulse levels	V_{IH} = (V_{DD}/2) + 1.25V
	V_{IL} = (V_{DD}/2) - 1.25V
Input rise and fall times	1ns
Input timing reference levels	V_{DD}/2
Output reference levels	$V_{DD}Q$/2
Output load	See Figures 3 and 4

2.5V I/O Output Load Equivalents

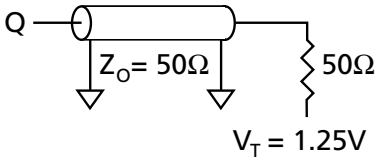

Figure 3

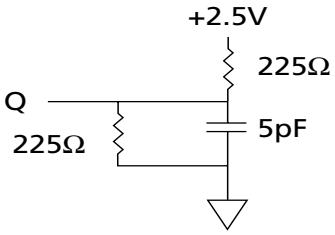

Figure 4

LOAD DERATING CURVES

Micron 256K x 72 ZBT SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.

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SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become disabled and all outputs go to High-Z.

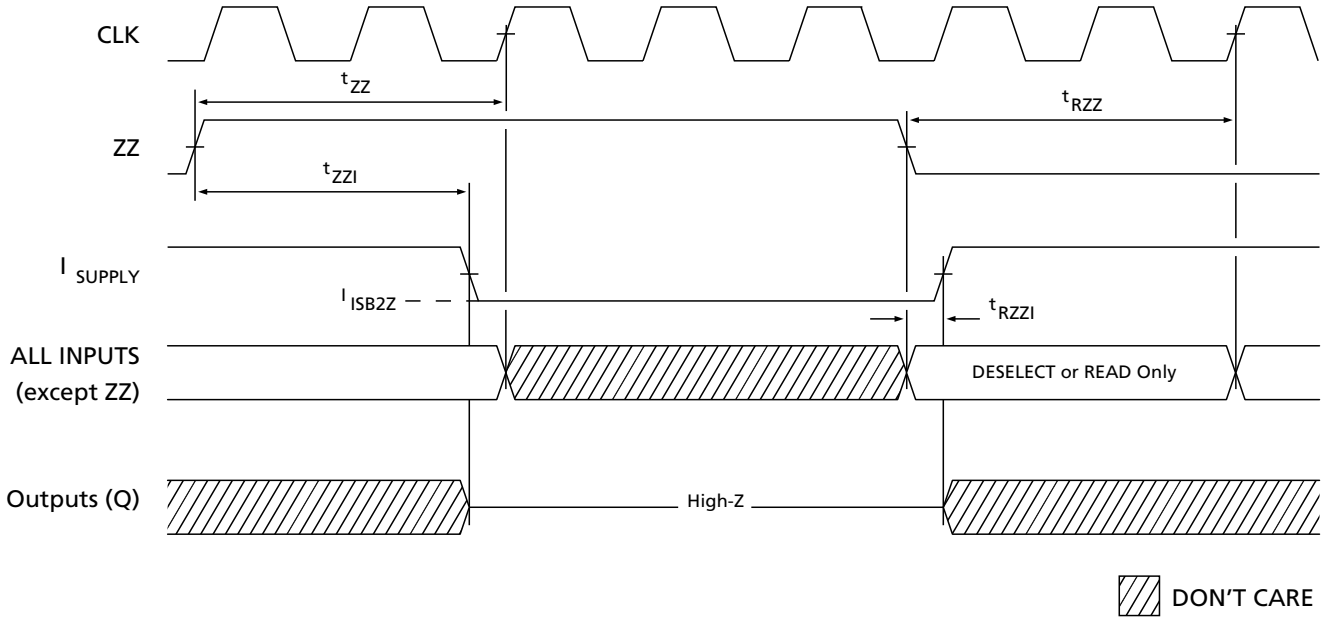
The ZZ pin is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH, I_{SB2Z} is guaranteed after the time ^{t}ZZI is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during ^{t}RZZ, only a DESELECT or READ cycle should be given.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	ZZ ≥ V_{IH}	I_{SB2Z}		10	mA	
ZZ active to input ignored		^{t}ZZ	0	2($^{t}KHKH$)	ns	1
ZZ inactive to input sampled		^{t}RZZ	0	2($^{t}KHKH$)	ns	1
ZZ active to snooze current		^{t}ZZI		2($^{t}KHKH$)	ns	1
ZZ inactive to exit snooze current		$^{t}RZZI$	0		ns	1

NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM



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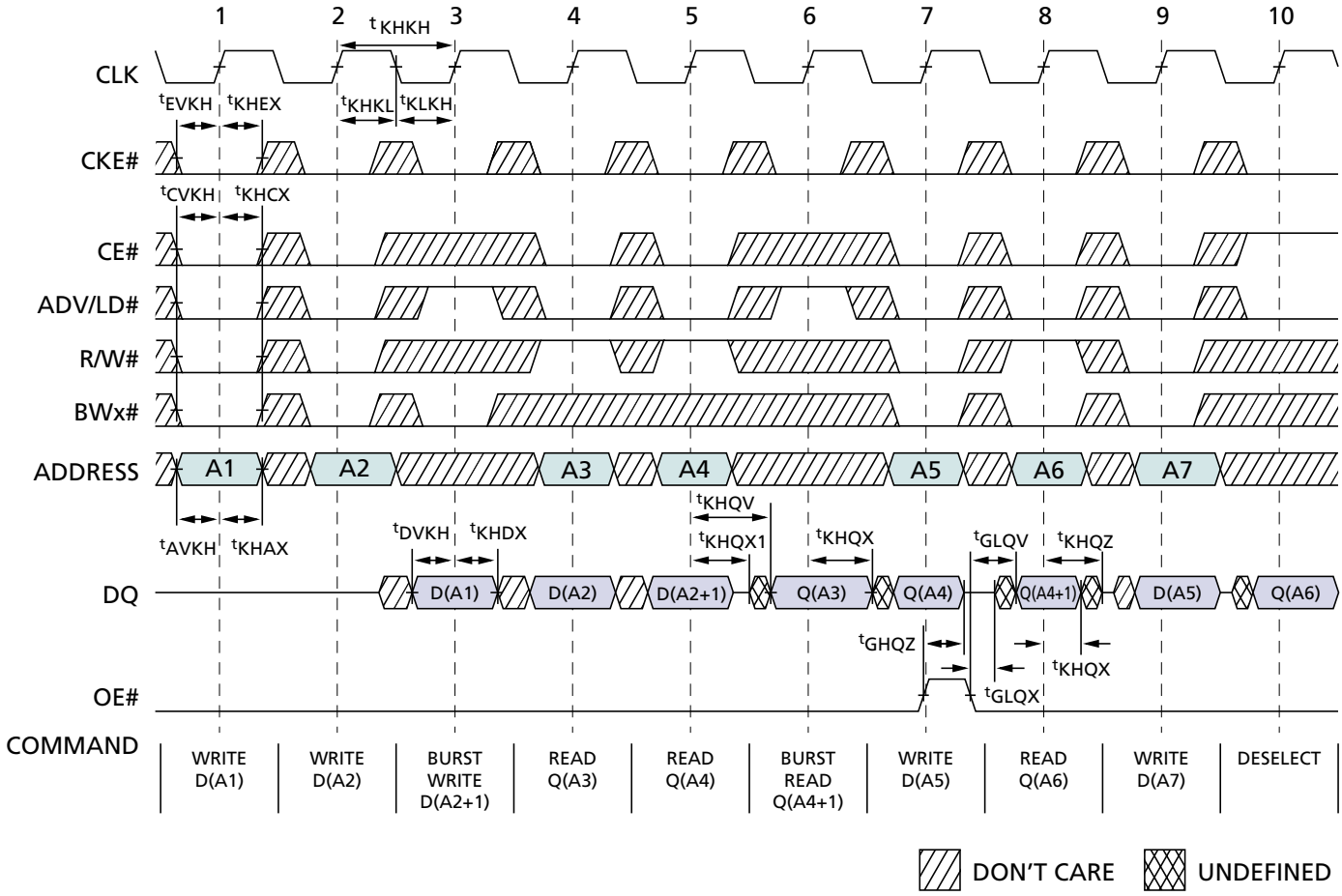
READ/WRITE TIMING FOR ORIGINAL ZBT



READ/WRITE TIMING PARAMETERS

	-6		-7.5		-10		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tKHKH	6.0		7.5		10		ns
tKHKL	1.8		2.2		3.2		ns
tKLKH	1.8		2.2		3.2		ns
tKHQV		3.5		4.2		5.0	ns
tKHQX	1.5		1.5		1.5		ns
tKHQX1	1.5		1.5		1.5		ns
tKHQZ	1.5	3.0	1.5	3.0	1.5	3.3	ns
tGLQV		3.5		4.2		5.0	ns
tGLQX	0		0		0		ns

	-6		-7.5		-10		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tGHQZ		3.5		4.2		5.0	ns
tAVKH	1.5		1.7		2.0		ns
tEVKH	1.5		1.7		2.0		ns
tCVKH	1.5		1.7		2.0		ns
tDVKH	1.5		1.7		2.0		ns
tKHAX	0.5		0.5		0.5		ns
tKHEX	0.5		0.5		0.5		ns
tKHCX	0.5		0.5		0.5		ns
tKHDX	0.5		0.5		0.5		ns

NOTE: 1. For this waveform, ZZ is tied LOW.
2. Burst sequence order is determined by MODE (0 = linear, 1 = interleaved). BURST operations are optional.
3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

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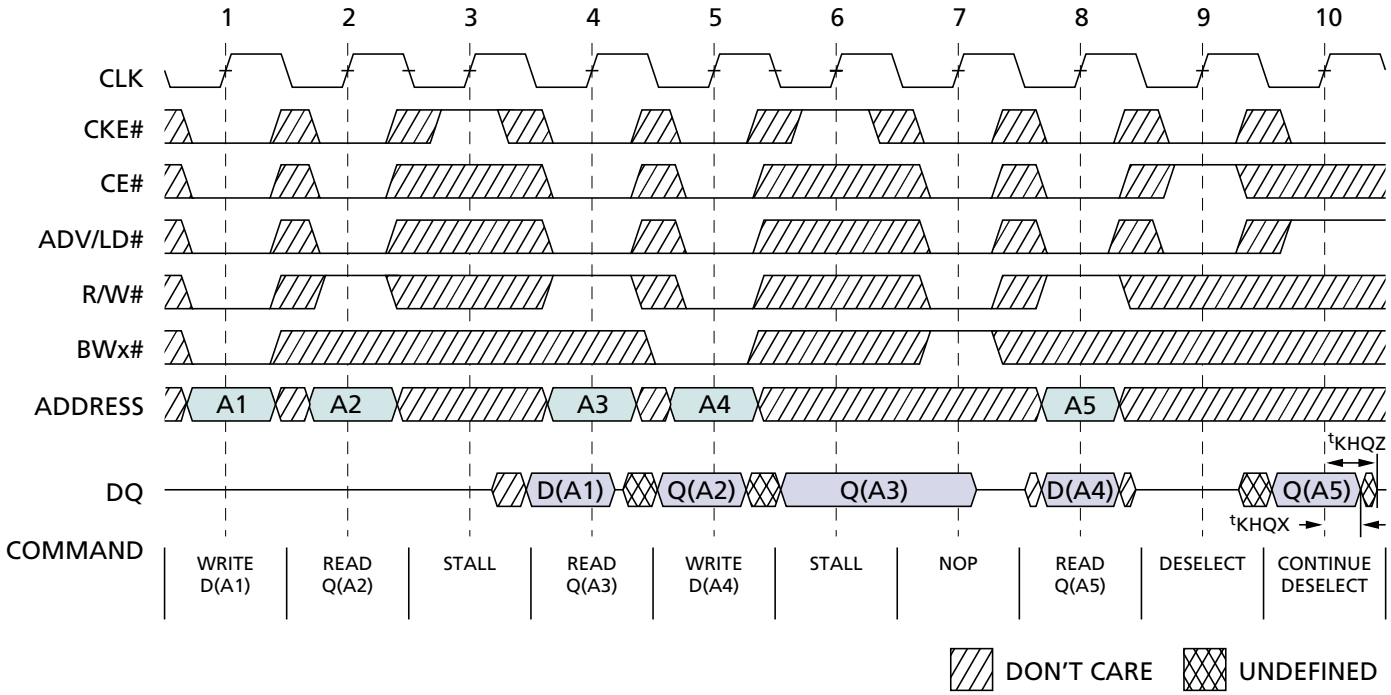
NOP, STALL AND DESELECT CYCLES



NOP, STALL AND DESELECT TIMING PARAMETERS

	-6		-7.5		-10		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}KHQX	1.5		1.5		1.5		ns
^{t}KHQZ	1.5	3.0	1.5	3.0	1.5	3.3	ns

NOTE:
1. The IGNORE CLOCK EDGE or STALL cycle (clock 3) illustrates CKE# being used to create a "pause." A WRITE is not performed during this cycle.
2. For this waveform, ZZ and OE# are tied LOW.
3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

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IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The 16Mb SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

DISABLING THE JTAG FEATURE

These pins can be left floating (unconnected), if the JTAG function is not to be implemented. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TEST ACCESS PORT (TAP)

TEST CLOCK (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

TEST MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 5. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 6.)

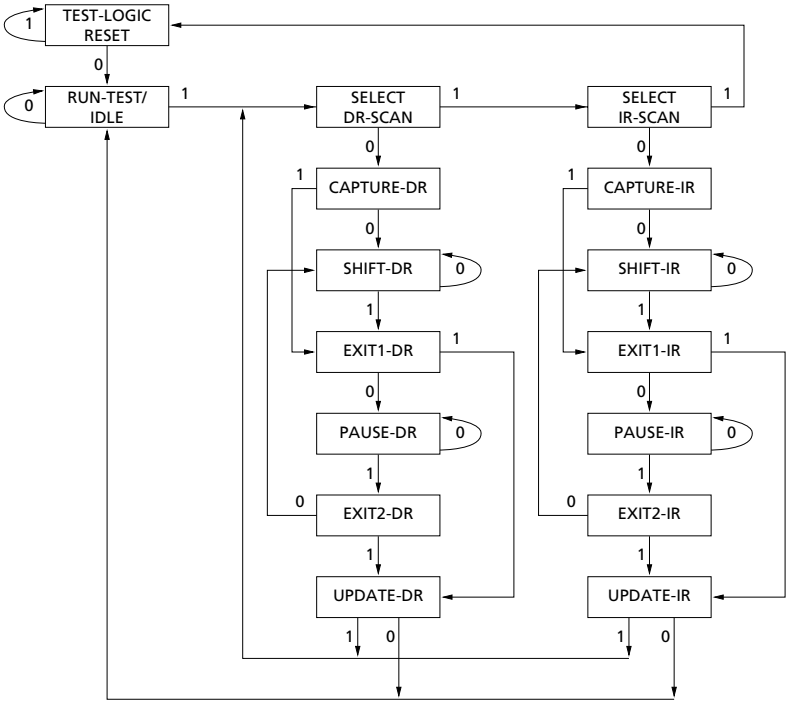

Figure 5
TAP Controller State Diagram

NOTE: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

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TEST DATA-OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. (See Figure 5.) The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Figure 6.)

PERFORMING A TAP RESET

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

INSTRUCTION REGISTER

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in Figure 5. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

BYPASS REGISTER

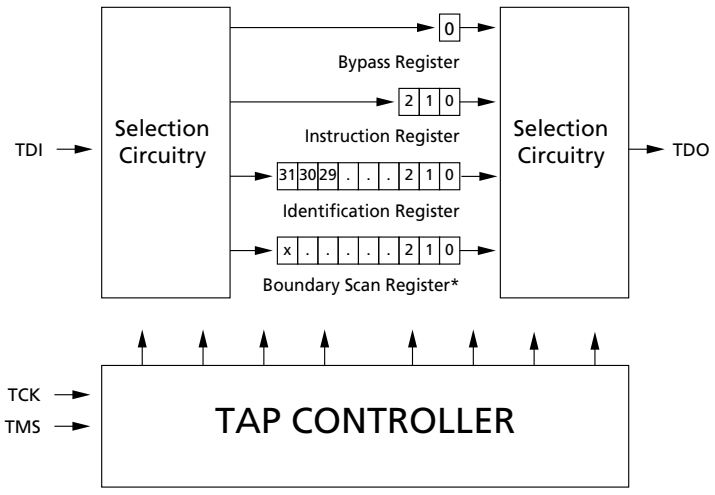
To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

BOUNDARY SCAN REGISTER

The boundary scan register is connected to all the input and bidirectional pins on the SRAM. The x72 configuration has a xxxTBD-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the pins on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.



*x = xxxTBD for the x72 configuration.

Figure 6
TAP Controller Block Diagram

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IDENTIFICATION (ID) REGISTER

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP INSTRUCTION SET

OVERVIEW

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

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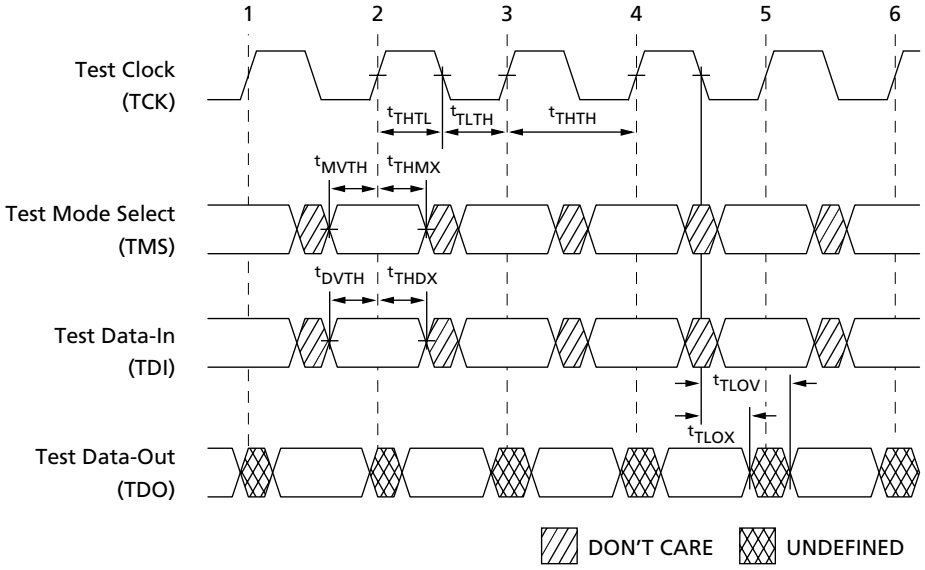
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

These instruction are not implemented but are reserved for future use. Do not use these instructions.

TAP TIMING



TAP AC ELECTRICAL CHARACTERISTICS

(Notes 1, 2) (+20°C ≤ T_J ≤ +100°C; +2.4V ≤ V_{DD} ≤ +2.6V)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	100		ns
Clock frequency	^fTF		10	MHz
Clock HIGH time	^tTHTL	40		ns
Clock LOW time	^tTLTH	40		ns
Output Times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		20	ns
TDI valid to TCK HIGH	^tDVTH	10		ns
TCK HIGH to TDI invalid	^tTHDX	10		ns
Setup Times				
TMS setup	^tMVTH	10		ns
Capture setup	^tCS	10		ns
Hold Times				
TMS hold	^tTHMX	10		ns
Capture hold	^tCH	10		ns

NOTE: 1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 7.

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TAP AC TEST CONDITIONS

Input pulse levels	V_{SS} to 2.5V
Input rise and fall times	1ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Test load termination supply voltage	1.25V

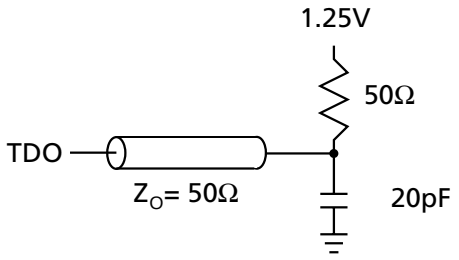

Figure 7
TAP AC Output Load Equivalent

TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+20°C ≤ T_J ≤ +110°C; +2.4V ≤ V_{DD} ≤ +2.6V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (DQx)	I_{LO}	-5.0	5.0	µA	
Output Low Voltage	I_{OLC} = 100µA	V_{OL1}		0.2	V	1
Output Low Voltage	I_{OLT} = 2mA	V_{OL2}		0.7	V	1
Output High Voltage	|I_{OHC}| = 100µA	V_{OH1}	2.1		V	1
Output High Voltage	|I_{OHT}| = 2mA	V_{OH2}	1.7		V	1

NOTE: 1. All voltages referenced to V_{SS} (GND).
2. Overshoot: V_{IH} (AC) ≤ V_{DD} + 1.5V for t ≤ $^tKHKH/2$
Undershoot: V_{IL} (AC) ≥ -0.5V for t ≤ $^tKHKH/2$
Power-up: V_{IH} ≤ +2.6V and V_{DD} ≤ 2.4V and $V_{DD}Q$ ≤ 1.4V for t ≤ 200ms
During normal operation, $V_{DD}Q$ must not exceed V_{DD}. Control input signals (such as LD#, R/W#, etc.) may not have pulse widths less than ^tKHKL (MIN) or operate at frequencies exceeding ^fKF (MAX).

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IDENTIFICATION REGISTER DEFINITIONS

INSTRUCTION FIELD	256K x 72	DESCRIPTION
REVISION NUMBER (31:28)	xxxx	Reserved for version number.
DEVICE DEPTH (27:23)	00111	Defines depth of 256K or 512K words.
DEVICE WIDTH (22:18)	xxxxxTBD	Defines width of x72 bits.
MICRON DEVICE ID (17:12)	xxxxxx	Reserved for future use.
MICRON JEDEC ID CODE (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

SCAN REGISTER SIZES

REGISTER NAME	BIT SIZE
Instruction	3
Bypass	1
ID	32
Boundary Scan	68

INSTRUCTION CODES

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

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BOUNDARY SCAN ORDER (x72)

BGA BIT#	SIGNAL NAME	PIN ID

BGA BIT#	SIGNAL NAME	PIN ID

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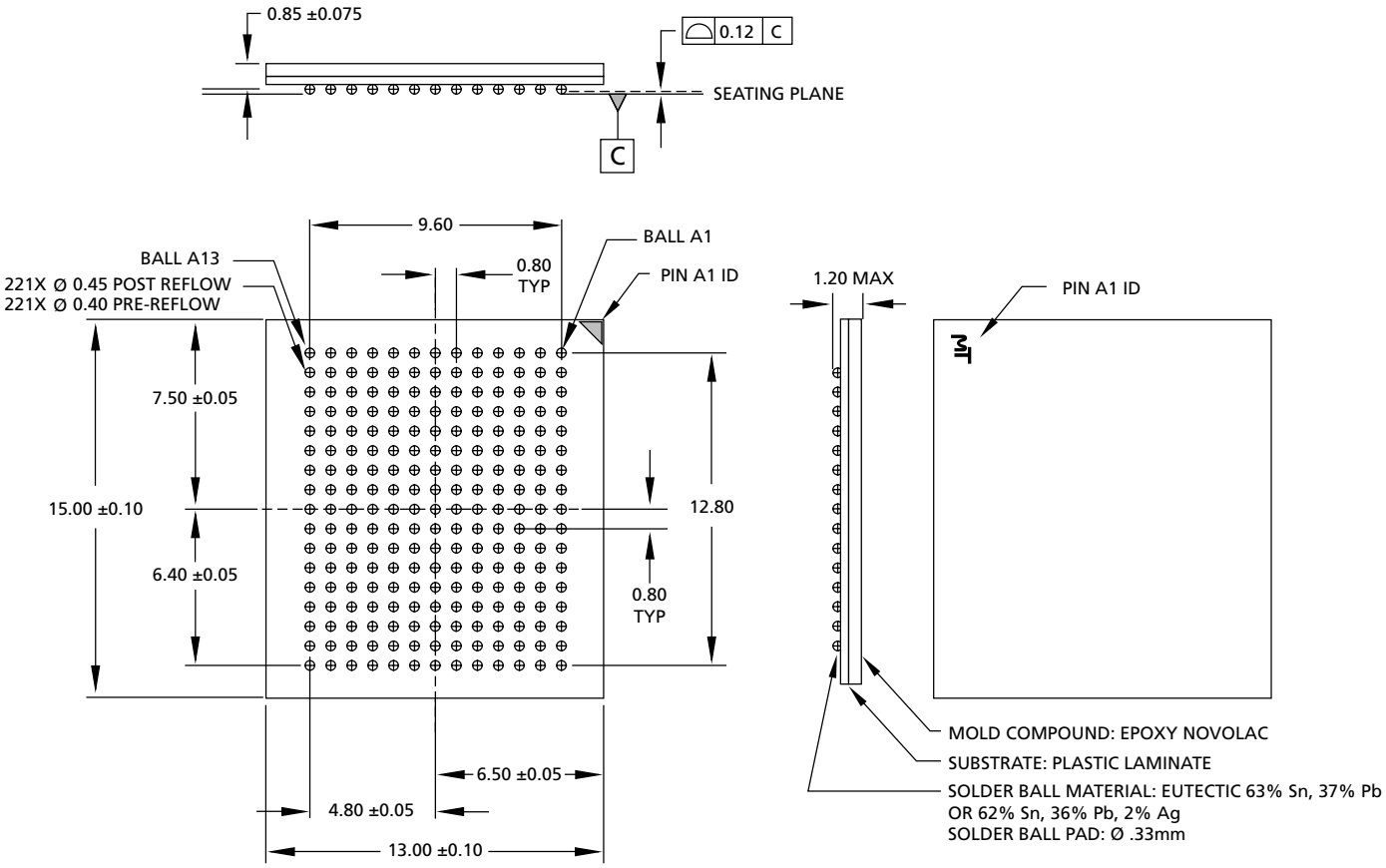
221-PIN FBGA



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

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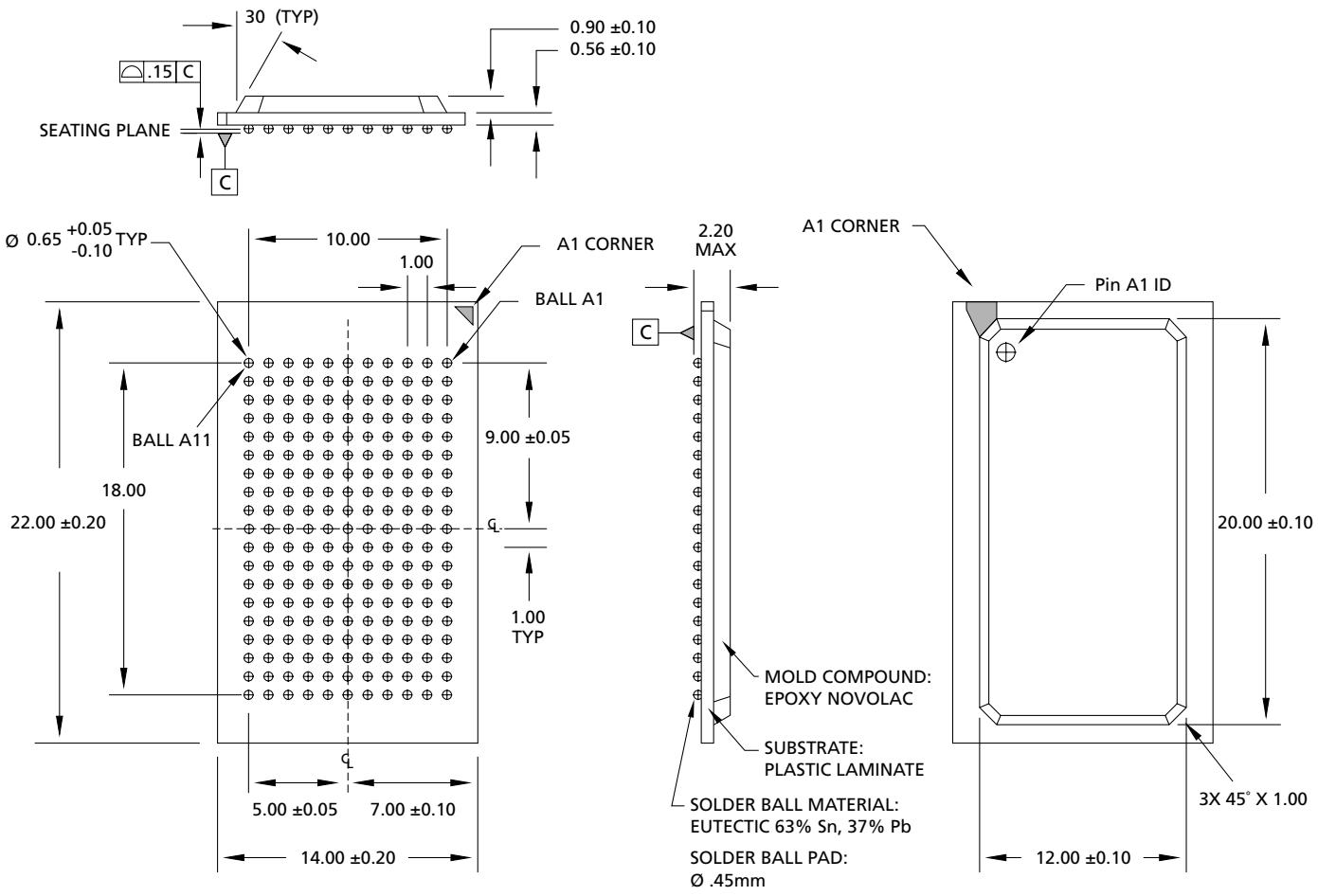
209-PIN PBGA



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
3. Solder ball land pad is Ø0.45mm.

DATA SHEET DESIGNATION

Advance: This data sheet contains initial descriptions of products still under development.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992

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REVISION HISTORY

Added 209-pin PBGApin diagram, Rev. 8/00, ADVANCE July/16/01

Changed 195-pin FBGA to 221-pin FBGA, Rev. 8/00, ADVANCE Aug/14/00

Original document, Rev. 5/00, ADVANCE May/00

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