

5 kV LED EMULATOR INPUT, 4.0 A ISOLATED GATE DRIVERS

Features

- Pin-compatible, drop-in upgrades for popular high speed opto-coupled gate drivers
- Low power diode emulator simplifies design-in process
- 0.6 and 4.0 Amp peak output drive current
- Rail-to-rail output voltage
- Performance and reliability advantages vs. opto-drivers
 - Resistant to temperature and age
 - 10x lower FIT rate for longer service life
 - 14x tighter part-to-part matching
 - Higher common-mode transient immunity: >50 kV/μs typical
- Robust protection features
 - Multiple UVLO ordering options (5, 8, and 12 V) with hysteresis
- 60 ns propagation delay, independent of input drive current
- Wide V_{DD} range: 5 to 30 V
- 3.75 and 5 kV reinforced isolation
 - UL, CSA, VDE
- AEC-Q100 qualified
- Wide operating temperature range
 - -40 to +125 °C
- RoHS-compliant packages
 - SOIC-8 (Narrow body)
 - DIP8 (Gull-wing)
 - SDIP6 (Stretched SO-6)
 - LGA8

Applications

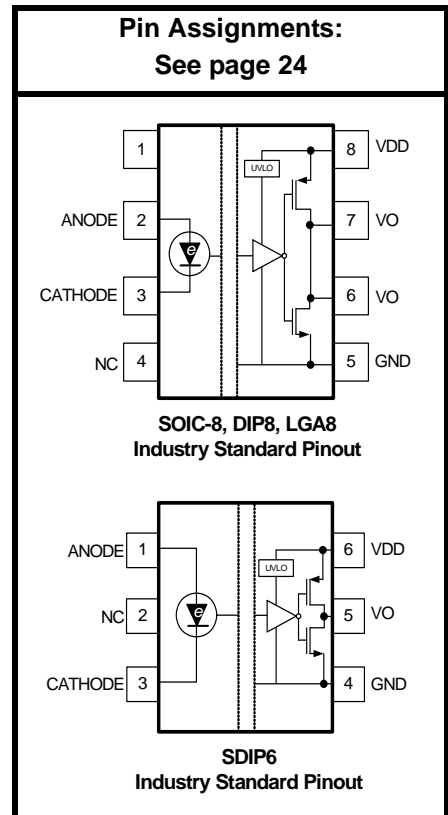
- IGBT/ MOSFET gate drives
- Industrial, HEV and renewable energy inverters
- AC, Brushless and DC motor controls and drives
- Variable speed motor control in consumer white goods
- Isolated switch mode and UPS power supplies

Safety Regulatory Approvals (Pending)

- UL 1577 recognized
 - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
 - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
 - IEC60747-5-2/VDE0884 Part 10 (basic/reinforced insulation)
- CQC certification approval
 - GB4943.1

Description

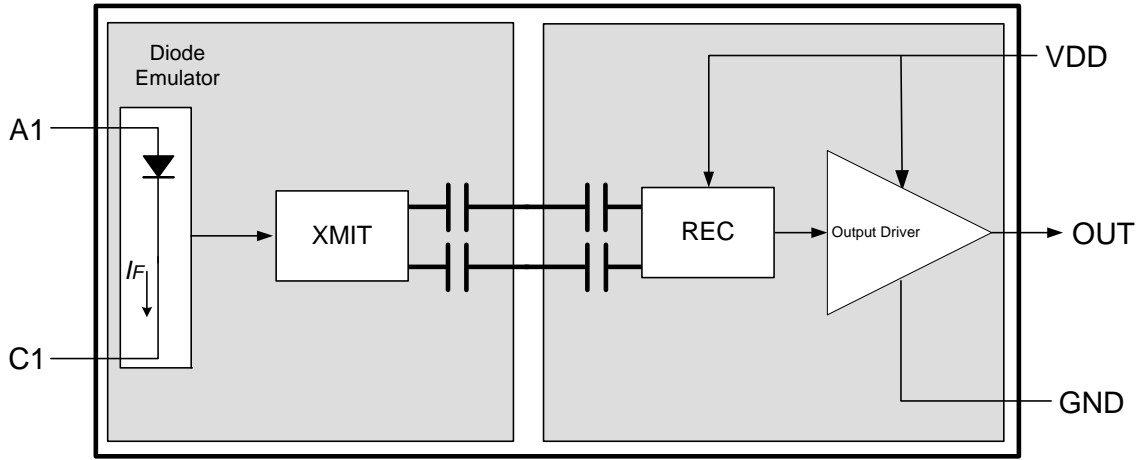
The Si826x isolators are pin-compatible, drop-in upgrades for popular opto-coupled gate drivers, such as 0.6 A ACPL-0302/3020, 2.5 A HCPL-3120/ACPL-3130, HCNW3120/3130, and similar opto-drivers. The devices are ideal for driving power MOSFETs and IGBTs used in a wide variety of inverter and motor control applications. The Si826x isolated gate drivers utilize Silicon Laboratories' proprietary silicon isolation technology, supporting up to 5.0 kV_{RMS} withstand voltage per UL1577. This technology enables higher-performance, reduced variation with temperature and age, tighter part-to-part matching, and superior common-mode rejection compared to opto-coupled gate drivers. While the input circuit mimics the characteristics of an LED, less drive current is required, resulting in higher efficiency. Propagation delay time is independent of input drive current, resulting in consistently short propagation times, tighter unit-to-unit variation, and greater input circuit design flexibility. As a result, the Si826x series offers longer service life and dramatically higher reliability compared to opto-coupled gate drivers.



Patent pending

Si826x

Functional Block Diagram



Diode Emulator Model and I-V Curve

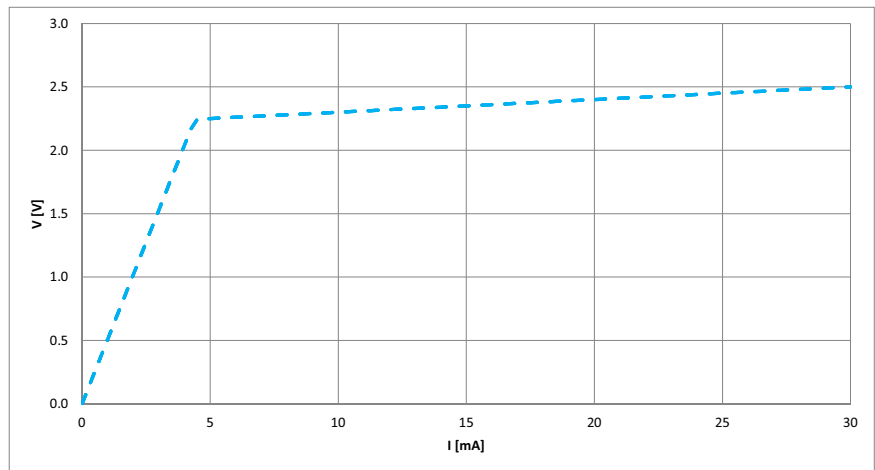
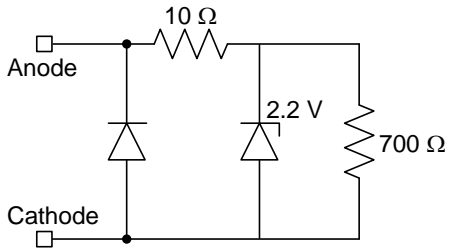


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Si826x

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	5	—	30	V
Input Current	$I_{F(ON)}$	6	—	30	mA
Operating Temperature (Ambient)	T_A	-40	—	125	°C

Table 2. Electrical Characteristics ¹

$V_{DD} = 15\text{ V or }30\text{ V}$, $GND = 0\text{ V}$, $I_F = 6\text{ mA}$, $T_A = -40\text{ to }+125\text{ °C}$; typical specs at 25 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DC Parameters						
Supply Voltage ²	V_{DD}	$(V_{DD} - GND)$	5	—	30	V
Supply Current (Output High)	I_{DD}	$I_F = 10\text{ mA}$	—	1.8	2.4	mA
		$V_{DD} = 15\text{ V}$ $V_{DD} = 30\text{ V}$	—	2.0	2.7	mA
Supply Current (Output Low)	I_{DD}	$V_F = -0.3\text{ to }+1.5\text{ V}$	—	1.5	2.1	mA
		$V_{DD} = 15\text{ V}$ $V_{DD} = 30\text{ V}$	—	1.7	2.4	mA
Input Current Threshold	$I_{F(TH)}$		6	—	—	mA
Input Current Hysteresis	I_{HYS}		—	0.34	—	mA
Input Forward Voltage (OFF)	$V_{F(OFF)}$	Measured at ANODE with respect to CATHODE.	—	—	1	V
Input Forward Voltage (ON)	$V_{F(ON)}$	Measured at ANODE with respect to CATHODE.	1.6	—	2.8	V
Input Capacitance	C_I	$f = 100\text{ kHz}$, $V_F = 0\text{ V}$, $V_F = 2\text{ V}$	—	15	—	pF
Output Resistance High (Source) ³	R_{OH}	Si826xAxx devices	—	15	—	Ω
		Si826xBxx devices ($I_{OH} = -1\text{ A}$)	—	2.6	5.1	
Output Resistance Low (Sink) ³	R_{OL}	Si826xAxx devices	—	5.0	—	
		Si826xBxx devices ($I_{OL} = 2\text{ A}$)	—	0.8	2.0	

Notes:

1. See "8.Ordering Guide" on page 25 for more information.
2. Minimum value of $(V_{DD} - GND)$ decoupling capacitor is 1 μF .
3. Both V_O pins are required to be shorted together for 4.0 A compliance.
4. When performing this test, it is recommended that the DUT be soldered to avoid trace inductances, which may cause over-stress conditions.

Table 2. Electrical Characteristics (Continued)¹
 $V_{DD} = 15\text{ V or }30\text{ V}$, $GND = 0\text{ V}$, $I_F = 6\text{ mA}$, $T_A = -40\text{ to }+125\text{ }^\circ\text{C}$; typical specs at $25\text{ }^\circ\text{C}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output High Current (Source) ^{3,4}	I_{OH}	Si826xAxx devices ($I_F = 0$), ($t_{PW_IOH} \leq 250\text{ ns}$) (see Figure 2)	—	0.4	—	A
		Si826xBxx devices ($I_F = 0$), ($t_{PW_IOH} \leq 250\text{ ns}$), ($V_{DD} - V_O = 4\text{ V}$) (see Figure 2)	0.5	1.8	—	
Output Low Current (Sink) ^{3,4}	I_{OL}	Si826xAxx devices ($I_F = 10\text{ mA}$), ($t_{PW_IOL} \leq 250\text{ ns}$) (see Figure 1)	—	0.6	—	A
		Si826xBxx devices ($I_F = 10\text{ mA}$), ($t_{PW_IOL} \leq 250\text{ ns}$), ($V_O - GND = 2.5\text{ V}$) (see Figure 1)	1.2	4.0	—	
High-Level Output Voltage	V_{OH}	Si826xAxx devices ($I_{OUT} = -100\text{ mA}$)	—	$V_{DD} - 0.4$	—	V
		Si826xBxx devices ($I_{OUT} = -100\text{ mA}$)	$V_{DD} - 0.5$	$V_{DD} - 0.25$	—	
		Si826xBxx devices ($I_{OUT} = 0\text{ mA}$), ($I_F = 0\text{ mA}$)	—	V_{DD}	—	
Low-Level Output Voltage	V_{OL}	Si826xAxx devices ($I_{OUT} = 100\text{ mA}$), ($I_F = 10\text{ mA}$)	—	320	—	mV
		Si826xBxx devices ($I_{OUT} = 100\text{ mA}$), ($I_F = 10\text{ mA}$)	—	80	200	
UVLO Threshold + (Si826xxAx mode)	$V_{DD_{UV+}}$	See Figure 10 on page 17. V_{DD} rising	5	5.6	6.3	V
UVLO Threshold – (Si826xxAx mode)	$V_{DD_{UV-}}$	See Figure 10 on page 17. V_{DD} falling	4.7	5.3	6.0	V
UVLO lockout hysteresis (Si826xxAx mode)	$V_{DD_{HYS}}$		—	300	—	mV
Notes:						
1. See "8.Ordering Guide" on page 25 for more information.						
2. Minimum value of ($V_{DD} - GND$) decoupling capacitor is $1\text{ }\mu\text{F}$.						
3. Both V_O pins are required to be shorted together for 4.0 A compliance.						
4. When performing this test, it is recommended that the DUT be soldered to avoid trace inductances, which may cause over-stress conditions.						

Table 2. Electrical Characteristics (Continued)¹

$V_{DD} = 15\text{ V or }30\text{ V}$, $GND = 0\text{ V}$, $I_F = 6\text{ mA}$, $T_A = -40\text{ to }+125\text{ }^\circ\text{C}$; typical specs at $25\text{ }^\circ\text{C}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
UVLO Threshold + (Si826xxBx mode)	$V_{DD_{UV+}}$	See Figure 11 on page 17. V_{DD} rising	7.5	8.4	9.4	V
UVLO Threshold – (Si826xxBx mode)	$V_{DD_{UV-}}$	See Figure 11 on page 17. V_{DD} falling	6.9	7.9	8.9	V
UVLO lockout hysteresis (Si826xxBx mode)	$V_{DD_{HYS}}$		—	500	—	mV
UVLO Threshold + (Si826xxCx mode)	$V_{DD_{UV+}}$	See Figure 12 on page 17. V_{DD} rising	10.5	12	13.5	V
UVLO Threshold – (Si826xxCx mode)	$V_{DD_{UV-}}$	See Figure 12 on page 17. V_{DD} falling	9.4	10.7	12.2	V
UVLO lockout hysteresis (Si826xxCx mode)	$V_{DD_{HYS}}$		—	1.3	—	V
AC Switching Parameters						
Propagation delay (Low-to-High)	t_{PLH}	$C_L = 200\text{ pF}$	20	40	60	ns
Propagation delay (High-to-Low)	t_{PHL}	$C_L = 200\text{ pF}$	10	30	50	ns
Pulse Width Distortion	PWD	$ t_{PLH} - t_{PHL} $	—	10	—	ns
Propagation Delay Difference	PDD	$ t_{PHL_{MAX}} - t_{PLH_{MIN}} $	—	—	20	ns
Rise time	t_R	$C_L = 200\text{ pF}$	—	5.5	15	ns
Fall time	t_F	$C_L = 200\text{ pF}$	—	8.5	20	ns
Device Startup Time	t_{START}		—	16	30	μs
Common Mode Transient Immunity	CMTI	Output = low or high ($V_{CM} = 1500\text{ V}$), ($I_F \geq 6\text{ mA}$) (See Figure 3)	35	50	—	kV/ μs
Notes:						
<ol style="list-style-type: none"> 1. See "8.Ordering Guide" on page 25 for more information. 2. Minimum value of ($V_{DD} - GND$) decoupling capacitor is $1\text{ }\mu\text{F}$. 3. Both V_O pins are required to be shorted together for 4.0 A compliance. 4. When performing this test, it is recommended that the DUT be soldered to avoid trace inductances, which may cause over-stress conditions. 						

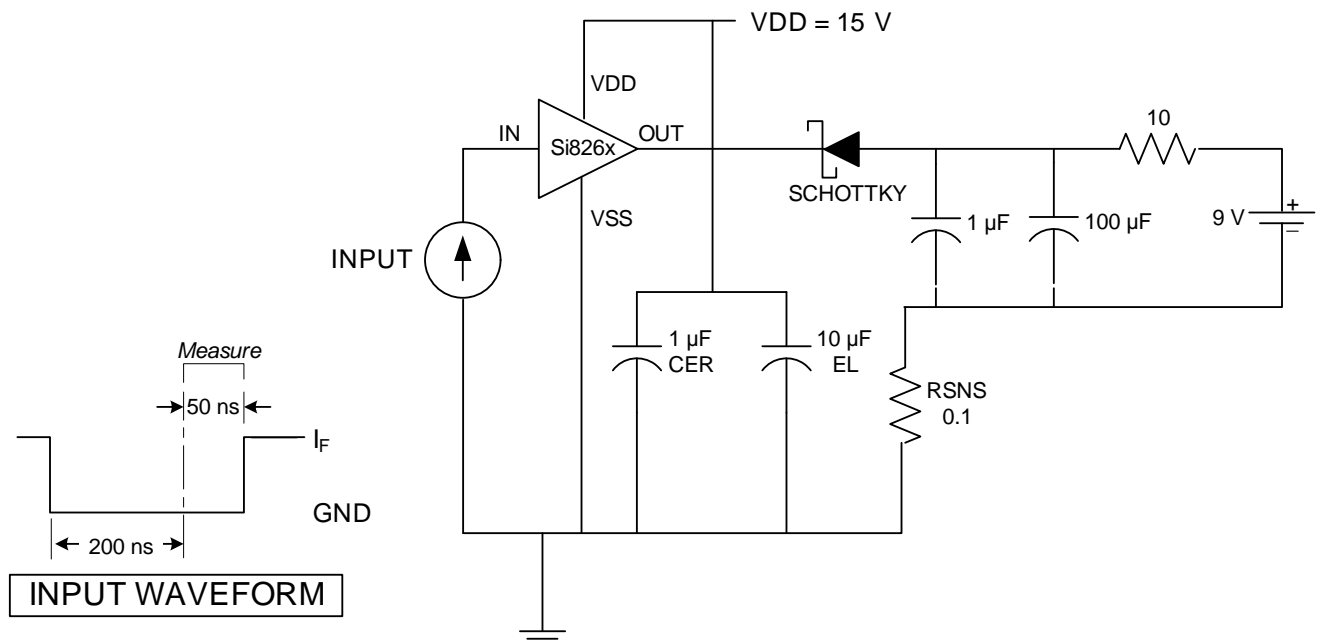


Figure 1. IOL Sink Current Test Circuit

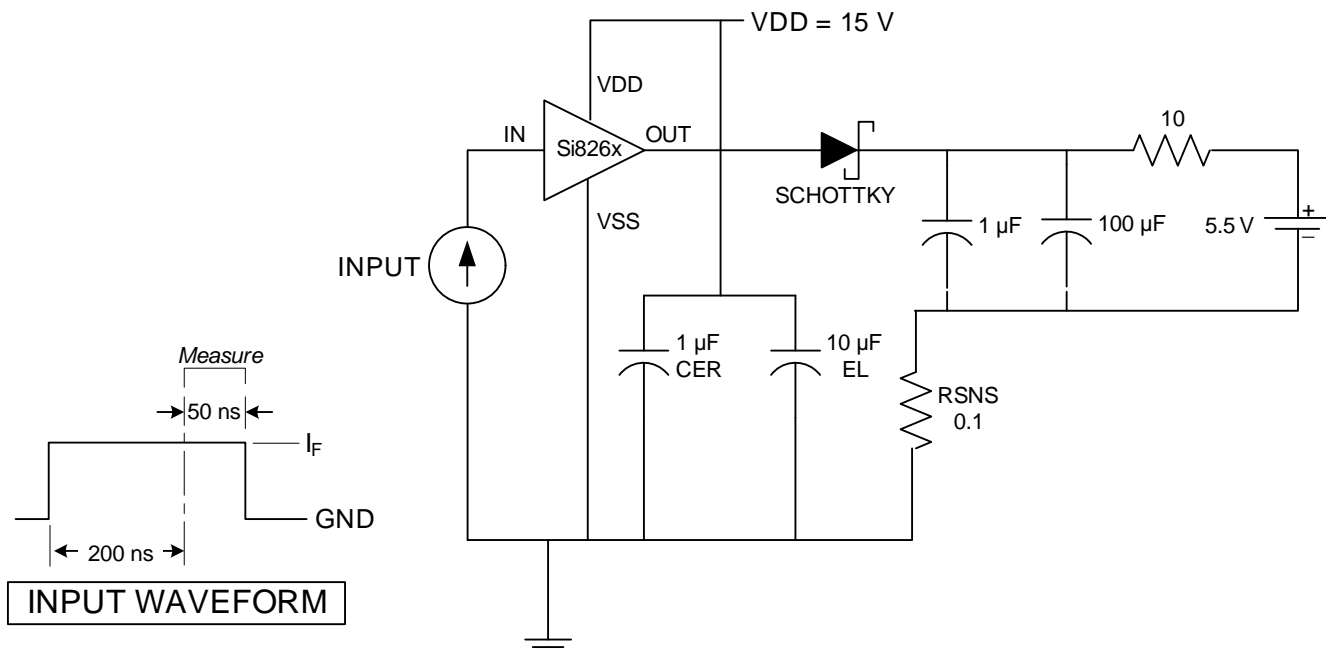


Figure 2. IOH Source Current Test Circuit

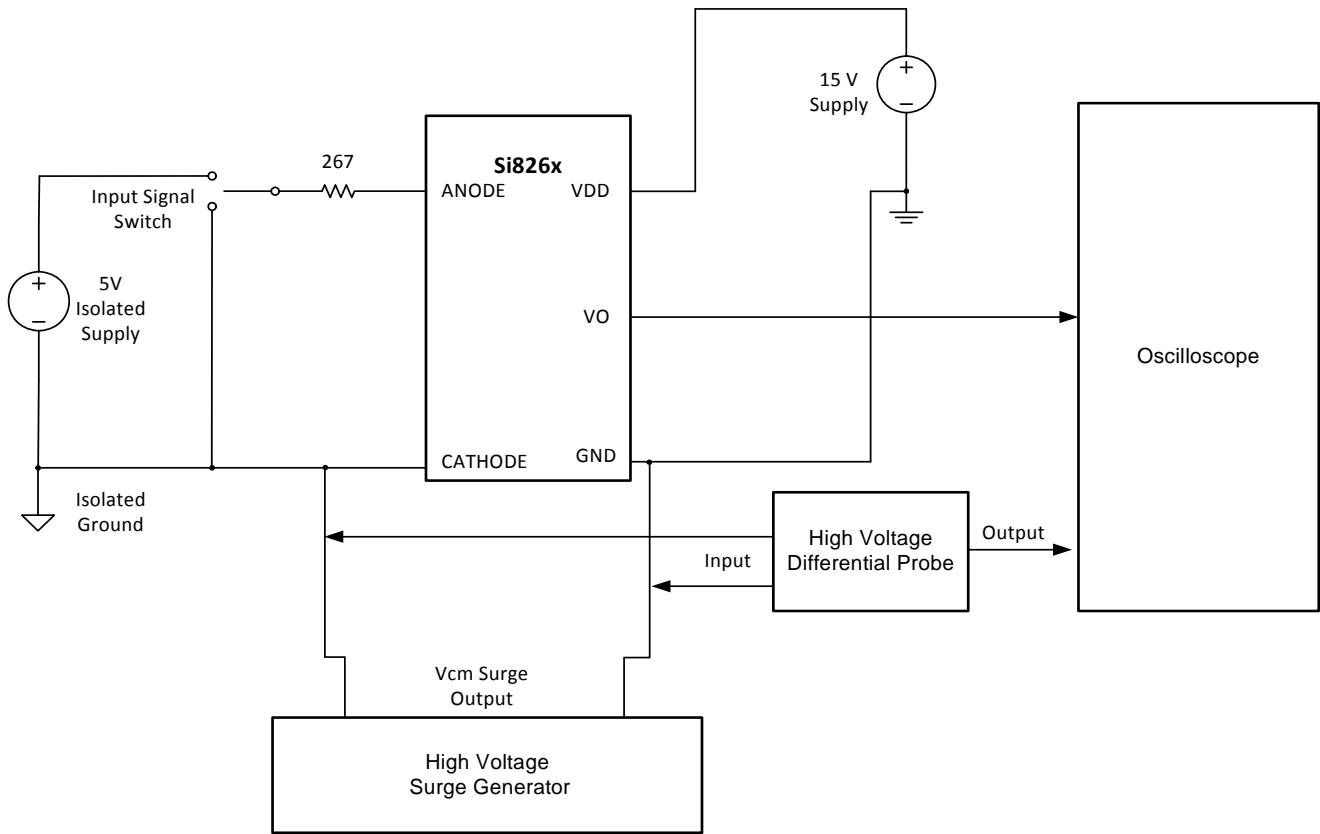


Figure 3. Common Mode Transient Immunity Characterization Circuit

2. Regulatory Information

Table 3. Regulatory Information (Pending)*

CSA
The Si826x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V _{RMS} reinforced insulation working voltage; up to 600 V _{RMS} basic insulation working voltage.
60950-1: Up to 1000 V _{RMS} reinforced insulation working voltage; up to 1000 V _{RMS} basic insulation working voltage.
60601-1: Up to 250 V _{RMS} reinforced insulation working voltage; up to 500 V _{RMS} basic insulation working voltage.
VDE
The Si826x is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 1414 V _{peak} for reinforced insulation working voltage.
UL
The Si826x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V _{RMS} isolation voltage for basic protection.
CQC
The Si826x is certified under GB4943.1-2011. For more details, see File number pending.
Rated up to 1000 V _{RMS} reinforced insulation working voltage; up to 1000 V _{RMS} basic insulation working voltage.
*Note: Regulatory Certifications apply to 3.75 kV _{RMS} rated devices which are production tested to 4.5 kV _{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV _{RMS} rated devices which are production tested to 6.0 kV _{RMS} for 1 sec. For more information, see "8.Ordering Guide" on page 25.

Table 4. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value				Unit
			SOIC-8	DIP8	SDIP6	LGA8	
Nominal Air Gap (Clearance)	L(IO1)		4.7 min	7.2 min	9.6 min	10.0 min	mm
Nominal External Tracking (Creepage)	L(IO2)		3.9 min	7.0 min	8.3 min	10.0 min	mm
Minimum Internal Gap (Internal Clearance)			0.016	0.016	0.016	0.016	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	600	600	V
Erosion Depth	ED		0.031	0.031	0.057	0.021	mm
Resistance (Input-Output)*	R _{IO}		10 ¹²	10 ¹²	10 ¹²	10 ¹²	Ω
Capacitance (Input-Output)*	C _{IO}	f = 1 MHz	1	1	1	1	pF
*Note: To determine resistance and capacitance, the Si826x is converted into a 2-terminal device. Pins 1–4 (1–3, SDIP6) are shorted together to form the first terminal, and pins 5–8 (4–6, SDIP6) are shorted together to form the second terminal. The parameters are then measured between these two terminals.							

Table 5. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Conditions	Specification			
		SOIC-8	DIP8	SDIP6	LGA8
Basic Isolation Group	Material Group	I	I	I	I
Installation Classification	Rated Mains Voltages \leq 150 V _{RMS}	I-IV	I-IV	I-IV	I-IV
	Rated Mains Voltages \leq 300 V _{RMS}	I-IV	I-IV	I-IV	I-IV
	Rated Mains Voltages \leq 450 V _{RMS}	I-III	I-III	I-IV	I-IV
	Rated Mains Voltages \leq 600 V _{RMS}	I-III	I-III	I-IV	I-IV
	Rated Mains Voltages \leq 1000 V _{RMS}	—	—	—	I-III

Table 6. IEC 60747-5-2 Insulation Characteristics*

Parameter	Symbol	Test Condition	Characteristic				Unit
			SOIC-8	DIP8	SDIP6	LGA8	
Maximum Working Insulation Voltage	V _{IORM}		630	891	1140	1414	V peak
Input to Output Test Voltage	V _{PR}	Method b1 (V _{IORM} × 1.875 = V _{PR} , 100% Production Test, t _m = 1 sec, Partial Discharge < 5 pC)	1181	1671	2138	2652	V peak
Transient Overvoltage	V _{IOTM}	t = 60 sec	6000	6000	8000	8000	V peak
Surge Voltage	V _{IOSM}	1.2 μs rise, 50 μs fall 50%	10	10	10	10	kV peak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	2	2	
Insulation Resistance at T _S , V _{IO} = 500 V	R _S		>10 ⁹	>10 ⁹	>10 ⁹	>10 ⁹	Ω

***Note:** This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si826x provides a climate classification of 40/125/21.

Table 7. IEC Safety Limiting Values*

Parameter	Symbol	Test Condition	Max				Unit
			SOIC-8	DIP8	SDIP6	LGA8	
Case Temperature	T_S		140	140	140	140	°C
Input Current	I_S	$\theta_{JA} = 110 \text{ }^\circ\text{C/W}$ (SOIC-8), 110 °C/W (DIP8), 105 °C/W (SDIP6), 220 °C (LGA8), $V_F = 2.8 \text{ V}$, $T_J = 140 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$	370	370	390	185	mA
Output Power	P_S		1	1	1	0.5	W

***Note:** Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 4, 5, 6, and 7.

Table 8. Thermal Characteristics

Parameter	Symbol	Typ				Unit
		SOIC-8	DIP8	SDIP6	LGA8	
IC Junction-to-Air Thermal Resistance	θ_{JA}	110	110	105	220	$^{\circ}\text{C}/\text{W}$

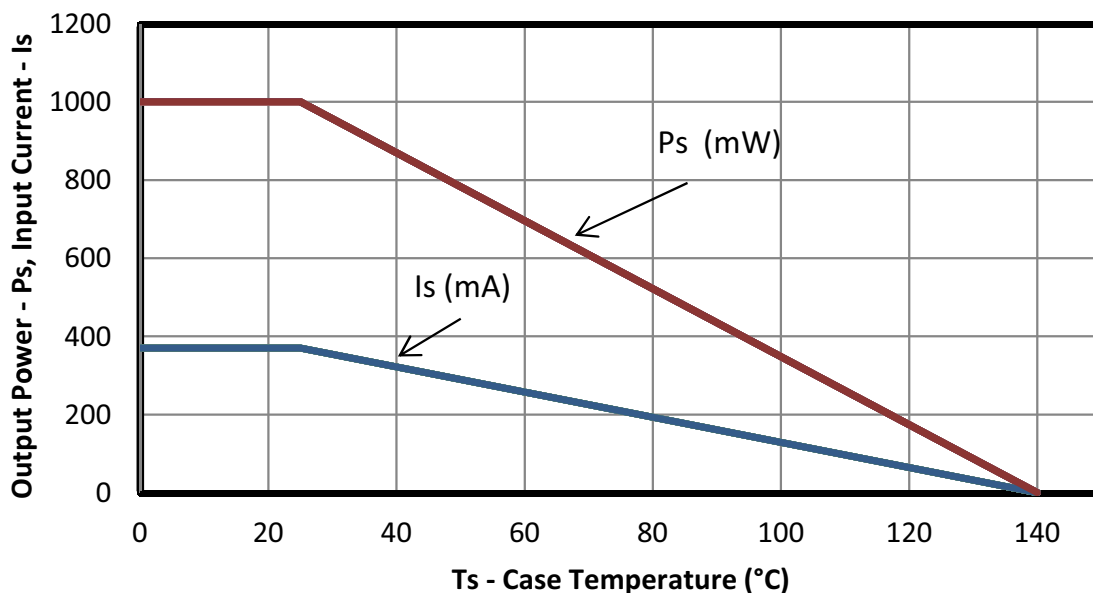


Figure 4. (SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

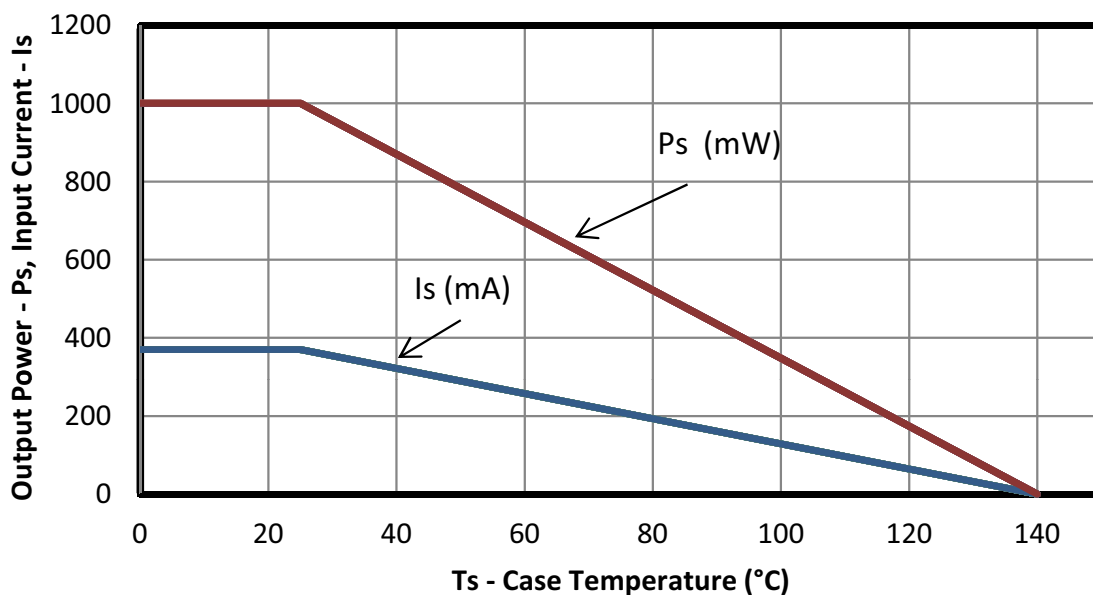


Figure 5. (DIP8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

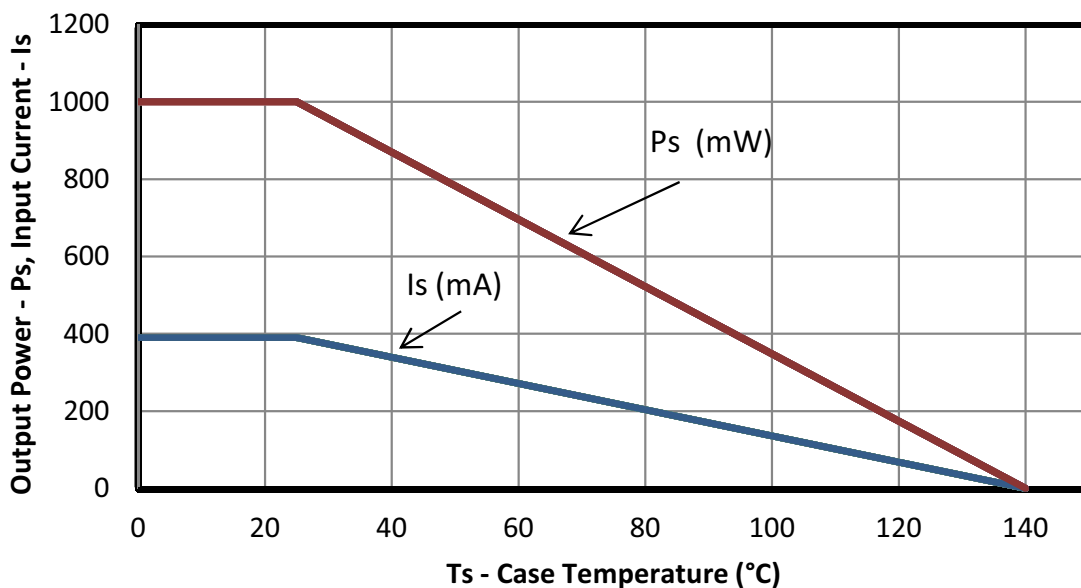


Figure 6. (SDIP6) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

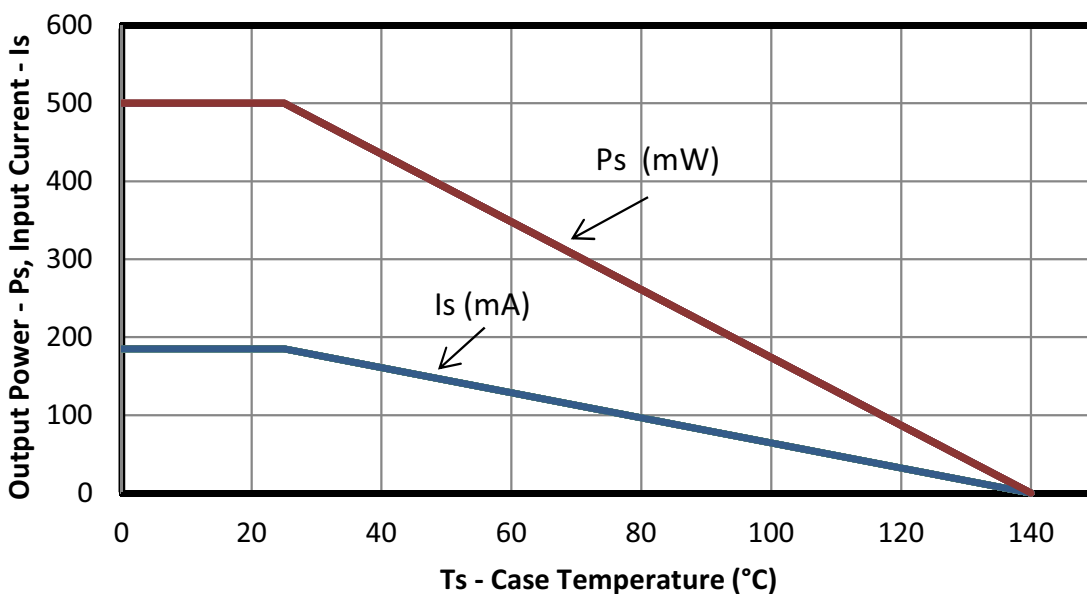


Figure 7. (LGA8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

Si826x

Table 9. Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_{STG}	-65	+150	°C
Operating Temperature	T_A	-40	+125	°C
Junction Temperature	T_J	—	+140	°C
Average Forward Input Current	$I_{F(AVG)}$	—	30	mA
Peak Transient Input Current ($< 1 \mu s$ pulse width, 300 ps)	I_{FTR}	—	1	A
Peak Output Current ($t_{PW} = 10 \mu s$) (Si826xA)	I_{OPK}	—	0.6	A
Peak Output Current ($t_{PW} = 10 \mu s$) (Si826xB)	I_{OPK}	—	4.0	A
Reverse Input Voltage	V_R	—	0.3	V
Supply Voltage	VDD	-0.5	36	V
Output Voltage	V_{OUT}	-0.5	36	V
Output Current	$I_{O(AVG)}$	—	10	mA
Input Power Dissipation	P_I	—	75	mW
Output Power Dissipation	P_O	—	225	mW
Total Power Dissipation (all packages limited by thermal derating curve)	P_T	—	300	mW
Lead Solder Temperature (10 s)		—	260	°C
HBM Rating ESD		4	—	kV
Machine Model ESD		300	—	V
CDM		2000	—	V
Maximum Isolation Voltage (1 s) SOIC-8		—	4500	V_{RMS}
Maximum Isolation Voltage (1 s) DIP8		—	6500	V_{RMS}
Maximum Isolation Voltage (1 s) SDIP6		—	6500	V_{RMS}
Maximum Isolation Voltage (1 s) LGA8		—	6500	V_{RMS}

***Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.

3. Functional Description

3.1. Theory of Operation

The Si826x is a functional upgrade for popular opto-isolated drivers, such as the Avago HPCL-3120, HPCL-0302, Toshiba TLP350, and others. The operation of an Si826x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for the Si826x is shown in Figure 8.

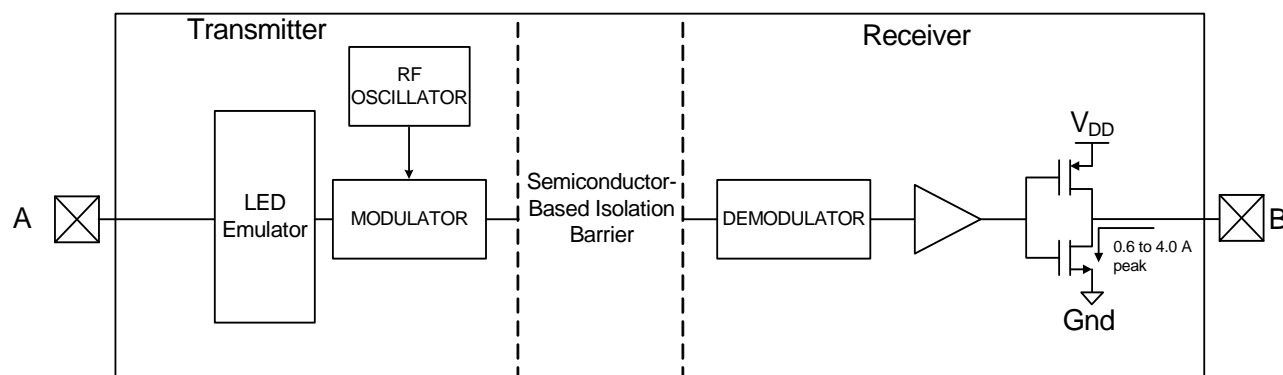


Figure 8. Simplified Channel Diagram

4. Technical Description

4.1. Device Behavior

Truth tables for the Si826x are summarized in Table 10.

Table 10. Si826x Truth Table Summary*

Input	V_{DD}	V_O
OFF	$> UVLO$	LOW
OFF	$< UVLO$	LOW
ON	$> UVLO$	HIGH
ON	$< UVLO$	LOW

*Note: This truth table assumes V_{DD} is powered. If V_{DD} is below $UVLO$, see "4.3.Under Voltage Lockout (UVLO)" on page 17 for more information.

4.2. Device Startup

Output V_O is held low during power-up until V_{DD} rises above the $UVLO+$ threshold for a minimum time period of t_{START} . Following this, the output is high when the current flowing from anode to cathode is $> I_{F(ON)}$. Device startup, normal operation, and shutdown behavior is shown in Figure 9.

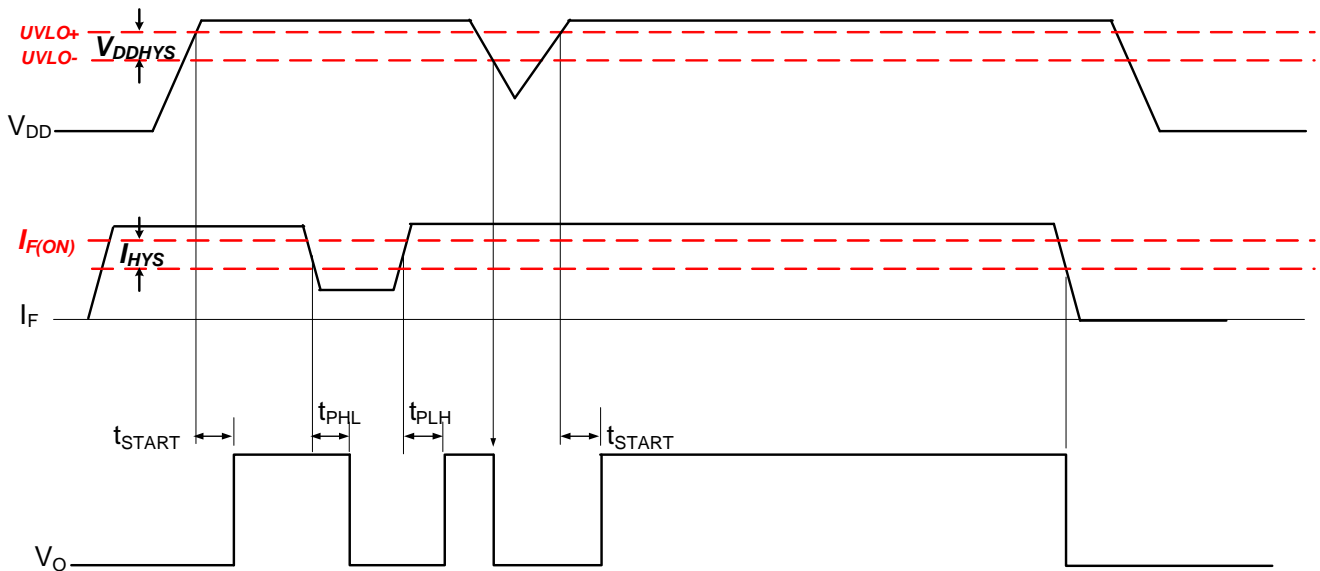


Figure 9. Si826x Operating Behavior ($I_F \geq I_{F(MIN)}$ when $V_F \geq V_{F(MIN)}$)

4.3. Under Voltage Lockout (UVLO)

The UVLO circuit unconditionally drives V_O low when V_{DD} is below the lockout threshold. Referring to Figures 10 through 12, upon power up, the Si826x is maintained in UVLO until V_{DD} rises above $V_{DD_{UV+}}$. During power down, the Si826x enters UVLO when V_{DD} falls below the UVLO threshold plus hysteresis (i.e., $V_{DD} \leq V_{DD_{UV+}} - V_{DD_{HYS}}$).

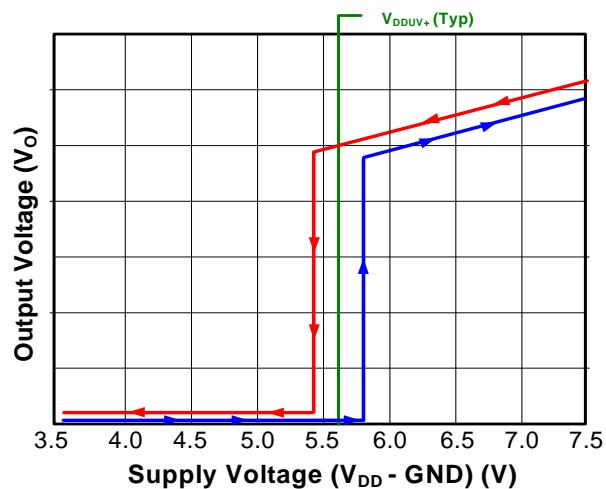


Figure 10. Si826xxAx UVLO Response (5 V)

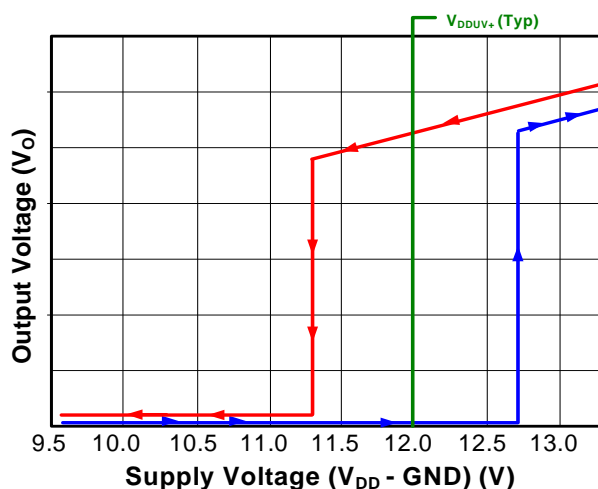


Figure 12. Si826xxCx UVLO Response (12 V)

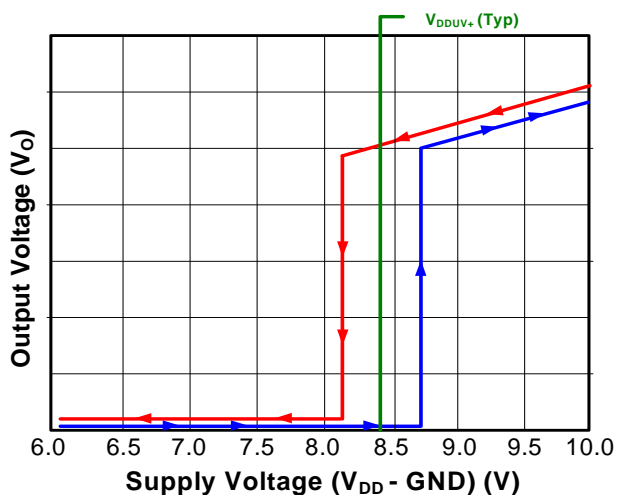


Figure 11. Si826xxBX UVLO Response (8 V)

5. Applications

The following sections detail the input and output circuits necessary for proper operation. Power dissipation and layout considerations are also discussed.

5.1. Input Circuit Design

Opto driver manufacturers typically recommend the circuits shown in Figures 13 and 14. These circuits are specifically designed to improve opto-coupler input common-mode rejection and increase noise immunity.

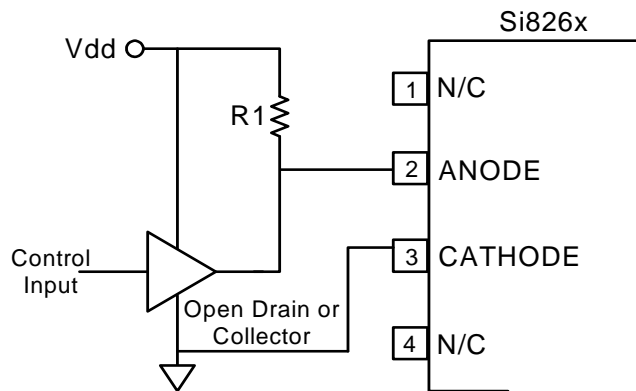


Figure 13. Si826x Input Circuit

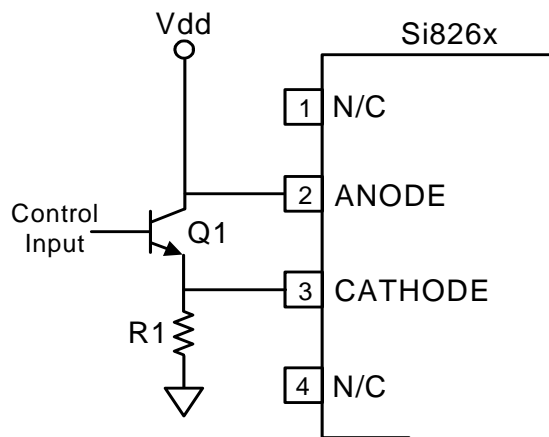


Figure 14. High CMR Si826x Input Circuit

The optically-coupled driver circuit of Figure 13 turns the LED on when the control input is high. However, internal capacitive coupling from the LED to the power and ground conductors can momentarily force the LED into its off state when the anode and cathode inputs are subjected to a high common-mode transient. The circuit shown in Figure 14 addresses this issue by using a value of R1 sufficiently low to overdrive the LED, ensuring it remains on during an input common-mode transient. Q1 shorts the LED off in the low output state, again increasing common-mode transient immunity.

Some opto driver applications recommend reverse-biasing the LED when the control input is off to prevent coupled noise from energizing the LED. The Si826x input circuit requires less current and has twice the off-state noise margin compared to opto couplers. However, high CMR opto coupler designs that overdrive the LED (see Figure 14) may require increasing the value of R1 to limit input current I_F to its maximum rating when using the Si826x. In addition, there is no benefit in driving the Si826x input diode into reverse bias when in the off state. Consequently, opto coupler circuits using this technique should either leave the negative bias circuitry unpopulated

or modify the circuitry (e.g., add a clamp diode or current limiting resistor) to ensure that the anode pin of the Si826x is no more than -0.3 V with respect to the cathode when reverse-biased.

New designs should consider the input circuit configurations of Figure 15, which are more efficient than those of Figures 13 and 14. As shown, S1 and S2 represent any suitable switch, such as a BJT or MOSFET, analog transmission gate, processor I/O, etc. Also, note that the Si826x input can be driven from the I/O port of any MCU or FPGA capable of sourcing a minimum of 6 mA (see Figure 15B). Additionally, note that the Si826x propagation delay and output drive do not significantly change for values of I_F between $I_{F(\text{MIN})}$ and $I_{F(\text{MAX})}$.

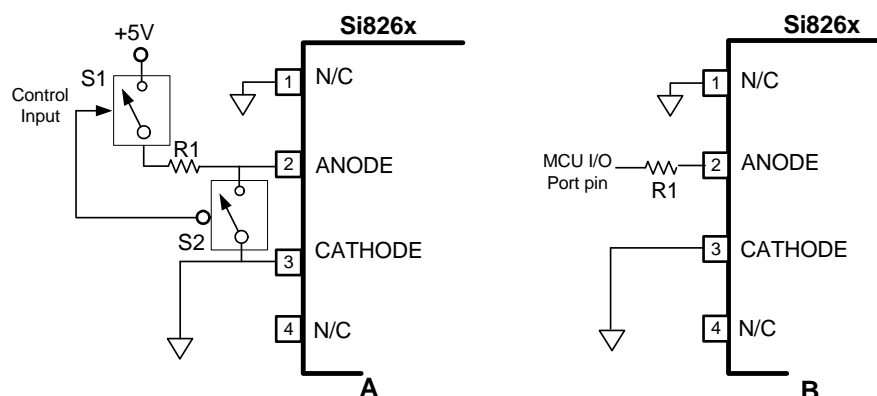


Figure 15. Si826x Other Input Circuit Configurations

5.2. Output Circuit Design

GND can be biased at, above, or below ground as long as the voltage on V_{DD} with respect to GND is a maximum of 30 V . V_{DD} decoupling capacitors should be placed as close to the package pins as possible. The optimum values for these capacitors depend on load current and the distance between the chip and its power source. It is recommended that 0.1 and $10\text{ }\mu\text{F}$ bypass capacitors be used to reduce high-frequency noise and maximize performance.

5.3. Layout Considerations

It is most important to minimize ringing in the drive path and noise on the V_{DD} lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si826x as close as possible to the device it is driving. In addition, the V_{DD} supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and V_{DD} planes for power devices and small signal components provides the best overall noise performance.

5.4. Power Dissipation Considerations

Proper system design must assure that the Si826x operates within safe thermal limits across the entire load range. The Si826x total power dissipation is the sum of the power dissipated by bias supply current, internal switching losses, and power delivered to the load, as shown in Equation 1.

$$P_D = I_F \times V_F \times DC + V_{DD} \times [I_{DDQ} + (Q_d + C_L \times V_{DD}) \times f]$$

where: P_D is the total device power dissipation (W)

I_F is the diode current (30 mA max)

V_F is the diode anode to cathode voltage (2.8 V max)

DC is duty cycle (0.5 typical)

V_{DD} is the driver-side supply voltage (30 V max)

I_{DDQ} is the driver maximum bias current (2.5 mA)

Q_d is 3 nC

C_L is the load capacitance

f is the switching frequency (Hz)

Equation 1.

The maximum allowable power dissipation for the Si826x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2.

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\theta_{ja}}$$

where:

P_{Dmax} is the maximum allowable power dissipation (W)

T_{jmax} is the maximum junction temperature (140 °C)

T_A is the ambient temperature (°C)

θ_{ja} is the package junction-to-air thermal resistance (110 °C/W)

Equation 2.

Substituting values for P_{Dmax} , T_{jmax} , T_A , and θ_{ja} into Equation 2 results in a maximum allowable total power dissipation of 1.0 W. Note that the maximum allowable load is found by substituting this limit and the appropriate datasheet values from Table 2 on page 4 into Equation 1 and simplifying. Graphs are shown in Figures 16 and 17. All points along the load lines in these graphs represent the package dissipation-limited value of C_L for the corresponding switching frequency.

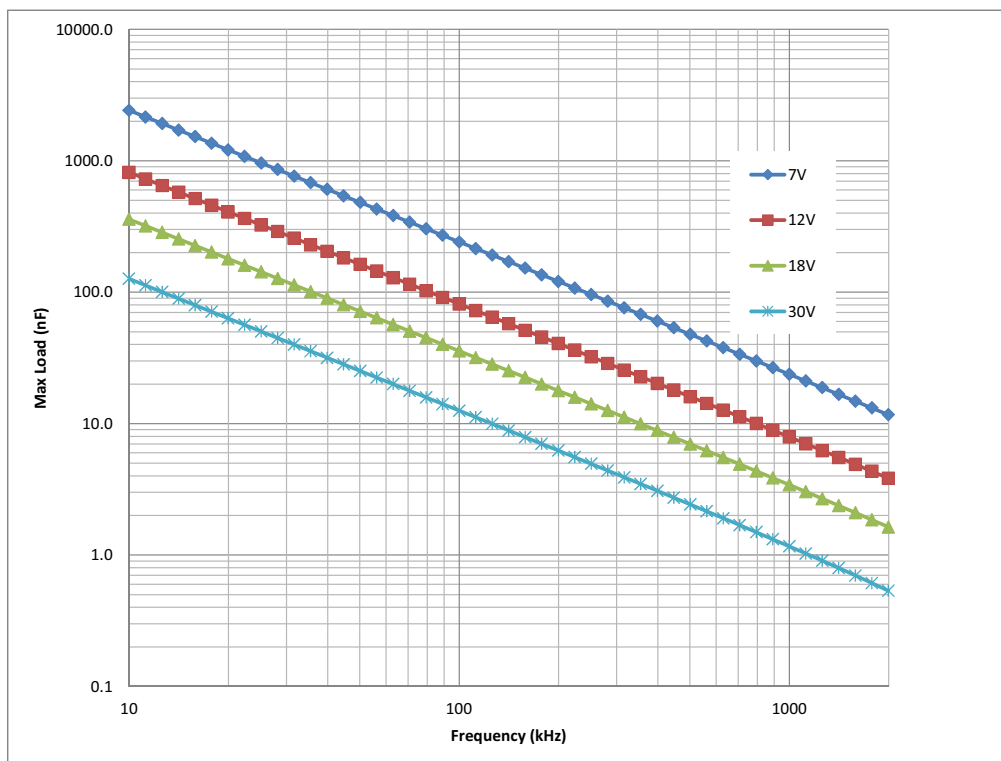


Figure 16. (SOIC-8, DIP8, SDIP6) Maximum Load vs. Switching Frequency (25 °C)

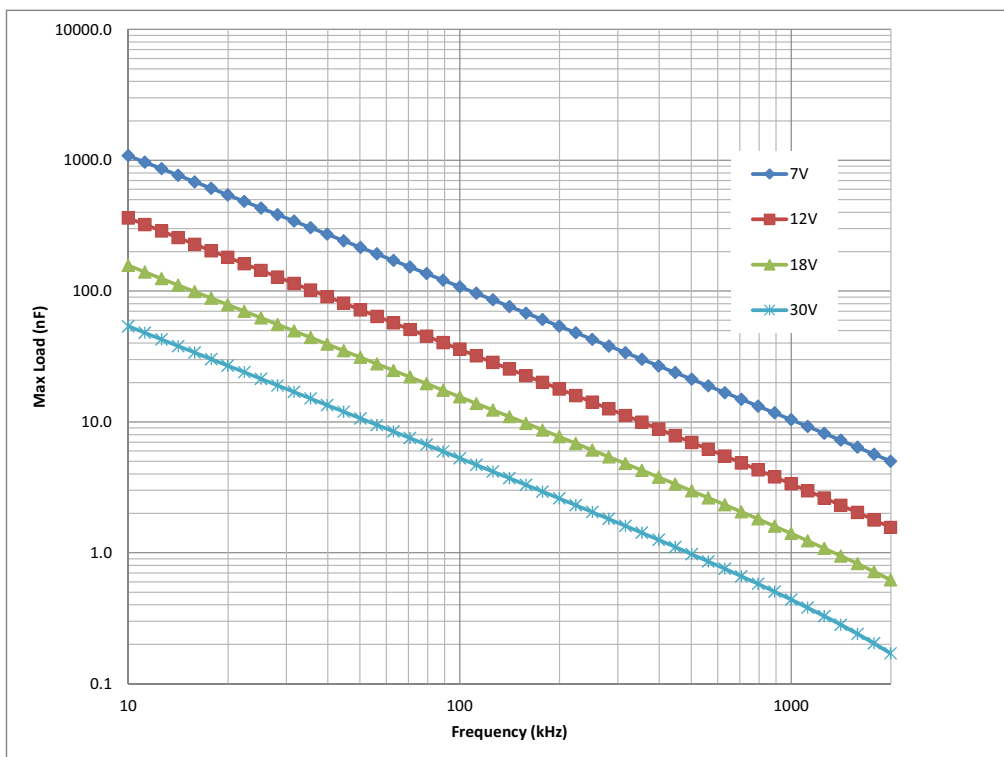


Figure 17. (LGA8) Maximum Load vs. Switching Frequency (25 °C)

5.5. Parametric Differences between Si826x and HCPL-0302 and HCPL-3120 Opto Drivers

The Si826x is designed to directly replace HCPL-3120 and similar opto drivers. Parametric differences are summarized in Tables 11 and 12 below.

Table 11. Parametric Differences of Si8261 vs. HCPL-3120

Parameter	Si8261	HCPL-3120	Units
Max supply voltage	30	30	V
ON state forward input current	6 to 30	7 to 16	mA
OFF state input voltage	-0.6 to +1.6	-0.3 to +0.8	V
Max reverse input voltage	-0.3	-5	V
UVLO threshold (rising)	5 to 10.5	11.0 to 13.5	V
UVLO threshold (falling)	4.7 to 9.4	9.7 to 12.0	V
UVLO hysteresis	0.3 to 1.3	1.6	V
Rise/fall time into 10 Ω in series with 10 nF	100	100	ns

Table 12. Parametric Differences of Si8261 vs. HCPL-0302

Parameter	Si8261	HCPL-0302	Units
Max supply voltage	30	30	V
ON state forward input current	6 to 30	7 to 16	mA
OFF state input voltage	-0.6 to +1.6	-0.3 to +0.8	V
Max reverse input voltage	-0.3	-5	V
UVLO threshold (rising)	5 to 10.5	11.0 to 13.5	V
UVLO threshold (falling)	4.7 to 9.4	9.7 to 12.0	V
UVLO hysteresis	0.3 to 1.3	1.6	V
Rise/fall time into 10 Ω in series with 10 nF	100	100	ns

5.5.1. Input Diode Differences

The Si826x input circuit requires less current and has twice the off-state noise margin compared to opto drivers. However, high CMR opto driver designs that overdrive the LED (see Figure 14) may require increasing the value of R1 to limit input current I_F to its maximum rating when using the Si826x. In addition, there is no benefit in driving the Si826x input diode into reverse bias when in the off state. Consequently, opto driver circuits using this technique should either leave the negative bias circuitry unpopulated or modify the circuitry (e.g. add a clamp diode or current limiting resistor) to ensure that the anode pin of the Si826x is no more than -0.3 V with respect to the cathode when reverse-biased. For more information on configuring the input, see "AN677: Using the Si826x Family of Isolated Gate Drivers".

5.5.2. Supply Voltage and UVLO Considerations

The supply voltage of the Si826x is limited to 30 V, from which the UVLO voltage thresholds are scaled accordingly. Opto replacement applications should limit their supply voltages to 30 V or less.

6. Pin Descriptions (SOIC-8, DIP8, LGA8)

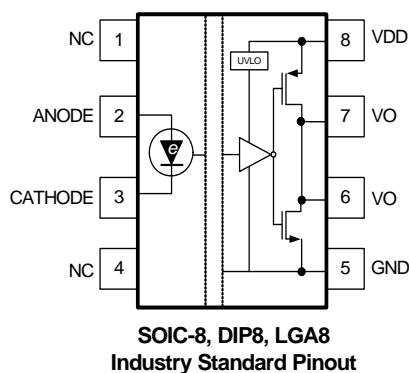


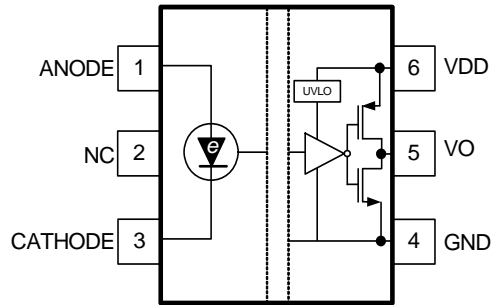
Figure 18. Pin Configuration

Table 13. Pin Descriptions (SOIC-8, DIP8, LGA8)

Pin	Name	Description
1	NC*	No connect.
2	ANODE	Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input.
3	CATHODE	Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input.
4	NC*	No connect.
5	GND	External MOSFET source connection and ground reference for V_{DD} . This terminal is typically connected to ground but may be tied to a negative or positive voltage.
6	V_O	Output signal. Both V_O pins are required to be shorted together for 4.0 A compliance.
7	V_O	Output signal. Both V_O pins are required to be shorted together for 4.0 A compliance.
8	V_{DD}	Output-side power supply input referenced to GND (30 V max).

***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

7. Pin Descriptions (SDIP6)



SDIP6
Industry Standard Pinout

Figure 19. Pin Configuration

Table 14. Pin Descriptions (SDIP6)

Pin	Name	Description
1	ANODE	Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input.
2	NC*	No connect.
3	CATHODE	Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input.
4	GND	External MOSFET source connection and ground reference for V_{DD} . This terminal is typically connected to ground but may be tied to a negative or positive voltage.
5	V_O	Output signal.
6	V_{DD}	Output-side power supply input referenced to GND (30 V max).

***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

8. Ordering Guide

Table 15. Si826x Ordering Guide^{1,2,3}

New Ordering Part Number (OPN)	Ordering Options					
	Output Configuration	Cross Reference	UVLO Voltage	Insulation Rating	Temp Range	Pkg Type
Si8261AAC-C-IS (Sampling)	0.6 A driver	HCPL-0314	5 V	3.75 kVrms	–40 to +125 °C	SOIC-8
Si8261BAC-C-IS (Sampling)	4.0 A driver	—	5 V	3.75 kVrms	–40 to +125 °C	SOIC-8
Si8261AAC-C-IP (Sampling)	0.6 A driver	HCPL-3140	5 V	3.75 kVrms	–40 to +125 °C	DIP8/GW
Si8261BAC-C-IP (Sampling)	4.0 A driver	TLP 350 HCPL-3120	5 V	3.75 kVrms	–40 to +125 °C	DIP8/GW
Si8261AAD-C-IS (Sampling)	0.6 A driver	ACPL-W314	5 V	5.0 kVrms	–40 to +125 °C	SDIP6
Si8261BAD-C-IS (Sampling)	4.0 A driver	TLP 700F	5 V	5.0 kVrms	–40 to +125 °C	SDIP6
Si8261AAD-C-IM (Sampling)	0.6 A driver	—	5 V	5.0 kVrms	–40 to +125 °C	LGA8
Si8261BAD-C-IM (Sampling)	4.0 A driver	HCNW-3120	5 V	5.0 kVrms	–40 to +125 °C	LGA8

Notes:

1. All packages are RoHS-compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 qualified.

Table 15. Si826x Ordering Guide^{1,2,3}

New Ordering Part Number (OPN)	Ordering Options					
	Output Configuration	Cross Reference	UVLO Voltage	Insulation Rating	Temp Range	Pkg Type
Si8261ABC-C-IS (Sampling)	0.6 A driver	HCPL-0314	8 V	3.75 kVrms	-40 to +125 °C	SOIC-8
Si8261BBC-C-IS (Sampling)	4.0 A driver	—	8 V	3.75 kVrms	-40 to +125 °C	SOIC-8
Si8261ABC-C-IP (Sampling)	0.6 A driver	HCPL-3140	8 V	3.75 kVrms	-40 to +125 °C	DIP8/GW
Si8261BBC-C-IP (Sampling)	4.0 A driver	TLP 350 HCPL-3120	8 V	3.75 kVrms	-40 to +125 °C	DIP8/GW
Si8261ABD-C-IS (Sampling)	0.6 A driver	ACPL-W314	8 V	5.0 kVrms	-40 to +125 °C	SDIP6
Si8261BBD-C-IS (Sampling)	4.0 A driver	TLP 700F	8 V	5.0 kVrms	-40 to +125 °C	SDIP6
Si8261ABD-C-IM (Sampling)	0.6 A driver	—	8 V	5.0 kVrms	-40 to +125 °C	LGA8
Si8261BBD-C-IM (Sampling)	4.0 A driver	HCNW-3120	8 V	5.0 kVrms	-40 to +125 °C	LGA8

Notes:

1. All packages are RoHS-compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.
2. "Si" and "SI" are used interchangeably.
3. AEC-Q100 qualified.

Table 15. Si826x Ordering Guide^{1,2,3}

New Ordering Part Number (OPN)	Ordering Options					
	Output Configuration	Cross Reference	UVLO Voltage	Insulation Rating	Temp Range	Pkg Type
Si8261ACC-C-IS (Sampling)	0.6 A driver	HCPL-0314	12 V	3.75 kVrms	–40 to +125 °C	SOIC-8
Si8261BCC-C-IS (Sampling)	4.0 A driver	—	12 V	3.75 kVrms	–40 to +125 °C	SOIC-8
Si8261ACC-C-IP (Sampling)	0.6 A driver	HCPL-3140	12 V	3.75 kVrms	–40 to +125 °C	DIP8/GW
Si8261BCC-C-IP (Sampling)	4.0 A driver	TLP 350 HCPL-3120	12 V	3.75 kVrms	–40 to +125 °C	DIP8/GW
Si8261ACD-C-IS (Sampling)	0.6 A driver	ACPL-W314	12 V	5.0 kVrms	–40 to +125 °C	SDIP6
Si8261BCD-C-IS (Sampling)	4.0 A driver	TLP 700F	12 V	5.0 kVrms	–40 to +125 °C	SDIP6
Si8261ACD-C-IM (Sampling)	0.6 A driver	—	12 V	5.0 kVrms	–40 to +125 °C	LGA8
Si8261BCD-C-IM (Sampling)	4.0 A driver	HCNW-3120	12 V	5.0 kVrms	–40 to +125 °C	LGA8

Notes:

1. All packages are RoHS-compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 qualified.

9. Package Outline: 8-Pin Narrow Body SOIC

Figure 20 illustrates the package details for the Si826x in an 8-pin narrow-body SOIC package. Table 16 lists the values for the dimensions shown in the illustration.

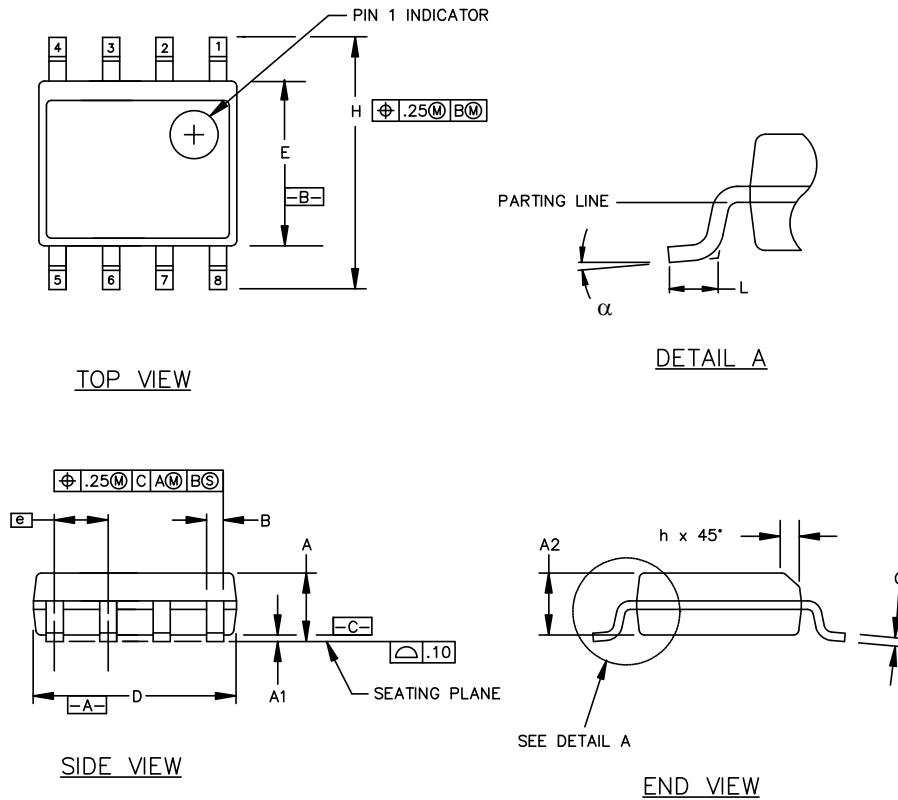


Figure 20. 8-Pin Narrow Body SOIC Package

Table 16. 8-Pin Narrow Body SOIC Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

10. Land Pattern: 8-Pin Narrow Body SOIC

Figure 21 illustrates the recommended land pattern details for the Si826x in an 8-pin narrow-body SOIC. Table 17 lists the values for the dimensions shown in the illustration.

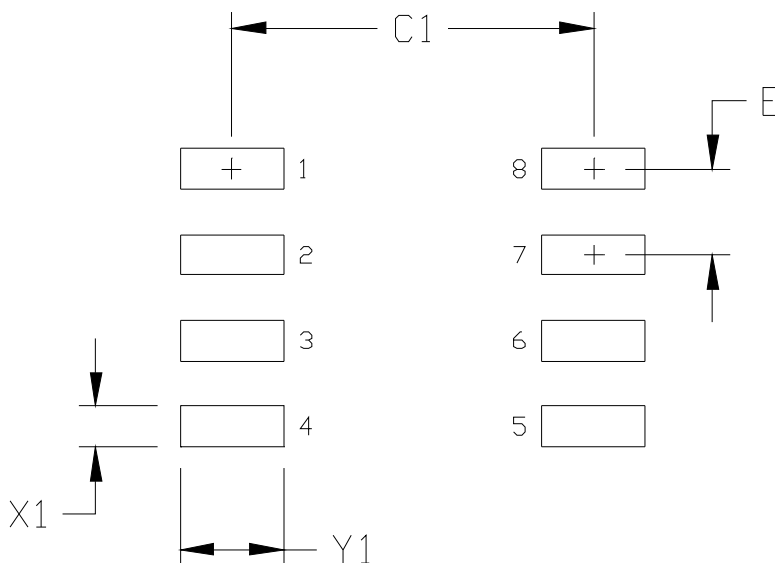


Figure 21. 8-Pin Narrow Body SOIC Land Pattern

Table 17. 8-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55
Notes:		
<ol style="list-style-type: none"> 1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion). 2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed. 		

11. Package Outline: DIP8

Figure 22 illustrates the package details for the Si826x in a DIP8 package. Table 18 lists the values for the dimensions shown in the illustration.

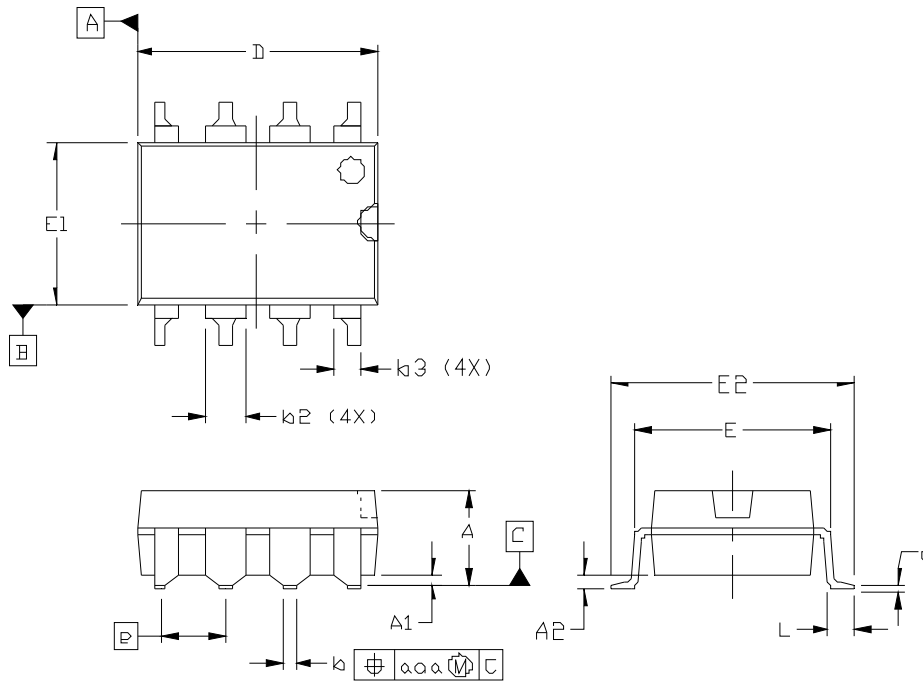


Figure 22. DIP8 Package

Table 18. DIP8 Package Diagram Dimensions

Dimension	Min	Max
A	—	4.19
A1	0.55	0.75
A2	3.17	3.43
b	0.35	0.55
b2	1.14	1.78
b3	0.76	1.14
c	0.20	0.33
D	9.40	9.90
E	7.37	7.87
E1	6.10	6.60
E2	9.40	9.90
e	2.54 BSC.	
L	0.38	0.89
aaa	—	0.25
Notes:		
1. All dimensions shown are in millimeters (mm) unless otherwise noted.		
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.		

12. Land Pattern: DIP8

Figure 23 illustrates the recommended land pattern details for the Si826x in a DIP8 package. Table 19 lists the values for the dimensions shown in the illustration.

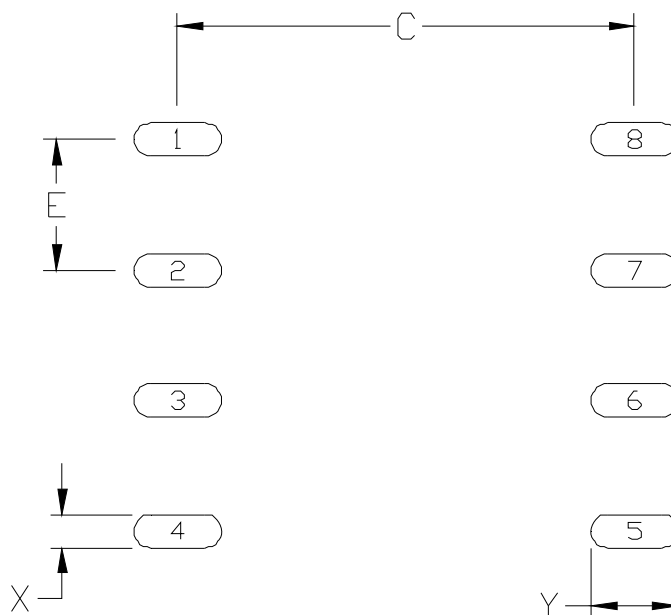


Figure 23. DIP8 Land Pattern

Table 19. DIP8 Land Pattern Dimensions*

Dimension	Min	Max
C	8.85	8.90
E	2.54 BSC	
X	0.60	0.65
Y	1.65	1.70

***Note:** This Land Pattern Design is based on the IPC-7351 specification.

13. Package Outline: SDIP6

Figure 24 illustrates the package details for the Si826x in an SDIP6 package. Table 20 lists the values for the dimensions shown in the illustration.

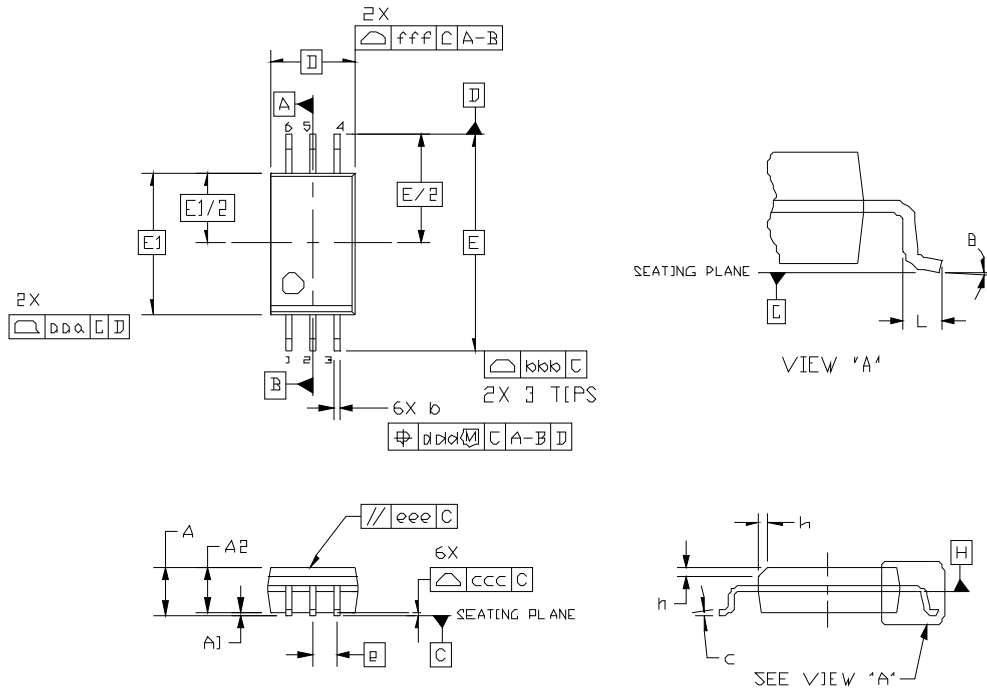


Figure 24. SDIP6 Package

Table 20. SDIP6 Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	4.58 BSC	
E	11.50 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

Table 20. SDIP6 Package Diagram Dimensions (Continued)

Dimension	Min	Max
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

14. Land Pattern: SDIP6

Figure 25 illustrates the recommended land pattern details for the Si826x in an SDIP6 package. Table 21 lists the values for the dimensions shown in the illustration.

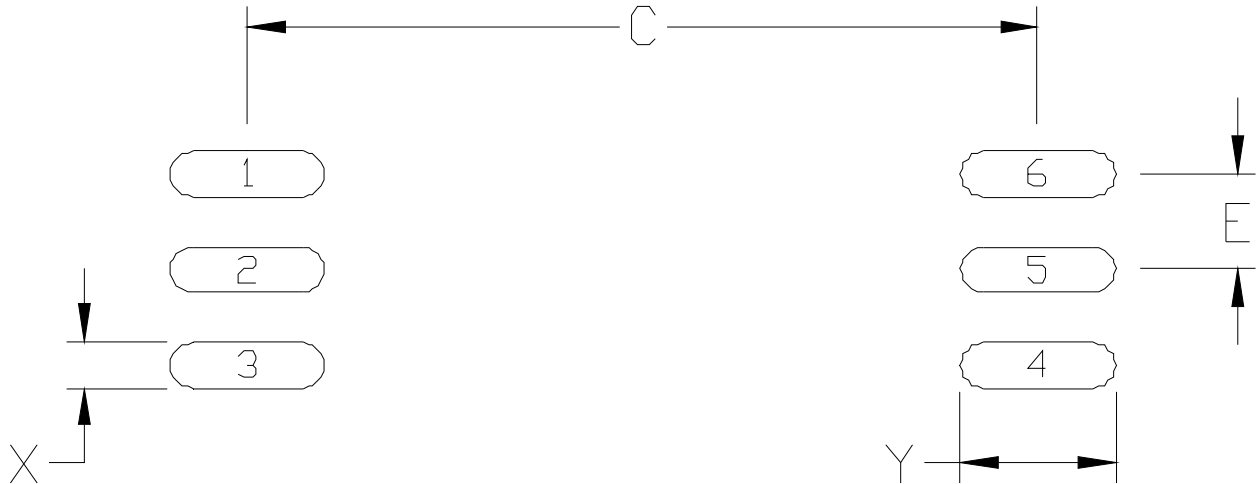


Figure 25. SDIP6 Land Pattern

Table 21. SDIP6 Land Pattern Dimensions*

Dimension	Min	Max
C	10.45	10.50
E	1.27 BSC	
X	0.55	0.60
Y	2.00	2.05
*Note: This Land Pattern Design is based on the IPC-7351 specification.		

15. Package Outline: LGA8

Figure 26 illustrates the package details for the Si826x in an LGA8 package. Table 22 lists the values for the dimensions shown in the illustration.

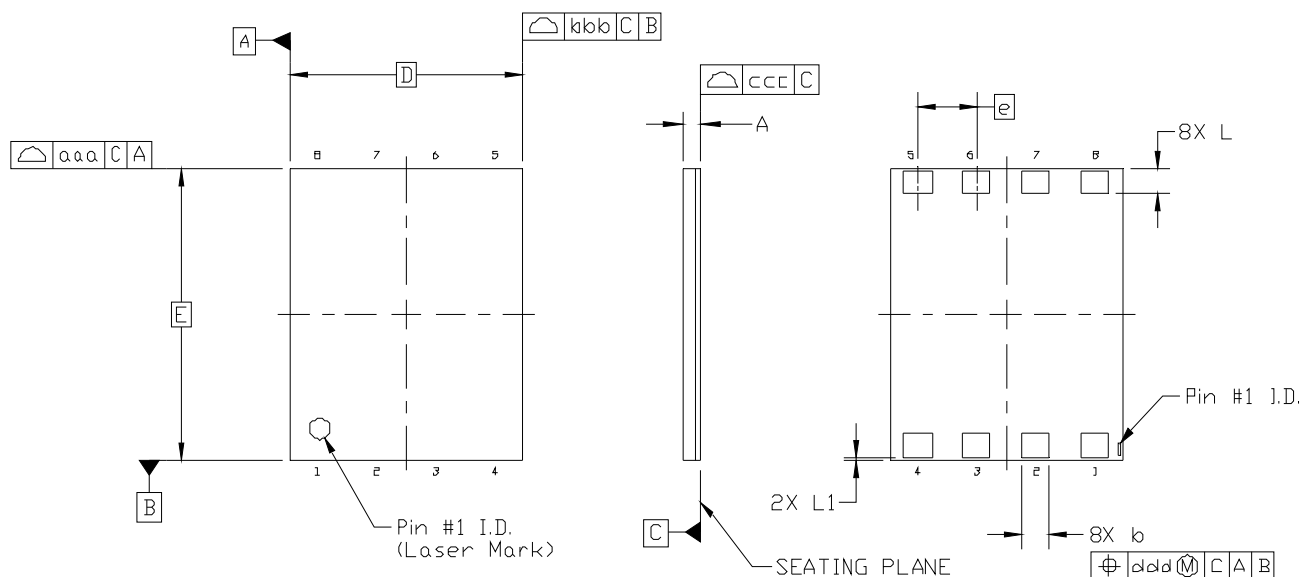


Figure 26. LGA8 Package

Table 22. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.74	0.84	0.94
b	1.15	1.20	1.25
D	10.00 BSC.		
e	2.54 BSC.		
E	12.50 BSC.		
L	1.05	1.10	1.15
L1	0.05	0.10	0.15
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.10
ddd	—	—	0.10
Notes:			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			

16. Land Pattern: LGA8

Figure 27 illustrates the recommended land pattern details for the Si826x in an LGA8 package. Table 23 lists the values for the dimensions shown in the illustration.

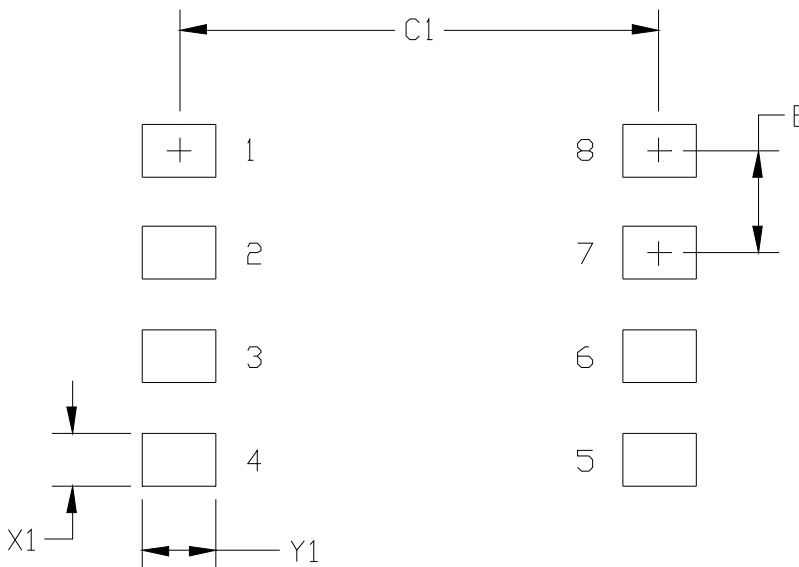


Figure 27. LGA8 Land Pattern

Table 23. LGA8 Land Pattern Dimensions

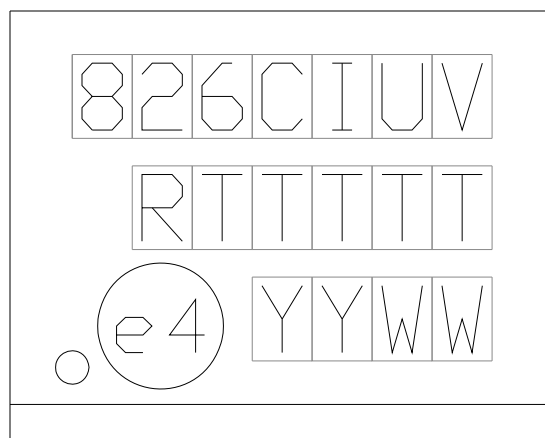
Dimension	Feature	(mm)
C1	Pad Column Spacing	11.80
E	Pad Row Pitch	2.54
X1	Pad Width	1.30
Y1	Pad Length	1.80

Notes:

1. This Land Pattern Design is based on IPC-7351 specifications.
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

17. Top Markings

17.1. Si826x Top Marking (Narrow Body SOIC)

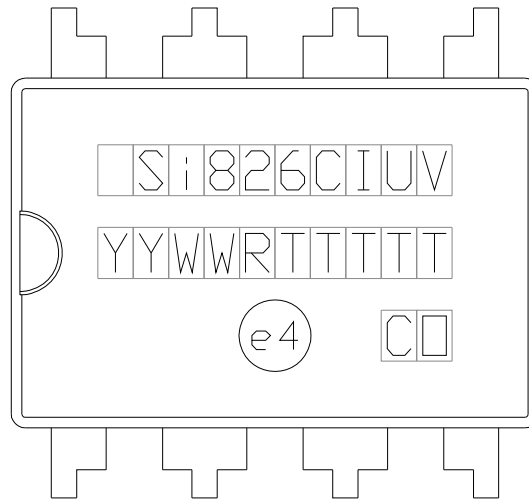


17.2. Top Marking Explanation

Line 1 Marking:	Customer Part Number	826 = ISOdriver product series C = Input configuration 1 = Opto input type I = Peak output current A = 0.6 A; B = 4.0 A U = UVLO level A = 5 V; B = 8 V; C = 12 V V = Isolation rating C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	RTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. "R" indicates revision.
Line 3 Marking:	Circle = 43 mils Diameter Left-Justified	"e4" Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

Si826x

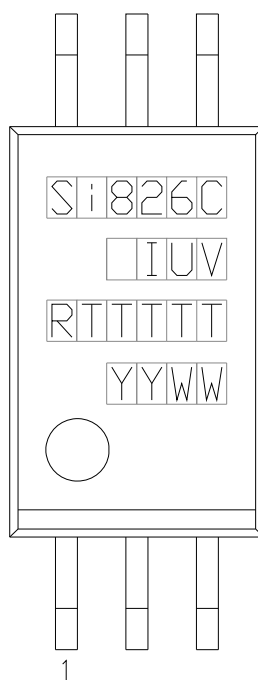
17.3. Si826x Top Marking (DIP8)



17.4. Top Marking Explanation

Line 1 Marking:	Customer Part Number	Si826 = ISOdriver product series C = Input configuration 1 = Opto input type I = Peak output current A = 0.6 A; B = 4.0 A U = UVLO level A = 5 V; B = 8 V; C = 12 V V = Isolation rating C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	RTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. "R" indicates revision.
Line 3 Marking:	Circle = 51 mils Diameter Center-Justified	"e4" Pb-Free Symbol
	CO = Country of Origin	Country of Origin ISO Code Abbreviation

17.5. Si826x Top Marking (SDIP6)

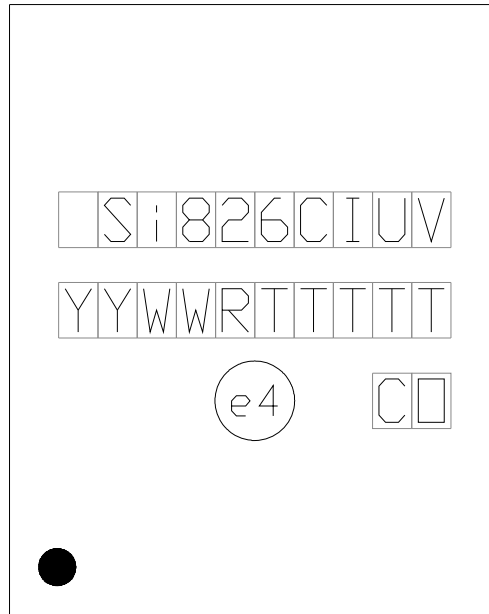


17.6. Top Marking Explanation

Line 1 Marking:	Device	Si826 = ISOdriver product series C = Input configuration 1 = Opto input type
Line 2 Marking:	Device Rating	I = Peak output current A = 0.6 A; B = 4.0 A U = UVLO level A = 5 V; B = 8 V; C = 12 V V = Isolation rating C = 3.75 kV; D = 5.0 kV
Line 3 Marking:	RTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. "R" indicates revision.
Line 4 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

Si826x

17.7. Si826x Top Marking (LGA8)



17.8. Top Marking Explanation

Line 1 Marking:	Device Part Number	Si826 = ISOdriver product series C = Input configuration 1 = Opto input type I = Peak output current A = 0.6 A; B = 4.0 A U = UVLO level A = 5 V; B = 8 V; C = 12 V V = Isolation rating C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	RTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. "R" indicates revision.
Line 3 Marking:	Circle = 1.6 mm Diameter Center-Justified	"e4" Pb-Free Symbol
	CO = Country of Origin	Country of Origin ISO Code Abbreviation
Line 4 Marking:	Circle = 0.75 mm Diameter Lower Left-Justified	Pin 1 Identifier

NOTES:

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