Monolithic 2A Step-Down Regulator

The EL7532 is a synchronous, integrated FET 2A step-down regulator with internal compensation. It operates with an input voltage range from 2.5V to 5.5V, which accommodates supplies of 3.3V, 5V, or a Li-Ion battery source. The output can be externally set from 0.8V to V_{IN} with a resistive divider.

The EL7532 features PWM mode control. The operating frequency is typically 1.5MHz. Additional features include a 100ms Power-On-Reset output, <1µA shut-down current, short-circuit protection, and over-temperature protection.

The EL7532 is available in the 10-pin MSOP and 10-pin DFN (3x3 mm) packages, making the entire converter occupy less than 0.15 in^2 of PCB area with components on one side only. Both packages are specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL7532IY	10-Pin MSOP	-	MDP0043
EL7532IY-T7	10-Pin MSOP	7”	MDP0043
EL7532IY-T13	10-Pin MSOP	13”	MDP0043
EL7532IL	10-Pin DFN	-	MDP0047
EL7532IL-T7	10-Pin DFN	7”	MDP0047
EL7532IL-T13	10-Pin DFN	13”	MDP0047

Features

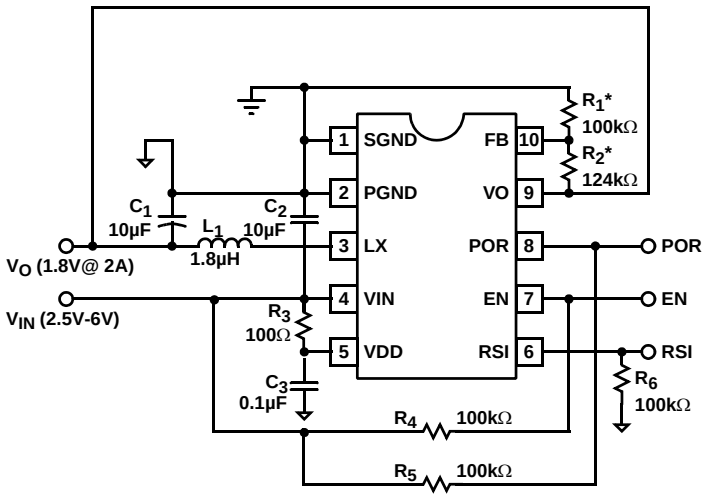
- Less than 0.15 in^2 (0.97 cm^2) footprint for the complete 2A converter
- Components on one side of PCB
- Max height 1.1mm MSOP10 or 1mm DFN 10 package
- 100ms Power-On-Reset output (POR)
- Internally-compensated voltage mode controller
- Up to 94% efficiency
- <1µA shut-down current
- Over-current and over-temperature protection

Applications

- PDA and pocket PC computers
- Bar code readers
- Cellular phones
- Portable test equipment
- Li-Ion battery powered devices
- Small form factor (SFP) modules

Pinout and Typical Application Diagram

EL7532
TOP VIEW



* $V_O = 0.8V * (1 + R_2 / R_1)$

Absolute Maximum Ratings (T_A = 25°C)

V_{IN}, V_{DD}, POR to SGND . . . . . -0.3V to +6.5V
LX to PGND . . . . . -0.3V to (V_{IN} + +0.3V)
RSI, EN, V_O, FB to SGND . . . . . -0.3V to (V_{IN} + +0.3V)
PGND to SGND . . . . . -0.3V to +0.3V
Peak Output Current 2.4A

Operating Ambient Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +145°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

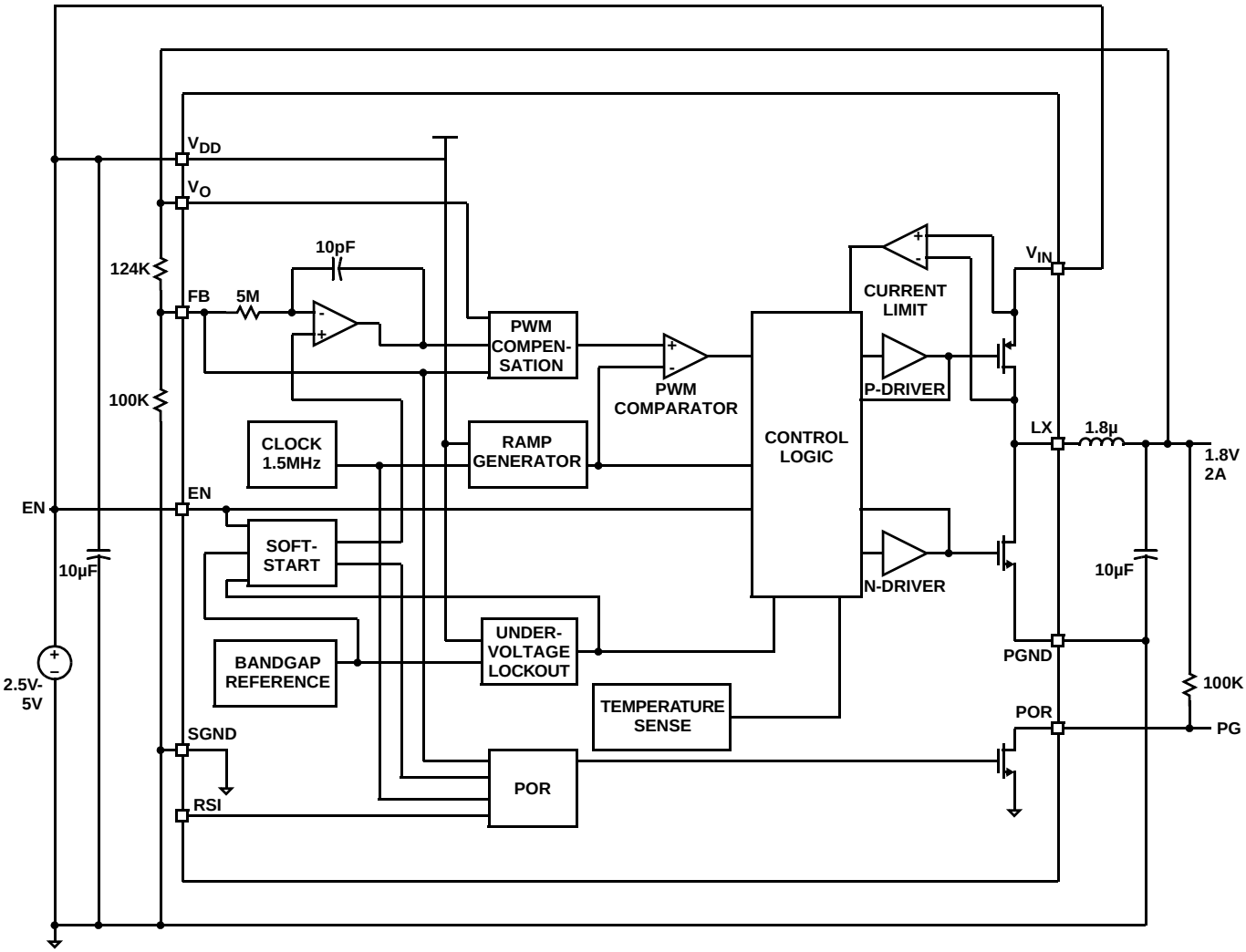
$V_{DD} = V_{IN} = V_{EN}$ = 3.3V, C1 = C2 = 10µF, L = 1.8µH, V_O = 1.8V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
V_{FB}	Feedback Input Voltage		790	800	810	mV
I_{FB}	Feedback Input Current				250	nA
V_{IN}, V_{DD}	Input Voltage		2.5		5.5	V
$V_{IN,OFF}$	Minimum Voltage for Shutdown	V_{IN} falling	2		2.2	V
$V_{IN,ON}$	Maximum Voltage for Startup	V_{IN} rising	2.2		2.4	V
I_{DD}	Supply Current	PWM, $V_{IN} = V_{DD}$ = 5V		400	500	µA
		EN = 0, $V_{IN} = V_{DD}$ = 5V		0.1	1	µA
$R_{DS(ON)-PMOS}$	PMOS FET Resistance	V_{DD} = 5V, wafer test only		52	80	mΩ
$R_{DS(ON)-NMOS}$	NMOS FET Resistance	V_{DD} = 5V, wafer test only		35	65	mΩ
I_{LMAX}	Current Limit			3		A
$T_{OT,OFF}$	Over-temperature Threshold	T rising		145		°C
$T_{OT,ON}$	Over-temperature Hysteresis	T falling		130		°C
I_{EN}, I_{RSI}	EN, RSI Current	V_{EN}, V_{RSI} = 0V and 3.3V	-1		1	V
V_{EN1}, V_{RSI1}	EN, RSI Rising Threshold	V_{DD} = 3.3V			2.4	V
V_{EN2}, V_{RSI2}	EN, RSI Falling Threshold	V_{DD} = 3.3V	0.8			V
V_{POR}	Minimum V_{FB} for POR, WRT Targeted V_{FB} Value	V_{FB} rising			95	%
		V_{FB} falling	86			%
V_{OLPOR}	POR Voltage Drop	I_{SINK} = 5mA		35	70	mV
AC CHARACTERISTICS						
F_{PWM}	PWM Switching Frequency		1.35	1.5	1.65	MHz
t_{RSI}	Minimum RSI Pulse Width	Guaranteed by design		25	50	ns
t_{SS}	Soft-start Time			650		µs
t_{POR}	Power On Reset Delay Time		50	100	150	ms

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	SGND	Negative supply for the controller stage
2	PGND	Negative supply for the power stage
3	LX	Inductor drive pin; high current digital output with average voltage equal to the regulator output voltage
4	VIN	Positive supply for the power stage
5	VDD	Power supply for the controller stage
6	RSI	Resets POR timer
7	EN	Enable
8	POR	Power on reset open drain output
9	VO	Output voltage sense
10	FB	Voltage feedback input; connected to an external resistor divider between V_O and SGND for variable output

Block Diagram



Typical Performance Curves

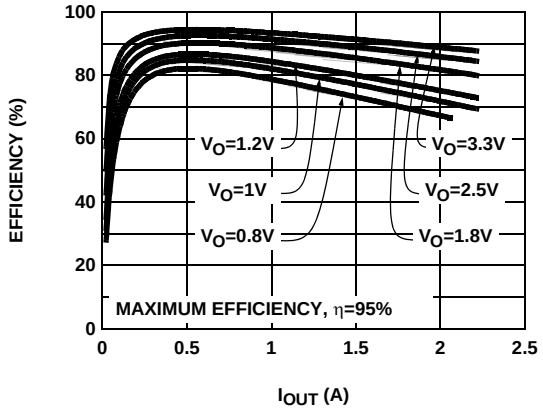


FIGURE 1. EFFICIENCY vs I_{OUT} @ V_{IN}=5V

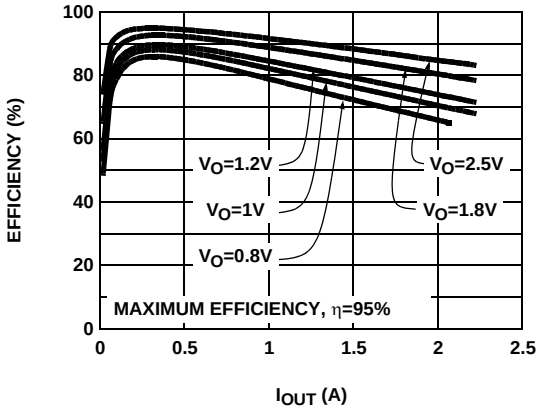


FIGURE 2. EFFICIENCY vs I_{OUT} @ V_{IN}=3.3V

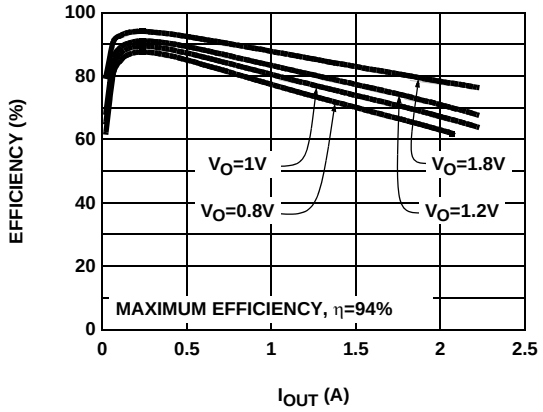


FIGURE 3. EFFICIENCY vs I_{OUT} @ V_{IN}=2.5V

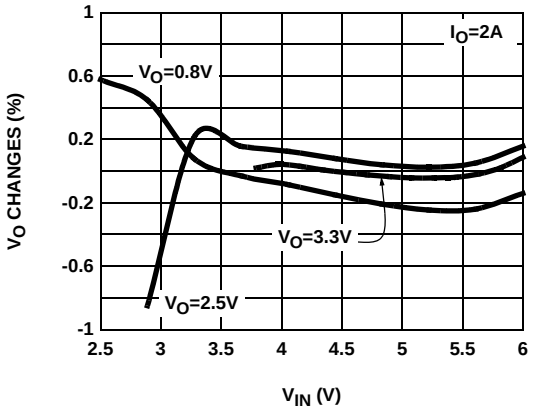


FIGURE 4. LINE REGULATION

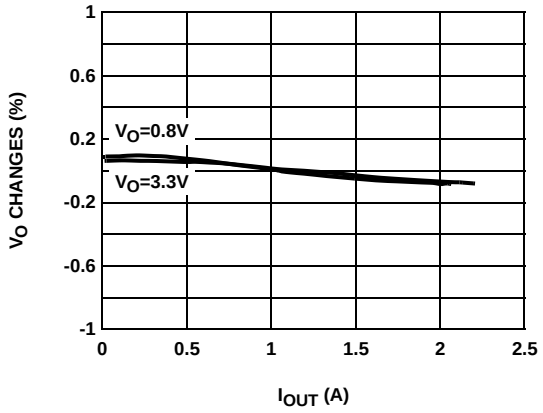


FIGURE 5. LOAD REGULATION @ V_{IN}=5V

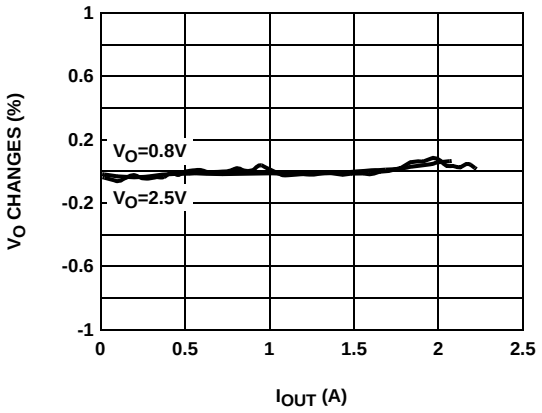


FIGURE 6. LOAD REGULATION @ V_{IN}=3.3V

Typical Performance Curves

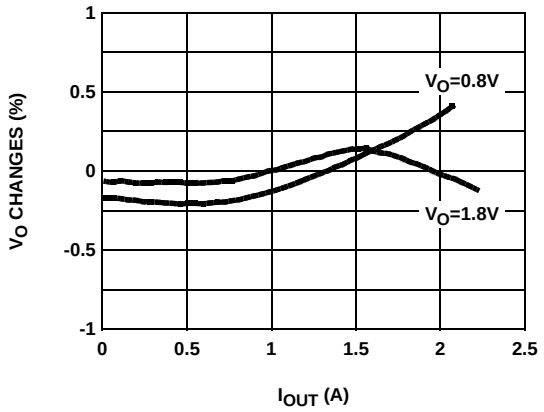


FIGURE 7. LOAD REGULATION @ V_{IN}=2.5V

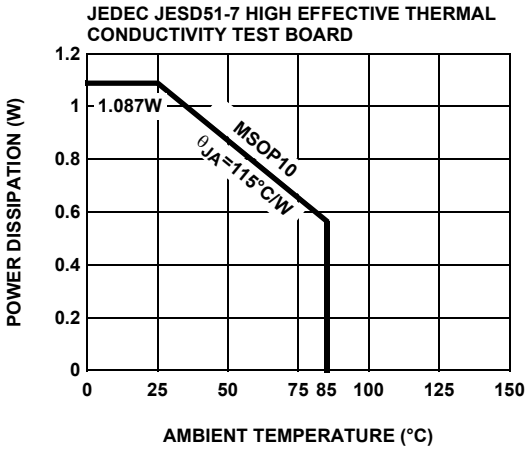


FIGURE 8. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

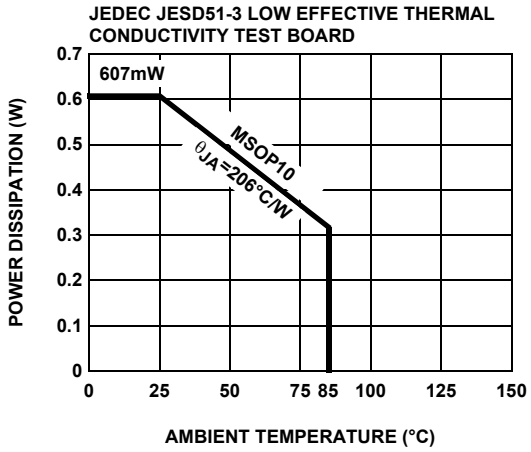


FIGURE 9. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Product Description

The EL7532 is a synchronous, integrated FET 2A step-down regulator which operates from an input of 2.5V to 6V. The output voltage is user-adjustable with a pair of external resistors.

The internally-compensated controller makes it possible to use only two ceramic capacitors and one inductor to form a complete, very small footprint 2A DC-DC converter.

Start-Up and Shut-Down

When the EN pin is tied to V_{IN}, and V_{IN} reaches approximately 2.4V, the regulator begins to switch. The output voltage is gradually increased to ensure proper soft-start operation.

When the EN pin is connected to a logic low, the EL7532 is in the shut-down mode. All the control circuitry and both MOSFETs are off, and V_{OUT} falls to zero. In this mode, the total input current is less than 1µA.

When the EN reaches logic HI, the regulator repeats the start-up procedure, including the soft-start function.

PWM Operation

In the PWM mode, the P channel MOSFET and N channel MOSFET always operate complementary. When the PMOSFET is on and the NMOSFET off, the inductor current increases linearly. The input energy is transferred to the output and also stored in the inductor. When the P channel MOSFET is off and the N channel MOSFET on, the inductor current decreases linearly, and energy is transferred from the inductor to the output. Hence, the average current through the inductor is the output current. Since the inductor and the output capacitor act as a low pass filter, the duty cycle ratio is approximately equal to V_O divided by V_{IN}.

The output LC filter has a second order effect. To maintain the stability of the converter, the overall controller must be compensated. This is done with the fixed internally compensated error amplifier and the PWM compensator. Because the compensations are fixed, the values of input and output capacitors are 10µF to 22µF ceramic. The inductor is nominally 1.8µH, though 1.5µA to 2.2µH can be used.

100% Duty Ratio Operation

EL7532 utilizes CMOS power FET's as the internal synchronous power switches. The upper switch is a PMOS and lower switch a NMOS. This not only saves a boot capacitor, it also allows 100% turn-on of the upper PFET switch, achieving V_O close to V_{IN}. The maximum achievable V_O is,

$$V_O = V_{IN} - (R_L + R_{DSON1}) \times I_O$$

Where RL is the DC resistance on the inductor and R_{DSON1} the PFET on-resistance, nominal 70mΩ at room temperature with tempco of 0.2mΩ/°C.

As the input voltage drops gradually close or even bellow the preset V_O, the converter gets into 100% duty ratio. At this condition, the upper PFET needs some minimum turn-off time if it is turned off. This off-time is related to input/output conditions. This makes the duty ratio appears randomly and increases the output ripple somewhat until the 100% duty ratio is reached. Larger output capacitor could reduce the random-looking ripple. Users need to verify if this condition has adverse effect on overall circuit if close to 100% duty ratio is expected.

RSI/POR Function

When powering up, the open-collector Power-On-Reset output holds low for about 100ms after V_O reaches the preset voltage. When the active-HI reset signal RSI is issued, POR goes to low immediately and holds for the same period of time after RSI comes back to LOW. The output voltage is unaffected. (Please refer to the timing diagram). When the function is not used, connect RSI to ground and leave open the pull-up resister R_4 at POR pin.

The POR output also serves as a 100ms delayed Power Good signal when the pull-up resister R_4 is installed. The RSI pin needs to be directly (or indirectly through a resister R_6) connected to Ground for this to function properly.

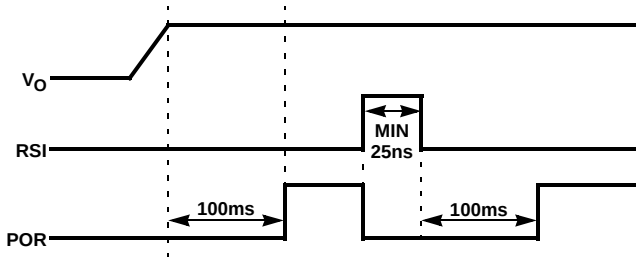


FIGURE 10. RSI & POR TIMING DIAGRAM

Output Voltage Selection

Users can set the output voltage of the converter with a resister divider, which can be chosen based on the following formula:

$$V_O = 0.8 \times \left(1 + \frac{R_2}{R_1}\right)$$

Component Selection

Because of the fixed internal compensation, the component choice is relatively narrow. We recommend 10µF to 22µF multi-layer ceramic capacitors with X5R or X7R rating for both the input and output capacitors, and 1.5µH to 2.2µH inductance for the inductor.

At extreme conditions (V_{IN} < 3V, I_O > 0.7A, and junction temperature higher than 75°C), input cap C_1 is recommended to be 22µF. Otherwise, if any of the above 3 conditions is not true, C_1 can remain as low as 10µF.

The RMS current present at the input capacitor is decided by the following formula:

$$I_{INRMS} = \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \times I_O$$

This is about half of the output current I_O for all the V_O. This input capacitor must be able to handle this current.

The inductor peak-to-peak ripple current is given as:

$$\Delta I_{IL} = \frac{(V_{IN} - V_O) \times V_O}{L \times V_{IN} \times f_S}$$

- L is the inductance
- f_S the switching frequency (nominally 1.5MHz)

The inductor must be able to handle I_O for the RMS load current, and to assure that the inductor is reliable, it must handle the 3A surge current that can occur during a current limit condition.

Current Limit and Short-Circuit Protection

The current limit is set at about 3A for the PMOS. When a short-circuit occurs in the load, the preset current limit restricts the amount of current available to the output, which causes the output voltage to drop below the preset voltage. In the meantime, the excessive current heats up the regulator until it reaches the thermal shut-down point.

Thermal Shut-Down

Once the junction reaches about 145°C, the regulator shuts down. Both the P channel and the N channel MOSFETs turn off. The output voltage will drop to zero. With the output MOSFETs turned off, the regulator will soon cool down. Once the junction temperature drops to about 130°C, the regulator will restart again in the same manner as EN pin connects to logic HI.

Thermal Performance

The EL7532 is in a fused-lead MSOP10 package. Compared with regular MSOP10 package, the fused-lead package provides lower thermal resistance. The θ_{JA} is 100°C/W on a 4-layer board and 125°C/W on 2-layer board. Maximizing the copper area around the pins will further improve the thermal performance.

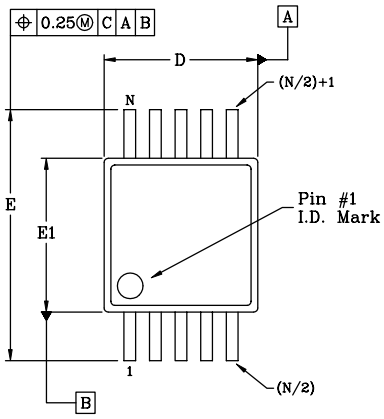
Layout Considerations

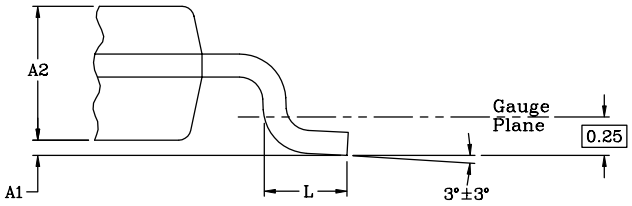
The layout is very important for the converter to function properly. The following PC layout guidelines should be followed:

- Separate the Power Ground (⏚) and Signal Ground (⏚); connect them only at one point right at the pins
- Place the input capacitor as close to V_{IN} and PGND pins as possible
- Make the following PC traces as small as possible:
  - from L_X pin to L
  - from C_O to PGND
- If used, connect the trace from the FB pin to R_1 and R_2 as close as possible
- Maximize the copper area around the PGND pin
- Place several via holes under the chip to additional ground plane to improve heat dissipation

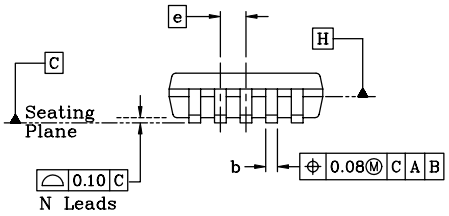
The demo board is a good example of layout based on this outline. Please refer to the EL7532 Application Brief.

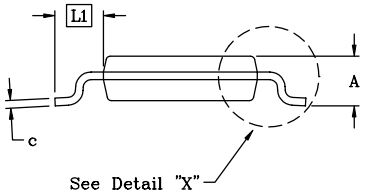
MSOP Package Outline Drawing





DETAIL X



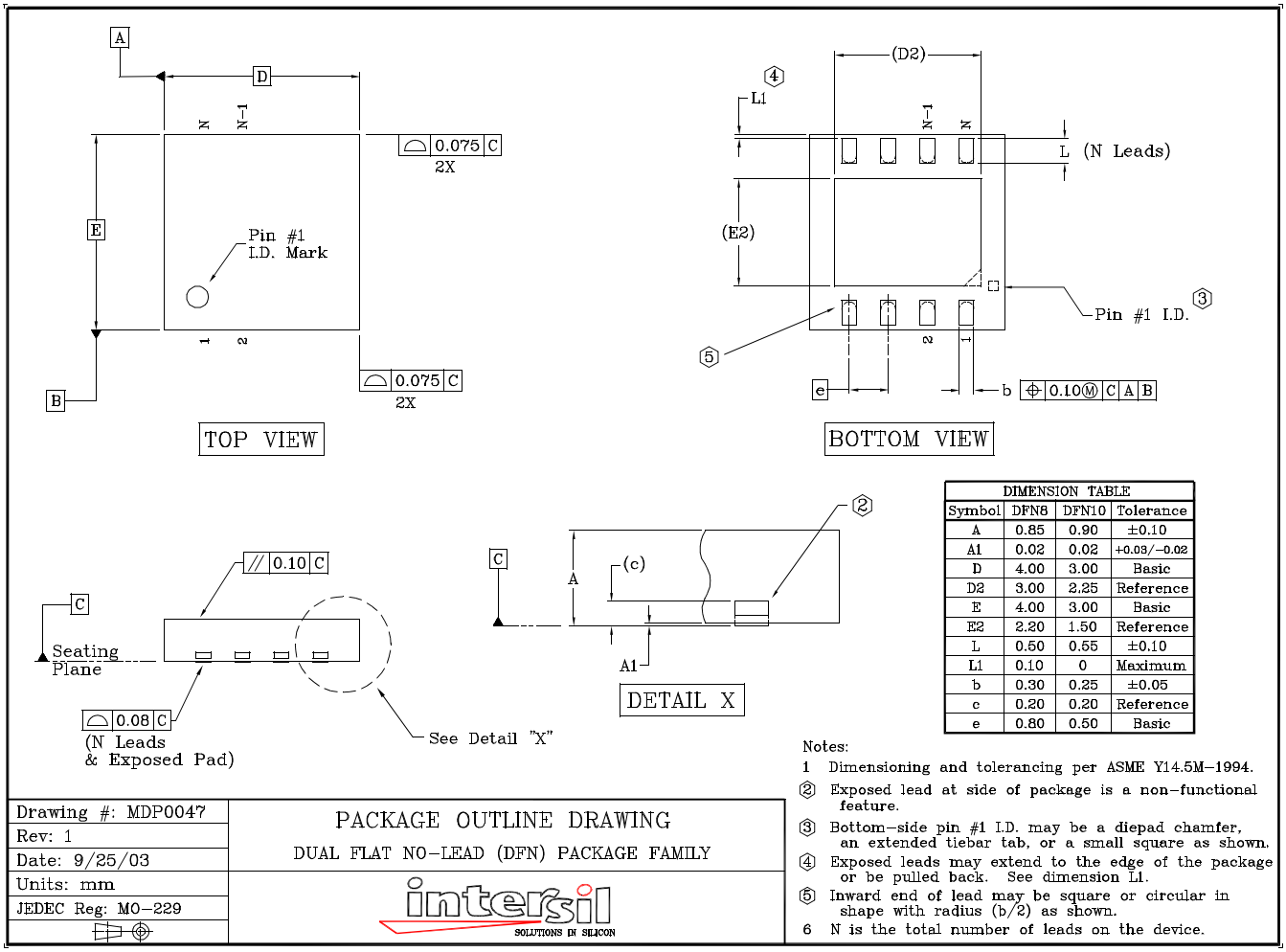


DIMENSION TABLE			
Symbol	MSOP8	MSOP10	Tolerance
A	1.10	1.10	MAX.
A1	0.10	0.10	+/− 0.05
A2	0.86	0.86	+/− 0.09
D (1)(3)	3.00	3.00	+/− 0.10
E	4.90	4.90	+/− 0.15
E1 (2)(3)	3.00	3.00	+/− 0.10
L	0.55	0.55	+/− 0.15
L1	0.95	0.95	Basic
b	0.33	0.23	+0.07/−0.08
c	0.18	0.18	+/− 0.05
e	0.65	0.50	Basic
N	8	10	Reference

Drawing #: MDP0043	PACKAGE OUTLINE DRAWING MINI SO PACKAGE (MSOP) PACKAGE FAMILY
Rev: C	
Date: 6/14/99	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
Units: mm	
JEDEC Reg: MO−187	

Notes:
(1) Plastic or metal protrusions of 0.15 mm maximum per side are not included.
(2) Plastic interlead protrusions of 0.25 mm maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M−1994.

DFN Package Outline Drawing



DIMENSION TABLE			
Symbol	DFN8	DFN10	Tolerance
A	0.85	0.90	±0.10
A1	0.02	0.02	+0.03/−0.02
D	4.00	3.00	Basic
D2	3.00	2.25	Reference
E	4.00	3.00	Basic
E2	2.20	1.50	Reference
L	0.50	0.55	±0.10
L1	0.10	0	Maximum
b	0.30	0.25	±0.05
c	0.20	0.20	Reference
e	0.80	0.50	Basic

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Exposed lead at side of package is a non-functional feature.
3. Bottom-side pin #1 I.D. may be a diepad chamfer, an extended tiebar tab, or a small square as shown.
4. Exposed leads may extend to the edge of the package or be pulled back. See dimension L1.
5. Inward end of lead may be square or circular in shape with radius (b/2) as shown.
6. N is the total number of leads on the device.

Drawing #: MDP0047	PACKAGE OUTLINE DRAWING
Rev: 1	DUAL FLAT NO-LEAD (DFN) PACKAGE FAMILY
Date: 9/25/03	
Units: mm	
JEDEC Reg: MO-229	

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>