
HM514265C Series HM51S4265C Series

262,144-word $\times$ 16-bit Dynamic Random Access Memory

HITACHI

ADE-203-309A (Z)

Rev. 1.0

Jul. 21, 1995

Description

The Hitachi HM51(S)4265C is a CMOS dynamic RAM organized 262,144-word $\times$ 16-bit. HM51(S)4265C has realized higher density, higher performance and various functions by employing 0.8 μ m CMOS process technology and some new CMOS circuit design technologies. The HM51(S)4265C offers Extended Data Out (EDO) Page Mode as a high speed access mode. Multiplexed address input permits the HM51(S)4265C to be packaged in standard 400-mil 40-pin plastic SOJ and standard 400-mil 44-pin plastic TSOPII. Internal refresh timer enables HM51S4265C self refresh operation.

Features

- Single 5 V ($\pm 10\%$) (HM51(S)4265C-6/7/8)
($\pm 5\%$) (HM51(S)4265C-6R)
- High speed
 - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Active mode: 825 mW/788 mW/770 mW/688 mW (max)
 - Standby mode: 11 mW (max) (HM51(S)4265C-6/7/8)
10.5 mW (max) (HM51(S)4265C-6R)
1.1 mW (max) (L-version) (HM51(S)4265CL-6/7/8)
1.05 mW (max) (L-version) (HM51(S)4265CL-6R)
- EDO page mode capability
- 512 refresh cycles : 8 ms
128 ms (L-version)
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- $2\overline{\text{CAS}}$ -byte control
- Battery backup operation (L-version)
- Self refresh operation (HM51S4265C)

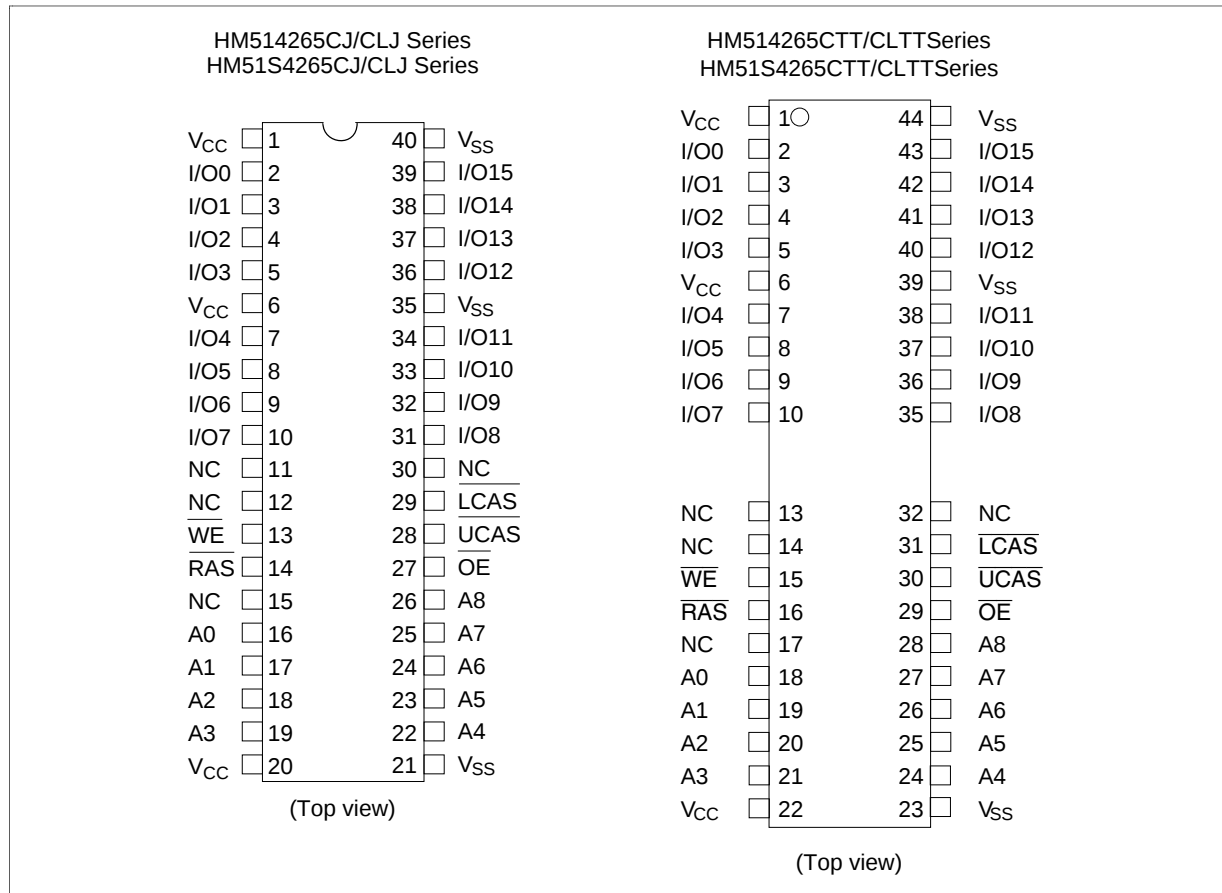
HM514265C, HM51S4265C Series

Ordering Information

Type No.	Access time	Package
HM514265CJ-6	60 ns	400-mil 40-pin plastic SOJ (CP-40DA)
HM514265CJ-6R	60 ns	
HM514265CJ-7	70 ns	
HM514265CJ-8	80 ns	
HM514265CLJ-6	60 ns	
HM514265CLJ-6R	60 ns	
HM514265CLJ-7	70 ns	
HM514265CLJ-8	80 ns	
HM51S4265CJ-6	60 ns	
HM51S4265CJ-6R	60 ns	
HM51S4265CJ-7	70 ns	
HM51S4265CJ-8	80 ns	
HM51S4265CLJ-6	60 ns	
HM51S4265CLJ-6R	60 ns	
HM51S4265CLJ-7	70 ns	
HM51S4265CLJ-8	80 ns	
HM514265CTT-6	60 ns	400-mil 44-pin plastic TSOPII (TTP-44/40DB)
HM514265CTT-6R	60 ns	
HM514265CTT-7	70 ns	
HM514265CTT-8	80 ns	
HM514265CLTT-6	60 ns	
HM514265CLTT-6R	60 ns	
HM514265CLTT-7	70 ns	
HM514265CLTT-8	80 ns	
HM51S4265CTT-6	60 ns	
HM51S4265CTT-6R	60 ns	
HM51S4265CTT-7	70 ns	
HM51S4265CTT-8	80 ns	
HM51S4265CLTT-6	60 ns	
HM51S4265CLTT-6R	60 ns	
HM51S4265CLTT-7	70 ns	
HM51S4265CLTT-8	80 ns	

HM514265C, HM51S4265C Series

Pin Arrangement

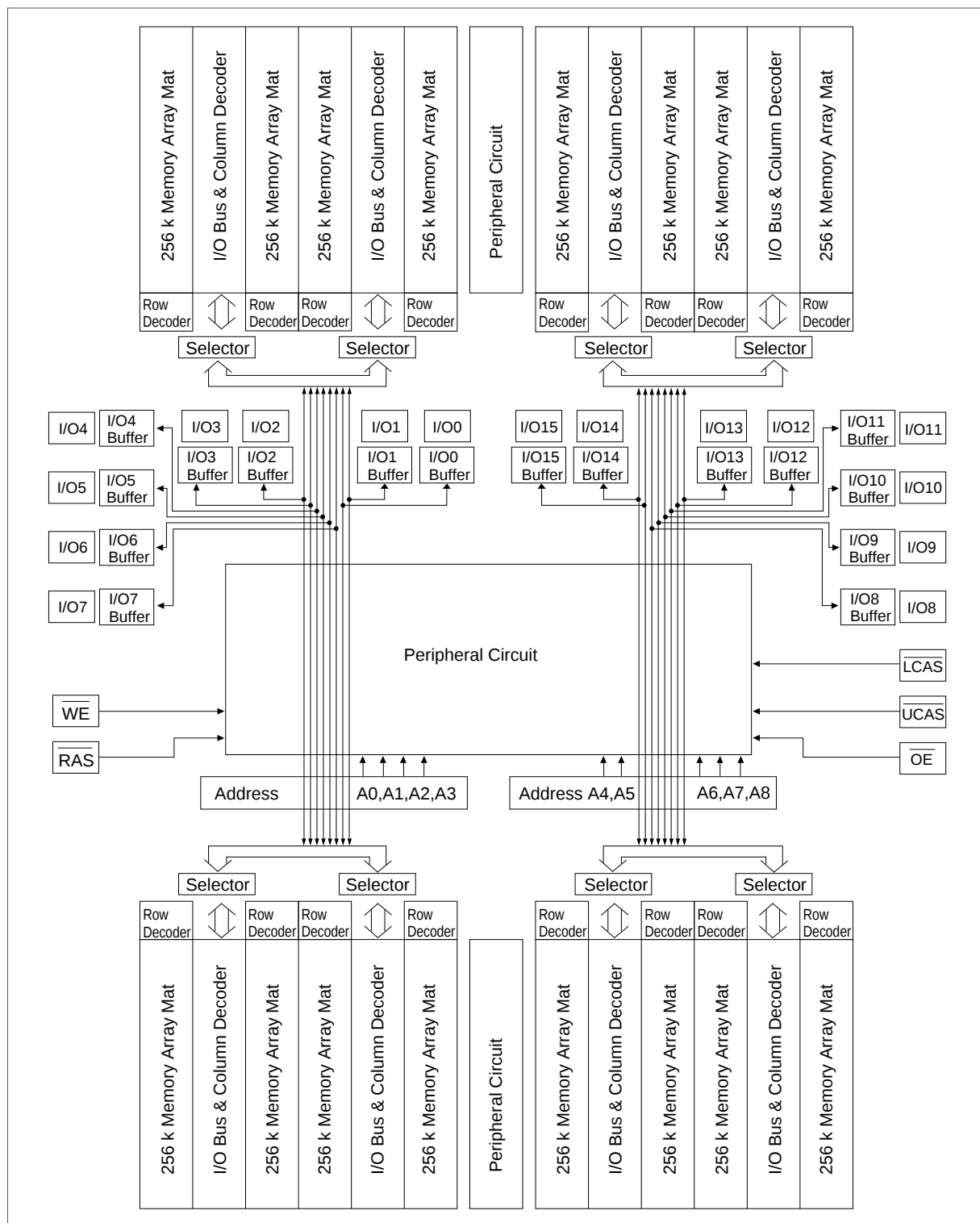


Pin Description

Pin name	Function
A0 – A8	Address input — Row address A0 – A8 — Column address A0 – A8 — Refresh address A0 – A8
I/O0 – I/O15	Data-in/data-out
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No connection

HM514265C, HM51S4265C Series

Block Diagram



HM514265C, HM51S4265C Series

Operation Mode

The HM51(S)4265C series has the following 11 operation modes.

1. Read cycle
2. Early write cycle
3. Delayed write cycle
4. Read-modify-write cycle
5. $\overline{\text{RAS}}$ -only refresh cycle
6. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle
7. Self refresh cycle (HM51S4265C)
8. EDO page mode read cycle
9. EDO page mode early write cycle
10. EDO page mode delayed write cycle
11. EDO page mode read- modify-write cycle

Inputs

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Output	Operation
H	H	H	D	D	Open	Standby
H	L	L	H	L	Valid	Standby
L	L	L	H	L	Valid	Read cycle
L	L	L	L ^{*2}	D	Open	Early write cycle
L	L	L	L ^{*2}	H	Undefined	Delayed write cycle
L	L	L	H to L	L to H	Valid	Read-modify-write cycle
L	H	H	D	D	Open	$\overline{\text{RAS}}$ -only refresh cycle
H to L	H	L	D	D	Open	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle
	L	H				Self refresh cycle (HM51S4265C)
	L	L				
L	H to L	H to L	H	L	Valid	EDO page mode read cycle
L	H to L	H to L	L ^{*2}	D	Open	EDO page mode early write cycle
L	H to L	H to L	L ^{*2}	H	Undefined	EDO page mode delayed write cycle
L	H to L	H to L	H to L	L to H	Valid	EDO page mode read-modify-write cycle
L	L	L	H	H	Open	Read cycle (Output disabled)

Notes: 1. H: High(inactive) L: Low(active) D: H or L

2. $t_{\text{WCS}} \geq 0$ ns Early write cycle

$t_{\text{WCS}} < 0$ ns Delayed write cycle

3. Mode is determined by the OR function of the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$. (Mode is set by the earliest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ active edge and reset by the latest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ inactive edge.) However write OPERATION and output HIZ control are done independently by each $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$.

ex. if $\overline{\text{RAS}} = \text{H to L}$, $\overline{\text{LCAS}} = \text{L}$, $\overline{\text{UCAS}} = \text{H}$, then $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle is selected.

HM514265C, HM51S4265C Series

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC} (HM51(S)4265C-6/7/8)	4.5	5.0	5.5	V	1, 2
	V_{CC} (HM51(S)4265C-6R)	4.75	5.0	5.25	V	1, 2
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Notes: 1. All voltage referred to V_{SS} .

2. The supply voltage with all V_{CC} pins must be on the same level.

The supply voltage with all V_{SS} pins must be on the same level.

HM514265C, HM51S4265C Series

DC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$) (HM51(S)4265C-6R)
 ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)
 (HM51(S)4265C-6/7/8)

HM514265C, HM51S4265C									
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current ^{*1, *2}	I_{CC1}	—	150	—	140	—	125	mA	$\overline{\text{RAS}}$ cycling $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ cycling $t_{RC} = \text{min}$
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}} = V_{IH}$ Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}, \overline{\text{WE}},$ $\overline{\text{OE}} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z
Standby current (L-version)	I_{CC2}	—	200	—	200	—	200	μA	CMOS interface $\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}, \overline{\text{WE}},$ $\overline{\text{OE}} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z
$\overline{\text{RAS}}$ -only refresh current ^{*2}	I_{CC3}	—	140	—	130	—	110	mA	$t_{RC} = \text{min}$
Standby current ^{*1}	I_{CC5}	—	5	—	5	—	5	mA	$\overline{\text{RAS}} = V_{IH}$ $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}} = V_{IL}$ Dout = enable
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current ^{*2}	I_{CC6}	—	140	—	130	—	110	mA	$t_{RC} = \text{min}$
EDO page mode current ^{*1, *3}	I_{CC4}	—	180	—	150	—	130	mA	$t_{HPC} = \text{min}$
Battery backup current ^{*4} (Standby with CBR refresh) (L-version)	I_{CC10}	—	300	—	300	—	300	μA	Standby: CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 250\text{ }\mu\text{s}$ $t_{RAS} \leq 1\text{ }\mu\text{s}$, $\overline{\text{UCAS}}, \overline{\text{LCAS}} = V_{IL}$ $\overline{\text{WE}}, \overline{\text{OE}} = V_{IH}$
Self-refresh mode current (HM51S4265C)	I_{CC11}	—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}} \leq 0.2\text{ V}$, Dout = High-Z
Self-refresh mode current (HM51S4265CL)	I_{CC11}	—	200	—	200	—	200	μA	CMOS interface $\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}} \leq 0.2\text{ V}$, Dout = High-Z
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 7\text{ V}$
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 7\text{ V}$ Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -2 mA

HM514265C, HM51S4265C Series

HM514265C, HM51S4265C									
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I _{out} = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
 2. Address can be changed twice or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less within one EDO page cycle.
 4. $V_{IH} \geq V_{CC} - 0.2 V$, $0 \leq V_{IL} \leq 0.2 V$, Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 5. All the V_{CC} pins should be supplied with the same voltage. And all the V_{SS} pins should be supplied with the same voltage.

Capacitance ($T_a = +25^\circ C$, $V_{CC} = 5 V \pm 5\%$) (HM51(S)4265C-6R)
 ($T_a = +25^\circ C$, $V_{CC} = 5 V \pm 10\%$) (HM51(S)4265C-6/7/8)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	C_{IO}	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{RAS}$, $\overline{UCAS}$ and $\overline{LCAS} = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0$ to $+70^\circ C$, $V_{CC} = 5 V \pm 5\%$, $V_{SS} = 0 V$)
 (HM51(S)4265C-6R) *1, *14, *15, *17, *18
 ($T_a = 0$ to $+70^\circ C$, $V_{CC} = 5 V \pm 10\%$, $V_{SS} = 0 V$)
 (HM51(S)4265C-6/7/8) *1, *14, *15, *17, *18

Test Conditions

- Input rise and fall time : 2 ns
- Input level : $V_{IL} = 0 V$, $V_{IH} = 3.0 V$
- Input timing reference levels : 0.8 V, 2.4 V
- Output timing reference levels : 0.8 V, 2.0 V
- Output load : 1 TTL gate + C_L (50 pF) (Including scope and jig)

HM514265C, HM51S4265C Series

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

HM514265C, HM51S4265C									
		-6/-6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	104	—	124	—	144	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	27
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	15	10000	ns	28
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	19
Column address hold time	t_{CAH}	10	—	13	—	15	—	ns	19
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	9
$\overline{RAS}$ hold time	t_{RSH}	15	—	18	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	48	—	58	—	68	—	ns	29
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	20
$\overline{OE}$ to Din delay time	t_{ODD}	15	—	18	—	20	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	7
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	

HM514265C, HM51S4265C Series

Read Cycle

HM514265C, HM51S4265C									
		-6/-6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	20	—	20	ns	3, 4, 13
Access time from address	t_{AA}	—	30	—	35	—	40	ns	3, 5, 13
Access time from $\overline{\text{OE}}$	t_{OAC}	—	15	—	20	—	20	ns	23
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	19
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	16, 19
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	16
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	28	—	ns	
Output buffer turn-off time	t_{OFF1}	—	15	—	15	—	15	ns	6, 25
Output buffer turn-off time to $\overline{\text{OE}}$	t_{OFF2}	—	15	—	15	—	15	ns	6
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	20	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	20	—	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WDD}	15	—	18	—	20	—	ns	
$\overline{\text{OE}}$ pulse width	t_{OEP}	15	—	20	—	20	—	ns	23
Turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	—	15	ns	6, 25
Turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	—	15	ns	6
Output data hold time	t_{OH}	5	—	5	—	5	—	ns	
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	80	—	ns	
Read command hold time from $\overline{\text{CAS}}$	t_{RCHC}	15	—	18	—	20	—	ns	
Read command hold time from column address	t_{RCHA}	30	—	35	—	40	—	ns	

HM514265C, HM51S4265C Series

Write Cycle

HM514265C, HM51S4265C									
		-6/-6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10, 19
Write command hold time	t_{WCH}	10	—	13	—	15	—	ns	19
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	15	—	ns	21
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	10	—	13	—	15	—	ns	11

Read-Modify-Write Cycle

HM514265C, HM51S4265C									
		-6/-6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	133	—	159	—	183	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	—	90	—	102	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	—	38	—	42	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	47	—	55	—	62	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	18	—	20	—	ns	

Refresh Cycle

HM514265C, HM51S4265C									
		-6/-6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	19
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	19
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	13	—	15	—	ns	22

HM514265C, HM51S4265C Series

EDO Page Mode Cycle

HM514265C, HM51S4265C									
		-6/-6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t_{HPC}	25	—	30	—	35	—	ns	24
EDO page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	15	—	ns	
EDO page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	35	—	40	—	45	ns	3, 13, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	—	40	—	45	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	3	—	ns	26
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	10	—	13	—	20	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHP}	35	—	40	—	45	—	ns	

EDO Page Mode Read-Modify-Write Cycle

HM514265C, HM51S4265C									
		-6/-6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode read-modify-write cycle time	t_{HPCM}	66	—	77	—	86	—	ns	
EDO page mode read-modify-write cycle $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	52	—	60	—	67	—	ns	10

Self Refresh Mode

HM51S4265C									
		-6/-6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	100	—	ns	30, 31, 32
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	110	—	130	—	150	—	ns	
$\overline{CAS}$ hold time (self refresh)	t_{CHS}	-50	—	-50	—	-50	—	ns	21

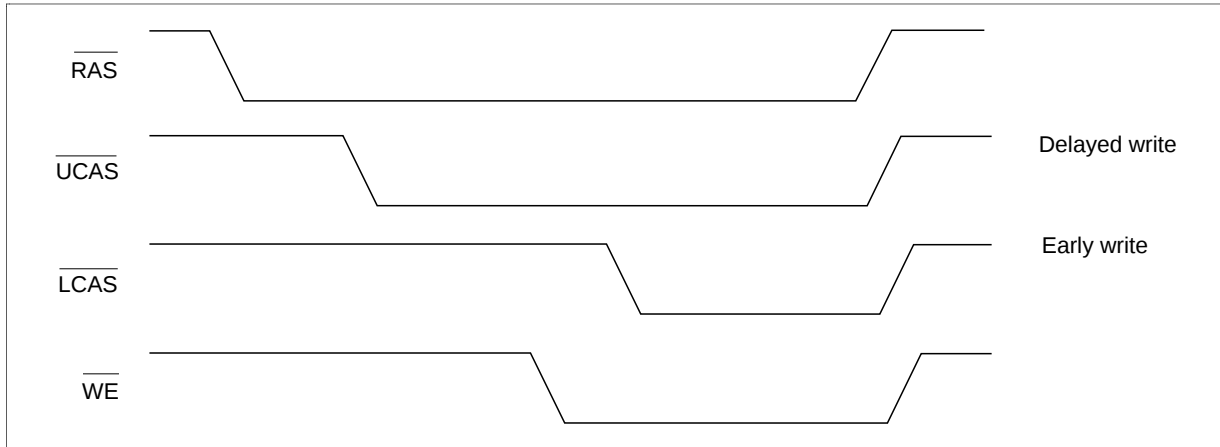
- Notes:
1. AC measurements assume $t_T = 2 \text{ ns}$.
 2. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 1 TTL loads and 50 pF.
 4. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$.
 5. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$.
 6. $t_{\text{OFF1}}(\text{max})$, $t_{\text{OFF2}}(\text{max})$, $t_{\text{OFR}}(\text{max})$ and $t_{\text{WEZ}}(\text{max})$ define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
 7. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referred to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
 12. t_{RASC} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 13. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{ACP} .
 14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles is required.
 15. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
 16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 17. When both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ go low at the same time, all 16-bit data are written into the device. $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ cannot be staggered within the same write/read cycles.
 18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 19. t_{ASC} , t_{CAH} , t_{RCS} , t_{RCH} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 20. t_{CRP} , t_{CHR} , t_{ACP} , t_{RCH} and t_{CPW} are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 21. t_{CWL} , t_{DH} , t_{DS} and t_{CHS} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
 22. t_{CPN} and t_{CP} are determined by the time that both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.
 23. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}}/V_{\text{SS}}$ line noise, which causes to degrade $V_{\text{IH min}}/V_{\text{IL max}}$ level.
 24. $t_{\text{HPC}}(\text{min})$ can be achieved during a series of EDO page mode early write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle t_{HPC} ($t_{\text{CAS}} + t_{\text{CP}} + 2t_{\text{T}}$) becomes greater than the specified $t_{\text{HPC}}(\text{min})$ value.
 25. t_{OFF1} and t_{OFR} are determined by the later rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$.
 26. t_{DOH} defines the time at which the output level satisfies the output timing reference levels. Measured with the test conditions.

HM514265C, HM51S4265C Series

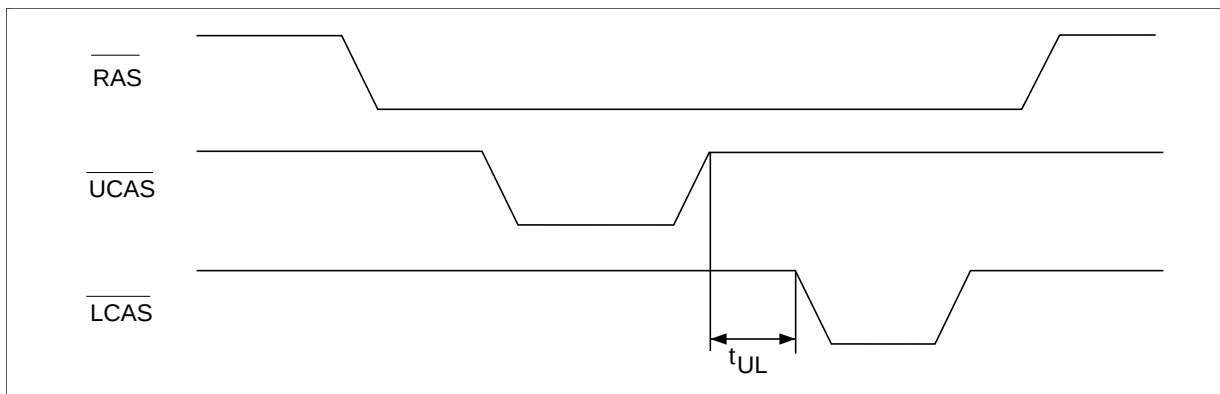
- 27. $t_{RAS}(\text{min}) = t_{RWD}(\text{min}) + t_{RWL}(\text{min}) + t_T$ in read-modify-write cycle.
- 28. $t_{CAS}(\text{min}) = t_{CWD}(\text{min}) + t_{CWL}(\text{min}) + t_T$ in read-modify-write cycle.
- 29. $t_{CSH}(\text{min})$ can be achieved when $t_{RCD} \leq t_{CSH}(\text{min}) - t_{CAS}(\text{min})$.
- 30. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
- 31. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with 15.6 μs interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
- 32. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
- 33.  H or L (H: $V_{IH}(\text{min}) \leq V_{IN} \leq V_{IH}(\text{max})$, L: $V_{IL}(\text{min}) \leq V_{IN} \leq V_{IL}(\text{max})$)
 Invalid Dout

Notes concerning $\overline{2CAS}$ control

- Each of the $\overline{UCAS}/\overline{LCAS}$ should satisfy the timing specifications individually.
- Different operation mode for upper/lower byte is not allowed; such as following.



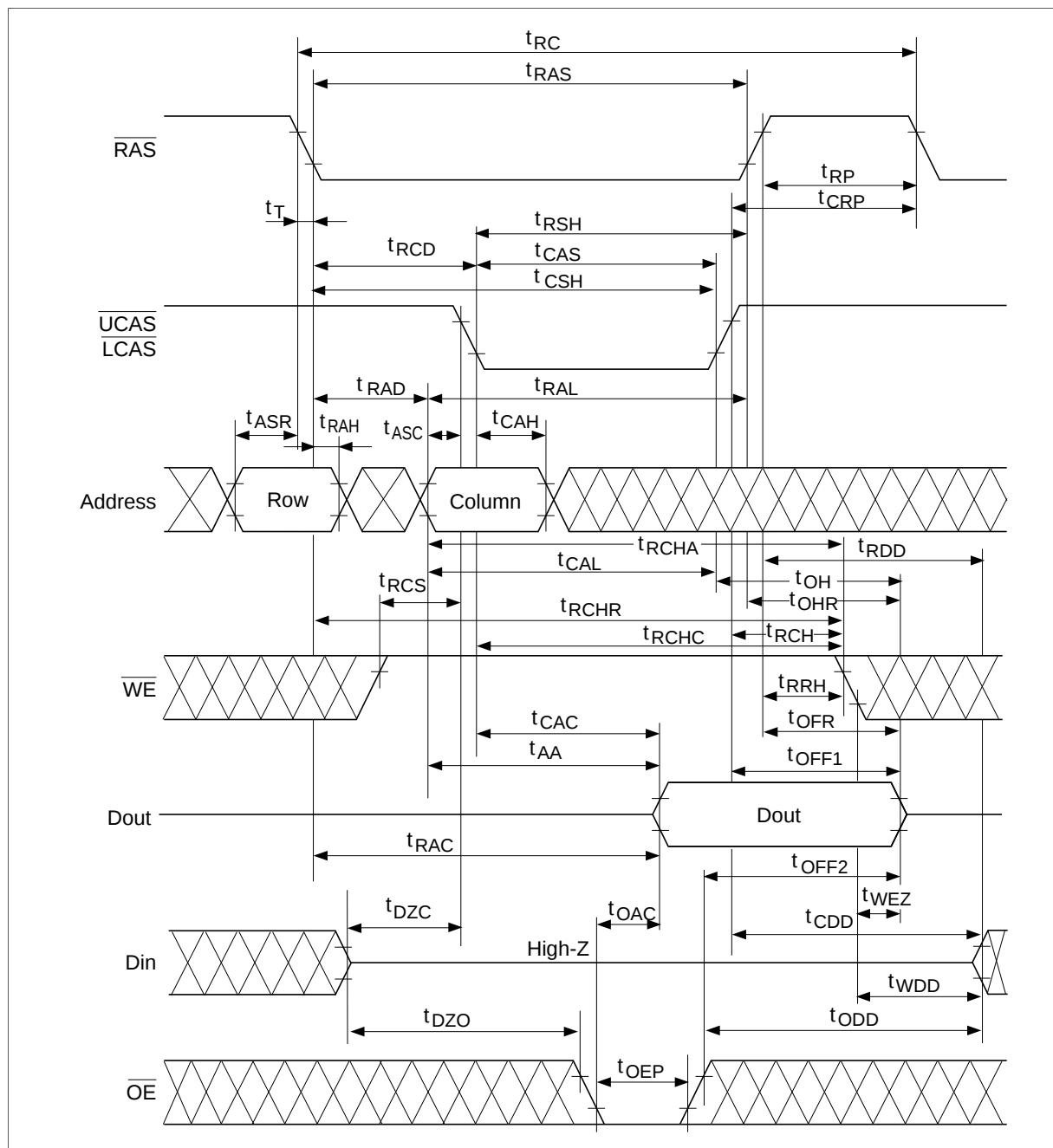
- Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, fast page mode can be performed.



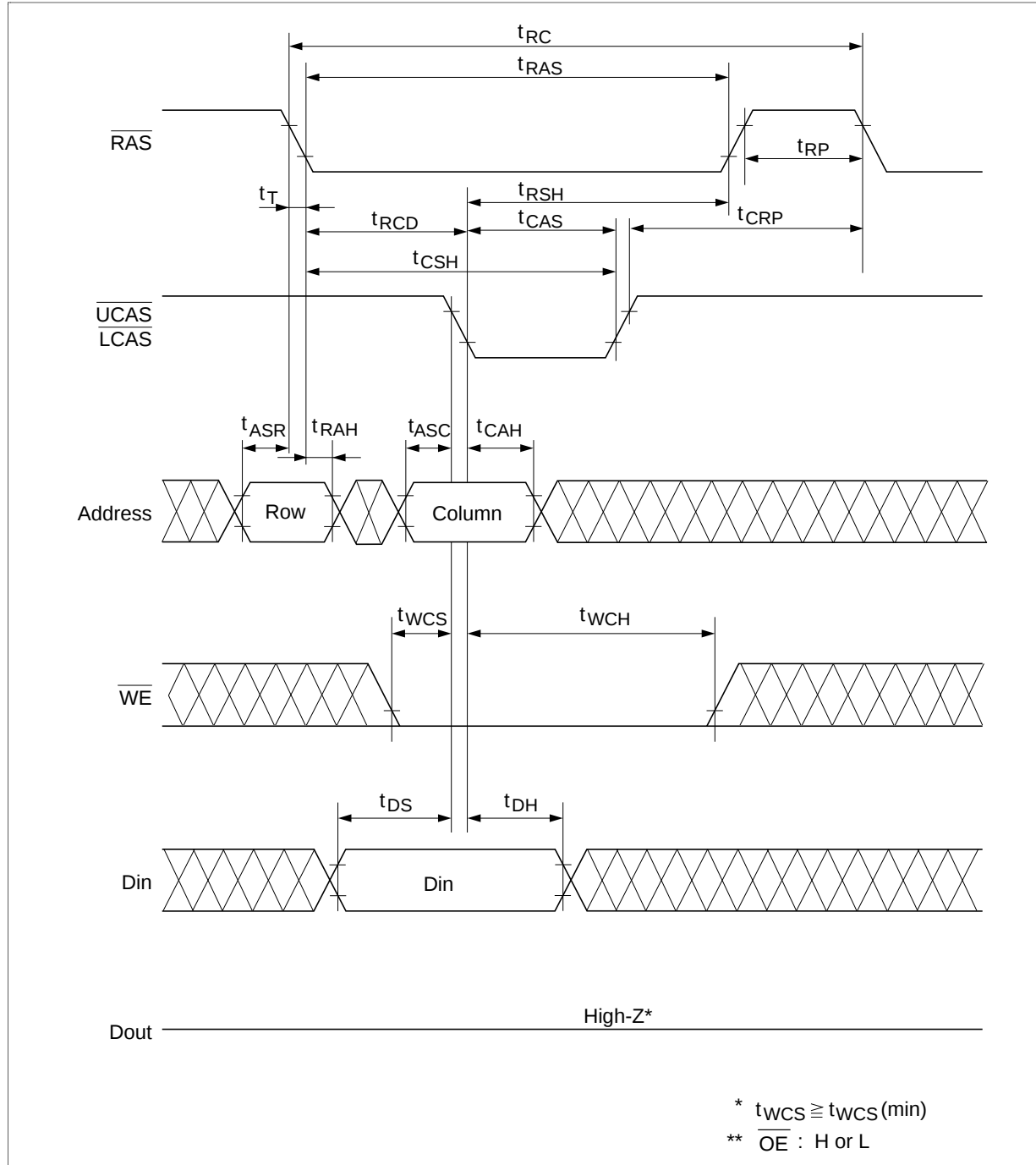
HM514265C, HM51S4265C Series

Timing Waveforms^{*33}

Read Cycle

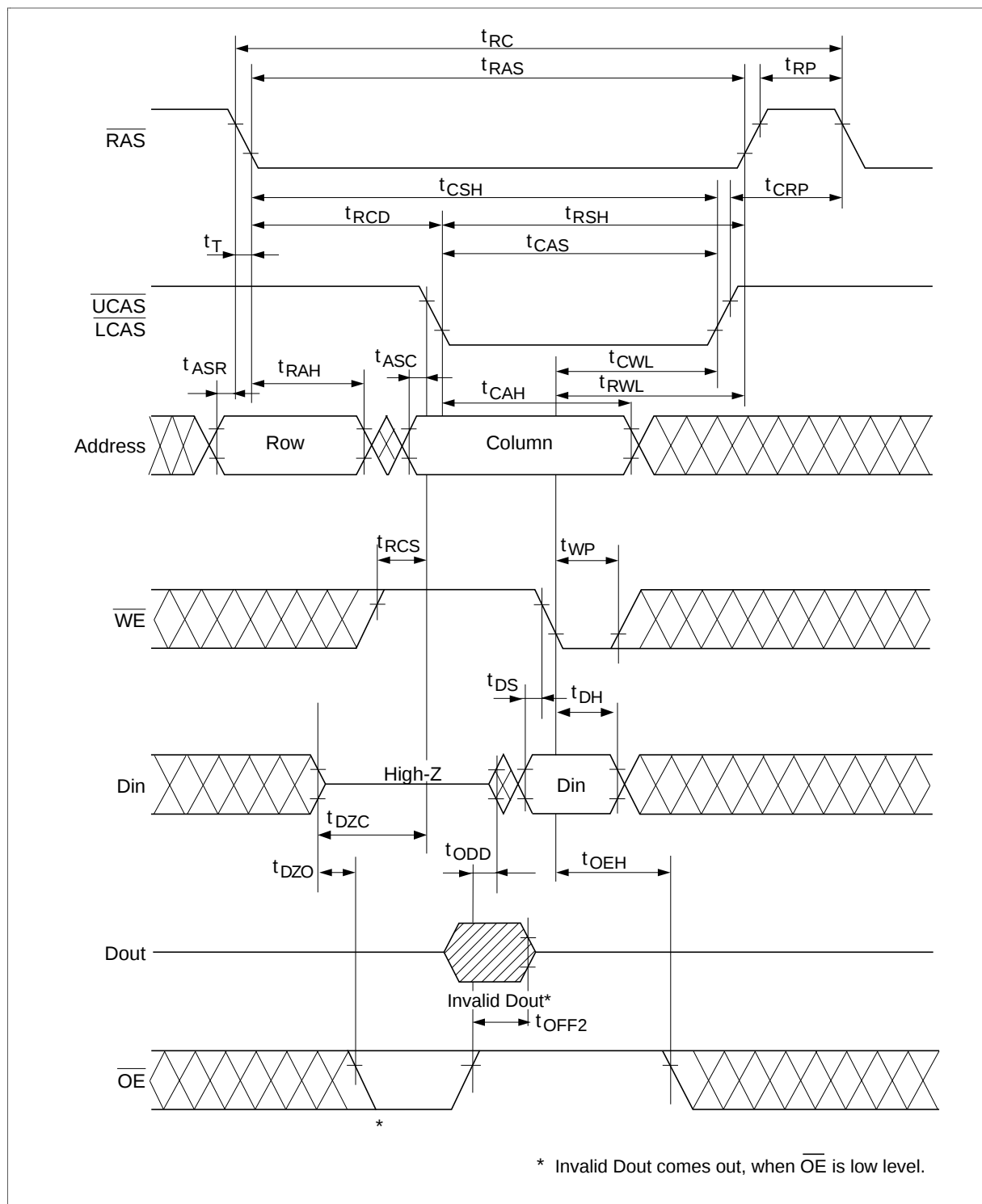


Early Write Cycle

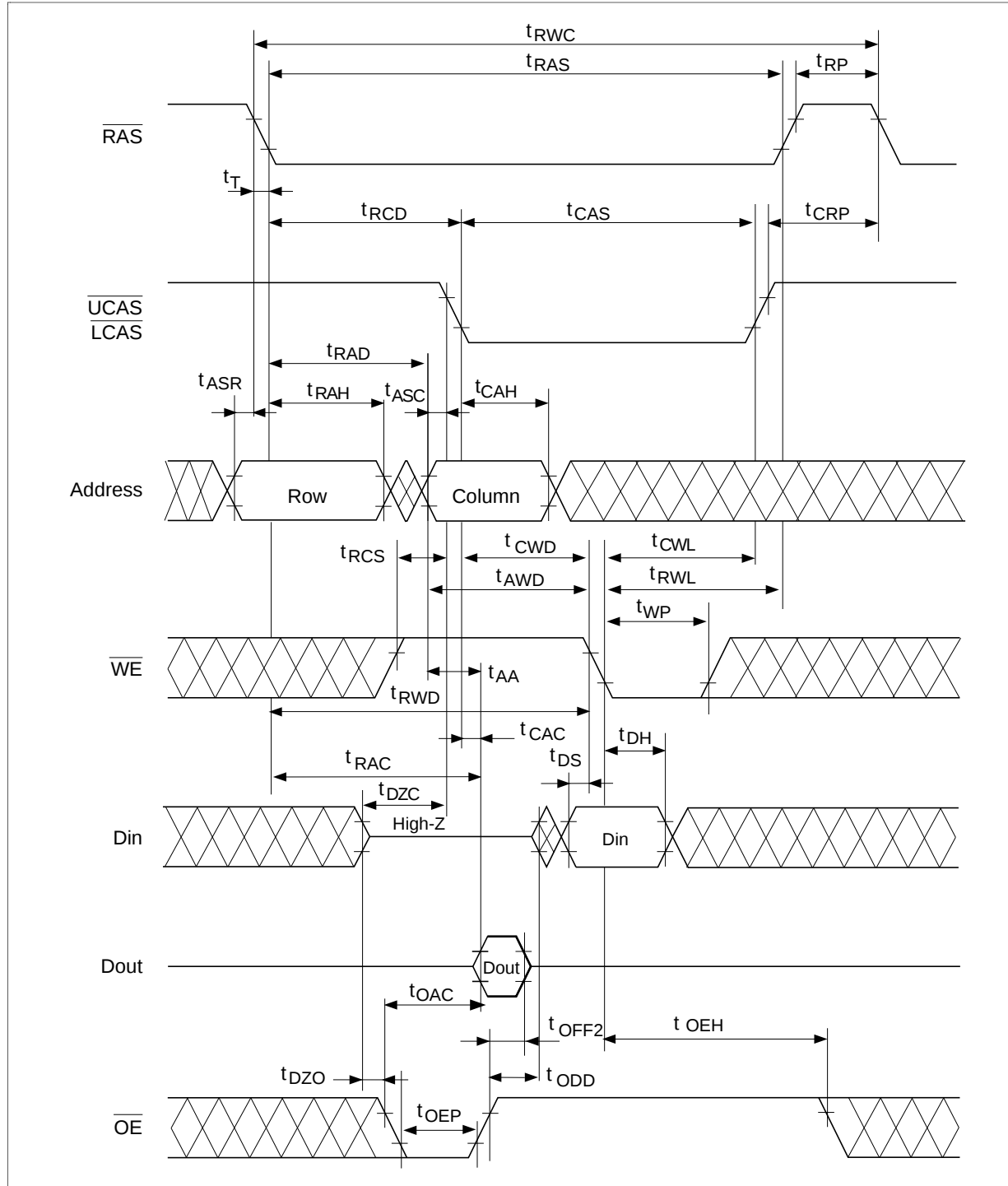


HM514265C, HM51S4265C Series

Delayed Write Cycle

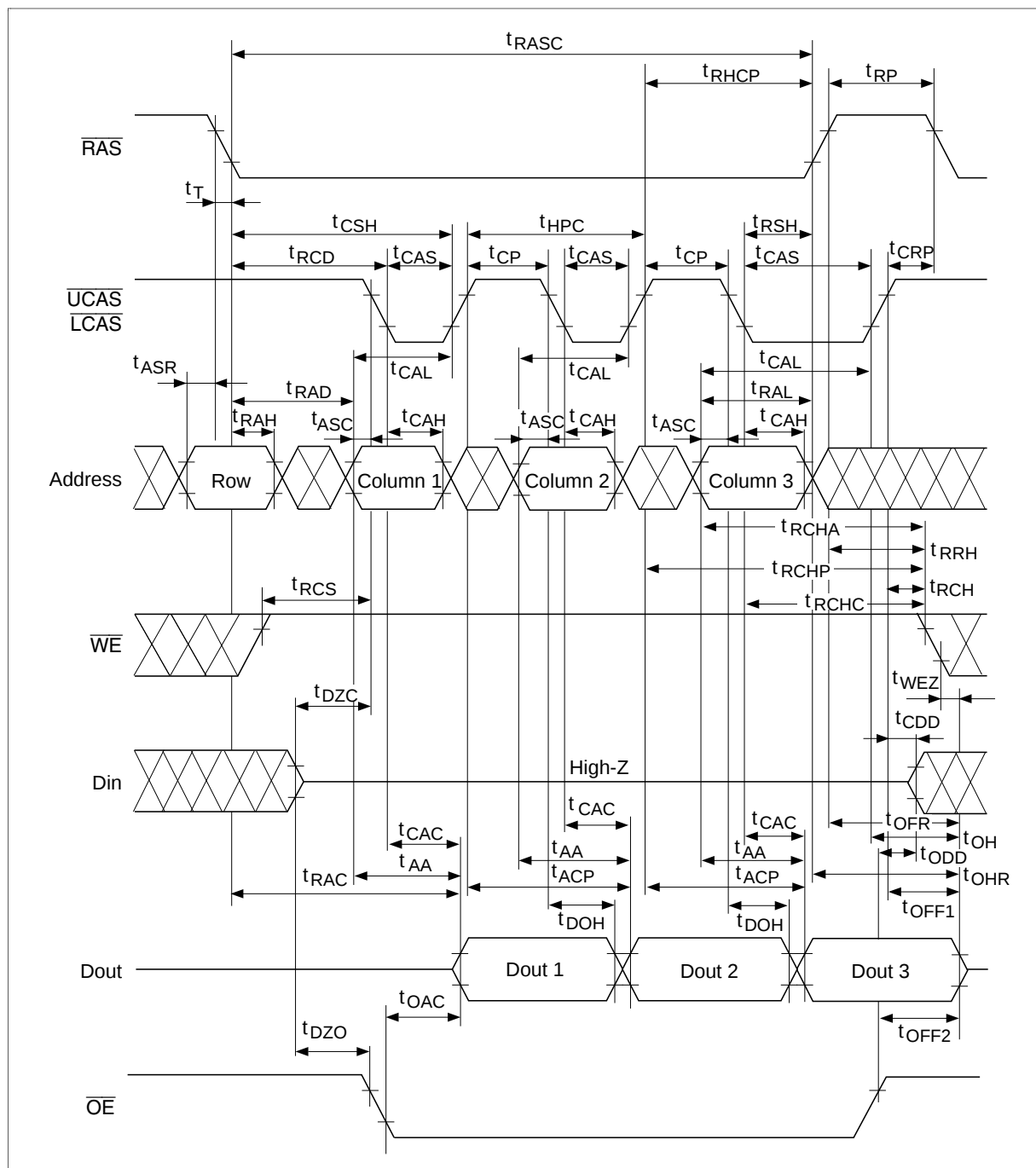


Read-Modify-Write Cycle



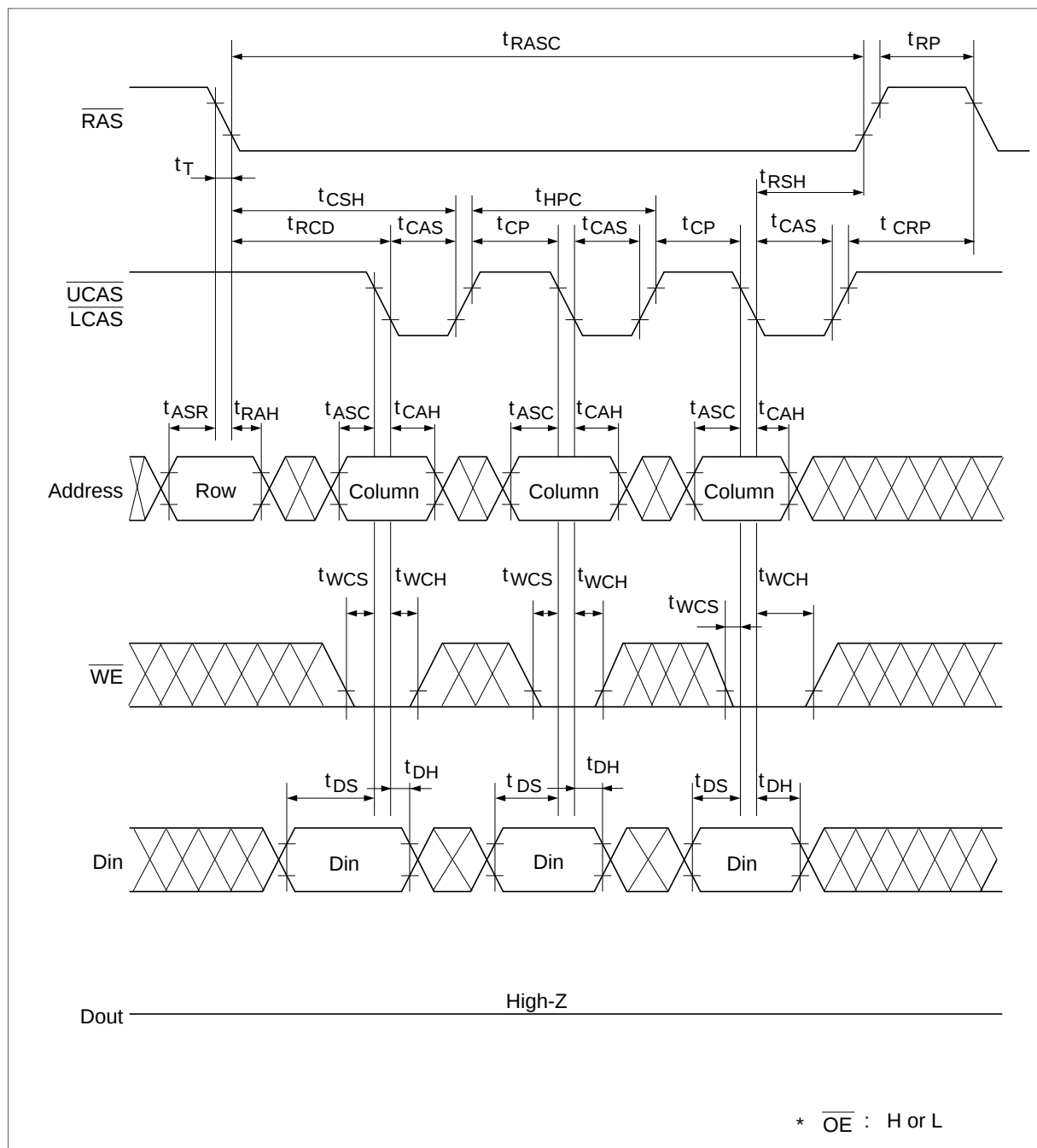
HM514265C, HM51S4265C Series

EDO Page Mode Read Cycle (t_{HPC} minimum cycle operation)

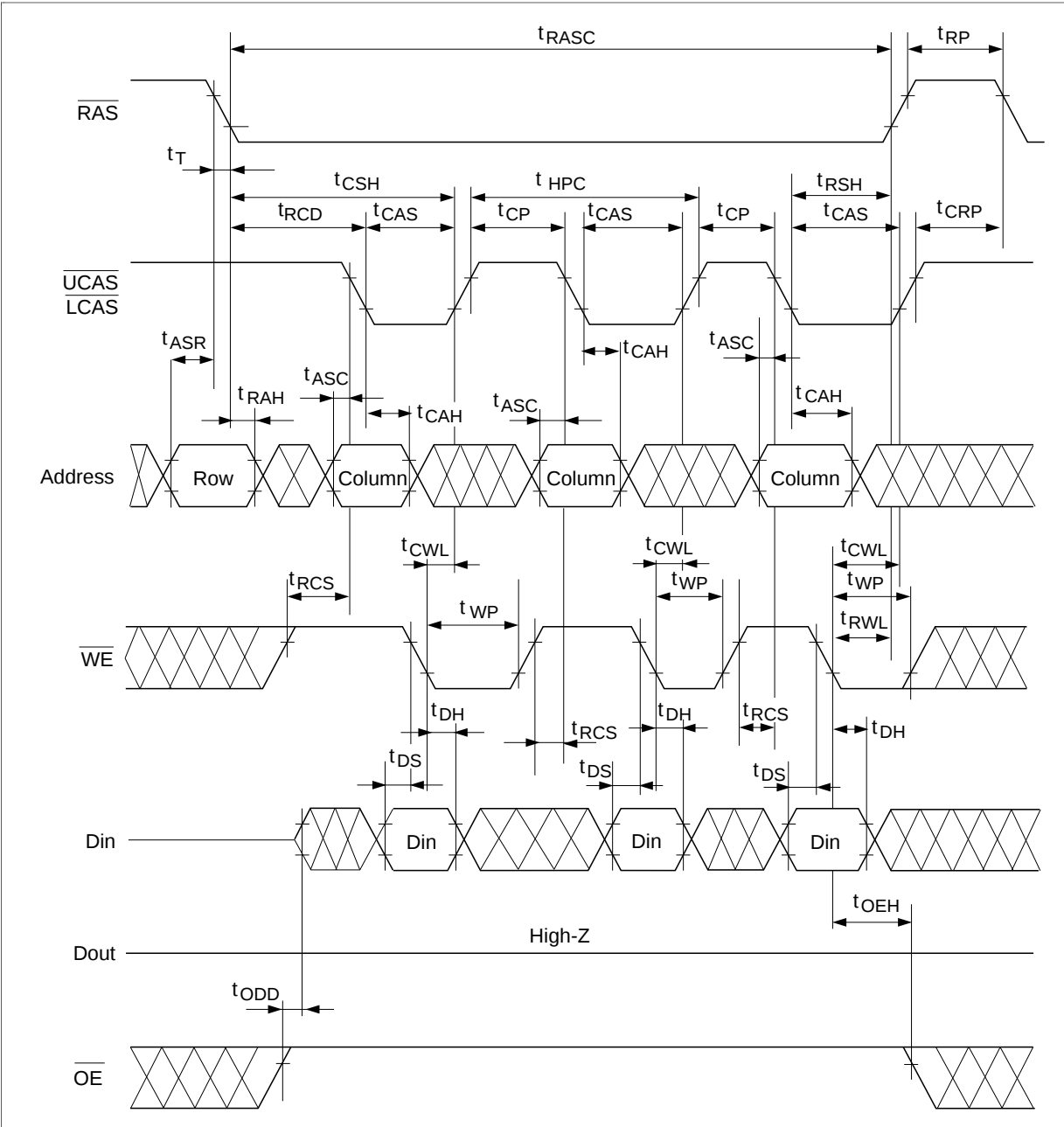


HM514265C, HM51S4265C Series

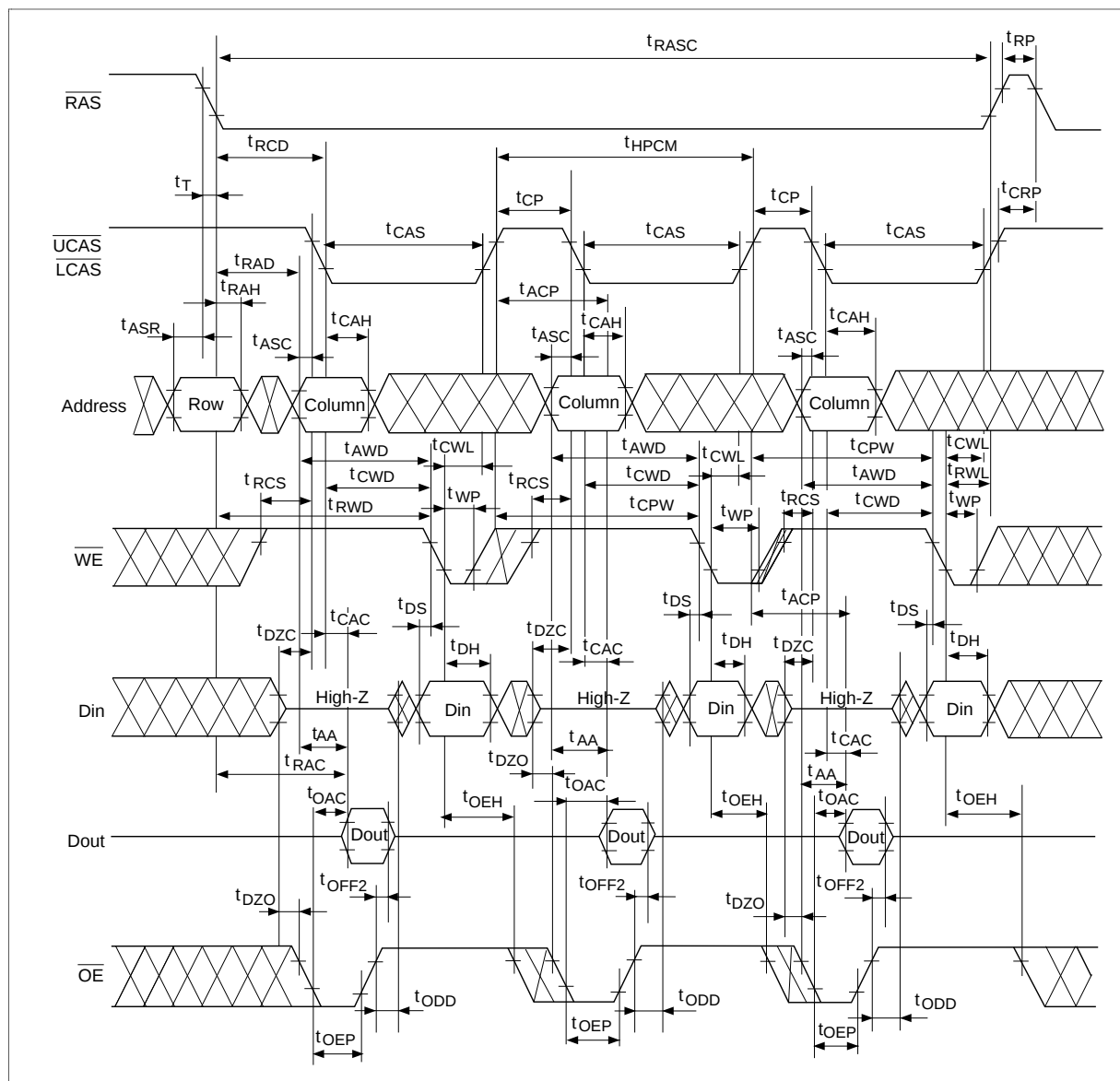
EDO Page Mode Early Write Cycle (t_{HPC} minimum cycle operation)



EDO Page Mode Delayed Write Cycle

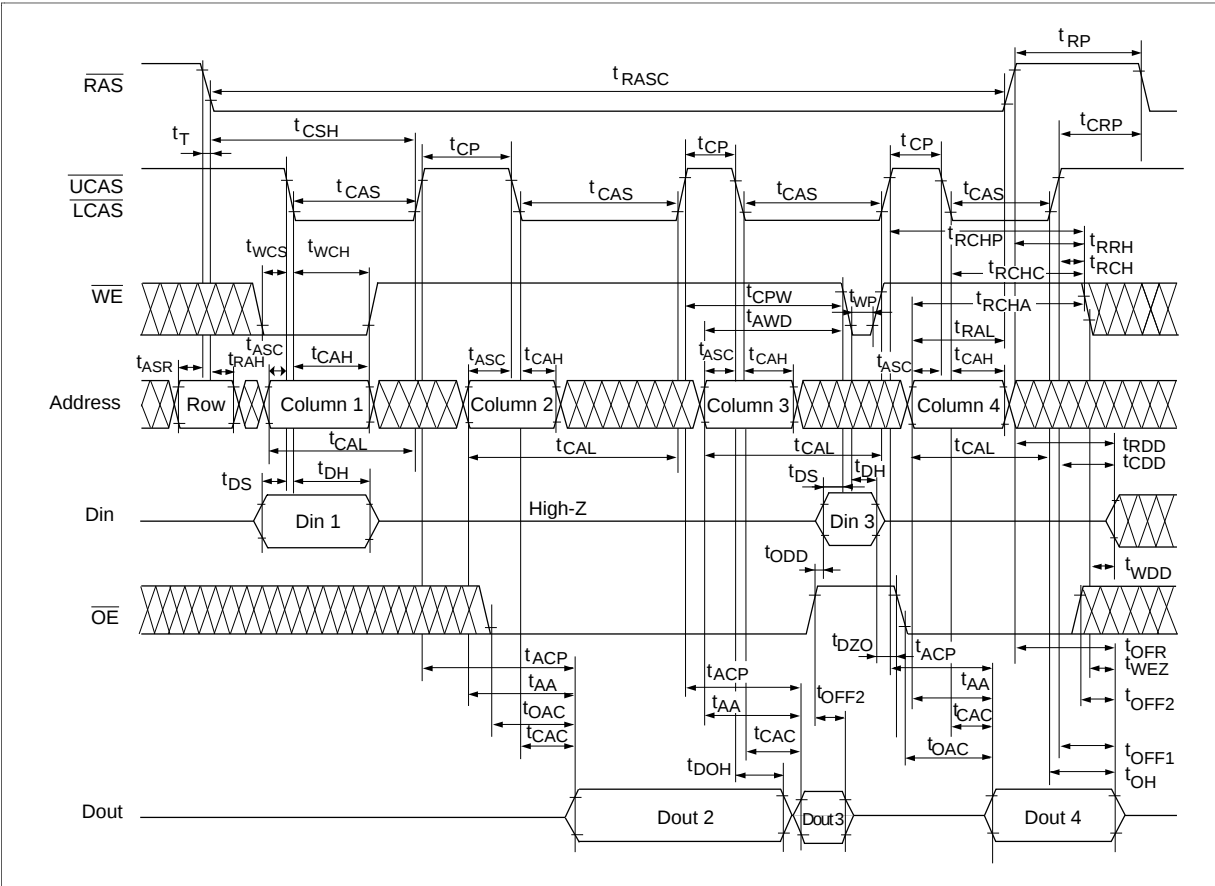


EDO Page Mode Read-Modify-Write Cycle

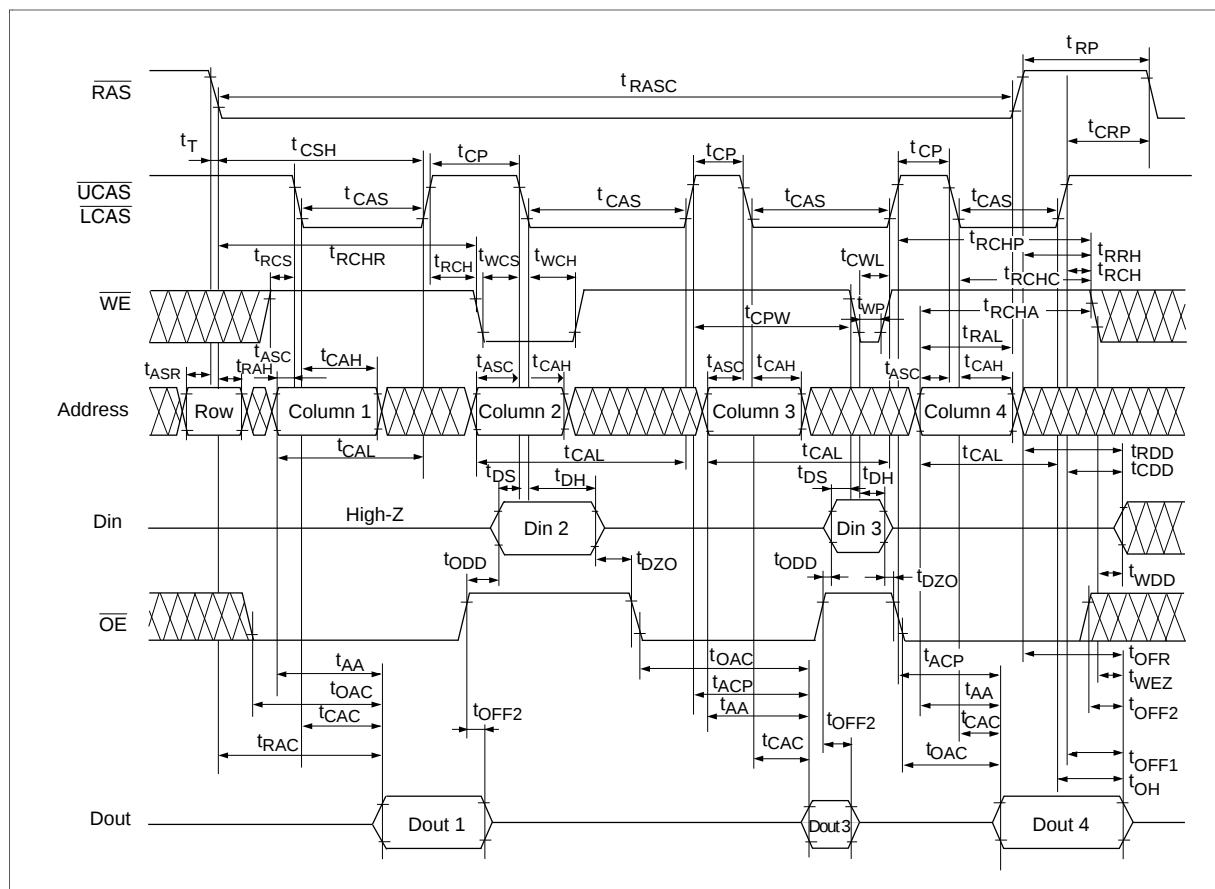


HM514265C, HM51S4265C Series

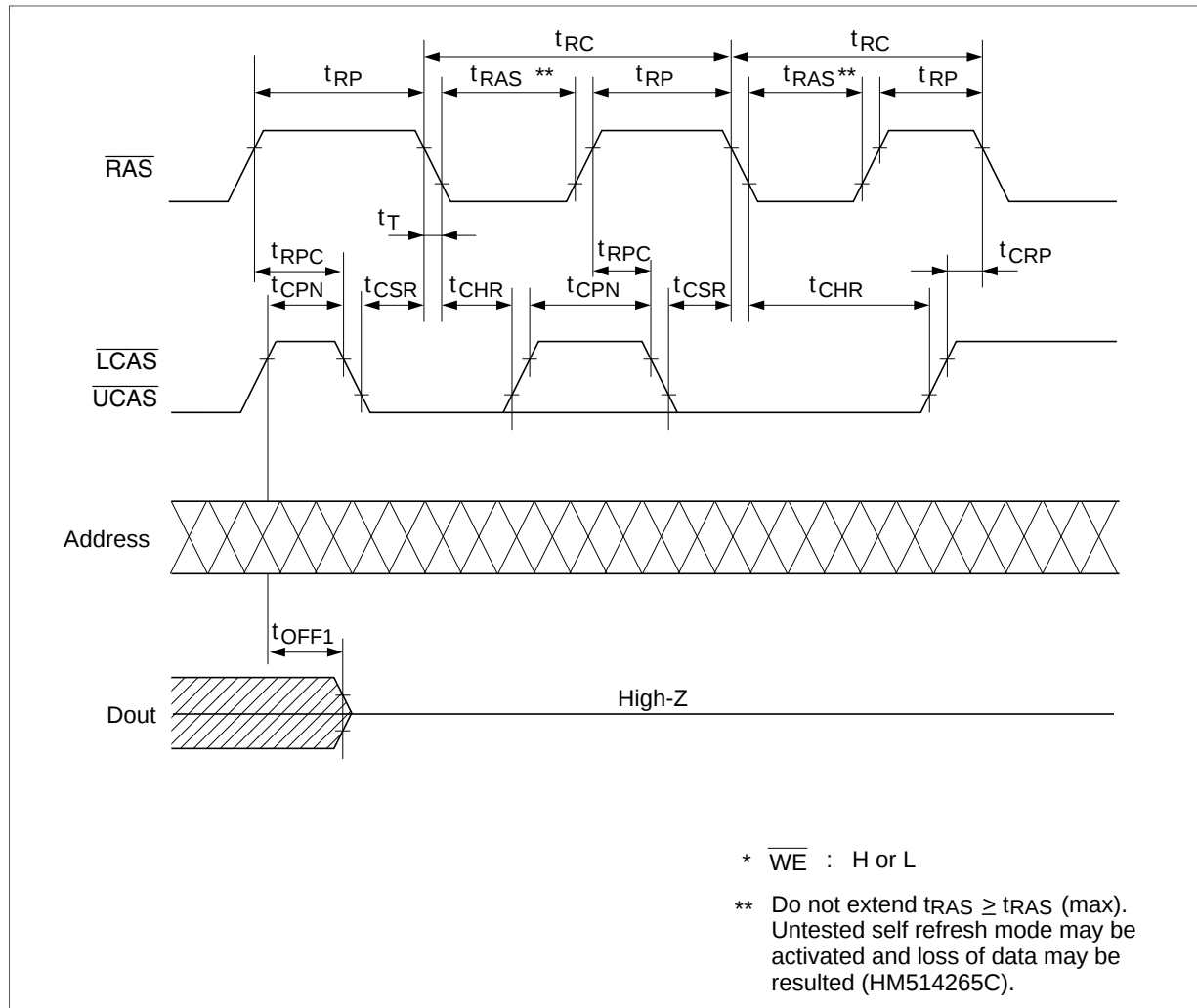
EDO Page Mode Mix Cycle (1)*24



EDO Page Mode Mix Cycle (2)^{*24}

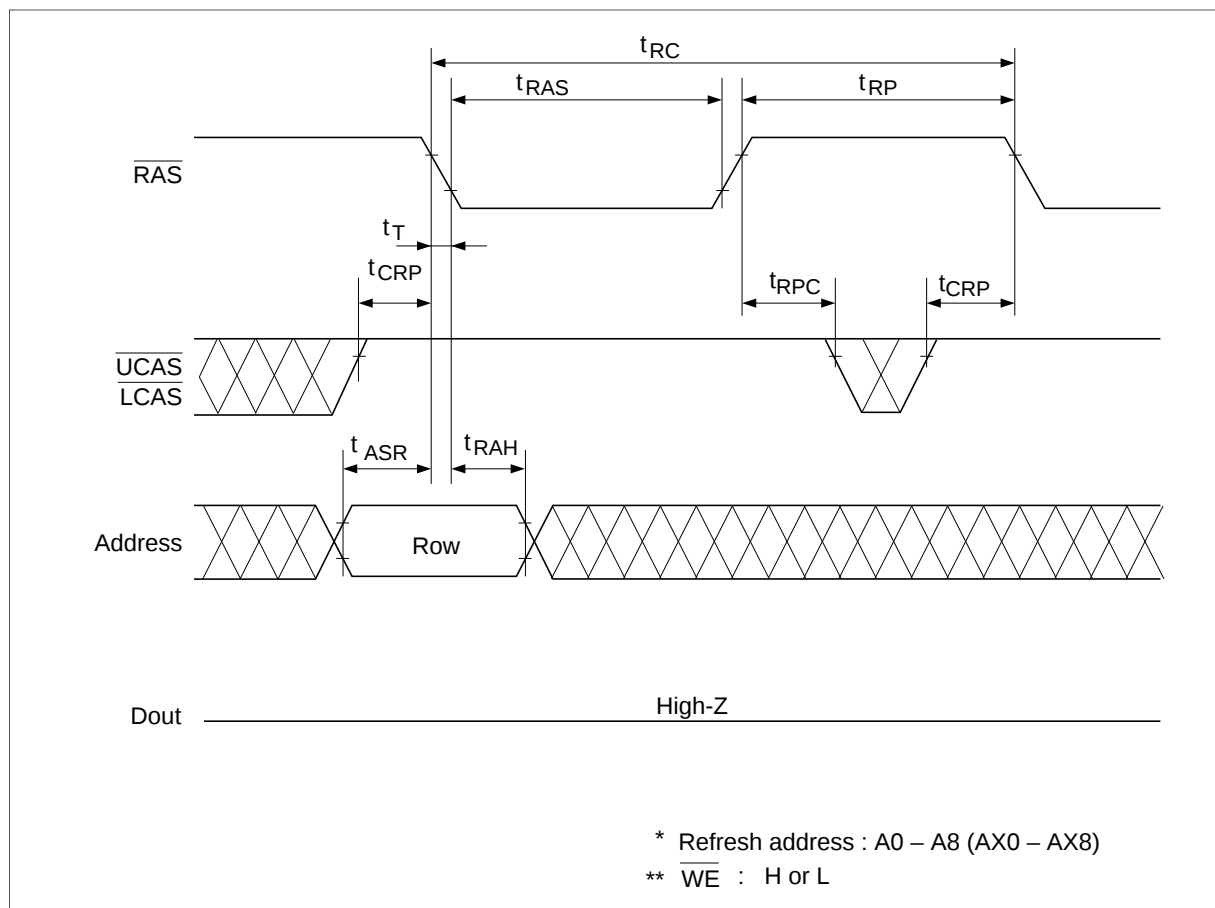


CAS-Before-RAS Refresh Cycle

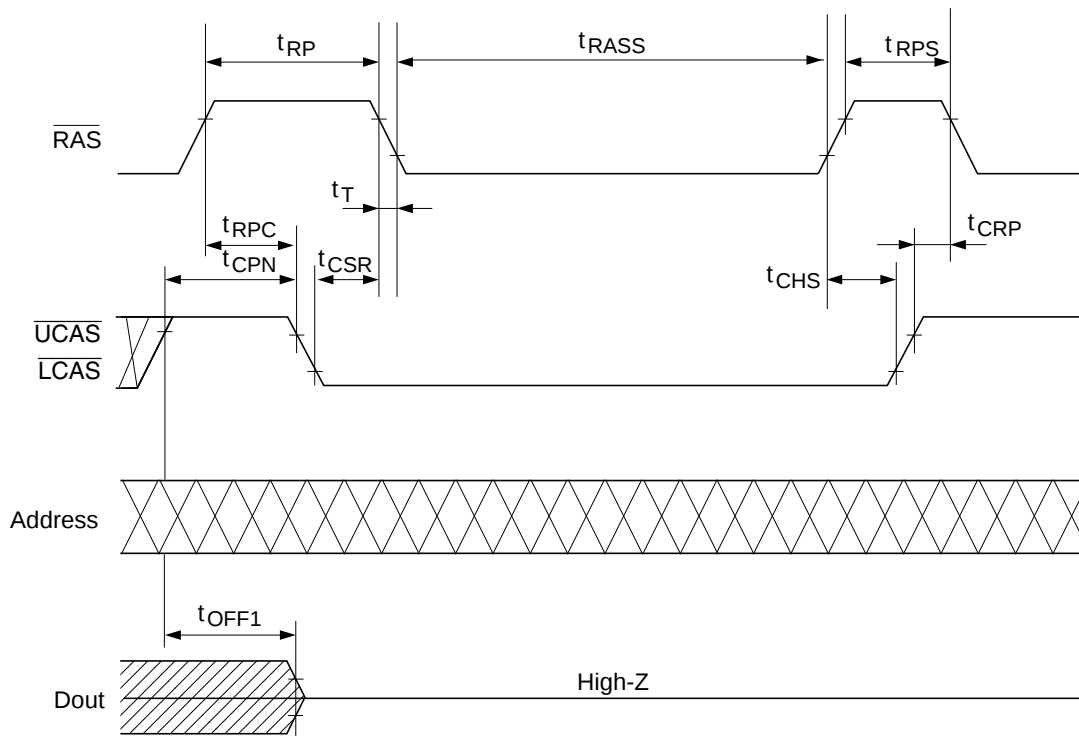


HM514265C, HM51S4265C Series

$\overline{\text{RAS}}$ -Only Refresh Cycle



Self Refresh Cycle



* $\overline{WE}$, $\overline{OE}$: H or L

The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, $10 \mu s \leq t_{RASS} \leq 100 \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100 \mu s$, then RAS precharge time should use t_{RPS} instead of t_{RP} .
2. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with $15.6 \mu s$ interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with $15.6 \mu s$ interval in normal read/write cycle, CBR refresh should be executed within $15.6 \mu s$ immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

HM514265C, HM51S4265C Series

HM514265CTT/CLTT Series (TTP-44/40DB)

Unit: mm

