DESCRIPTION

This family is a 16M bit dynamic RAM organized 16,777,216 x 1-bit configuration with Fast Page mode CMOS DRAMs. Fast Page mode offers high speed random access of memory cells within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(50,60 or 70ns). Package type(SOJ or TSOP-II) and power consumption(Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high band-width, low power consumption and high reliability.

ORDERING INFORMATION

Part Number	Ref.	Power	Pkg.
HY5116100BJ	4K		SOJ
HY5116100BSLJ	4K	SL-part	SOJ
HY5116100BT	4K		TSOP-II
HY5116100BSLT	4K	SL-part	TSOP-II

* Reverse TSOP-II packages are also available

FEATURES

- Part Number Information
  - HY5116100B: 4K Ref.
- Max. Active Power Dissipation

Speed	4K
50	605 mW
60	495 mW
70	440 mW

- Fast access time and cycle time

Speed	tRAC	tCAC	tPC
50ns	50ns	13ns	35ns
60ns	60ns	15ns	40ns
70ns	70ns	18ns	45ns

- Fast Page Mode Operation
- Single power supply of 5.0V ± 10%
- Read-Modify-Write Capability
- Early Write or Output Enable controlled write
- TTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self Refresh Capability
- Refresh cycles

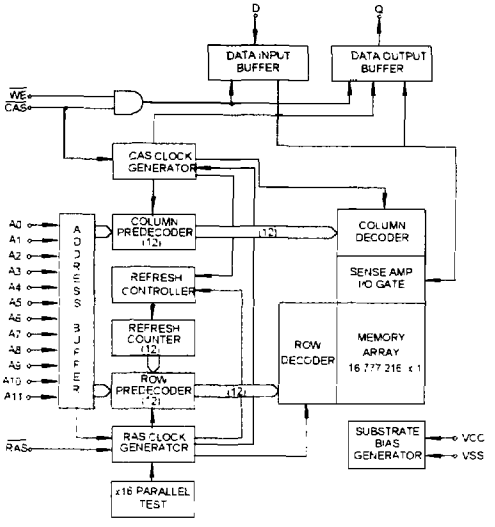
Part No.	Ref.	Normal	SL-part
HY5116100B	4K	64ms	256ms

- JEDEC standard pinout

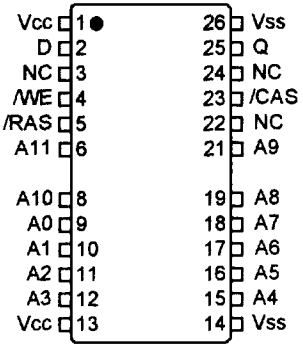
  24/26-pin Plastic SOJ (300 mil)

  24/26-pin Plastic TSOP-II (300mil)

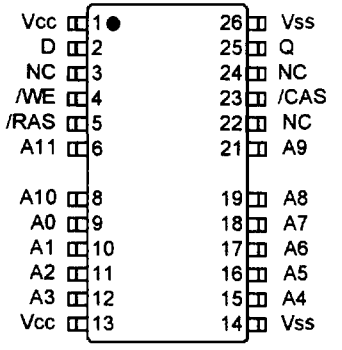
BLOCK DIAGRAM



PIN CONFIGURATION (Marking Side)



24/26-pin Plastic SOJ (300mil)



24/26-pin Plastic TSOP-II (300mil)

PIN DESCRIPTION

/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
A0-A11	Address Inputs
D	Data Input
Q	Data Output
Vcc	Power (+5.0V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	-55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin relative to Vss	-1.0 to 7.0	V
V_{CC}	Voltage on Vcc relative to Vss	-1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	℃ · sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0℃to 70℃)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	Vcc+1.0	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

Note: All voltages are referenced to Vss.

DC CHARACTERISTICS

(T_A=0℃to 70℃, Vcc=5.0V ± 10% and Vss=0V, unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed/ Power	Max. Current	UNIT
I_{CC1}	Operating Current	/RAS and /CAS cycling tRC=tRC (min.)	50 60 70	110 90 80	mA
I_{CC2}	TTL Standby Current	/RAS=/CAS ≥ V_{IH} other inputs ≥ Vss	 SL-part	2 1	mA
I_{CC3}	/RAS-only Refresh Current	/CAS=V_{IH}, /RAS cycling tRC=tRC (min.)	50 60 70	110 90 80	mA
I_{CC4}	Fast Page Mode Current	/RAS=V_{IL}, /CAS, Address cycling tPC=tPC (min.)	50 60 70	80 70 60	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS≥Vcc-0.2V	 SL-part	1 300	mA μA
I_{CC6}	/CAS-before-/RAS Refresh Current	/RAS and /CAS cycling tRC=tRC (min.)	50 60 70	110 90 80	mA
I_{CC7}	Battery Back-up Current (SL-part)	tRC= 62.5μs /CAS = CBR cycling or 0.2V /OE & /WE=Vcc - 0.2V Address =Vcc-0.2V or 0.2V D =Vcc-0.2V, 0.2V or open , Q =open	tRAS≤ 300ns	350	μA
			tRAS≤ 1μs	600	μA
I_{CC8}	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as Icc7		300	μA

Symbol	Parameter	Test condition	Min.	Max.	UNIT
I_{LI}	Input Leakage current (Any Input Pin)	Vss ≤ V_{IN} ≤ Vcc + 1.0 All other pins not under test=Vss	-10	10	μA
I_{LO}	Output Leakage current (Any Input Pin)	Vss ≤ V_{OUT} ≤ Vcc /RAS & /CAS at V_{IH}	-10	10	μA
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -5.0mA	2.4	-	V

NOTE

1. cc1, Icc3, Icc4 and Icc6 depend on output loading and cycle rates(tRC and tPC).
2. Specified values are obtained with outputs unloaded.
3. cc is specified as an average current. In Icc1, Icc3, Icc6, address can be changed only once while /RAS=VIL. In Icc4, address can be changed maximum once while /CAS=V_{IH} within one Fast Page mode cycle time tPC.
4. Only /RAS(max.) = 1μs is applied to refresh of battery backup but tRAS(max.) = 10μs is to applied to normal functional operation.
5. Icc5(max.) = 300μA, Icc7 and Icc8 are applied to SL-part only.

AC CHARACTERISTICS

(T_A=0℃ to 70℃, Vcc=5.0V ± 10% and Vss=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY5116100B						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	110	-	130	-	155	-	ns	
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	55	-	60	-	70	-	ns	
5	tRAC	Access Time from /RAS	-	50	-	60	-	70	ns	4,5,6
6	tCAC	Access Time from /CAS	-	13	-	15	-	18	ns	4,5
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,6
8	tCPA	Access Time from Column Precharge	-	30	-	35	-	40	ns	4,9
9	tCLZ	/CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Out Buffer Turn-Off Delay Time	0	10	0	13	0	15	ns	7
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	2
12	tRP	/RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	/RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	/RAS Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	/RAS Hold Time	13	-	15	-	18	-	ns	
16	tCSH	/CAS Hold Time	50	-	60	-	70	-	ns	
17	tCAS	/CAS Pulse Width	13	10K	15	10K	18	10K	ns	
18	tRCD	/RAS to /CAS Delay Time	18	37	20	45	20	52	ns	5
19	tRAD	/RAS to Column Address Delay Time	13	25	15	30	15	35	ns	6
20	tCRP	/CAS to /RAS Precharge Time	5	-	5	-	5	-	ns	10
21	tCP	/CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	10	-	ns	
26	tRAL	Column Address to /RAS Lead Time	25	-	30	-	35	-	ns	
27	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
28	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	8
29	tRRH	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	8
30	tWCH	Write Command Hold Time	8	-	10	-	10	-	ns	
31	tWP	Write Command Pulse Width	8	-	10	-	10	-	ns	
32	tRWL	Write Command to /RAS Lead Time	13	-	15	-	18	-	ns	
33	tCWL	Write Command to /CAS Lead Time	13	-	15	-	18	-	ns	
34	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	9
35	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	9

AC CHARACTERISTICS

(Continued)

#	SYMBOL	PARAMETER	HY5116100B						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	tREF	Refresh Period (4096 cycles)	64	-,	64	-	64	-	ms	
		Refresh Period (SL-part)	256	-	256	-	256	-	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	10
38	tCWD	/CAS to /WE Delay Time	13	-	15	-	20	-	ns	10
39	tRWD	/RAS to /WE Delay Time	50	-	60	-	70	-	ns	10
40	tAWD	Column Address to /WE Delay Time	25	-	30	-	35	-	ns	10
41	tCSR	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	tCHR	/CAS Hold Time (CBR Cycle)	10	-	10	-	15	-	ns	
43	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	
44	tCPT	/CAS Precharge Time (CBR Counter Test)	15	-	20	-	25	-	ns	
45	tCPWD	/WE Delay Time from /CAS Precharge	30	-	35	-	40	-	ns	10
46	tRHCP	/RAS Hold Time from /CAS Precharge	30	-	35	-	40	-	ns	
47	tWRP	/WE to /RAS Precharge Time(CBR cycle)	10	-	10	-	10	-	ns	
48	tWRH	/WE to /RAS Hold Time (CBR cycle)	10	-	10	-	10	-	ns	
49	tRASS	/RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	μs	
50	tRPS	/RAS Precharge Time (Self Refresh)	90	-	110	-	130	-	ns	
51	tCHS	/CAS Hold Time (Self Refresh)	-50	-	-50	-	-50	-	ns	

TEST MODE

#	SYMBOL	PARAMETER	HY5116100B						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	95	-	115	-	135	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	115	-	135	-	160	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	60	-	65	-	75	-	ns	
5	tRAC	Access Time from /RAS	-	55	-	65	-	75	ns	4,5,6
6	tCAC	Access Time from /CAS	-	18	-	20	-	23	ns	4,5
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,6
8	tCPA	Access Time from Column Precharge	-	35	-	40	-	45	ns	4,9
13	tRAS	/RAS Pulse Width	55	10K	65	10K	75	10K	ns	
14	tRASP	/RAS Pulse Width (Fast Page Mode)	55	200K	65	200K	75	200K	ns	
15	tRSH	/RAS Hold Time	18	-	20	-	23	-	ns	
16	tCSH	/CAS Hold Time	55	-	65	-	75	-	ns	
17	tCAS	/CAS Pulse Width	18	10K	20	10K	23	10K	ns	
26	tRAL	Column Address to /RAS Lead Time	30	-	35	-	40	-	ns	
38	tCWD	/CAS to /WE Delay Time	18	-	20	-	25	-	ns	10
39	tRWD	/RAS to /WE Delay Time	55	-	65	-	75	-	ns	10
40	tAWD	Column Address to /WE Delay Time	30	-	35	-	40	-	ns	10
45	tCPWD	/WE Delay Time from /CAS Precharge	35	-	40	-	45	-	ns	10

In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0, A1 and A11 are not used. If, upon reading, all bits are equal (all `1`s or `0`s), the Q pin indicates a `1`. If they are not equal, the Q pin indicates a `0`. The 16M x 1 DRAM can be tested in the same way as a 1M x 1 DRAM is tested.

/WE (when in /CAS-before-/RAS cycle) puts the 16Mx1 DRAM into Test Mode and a /CAS-before-/RAS or a /RAS-only refresh cycle put it back into Normal Mode. /WE (when in /CAS-before-/RAS cycle) shall be used for the refresh operation in the test mode. The Test Mode function reduces test time(1/16 in case of N test pattern).

NOTE

1. An initial pause of 200 μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS only refresh cycles are required.
2. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.)
3. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA = 0 to 70 ℃) is assured.
4. Measured at VOH=2.4V and VOL=0.4V with a load equivalent to 2 TTL loads and 100pF.
5. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC
6. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA
7. tOFF(max.) define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
8. Either tRCH or tRRH must be satisfied for a read cycle..
9. These parameters are referred to /CAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
10. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tCWD ≥ tCWD(min.), tRWD ≥ tRWD(min.) and tCPWD ≥ tCPWD(min.), then the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

CAPACITANCE

(T_A=25 ℃, Vcc=5.0V ± 10%, Vss=0V and f = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0 - A11,D)	-	5	pF
C_{IN2}	Input Capacitance (/RAS, /CAS, /WE)	-	7	pF
C_{OUT}	Output Capacitance (Q)	-	7	pF