



## 3.3V CMOS 12-BIT SYNCHRONOUS BUS EXCHANGER WITH BUS-HOLD

IDT74ALVCH16276

### FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{SK(0)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;  
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,  
and 0.40mm pitch TVSOP packages
- Extended commercial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ , Normal Range
- $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4 $\mu\text{W}$  typ. static)
- Rail-to-Rail output swing for increased noise margin

### Drive Features for ALVCH16276:

- High Output Drivers:  $\pm 24\text{mA}$
- Suitable for heavy loads

### APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

### DESCRIPTION:

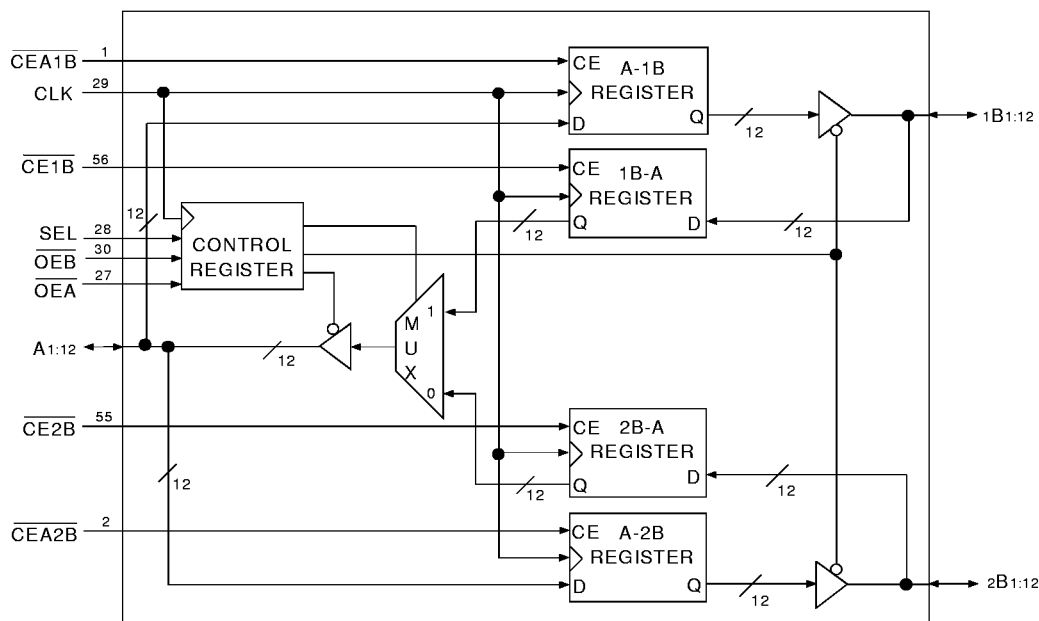
This 12-bit synchronous bus exchanger is built using dual metal CMOS technology. The ALVCH16276 device is a high-speed, bidirectional, 12-bit, registered, bus multiplexer for use in synchronous memory interleaving applications. All registers have a common clock and use a clock enable ( $\overline{\text{CE}}_{\text{xxx}}$ ) on each data register to control data sequencing. The output enables and mux select ( $\overline{\text{OE}}_{\text{A}}$ ,  $\overline{\text{OE}}_{\text{B}}$  and SEL) are also under synchronous control allowing direction changes to be edge triggered events.

The ALVCH16276 has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The clock enable ( $\overline{\text{CE}}_{1\text{B}}$ ,  $\overline{\text{CE}}_{2\text{B}}$ ,  $\overline{\text{CE}}_{\text{A1B}}$  and  $\overline{\text{CE}}_{\text{A2B}}$ ) inputs control data storage. Both B ports have a common output enable ( $\overline{\text{OE}}_{\text{B}}$ ) to aid in synchronously loading the B registers from the B port.

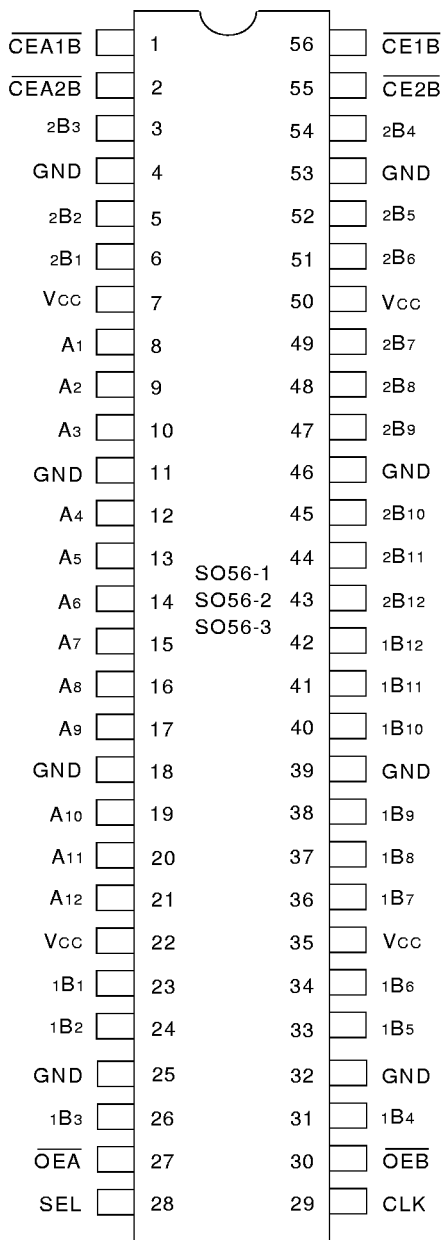
The ALVCH16276 has been designed with a  $\pm 24\text{mA}$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16276 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

### Functional Block Diagram



## PIN CONFIGURATION



**SSOP/  
TSSOP/TVSOP  
TOP VIEW**

## ABSOLUTE MAXIMUM RATING (1)

| Symbol                             | Description                                                          | Max.               | Unit |
|------------------------------------|----------------------------------------------------------------------|--------------------|------|
| VTERM <sup>(2)</sup>               | Terminal Voltage with Respect to GND                                 | – 0.5 to + 4.6     | V    |
| VTERM <sup>(3)</sup>               | Terminal Voltage with Respect to GND                                 | – 0.5 to VCC + 0.5 | V    |
| TSTG                               | Storage Temperature                                                  | – 65 to + 150      | °C   |
| IOUT                               | DC Output Current                                                    | – 50 to + 50       | mA   |
| I <sub>IK</sub>                    | Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > VCC | ± 50               | mA   |
| I <sub>OK</sub>                    | Continuous Clamp Current, V <sub>O</sub> < 0                         | – 50               | mA   |
| I <sub>CC</sub><br>I <sub>SS</sub> | Continuous Current through each VCC or GND                           | ± 100              | mA   |

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- All terminals except VCC.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

| Symbol           | Parameter <sup>(1)</sup> | Conditions            | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 5    | 7    | pF   |
| C <sub>OUT</sub> | Output Capacitance       | V <sub>OUT</sub> = 0V | 7    | 9    | pF   |
| C <sub>I/O</sub> | I/O Port Capacitance     | V <sub>IN</sub> = 0V  | 7    | 9    | pF   |

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### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

| Pin Names                 | I/O | Description                                                                                                                                                                                                   |
|---------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Ax(1:12)                  | I/O | Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. <sup>(1)</sup>                                                                                                                    |
| 1Bx(1:12)                 | I/O | Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory. <sup>(1)</sup>                                                                                                         |
| 2Bx(1:12)                 | I/O | Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory. <sup>(1)</sup>                                                                                                           |
| CLK                       | I   | Clock Input                                                                                                                                                                                                   |
| $\overline{\text{CEA1B}}$ | I   | Clock Enable Input for the A-1B Register. If $\overline{\text{CEA1B}}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).                                            |
| $\overline{\text{CEA2B}}$ | I   | Clock Enable Input for the A-2B Register. If $\overline{\text{CEA2B}}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).                                            |
| $\overline{\text{CE1B}}$  | I   | Clock Enable Input for the 1B-A Register. If $\overline{\text{CE1B}}$ is LOW during the rising edge of CLK, data will be clocked into register 1B-A (Active LOW).                                             |
| $\overline{\text{CE2B}}$  | I   | Clock Enable Input for the 2B-A Register. If $\overline{\text{CE2B}}$ is LOW during the rising edge of CLK, data will be clocked into register 2B-A (Active LOW).                                             |
| SEL                       | I   | 1B or 2B Port Selection. When HIGH during the rising edge of CLK, SEL enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, SEL enables data transfer from 2B Port to A Port. |
| $\overline{\text{OEA}}$   | I   | Synchronous Output Enable for A Port (Active LOW).                                                                                                                                                            |
| $\overline{\text{OEB}}$   | I   | Synchronous Output Enable for 1B Port and 2B Port (Active LOW).                                                                                                                                               |

### NOTE:

1. These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLES<sup>(1)</sup>

| Inputs |     |     |                          |                          |                         |     | Output            |
|--------|-----|-----|--------------------------|--------------------------|-------------------------|-----|-------------------|
| 1Bx    | 2Bx | SEL | $\overline{\text{CE1B}}$ | $\overline{\text{CE2B}}$ | $\overline{\text{OEA}}$ | CLK | Ax                |
| H      | X   | H   | L                        | X                        | L                       | —   | H                 |
| L      | X   | H   | L                        | X                        | L                       | —   | L                 |
| X      | X   | H   | H                        | X                        | L                       | —   | Ao <sup>(2)</sup> |
| X      | H   | L   | X                        | L                        | L                       | —   | H                 |
| X      | L   | L   | X                        | L                        | L                       | —   | L                 |
| X      | X   | L   | X                        | H                        | L                       | —   | Ao <sup>(2)</sup> |
| X      | X   | X   | X                        | X                        | H                       | —   | Z                 |

| Inputs |                           |                           |                         |     | Outputs           |                   |
|--------|---------------------------|---------------------------|-------------------------|-----|-------------------|-------------------|
| Ax     | $\overline{\text{CEA1B}}$ | $\overline{\text{CEA2B}}$ | $\overline{\text{OEB}}$ | CLK | 1Bx               | 2Bx               |
| H      | L                         | L                         | L                       | —   | H                 | H                 |
| L      | L                         | L                         | L                       | —   | L                 | L                 |
| H      | L                         | H                         | L                       | —   | H                 | Bo <sup>(2)</sup> |
| L      | L                         | H                         | L                       | —   | L                 | Bo <sup>(2)</sup> |
| H      | H                         | L                         | L                       | —   | Bo <sup>(2)</sup> | H                 |
| L      | H                         | L                         | L                       | —   | Bo <sup>(2)</sup> | L                 |
| X      | H                         | H                         | L                       | —   | Bo <sup>(2)</sup> | Bo <sup>(2)</sup> |
| X      | X                         | X                         | H                       | —   | Z                 | Z                 |
| X      | X                         | X                         | L                       | —   | Active            | Active            |

### NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance
- Output level before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40 °C to +85 °C

| Symbol           | Parameter                                              | Test Conditions                                                                |                                  | Min. | Typ. <sup>(1)</sup> | Max.  | Unit |
|------------------|--------------------------------------------------------|--------------------------------------------------------------------------------|----------------------------------|------|---------------------|-------|------|
| V <sub>IH</sub>  | Input HIGH Voltage Level                               | V <sub>CC</sub> = 2.3V to 2.7V                                                 |                                  | 1.7  | —                   | —     | V    |
|                  |                                                        | V <sub>CC</sub> = 2.7V to 3.6V                                                 |                                  | 2    | —                   | —     |      |
| V <sub>IL</sub>  | Input LOW Voltage Level                                | V <sub>CC</sub> = 2.3V to 2.7V                                                 |                                  | —    | —                   | 0.7   | V    |
|                  |                                                        | V <sub>CC</sub> = 2.7V to 3.6V                                                 |                                  | —    | —                   | 0.8   |      |
| I <sub>IH</sub>  | Input HIGH Current                                     | V <sub>CC</sub> = 3.6V                                                         | V <sub>I</sub> = V <sub>CC</sub> | —    | —                   | ± 5   | μA   |
| I <sub>IL</sub>  | Input LOW Current                                      | V <sub>CC</sub> = 3.6V                                                         | V <sub>I</sub> = GND             | —    | —                   | ± 5   |      |
| I <sub>OZH</sub> | High Impedance Output Current<br>(3-State Output pins) | V <sub>CC</sub> = 3.6V                                                         | V <sub>O</sub> = V <sub>CC</sub> | —    | —                   | ± 10  | μA   |
| I <sub>OZL</sub> |                                                        |                                                                                | V <sub>O</sub> = GND             | —    | —                   | ± 10  | μA   |
| V <sub>IK</sub>  | Clamp Diode Voltage                                    | V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = – 18mA                               |                                  | —    | – 0.7               | – 1.2 | V    |
| V <sub>H</sub>   | Input Hysteresis                                       | V <sub>CC</sub> = 3.3V                                                         |                                  | —    | 100                 | —     | mV   |
| I <sub>CCL</sub> | Quiescent Power Supply Current                         | V <sub>CC</sub> = 3.6V                                                         |                                  | —    | 0.1                 | 40    | μA   |
| I <sub>CCH</sub> |                                                        | V <sub>IN</sub> = GND or V <sub>CC</sub>                                       |                                  |      |                     |       |      |
| I <sub>CCZ</sub> |                                                        |                                                                                |                                  |      |                     |       |      |
| ΔI <sub>CC</sub> | Quiescent Power Supply Current Variation               | One input at V <sub>CC</sub> – 0.6V,<br>other inputs at V <sub>CC</sub> or GND |                                  | —    | —                   | 750   | μA   |

### NOTE:

1. Typical values are at V<sub>CC</sub> = 3.3V, +25 °C ambient.

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## BUS-HOLD CHARACTERISTICS

| Symbol            | Parameter <sup>(1)</sup>         | Test Conditions        |                            | Min. | Typ. <sup>(2)</sup> | Max.  | Unit |
|-------------------|----------------------------------|------------------------|----------------------------|------|---------------------|-------|------|
| I <sub>BHH</sub>  | Bus-Hold Input Sustain Current   | V <sub>CC</sub> = 3.0V | V <sub>I</sub> = 2.0V      | – 75 | —                   | —     | μA   |
| I <sub>BHL</sub>  |                                  |                        | V <sub>I</sub> = 0.8V      | 75   | —                   | —     |      |
| I <sub>BHH</sub>  | Bus-Hold Input Sustain Current   | V <sub>CC</sub> = 2.3V | V <sub>I</sub> = 1.7V      | – 45 | —                   | —     | μA   |
| I <sub>BHL</sub>  |                                  |                        | V <sub>I</sub> = 0.7V      | 45   | —                   | —     |      |
| I <sub>BHHO</sub> | Bus-Hold Input Overdrive Current | V <sub>CC</sub> = 3.6V | V <sub>I</sub> = 0 to 3.6V | —    | —                   | ± 500 | μA   |
| I <sub>BHLO</sub> |                                  |                        |                            |      |                     |       |      |

### NOTES:

1. Pins with Bus-hold are identified in the pin description.

2. Typical values are at V<sub>CC</sub> = 3.3V, +25 °C ambient.

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## OUTPUT DRIVE CHARACTERISTICS

| Symbol          | Parameter           | Test Conditions <sup>(1)</sup> |                           | Min.                  | Max. | Unit |
|-----------------|---------------------|--------------------------------|---------------------------|-----------------------|------|------|
| V <sub>OH</sub> | Output HIGH Voltage | V <sub>CC</sub> = 2.3V to 3.6V | I <sub>OH</sub> = - 0.1mA | V <sub>CC</sub> - 0.2 | —    | V    |
|                 |                     | V <sub>CC</sub> = 2.3V         | I <sub>OH</sub> = - 6mA   | 2                     | —    |      |
|                 |                     | V <sub>CC</sub> = 2.3V         | I <sub>OH</sub> = - 12mA  | 1.7                   | —    |      |
|                 |                     | V <sub>CC</sub> = 2.7V         |                           | 2.2                   | —    |      |
|                 |                     | V <sub>CC</sub> = 3.0V         |                           | 2.4                   | —    |      |
|                 |                     | V <sub>CC</sub> = 3.0V         | I <sub>OH</sub> = - 24mA  | 2                     | —    |      |
| V <sub>OL</sub> | Output LOW Voltage  | V <sub>CC</sub> = 2.3V to 3.6V | I <sub>OL</sub> = 0.1mA   | —                     | 0.2  | V    |
|                 |                     | V <sub>CC</sub> = 2.3V         | I <sub>OL</sub> = 6mA     | —                     | 0.4  |      |
|                 |                     |                                | I <sub>OL</sub> = 12mA    | —                     | 0.7  |      |
|                 |                     | V <sub>CC</sub> = 2.7V         | I <sub>OL</sub> = 12mA    | —                     | 0.4  |      |
|                 |                     | V <sub>CC</sub> = 3.0V         | I <sub>OL</sub> = 24mA    | —                     | 0.55 |      |

### NOTE:

- V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = - 40°C to + 85°C.

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## OPERATING CHARACTERISTICS, T<sub>A</sub> = 25°C

| Symbol | Parameter                                         | Test Conditions                 | V <sub>CC</sub> = 2.5V ± 0.2V | V <sub>CC</sub> = 3.3V ± 0.3V | Unit |
|--------|---------------------------------------------------|---------------------------------|-------------------------------|-------------------------------|------|
|        |                                                   |                                 | Typical                       | Typical                       |      |
| CPD    | Power Dissipation Capacitance<br>Outputs enabled  | C <sub>L</sub> = 0pF, f = 10Mhz | 55                            | 59                            | pF   |
| CPD    | Power Dissipation Capacitance<br>Outputs disabled |                                 | 46                            | 49                            | pF   |

## SWITCHING CHARACTERISTICS <sup>(1)</sup>

| Symbol                               | Parameter                                                                                                                                                                                                                                                 | V <sub>CC</sub> = 2.5V ± 0.2V |      | V <sub>CC</sub> = 2.7V |      | V <sub>CC</sub> = 3.3V ± 0.3V |      | Unit |
|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|------|------------------------|------|-------------------------------|------|------|
|                                      |                                                                                                                                                                                                                                                           | Min.                          | Max. | Min.                   | Max. | Min.                          | Max. |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>CLK to 1Bx or CLK to 2Bx                                                                                                                                                                                                             | 1.5                           | 5    | 1.5                    | 4.7  | 1.5                           | 4.3  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>CLK to Ax, SEL stable and $\overline{\text{CE}}\text{x}\overline{\text{B}}$ enabled                                                                                                                                                  | 1.5                           | 5.3  | 1.5                    | 5    | 1.5                           | 4.6  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>SEL changing and $\overline{\text{CE}}\text{x}\overline{\text{B}}$ disabled                                                                                                                                                          | 1.5                           | 5.7  | 1.5                    | 5.3  | 1.5                           | 5.1  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>SEL changing and $\overline{\text{CE}}\text{x}\overline{\text{B}}$ enabled                                                                                                                                                           | 1.5                           | 5.8  | 1.5                    | 5.4  | 1.5                           | 5.1  | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time<br>CLK to Ax, CLK to 1Bx, or CLK to 2Bx                                                                                                                                                                                                | 1.5                           | 5.6  | 1.5                    | 5.2  | 1.5                           | 5    | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time<br>CLK to Ax, CLK to 1Bx, or CLK to 2Bx                                                                                                                                                                                               | 1.3                           | 4.7  | 1.5                    | 5.2  | 1.5                           | 5    | ns   |
| t <sub>SU</sub>                      | Setup Time, data to CLK, HIGH or LOW                                                                                                                                                                                                                      | 1                             | —    | 1                      | —    | 1                             | —    | ns   |
| t <sub>SU</sub>                      | Setup Time, $\overline{\text{OE}}\text{A}$ to CLK, $\overline{\text{OE}}\text{B}$ to CLK                                                                                                                                                                  | 1                             | —    | 1                      | —    | 1                             | —    | ns   |
| t <sub>SU</sub>                      | Setup Time, SEL to CLK                                                                                                                                                                                                                                    | 1                             | —    | 1                      | —    | 1                             | —    | ns   |
| t <sub>SU</sub>                      | Setup Time, $\overline{\text{CE}}\text{A}1\overline{\text{B}}$ to CLK, $\overline{\text{CE}}\text{1}\overline{\text{B}}$ to CLK<br>$\overline{\text{CE}}\text{2}\overline{\text{B}}$ to CLK, or $\overline{\text{CE}}\text{A}2\overline{\text{B}}$ to CLK | 1                             | —    | 1                      | —    | 1                             | —    | ns   |
| t <sub>H</sub>                       | Hold Time, CLK to data                                                                                                                                                                                                                                    | 1                             | —    | 1                      | —    | 1                             | —    | ns   |
| t <sub>H</sub>                       | Hold Time, CLK to $\overline{\text{OE}}\text{A}$ , CLK to $\overline{\text{OE}}\text{B}$ ,<br>CLK to SEL                                                                                                                                                  | 1                             | —    | 1                      | —    | 1                             | —    | ns   |
| t <sub>H</sub>                       | Hold Time, CLK to $\overline{\text{CE}}\text{A}1\overline{\text{B}}$ , CLK to $\overline{\text{CE}}\text{1}\overline{\text{B}}$ ,<br>CLK to $\overline{\text{CE}}\text{2}\overline{\text{B}}$ , CLK to $\overline{\text{CE}}\text{A}2\overline{\text{B}}$ | 1                             | —    | 1                      | —    | 1                             | —    | ns   |
| t <sub>W</sub>                       | Pulse Width, CLK HIGH                                                                                                                                                                                                                                     | 2.5                           | —    | 2.5                    | —    | 2.5                           | —    | ns   |
| t <sub>SK(o)</sub>                   | Output Skew <sup>(2)</sup>                                                                                                                                                                                                                                | —                             | —    | —                      | —    | —                             | 500  | ps   |

### NOTES:

1. See test circuits and waveforms. T<sub>A</sub> = – 40 °C to + 85 °C.
2. Skew between any two outputs of the same package and switching in the same direction.

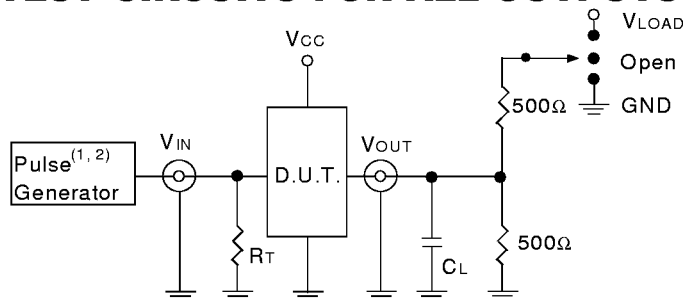
## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

| Symbol            | V <sub>CC</sub> (1)= 3.3V±0.3V | V <sub>CC</sub> (1)= 2.7V | V <sub>CC</sub> (2)= 2.5V±0.2V | Unit |
|-------------------|--------------------------------|---------------------------|--------------------------------|------|
| V <sub>LOAD</sub> | 6                              | 6                         | 2 x V <sub>CC</sub>            | V    |
| V <sub>IH</sub>   | 2.7                            | 2.7                       | V <sub>CC</sub>                | V    |
| V <sub>T</sub>    | 1.5                            | 1.5                       | V <sub>CC</sub> / 2            | V    |
| V <sub>LZ</sub>   | 300                            | 300                       | 150                            | mV   |
| V <sub>HZ</sub>   | 300                            | 300                       | 150                            | mV   |
| C <sub>L</sub>    | 50                             | 50                        | 30                             | pF   |

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### TEST CIRCUITS FOR ALL OUTPUTS



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#### DEFINITIONS:

C<sub>L</sub> = Load capacitance; includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance; should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

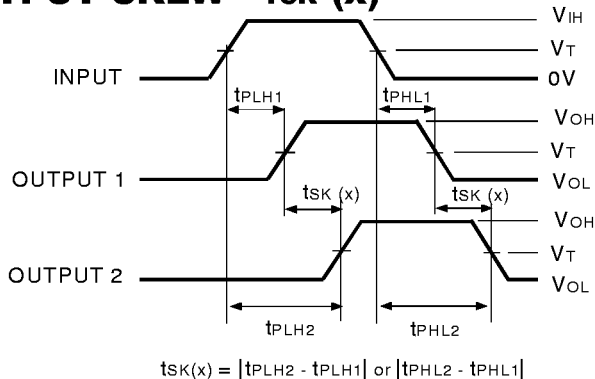
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

### SWITCH POSITION

| Test                                    | Switch            |
|-----------------------------------------|-------------------|
| Open Drain<br>Disable Low<br>Enable Low | V <sub>LOAD</sub> |
| Disable High<br>Enable High             | GND               |
| All Other tests                         | Open              |

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### OUTPUT SKEW - t<sub>SK</sub> (x)



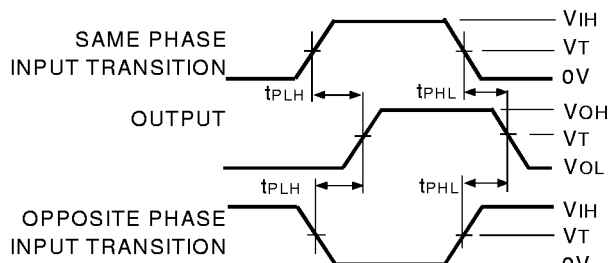
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

ALVC Link

#### NOTES:

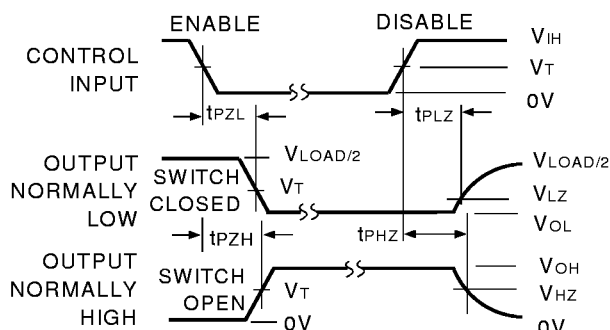
1. For t<sub>SK</sub>(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.

### PROPAGATION DELAY



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### ENABLE AND DISABLE TIMES

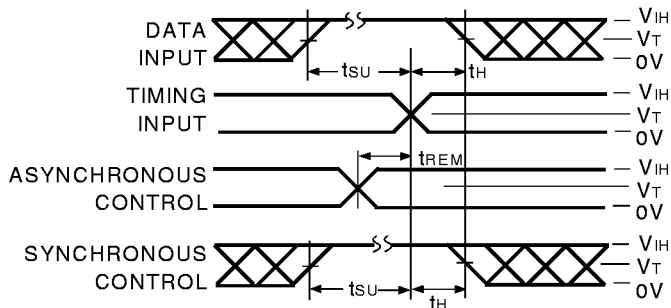


ALVC Link

#### NOTE:

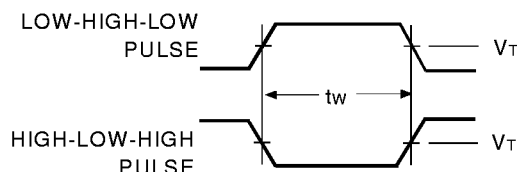
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SET-UP, HOLD, AND RELEASE TIMES



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### PULSE WIDTH



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## ORDERING INFORMATION

| IDT         | XX       | ALVC   | X           | XXX     | XXX | XX |                                                  |
|-------------|----------|--------|-------------|---------|-----|----|--------------------------------------------------|
| Temp. Range | Bus-Hold | Family | Device Type | Package |     |    |                                                  |
|             |          |        |             |         |     | PV | Shrink Small Outline Package (SO56-1)            |
|             |          |        |             |         |     | PA | Thin Shrink Small Outline Package (SO56-2)       |
|             |          |        |             |         |     | PF | Thin Very Small Outline Package (SO56-3)         |
|             |          |        |             |         | 276 |    | 12-Bit Synchronous Bus Exchanger                 |
|             |          |        |             | 16      |     |    | Double-Density with Resistors, $\pm 24\text{mA}$ |
|             |          |        |             |         |     | H  | Bus-Hold                                         |
|             |          |        |             |         |     | 74 | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$   |



**CORPORATE HEADQUARTERS**  
 2975 Stender Way  
 Santa Clara, CA 95054

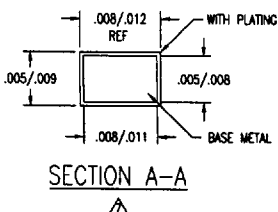
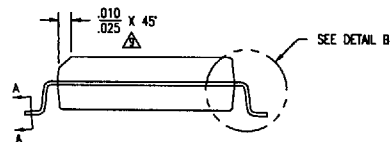
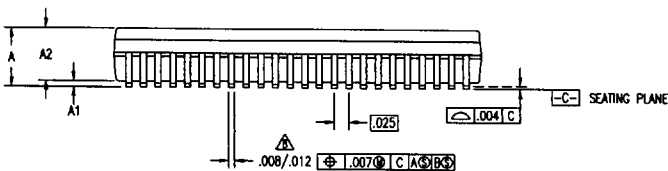
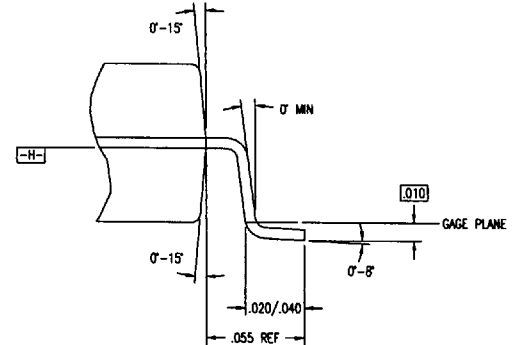
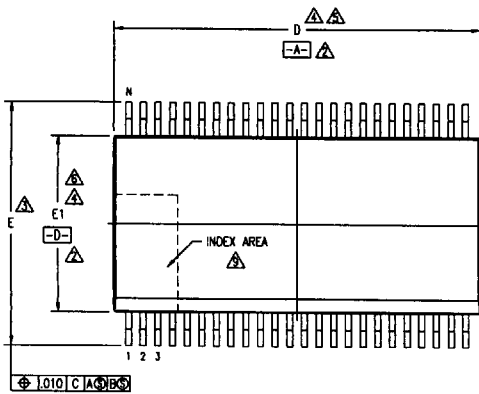
**for SALES:**  
 800-345-7015 or 408-727-6116  
 fax: 408-492-8674  
[www.idt.com](http://www.idt.com)\*

\*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.  
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# PACKAGE DIAGRAM OUTLINES

## SSOP

| REVISIONS |     |                             |          |            |
|-----------|-----|-----------------------------|----------|------------|
| DCN       | REV | DESCRIPTION                 | DATE     | APPROVED   |
| 17893     | 00  | INITIAL RELEASE             | 07/15/90 | A. FUNCELL |
| 22377     | 01  | REMOVE CHAMFER FROM PACKAGE | 04/15/92 | T. VU      |
| 27492     | 02  | REDRAW TO JEDEC FORMAT      | 02/01/95 |            |



|                             |          |                                         |     |
|-----------------------------|----------|-----------------------------------------|-----|
| TOLERANCES UNLESS SPECIFIED |          | Integrated Device Technology, Inc.      |     |
| DECIMAL                     | ANGULAR  | 2075 Slender Way, Santa Clara, CA 95054 |     |
| XXX                         | ±        | PHONE: (408) 727-8118                   |     |
| XXX                         |          | FAX: (408) 482-8874                     |     |
| XXX                         |          | TWC: 910-338-2070                       |     |
| APPROVALS                   | DATE     | TITLE                                   | REV |
| DRAWN                       | 08/15/90 | PV PACKAGE OUTLINE                      | 02  |
| CHECKED                     |          | .300" BODY WIDTH SSOP                   |     |
|                             |          | .025" PITCH                             |     |
|                             |          | SIZE C                                  |     |
|                             |          | DRAWING No. PSC-4029                    |     |
|                             |          | DO NOT SCALE DRAWING                    |     |

# PACKAGE DIAGRAM OUTLINES SSOP (Continued)

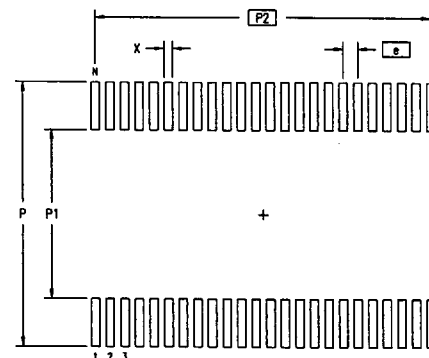
| REVISIONS |     |                             |          |            |
|-----------|-----|-----------------------------|----------|------------|
| DCN       | REV | DESCRIPTION                 | DATE     | APPROVED   |
| 17893     | 00  | INITIAL RELEASE             | 07/15/90 | A. FUNCELL |
| 22377     | 01  | REMOVE CHAMFER FROM PACKAGE | 04/15/92 | T. WJ      |
| 27492     | 02  | REDRAW TO JEDEC FORMAT      | 02/01/95 |            |

| DWG #  |                 | S048-1 |      |     |      | DWG #           |      | S056-1 |     |      |  |
|--------|-----------------|--------|------|-----|------|-----------------|------|--------|-----|------|--|
| SYMBOL | JEDEC VARIATION |        |      |     | NOTE | JEDEC VARIATION |      |        |     | NOTE |  |
|        | AA              |        |      | AB  |      |                 |      |        |     |      |  |
|        | MIN             | NOM    | MAX  | MIN |      | NOM             | MAX  |        |     |      |  |
| A      | .095            | .102   | .110 |     |      | .095            | .102 | .110   |     |      |  |
| A1     | .008            | .012   | .016 |     |      | .008            | .012 | .016   |     |      |  |
| A2     | .088            | .090   | .092 |     |      | .088            | .090 | .092   |     |      |  |
| D      | .620            | .625   | .630 | 4,5 |      | .720            | .725 | .730   | 4,5 |      |  |
| E      | .395            | .405   | .420 | 3   |      | .395            | .405 | .420   | 3   |      |  |
| E1     | .291            | .295   | .299 | 4,6 |      | .291            | .295 | .299   | 4,6 |      |  |
| N      | 48              |        |      |     |      | 56              |      |        |     |      |  |

## NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARIATION AA & AB

## LAND PATTERN DIMENSIONS



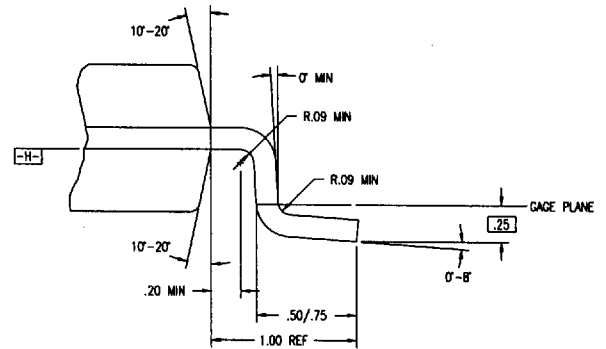
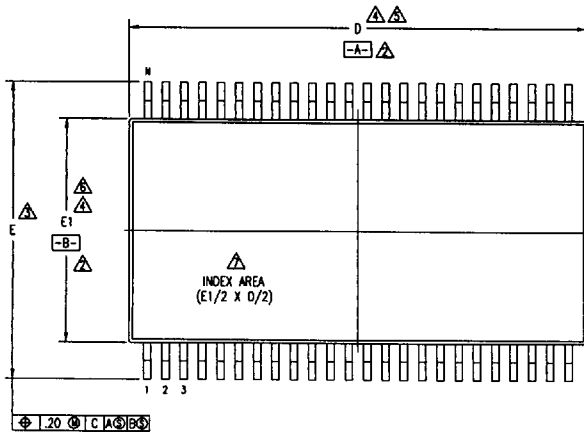
|    | MIN      | MAX  | MIN      | MAX  |
|----|----------|------|----------|------|
| P  | .450     | .458 | .450     | .458 |
| P1 | .282     | .290 | .282     | .290 |
| P2 | .575 BSC |      | .675 BSC |      |
| X  | .010     | .018 | .010     | .018 |
| e  | .025 BSC |      | .025 BSC |      |
| N  | 48       |      | 56       |      |

| TOLERANCES UNLESS SPECIFIED |          | Integrated Device Technology, Inc.     |     |
|-----------------------------|----------|----------------------------------------|-----|
| DECIMAL                     | ANGULAR  | 2075 Stoner Way, Santa Clara, CA 95054 |     |
| X.XX                        | ±        | PHONE: (408) 727-8116                  |     |
| X.XXX                       | ±        | FAX: (408) 482-8874                    |     |
| X.XXX                       | ±        | TW: 810-338-2070                       |     |
| APPROVALS                   | DATE     | TITLE                                  | REV |
| DRN                         | 06/15/90 | PV PACKAGE OUTLINE                     |     |
| CHECKED                     |          | .300" BODY WIDTH SSOP                  |     |
|                             |          | .025" PITCH                            |     |
|                             |          | SIZE                                   | REV |
|                             |          | C                                      | 02  |
|                             |          | DRAWING No.                            |     |
|                             |          | PSC-4029                               |     |
|                             |          | DO NOT SCALE DRAWING                   |     |

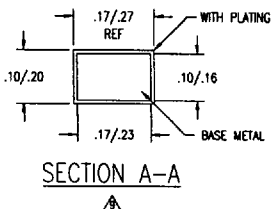
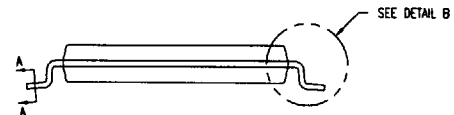
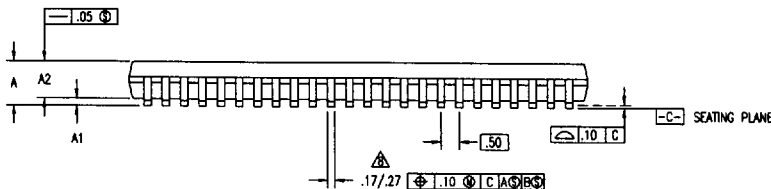
# PACKAGE DIAGRAM OUTLINES

## TSSOP

| REVISIONS |     |                        |          |          |
|-----------|-----|------------------------|----------|----------|
| DCN       | REV | DESCRIPTION            | DATE     | APPROVED |
| 23757     | 00  | INITIAL RELEASE        | 02/15/93 | T. VU    |
| 26315     | 01  | CHANGE DIMS A1 & A2    | 05/18/94 | DG       |
| 26490     | 02  | CHANGE DIM A1          | 07/21/94 | T. VU    |
| 27494     | 03  | REDRAW TO JEDEC FORMAT | 03/08/95 |          |



DETAIL B



| TOLERANCES UNLESS SPECIFIED |          | INTEGRATED DEVICE TECHNOLOGY, Inc.      |                  |
|-----------------------------|----------|-----------------------------------------|------------------|
| DECIMAL                     | ANGULAR  | 2975 Slender Way, Santa Clara, CA 95054 |                  |
| XXX.X                       | ±        | PHONE: (408) 727-8118                   |                  |
| XXXX.X                      |          | FAX: (408) 492-8674                     | TW: 910-336-2070 |
| XXXXX                       |          |                                         |                  |
| APPROVALS                   | DATE     | TITLE                                   |                  |
| DRAWN                       | 01/15/93 | PA PACKAGE OUTLINE                      |                  |
| CHECKED                     |          | 6.10 mm BODY WIDTH TSSOP                |                  |
|                             |          | .50 mm PITCH                            |                  |
|                             |          | SIZE                                    | REV              |
|                             |          | C                                       | 03               |
|                             |          | DRAWING No.                             |                  |
|                             |          | PSC-4039                                |                  |
|                             |          | DO NOT SCALE DRAWING                    |                  |

# PACKAGE DIAGRAM OUTLINES TSSOP (Continued)

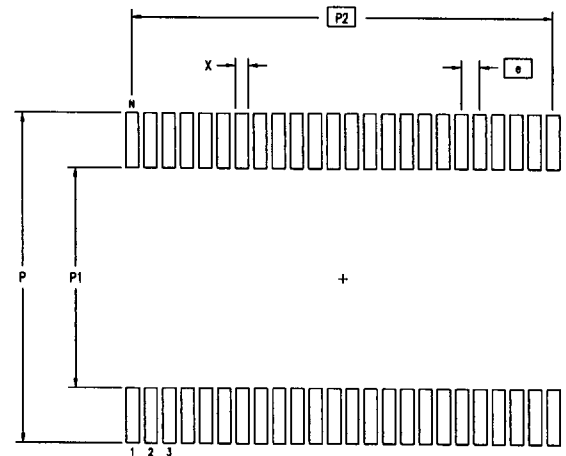
| DWG #  |                 |       |       | S048-2 |                 | DWG # |       |      |  | S056-2 |  |
|--------|-----------------|-------|-------|--------|-----------------|-------|-------|------|--|--------|--|
| SYMBOL | JEDEC VARIATION |       |       | NOTE   | JEDEC VARIATION |       |       | NOTE |  |        |  |
|        | ED              |       |       |        | EE              |       |       |      |  |        |  |
|        | MIN             | NOM   | MAX   |        | MIN             | NOM   | MAX   |      |  |        |  |
|        |                 |       |       |        |                 |       |       |      |  |        |  |
| A      | -               | -     | 1.10  |        | -               | -     | 1.10  |      |  |        |  |
| A1     | .05             | -     | .15   |        | .05             | -     | .15   |      |  |        |  |
| A2     | .85             | 1.00  | 1.05  |        | .85             | 1.00  | 1.05  |      |  |        |  |
| D      | 12.40           | 12.50 | 12.60 | 4,5    | 13.90           | 14.00 | 14.10 | 4,5  |  |        |  |
| E      | 7.95            | 8.10  | 8.25  | 3      | 7.95            | 8.10  | 8.25  | 3    |  |        |  |
| E1     | 6.00            | 6.10  | 6.20  | 4,6    | 6.00            | 6.10  | 6.20  | 4,6  |  |        |  |
| N      | 48              |       |       |        | 56              |       |       |      |  |        |  |

## NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS  $\square$ -A- and  $\square$ -B- TO BE DETERMINED AT DATUM PLANE  $\square$ -H-
- DIMENSION E TO BE DETERMINED AT SEATING PLANE  $\square$ -C-
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE  $\square$ -H-
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MQ-153, VARIATION ED & EE

| REVISIONS |     |                        |          |          |
|-----------|-----|------------------------|----------|----------|
| DCN       | REV | DESCRIPTION            | DATE     | APPROVED |
| 23757     | 00  | INITIAL RELEASE        | 02/15/93 | T. VU    |
| 26315     | 01  | CHANGE DIMS A1 & A2    | 05/18/94 | DG       |
| 26490     | 02  | CHANGE DIM A1          | 07/21/94 | T. VU    |
| 27494     | 03  | REDRAW TO JEDEC FORMAT | 03/08/95 |          |

## LAND PATTERN DIMENSIONS



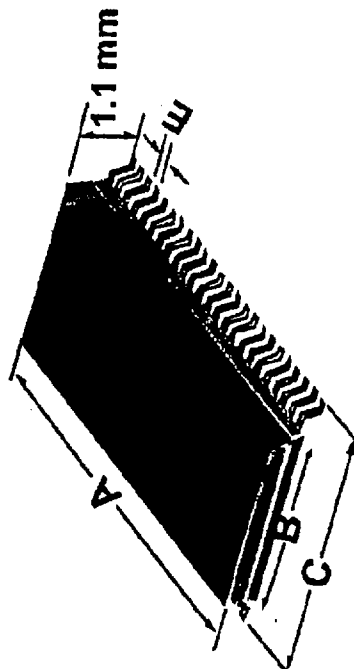
|    | MIN       | MAX  | MIN       | MAX  |
|----|-----------|------|-----------|------|
| P  | 8.90      | 9.10 | 8.90      | 9.10 |
| P1 | 5.90      | 6.10 | 5.90      | 6.10 |
| P2 | 11.50 BSC |      | 13.50 BSC |      |
| X  | .30       | .40  | .30       | .40  |
| e  | .50 BSC   |      | .50 BSC   |      |
| N  | 48        |      | 56        |      |

|                             |          |                                         |                    |
|-----------------------------|----------|-----------------------------------------|--------------------|
| TOLERANCES UNLESS SPECIFIED |          | Integrated Device Technology, Inc.      |                    |
| DECIMAL                     | ANGULAR  | 2075 Slender Way, Santa Clara, CA 95054 |                    |
| XXX.X                       | ±        | PHONE: (408) 727-8118                   |                    |
| XXXX.XX                     |          | FAX: (408) 482-8874                     |                    |
| XXXX.XXX                    |          | TWC: 910-338-2070                       |                    |
| APPROVALS                   | DATE     | TITLE                                   | PA PACKAGE OUTLINE |
| DRAWN                       | 01/19/93 | 6.10 mm BODY WIDTH TSSOP                |                    |
| CHECKED                     |          | .50 mm PITCH                            |                    |
|                             |          | SIZE                                    | C                  |
|                             |          | DRAWING No.                             | PSC-4039           |
|                             |          | REV                                     | 03                 |
| DO NOT SCALE DRAWING        |          |                                         |                    |



# TVSOP

## The Most Compact Double Density Package

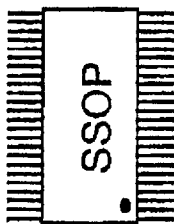


| TVSOP Package | Typical Dimensions (in mm) |      |      |      | Area (mm <sup>2</sup> ) |
|---------------|----------------------------|------|------|------|-------------------------|
|               | A                          | B    | C    | E    |                         |
| 48 Pin        | 9.80                       | 4.40 | 6.40 | 0.40 | 63.00                   |
| 56 Pin        | 11.30                      | 4.40 | 6.40 | 0.40 | 72.30                   |
| 80 Pin        | 17.00                      | 6.10 | 8.10 | 0.40 | 137.80                  |
| 100 Pin       | 20.80                      | 6.10 | 8.10 | 0.40 | 168.50                  |



# Double Density Packaging

## 48-Pin



16.0 x 10.3 x 2.6 mm  
pin pitch = 0.635 mm  
Area = 164.8 mm<sup>2</sup>

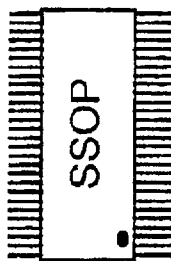


12.5 x 8.1 x 1.1 mm  
pin-pitch = 0.5 mm  
Area = 101.3 mm<sup>2</sup>



9.8 x 6.4 x 1.1 mm  
pin-pitch = 0.4 mm  
Area = 62.7 mm<sup>2</sup>

## 56-Pin



18.4 x 10.3 x 2.6 mm  
pin-pitch = 0.635 mm  
Area = 189.5 mm<sup>2</sup>



14.0 x 8.1 x 1.1 mm  
pin-pitch = 0.5 mm  
Area = 113.4 mm<sup>2</sup>



11.3 x 6.4 x 1.1 mm  
pin-pitch = 0.4 mm  
Area = 72.3 mm<sup>2</sup>

| TVSOP  | Area<br>(mm <sup>2</sup> ) | %Smaller<br>Than<br>SSOP | %Smaller<br>Than<br>TSSOP |
|--------|----------------------------|--------------------------|---------------------------|
| 48 pin | 63.00                      | 61.9                     | 38.0                      |
| 56 pin | 72.30                      | 62.2                     | 36.0                      |