8M-Bit (1Mx8 / 512Kx16) CMOS MASK ROM

FEATURES

- Switchable organization
  1,048,576 x 8(byte mode)
  524,288 x 16(word mode)
- Fast access time
  100ns(Max.) : C_L=50pF
  120ns(Max.) : C_L=100pF
- Supply voltage : single +5V
- Current consumption
  Operating : 50mA(Max.)
  Standby : 50μA(Max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Package
  -. K3N4C1000E-DC : 42-DIP-600
  -. K3N4C1000E-GC : 44-SOP-600

GENERAL DESCRIPTION

The K3N4C1000E-D(G)C is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576 x 8(byte mode) or as 524,288 x 16(word mode) depending on BHE voltage level.(See mode selection table)

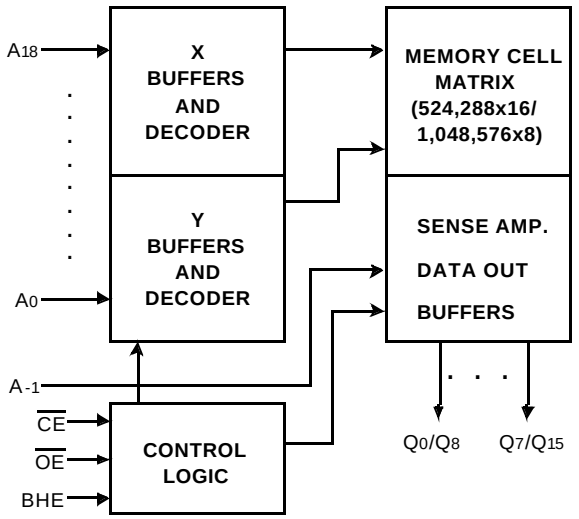
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

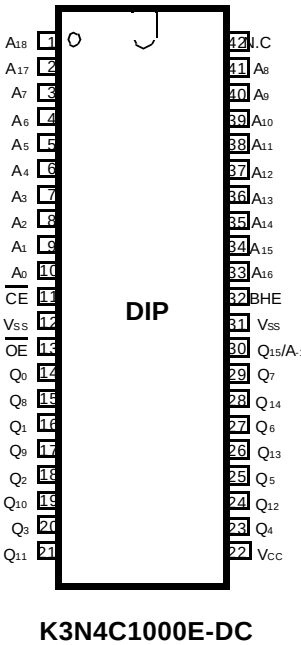
The K3N4C1000E-DC is packaged in a 42-DIP and the K3N4C1000E-GC in a 44-SOP.

FUNCTIONAL BLOCK DIAGRAM

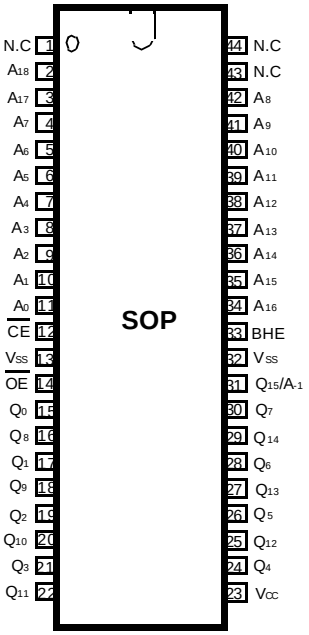


Pin Name	Pin Function
A_0 - A_{18}	Address Inputs
Q_0 - Q_{14}	Data Outputs
Q_{15}/A_{-1}	Output 15(Word mode)/ LSB Address(Byte mode)
BHE	Word/Byte selection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C	No Connection

PIN CONFIGURATION



K3N4C1000E-DC



K3N4C1000E-GC

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to +7.0	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{Stg}	-55 to +150	°C

NOTE : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	Cycle=5MHz, all outputs open $\overline{CE}$=$\overline{OE}$=V_{IL}, V_{IN}=0V to 3V (AC Test Condition)	-	50	mA
Standby Current(TTL)	I_{SB1}	$\overline{CE}$=V_{IH}, all outputs open	-	1	mA
Standby Current(CMOS)	I_{SB2}	$\overline{CE}$=V_{CC}, all outputs open	-	50	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	-	10	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	-	10	µA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		-0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = -400µA	2.4	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	-	0.4	V

NOTE : Minimum DC Voltage(V_{IL}) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input pins(V_{IH}) is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
H	X	X	X	Standby	High-Z	Standby
L	H	X	X	Operating	High-Z	Active
L	L	H	Output	Operating	Q_0~Q_{15} : Dout	Active
		L	Input	Operating	Q_0~Q_7 : Dout Q_8~Q_{14} : Hi-Z	Active

CAPACITANCE(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	12	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

AC CHARACTERISTICS(T_A=0°C to +70°C, V_{CC}=5V±10%, unless otherwise noted.)

TEST CONDITIONS

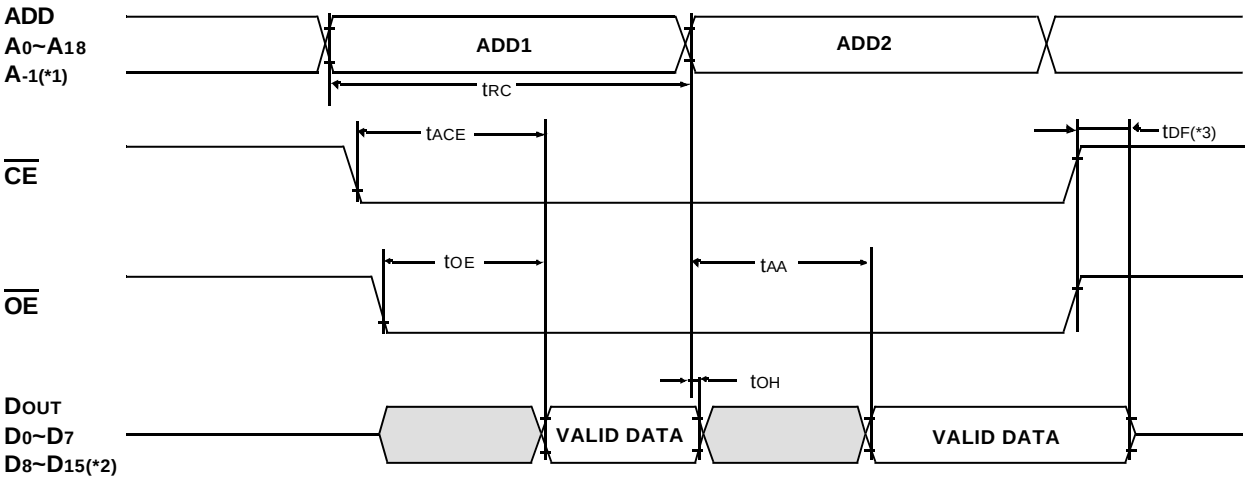
Item	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L=50pF or 100pF

READ CYCLE

Item	Sym-bol	K3N4C1000E-D(G)C10(C_L=50pF)		K3N4C1000E-D(G)C12(C_L=100pF)		K3N4C1000E-D(G)C15(C_L=100pF)		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ



NOTES :

*1. Byte Mode only. A_1 is Least Significant Bit Address.(BHE = V_{IL})

*2. Word Mode only.(BHE = V_{IH})

*3. t_{DF} is defined as the time at which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} level.