64Kx8 bit Low Power CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.6 um CMOS
- Organization : 64K x8
- Power Supply Voltage : Single 5V +/- 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(I)-Forward

GENERAL DESCRIPTION

The KM68512A family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ragnges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

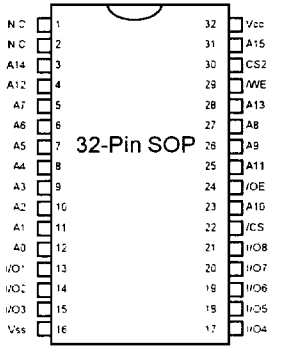
2

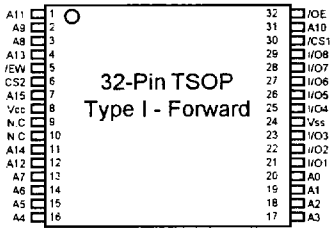
PRODUCT FAMILY

Product Family	Operating Temperature	Speed	PKG Type	Power Dissipation	
				Standby(Isb1, Max)	Operating(Icc2)
KM68512AL	Commercial (0~70 °C)	45*/55/70ns	32-SOP	100uA	70mA
KM68512AL-L			32-TSOP(I) F	20uA	
KM68512ALI	Industrial (-40~85 °C)	70/100ns	32-SOP	100uA	
KM68512ALI-L			32-TSOP(I) F	50uA	

* measured with 30pF test load

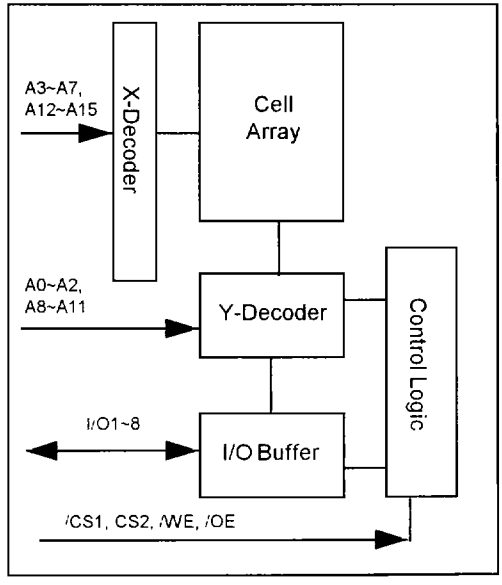
PIN DESCRIPTION





Name	Function	Name	Function
A0~A15	Address Inputs	Vcc	Power
/WE	Write Enable Input	Vss	Ground
/CS1, CS2	Chip Select Input	N.C	No Connection
/OE	Output Enable Input		
I/O1~I/O16	Data Input/Output		

FUNCTIONAL BLOCK DIAGRAM



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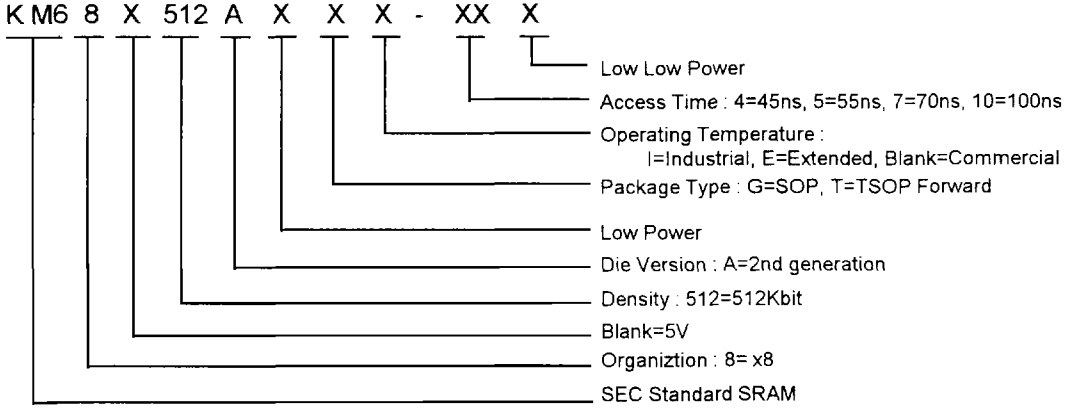
PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**
KM68512ALG-4	32-SOP, 45ns, L-pwr	KM68512ALGI-7	32-SOP, 70ns, L-pwr
KM68512ALG-4L	32-SOP, 45ns, LL-pwr	KM68512ALGI-7L	32-SOP, 70ns, LL-pwr
KM68512ALG-5	32-SOP, 55ns, L-pwr	KM68512ALGI-10	32-SOP, 100ns, L-pwr
KM68512ALG-5L	32-SOP, 55ns, LL-pwr	KM68512ALGI-10L	32-SOP, 100ns, LL-pwr
KM68512ALG-7	32-SOP, 70ns, L-pwr	KM68512ALTI-7	32-TSOP F, 70ns, L-pwr
KM68512ALG-7L	32-SOP, 70ns, LL-pwr	KM68512ALTI-7L	32-TSOP F, 70ns, LL-pwr
KM68512ALT-4	32-TSOP F, 45ns, L-pwr	KM68512ALTI-10	32-TSOP F, 100ns, L-pwr
KM68512ALT-4L	32-TSOP F, 45ns, LL-pwr	KM68512ALTI-10L	32-TSOP F, 100ns, LL-pwr
KM68512ALT-5	32-TSOP F, 55ns, L-pwr		
KM68512ALT-5L	32-TSOP F, 55ns, LL-pwr		
KM68512ALT-7	32-TSOP F, 70ns, L-pwr		
KM68512ALT-7L	32-TSOP F, 70ns, LL-pwr		

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	Pd	1.0	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM68512AL/L-L
		-40 to 85	°C	KM68512ALI/LI-L
Soldering temperature and time	Tsolder	260 °C,10sec(Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	Vih	2.2	-	Vcc+0.5	V
Input low voltage	Vil	-0.5***	-	0.8	V

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ≤50ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

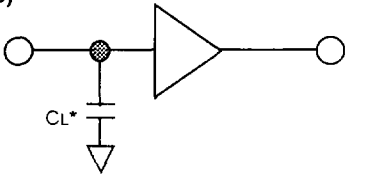
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS1=Vih or CS2=Vil or /WE=Vil, Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current Average operating current		Icc	/CS1=Vil, CS2=Vih, Vin=Vih or Vil, Iio=0mA		-	7	15	mA
		Icc1	Cycle time=1uS 100% duty /CS1≤0.2V, CS2≥Vcc-0.2V Vil≤0.2V, Vih≥Vcc-0.2V, Iio=0mA		-	-	10	mA
		Icc2	Min cycle, 100% duty /CS1=Vil, CS2=Vih, Iio=0mA		-	-	70	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.4	-	-	V
Standby Current(TTL)		Isb	/CS1=Vih, CS2=Vil		-	-	3	mA
Standby Current (CMOS)	KM68512AL/L-L	Isb1	/CS1≥Vcc-0.2V and CS2≥Vcc-0.2V	L	-	2	100	uA
				LL	-	1	20	uA
	KM68512ALI/LI-L		or CS2≤0.2V Vin≤0.2V or Vin≥Vcc-0.2V	L	-	2	100	uA
				LL		1	50	uA

* 1) Commercial Product : Ta=0 to 70 °C , Vcc=5V+/-10%, unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C , Vcc=5V+/-10%, unless otherwise specified
** Ta=25 °C

AC CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rise and fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	C_L=100pF+1TTL	-
	**C_L=30pF+1TTL	



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics
** Test load for 45ns Commercial Product

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TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68512AL/L-L	0~70 °C	5V +/- 10%	45*/55/70ns	Commercial
KM68512ALI/LI-L	-40~85 °C	5V +/- 10%	70/100ns	Industrial

* parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins								Units
			45ns*		55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	100	-	ns
	Address access time	tAA	-	45	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	45	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	45	-	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	5	-	ns

* All the parameters are measured with 30pF test load

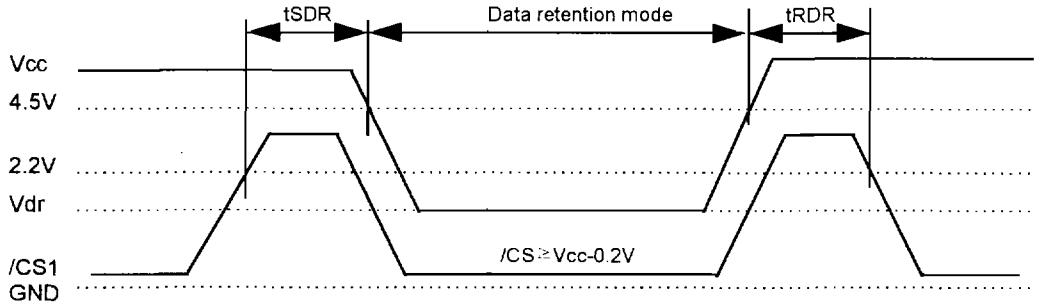
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		***/CS ≥ Vcc-0.2V		2.0	-	5.5	V
Data retention current	Idr	KM68512AL/L-L	Vcc=3.0V /CS ≥ Vcc-0.2V	L-Ver	-	1	50	uA
				LL-Ver	-	0.5	10	
		KM68512ALI/LI-L		L-Ver	-	-	50	
				LL-Ver	-	-	25	
Data retention set-up time	tSDR	See data retention waveform			0	-	-	ms
Recovery time	tRDR				5	-	-	

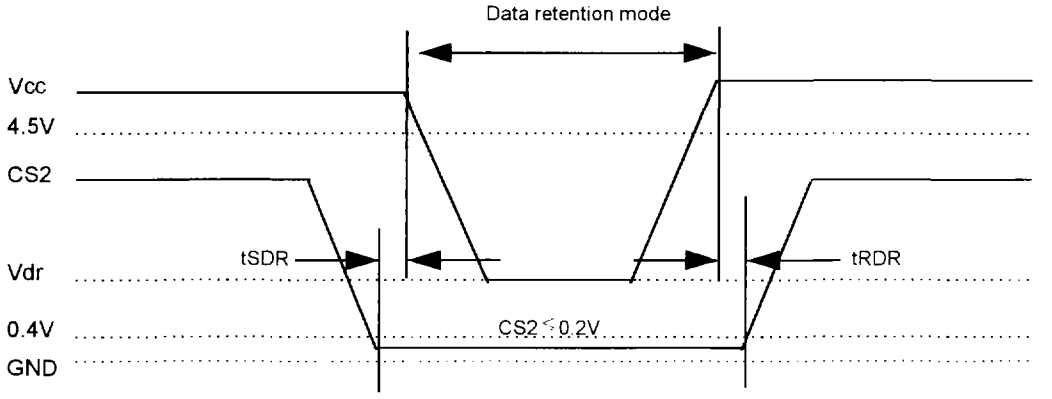
* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C
*** /CS1 ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V(/CS1 controlled) or CS2 ≤ 0.2V(CS2 controlled)

DATA RETENTION TIMING DIAGRAM

1) /CS1 Controlled



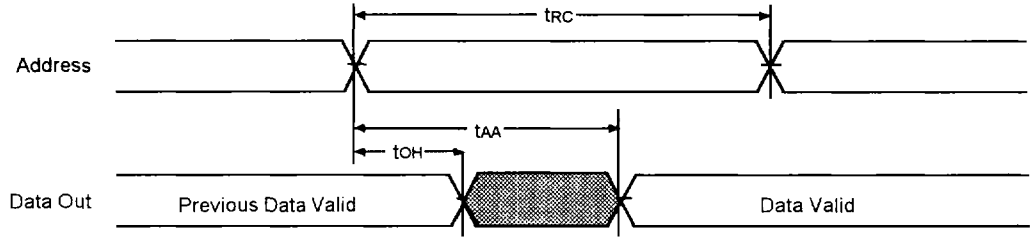
2) CS2 Controlled



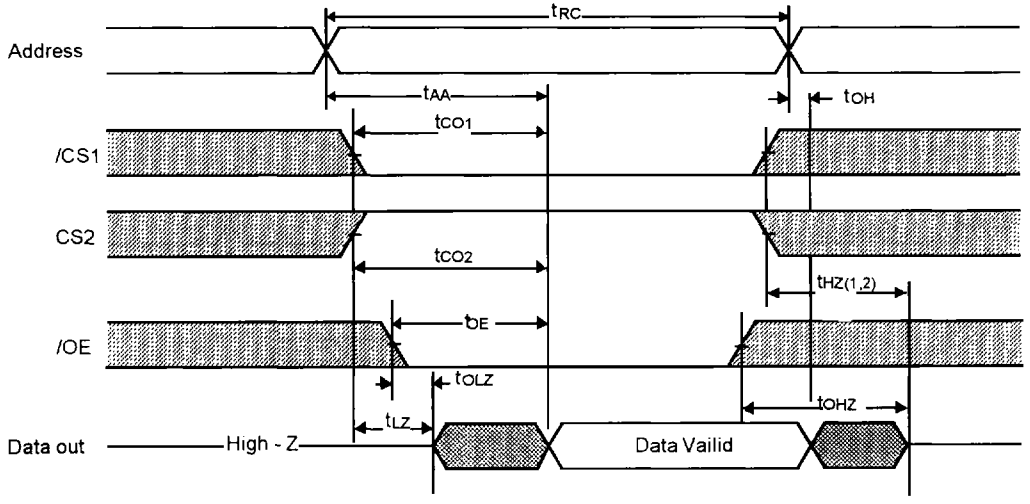
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, CS2=/WE=Vih)



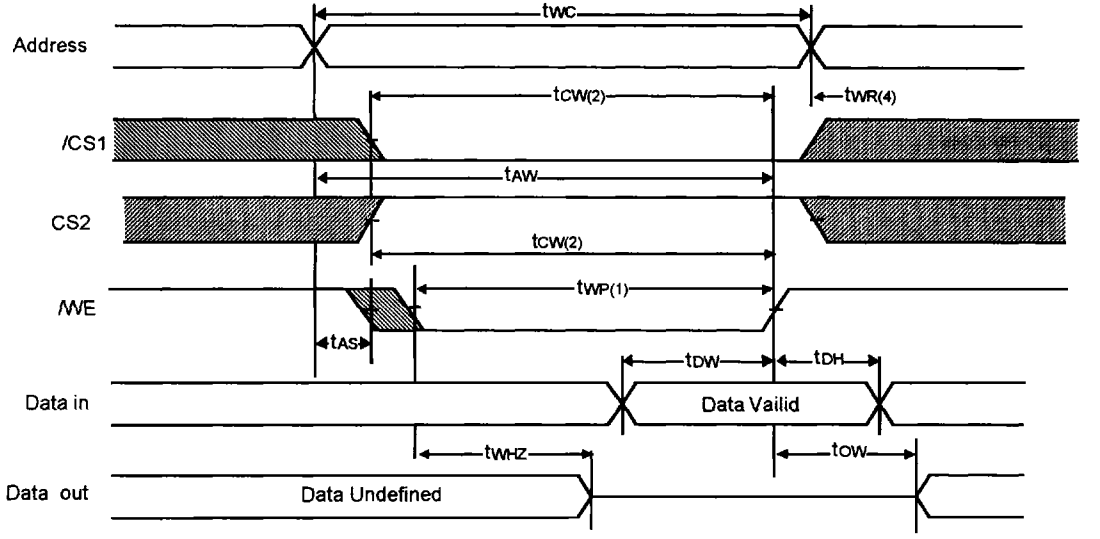
TIMING WAVE FORM OF READ CYCLE(2) (/WE= VIH)



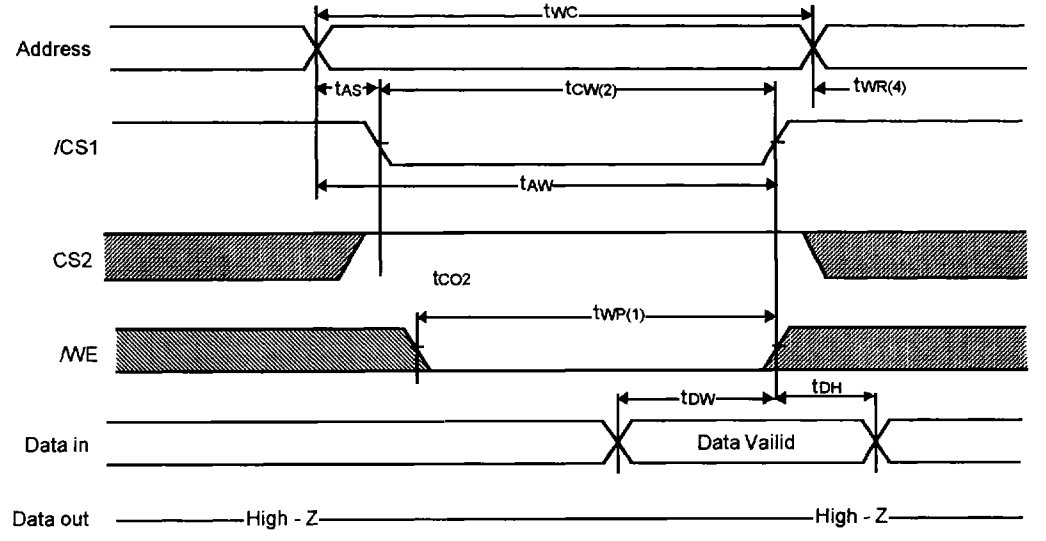
Notes(Read Cycle)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max) is less than tLZ(Min) both for a given device and device to device interconnection.

TIMING WAVE FORM OF WRITE CYCLE(1) (/WE Controlled)



TIMING WAVE FORM OF WRITE CYCLE(2) (/CS1 Controlled)



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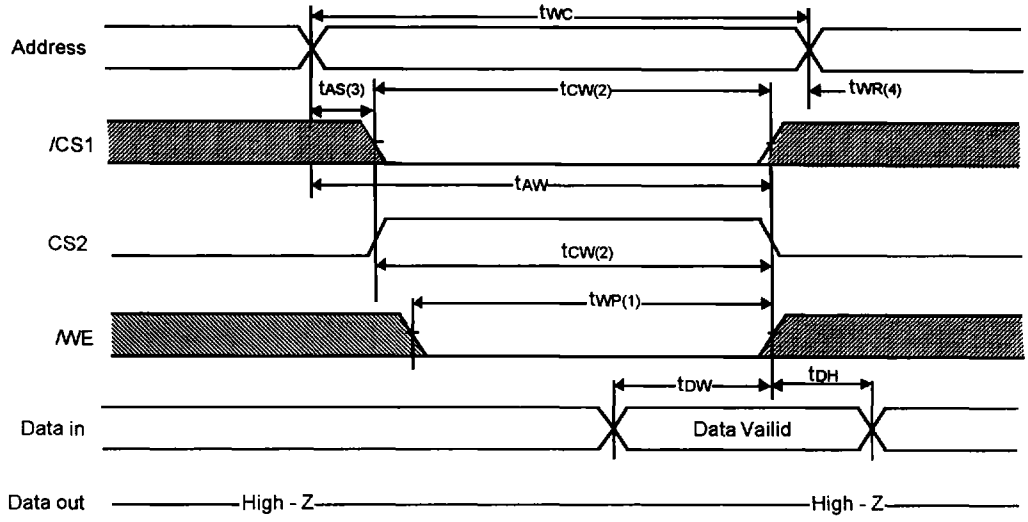
TIMING WAVE FORM OF WRITE CYCLE(3)(CS2 Controlled)



Notes(Write Cycle)

1. A write occurs during the overlap of a low /CS1, a high CS2 and a low /WE. A write begins at the latest transition among /CS1 going low, CS2 going high and /WE going low. A write ends at the earliest transition among /CS1 going high, CS2 going low and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR(1) applied in case a write ends at/CS1, or /WE going high, tWR2 applied in case a write ends at CS2 going to low.

FUNCTIONAL DESCRIPTION

/CS1	CS2	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	Isb, Isb1
X	L	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	H	Ouput Disable	High-Z	Icc
L	H	H	L	Read	Dout	Icc
L	H	L	X	Write	Din	Icc