

BIPOLAR ANALOG INTEGRATED CIRCUIT
PPC8110GR**1 GHz DIRECT QUADRATURE MODULATOR
FOR DIGITAL MOBILE COMMUNICATION****DESCRIPTION**

The PPC8110GR is a silicon monolithic integrated circuit designed as 1 GHz direct quadrature modulator for digital mobile communication systems. This modulator housed in a 20 pin plastic SSOP that easy to install and contributes to miniaturizing the system.

The device has power save function and can operates 2.7 to 3.6 V supply voltage to realize low power consumption.

FEATURES

- Direct modulation range : 800 MHz to 1 GHz
- Supply voltage range : $V_{CC} = 2.7$ to 3.6 V
- Low operation current : $I_{CC} = 24$ mA typical @ $V_{CC} = 3$ V
- Low phase difference due to digital phase shifter is adopted.
- 20 pin SSOP suitable for high density surface mounting.
- Low current sleep mode

APPLICATION

- Digital cellular phone (PDC, IS-54/IS-136, GSM etc..)

ORDERING INFORMATION

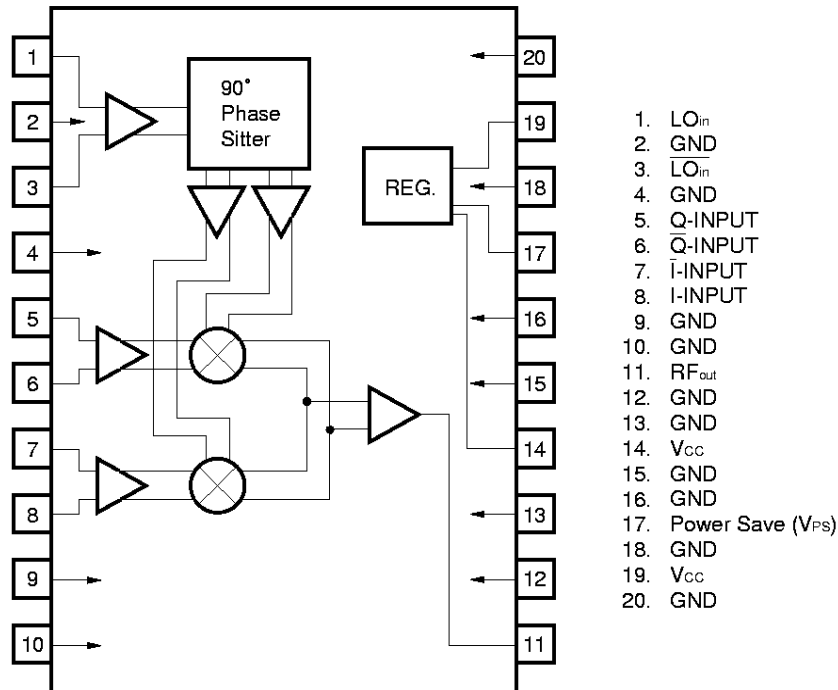
PART NUMBER	PACKAGE	PACKING FORM
PPC8110GR-E1	20 pin plastic SSOP	Carrier tape width 12 mm. Q'ty 2.5 kp/Reel Pin 1 indicated pull-out direction of tape.

Remark For evaluation sample order, please contact your local NEC sales office. (Order number: PPC8110GR)

Caution: Electro-static sensitive device

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS

(Top View)



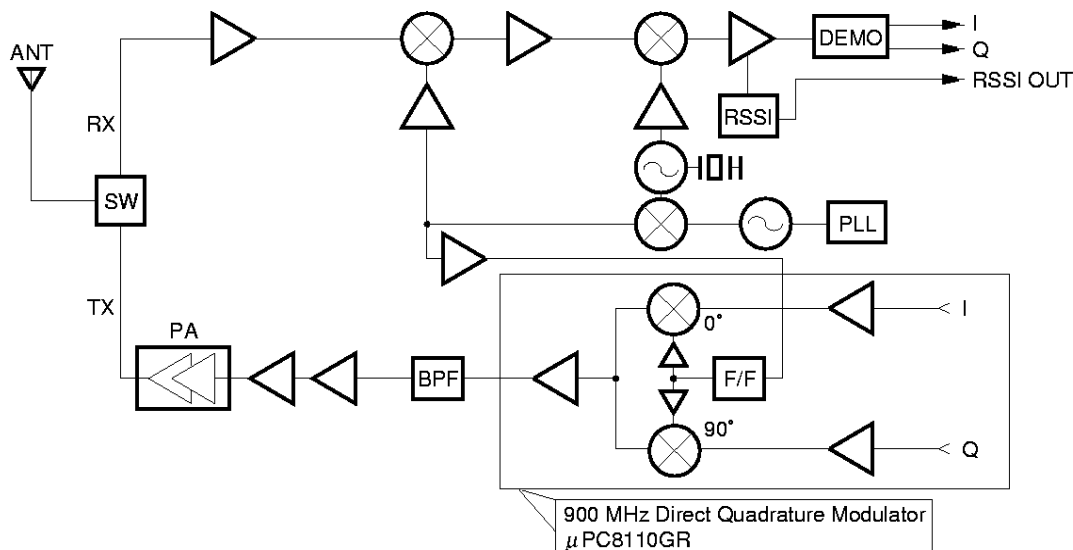
SERIES PRODUCTS

SERIES TYPE	PART NUMBER	f_{LO1in} (MHz)	f_{MODout} (MHz)	$f_{I/Q}$ (MHz)	Up-Converter f_{RFout} (MHz)	APPLICATION
150 MHz Quadrature MOD	PPC8101GR	100 to 300	50 to 150	DC to 0.5	External	CT2, Digital Comm.
Up-Con+Quadrature MOD	PPC8104GR	100 to 400		DC to 10	900 to 1900	PHS, PDC etc..
400 MHz Quadrature MOD	PPC8105GR	100 to 400		DC to 10	External	PDC, IS-136, GSM, PHS
1 GHz direct Quad MOD	PPC8110GR	800 to 1000		DC to 10	Direct	PDC, IS-136, GSM etc.

Remark As for detail information of series products, please refer to each data sheet.

APPLICATION EXAMPLE

PDC 900 MHz (Direct Modulation Type)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	TEST CONDITIONS
Supply Voltage	V _{CC}	4.0	V	T _A = +25 °C
Power Save Voltage	V _{PS}	4.0	V	T _A = +25 °C
Power Dissipation	P _D	430	mW	T _A = +85 °C ^{Note 1}
Operating Temperature	T _{opt}	40 to +85	°C	
Storage Temperature	T _{stg}	55 to +150	°C	

Note 1. Mounted on 50 u 50 u 1.6 mm double copper clad epoxy glass board

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V _{CC}	2.7	3.0	3.6	V	
Operating Temperature	T _{opt}	40	+25	+85	°C	
Lo Input Frequency	f _{LOin}	800	900	1000	MHz	
Lo Input Power Level	PL _{Oin}	15	10	7	dBm	
I/Q Input Frequency	f _{I/Qin}	DC		10	MHz	
I/Q Input Voltage	V _{I/Qin}			500	mV _{p-p}	Single ended input
				250		Differential input

ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.0\text{ V}$, Unless Otherwise Specified V_{PS} to 2.2 V (High))

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	20	24	33	mA	No input signal
Circuit Current at Power Save Mode	$I_{CC(PS)}$			10	uA	V_{PS} to 0.5 V (Low)
Maximum Output Power	$P_{O(sat)}$	13	10		dBm	$f_{LOin} = 948\text{ MHz}$ $P_{LOin} = -10\text{ dBm}$ $f_{I/Q} = 2.625\text{ kHz}$ $I/Q\text{ (DC)} = V_{CC}/2$ $V_{I/Qin} = 500\text{ mV}_{p-p}$ (Single ended)
Lo Carrier Leak	LoL		35	30	dBc	
Image Rejection (Side Band Leak)	ImR		40	30	dBc	
I/Q 3rd Order Intermodulation Distortion	$IM_{3I/Q}$		45	30	dBc	
Power Save Rise Time	$T_{PS(RISE)}$		3	5	μs	V_{PS} : Low to High
Power Save Fall Time	$T_{PS(FALL)}$		2	5	μs	V_{PS} : High to Low

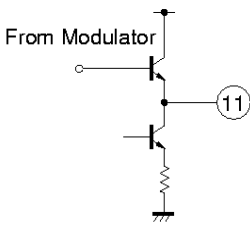
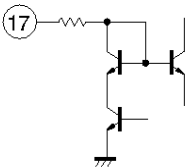
STANDARD CHARACTERISTICS FOR REFERENCE

($T_A = +25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.0\text{ V}$, Unless Otherwise Specified V_{PS} to 2.2 V (High))

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I/Q Input Impedance	$Z_{I/Qin}$		150		k:	$f_{I/Q} = \text{DC to } 10\text{ MHz}$
Lo Input VSWR	$VSWR(Lo)$		1.5 : 1			$f_{Lo} = 948\text{ MHz}$
RF Output VSWR	$VSWR(RF)$		1.5 : 1			$f_{Lo} = 948\text{ MHz}$

PIN EXPLANATION

Pin No.	ASSIGNMENT	SUPPLY VOL. (V)	PIN VOL. (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
1	L_{in}		2.6	L_o input for phase shifter. Connect around 50 Ω between 1 and 3 pin to match to 50 Ω .	
2 18	GND (for Local Amp. Block)	0		Connect to the ground with minimum inductance. Track length should be kept as short as possible.	
3	$\overline{L_{in}}$		2.6	Bypass of L_o input. This pin is grounded through around 33 pF capacitor.	
5	Q	$V_{cc}/2$		Input for Q signal. This input impedance is 150 k Ω . In case of that I/Q input signals are single ended, amplitude of the signal is 500 mVp-p max. Note 2	
6	$\overline{Q}$	$V_{cc}/2$		Input for Q signal. This input impedance is 150 k Ω . In case of that I/Q input signals are single ended, $V_{cc}/2$ biased DC signal should be input. In case of that I/Q input signals are differential, amplitude of the signal is 250 mVp-p max. Note 2	
7	$\overline{I}$	$V_{cc}/2$		Input for I signal. This input impedance is 150 k Ω . In case of that I/Q input signals are single ended, $V_{cc}/2$ biased DC signal should be input. In case of that I/Q input signals are differential, amplitude of the signal is 250 mVp-p max. Note 2	
8	I	$V_{cc}/2$		Input for I signal. This input impedance is 150 k Ω . In case of that I/Q input signals are single ended, amplitude of the signal is 500 mVp-p max. Note 2	
9 13 16	GND (for Quadrature Modulator Block)	0		Connect to the ground with minimum inductance. Track length should be kept as short as possible.	

Pin No.	ASSIGNMENT	SUPPLY VOL. (V)	PIN VOL. (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT						
11	RF _{out}		1.6	Output from modulator. This is single-end push-pull amplifier. So this output impedance is Low.							
12	GND (for Output Push-pull Amplifier)	0		Connect to the ground with minimum inductance. Track length should be kept as short as possible.							
14	V _{CC} (for Output Amplifier of Modulator)	2.7 to 3.6		Supply voltage pin for Output Amplifier of modulator. Internal regulator can be kept stable condition of supply bias against the variable temperature or V _{CC} .							
17	Power Save	V _{P/S}		Power save control pin can be controlled ON/SLEEP state with bias as follows; <table border="1" data-bbox="695 836 956 976"><thead><tr><th>V_{P/S}</th><th>STATE</th></tr></thead><tbody><tr><td>2.2 to 3.6</td><td>ON</td></tr><tr><td>0 to 0.5</td><td>SLEEP</td></tr></tbody></table>	V _{P/S}	STATE	2.2 to 3.6	ON	0 to 0.5	SLEEP	
V _{P/S}	STATE										
2.2 to 3.6	ON										
0 to 0.5	SLEEP										
19	V _{CC}	2.7 to 3.6		Supply voltage pin for modulator except output Amplifier. Internal regulator can be kept stable condition of supply bias against the variable temperature or V _{CC} .							
4	GND	0		Connect to the ground with minimum inductance. Track length should be kept as short as possible.							
10											
15											
20											

Note 2. Relations between amplitude and V_{CC}/2 bias of input signal are following.

Supply Voltage V _{CC} (V)	I/Q DC Voltage (V) $V_{CC}/2 = I = \overline{I} = Q = \overline{Q}$	P _{I/Qin} - I/Q Input Signal - mVp-p	
		Single ended input I = Q	Differential input I = $\overline{I}$ = Q = $\overline{Q}$
2.7 to 3.6	1.35 to 1.8	d 500	d 250

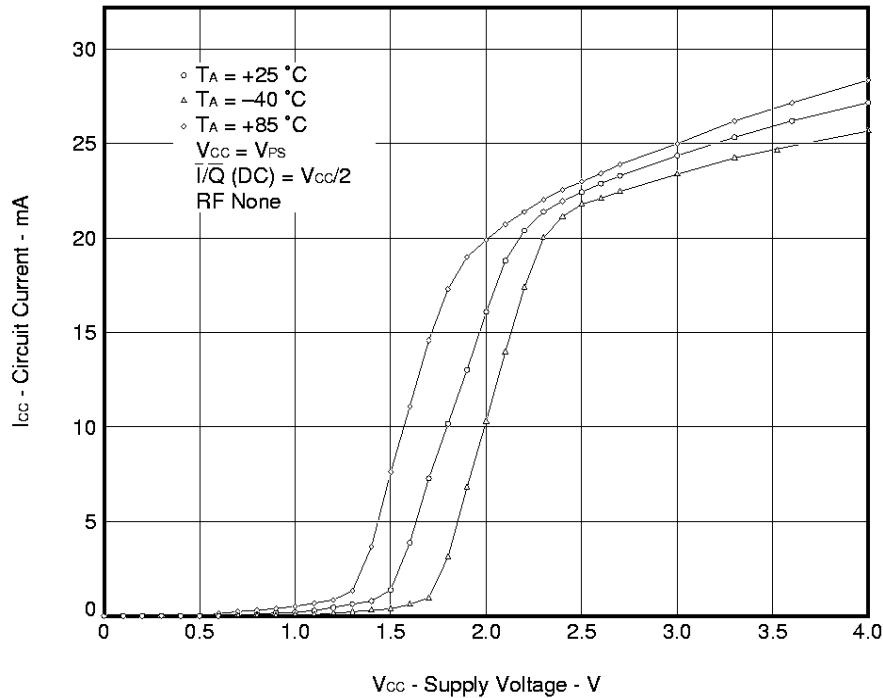
EXPLANATION OF INTERNAL FUNCTION

BLOCK	FUNCTION/OPERATION	BLOCK DIAGRAM
90 ° PHASE SHIFTER	Input signal from L_o is send to digital circuit of T-type flip-flop through frequency doubler. Output signal from T-type F/F is changed to same frequency as L_o input and that have quadrature phase shift, 0 °, 90 °, 180 °, 270 °. These circuits have function of self phase correction to make correctly quadrature signals.	The block diagram illustrates the internal signal processing flow. It begins with an input signal 'from L_{Oin}' entering a frequency doubler block labeled $\times 2$. The output of this block goes into a divider block labeled $\div 2 F/F$. From the divider, the signal splits into two paths, each passing through a phase shifter (represented by a triangle). These signals then enter two mixers (represented by circles with an 'X'). The first mixer has inputs I and $\bar{I}$. The second mixer has inputs $\bar{Q}$ and Q. The outputs of the mixers are combined and pass through a final phase shifter (triangle) before reaching the output labeled 'to MOD_{out}'.
BUFFER AMP.	Buffer amplifiers for each phase signals to send to each mixers.	
MIXER	Each signals from buffer amp. are quadrature modulated with two double-balanced mixers. High accurate phase and amplitude inputs are realized to good performance for image rejection.	
ADDER	Output signals from each mixers are added with adder and send to final amplifier.	

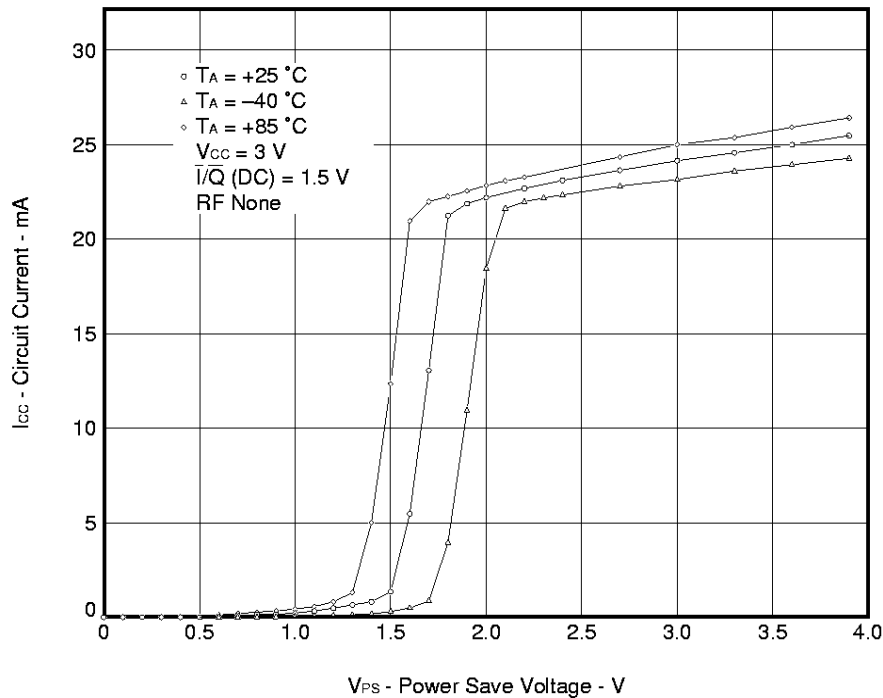
TYPICAL CHARACTERISTICS

Unless otherwise specified $T_A = +25\text{ }^{\circ}\text{C}$, $V_{CC} = V_{PS} = 3\text{ V}$, I/Q DC/offset = $\overline{I/Q}$ DC offset = 1.5 V, I/Q Input signal = 500 mV_{p-p} (Single ended), $f_{I/Q} = 2.625\text{ kHz}$, $f_{LOin} = 948\text{ MHz}$, $P_{LOin} = 10\text{ dBm}$, <PDC> Transmission speed: 42 kbps, RNYQ: $a = 0.5$.

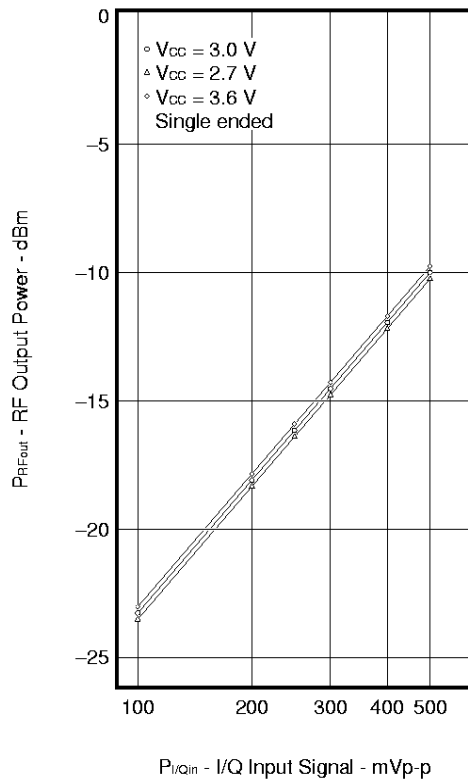
CIRCUIT CURRENT vs SUPPLY VOLTAGE



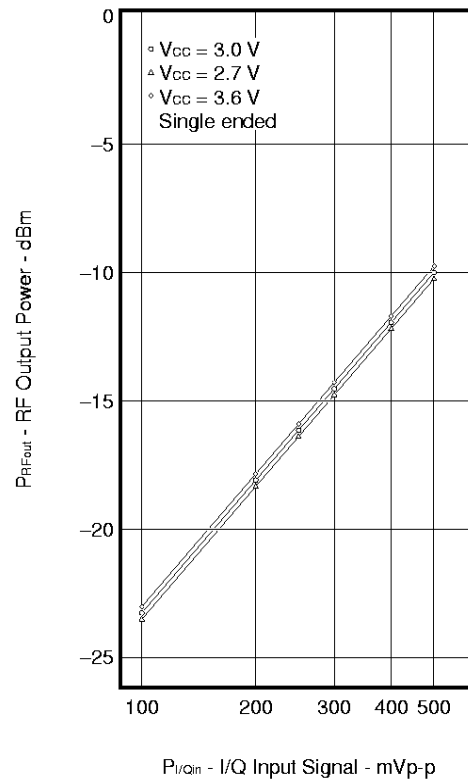
CIRCUIT CURRENT vs POWER SAVE VOLTAGE



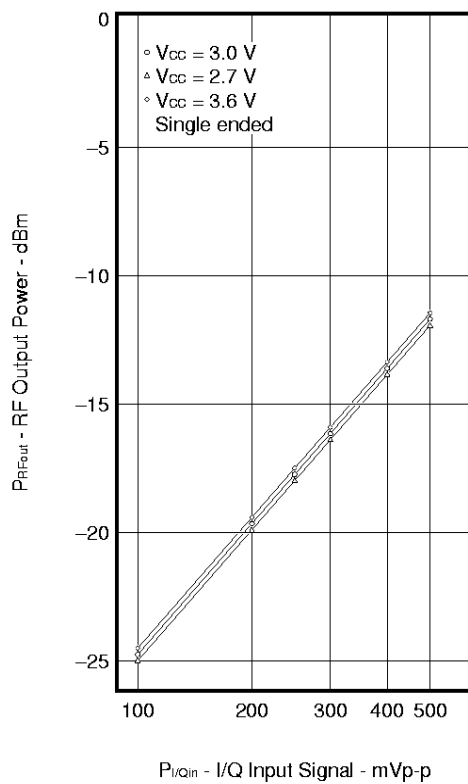
RF OUTPUT POWER vs I/Q INPUT SIGNAL
(at $T_A = -40^\circ\text{C}$)



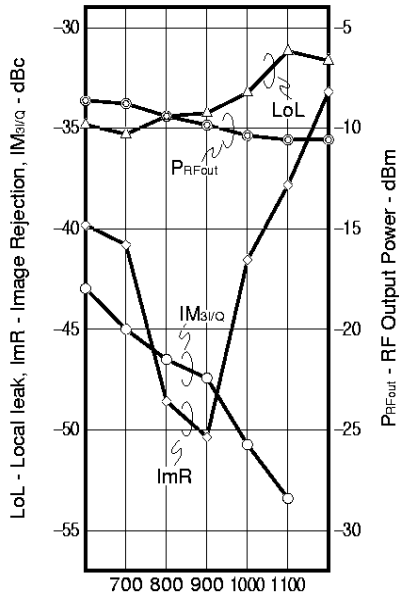
RF OUTPUT POWER vs I/Q INPUT SIGNAL
(at $T_A = +25^\circ\text{C}$)



RF OUTPUT POWER vs I/Q INPUT SIGNAL
(at $T_A = +85^\circ\text{C}$)

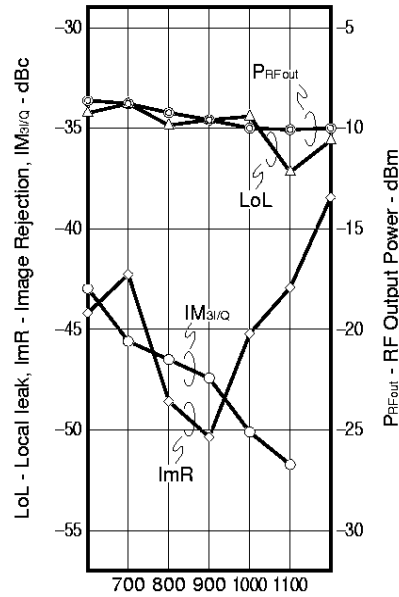


Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/3/Q}
(at V_{CC} = 2.7 V, T_A = -40 °C)



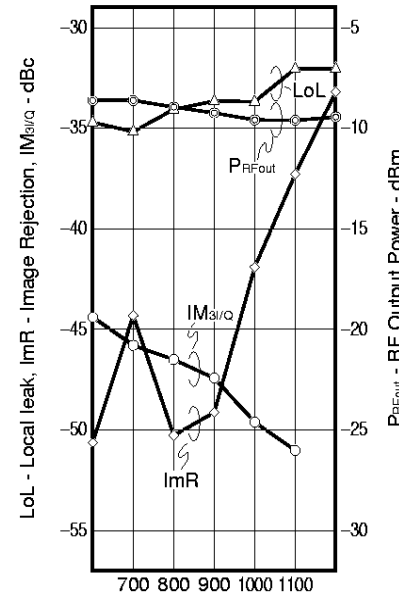
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/3/Q}
(at V_{CC} = 3.0 V, T_A = -40 °C)



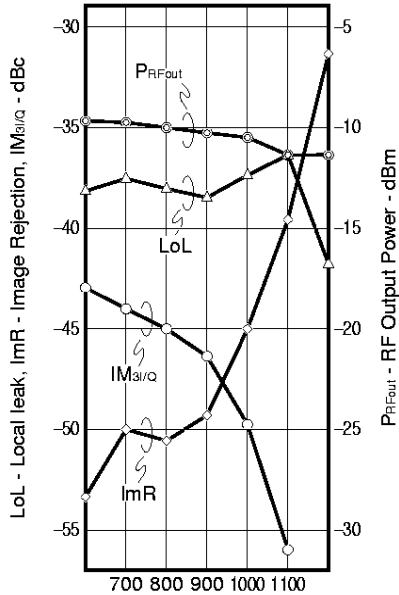
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/3/Q}
(at V_{CC} = 3.6 V, T_A = -40 °C)



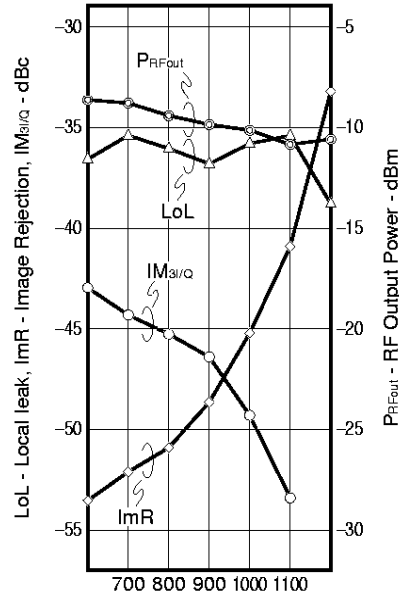
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/3/Q}
(at V_{CC} = 2.7 V, T_A = +25 °C)



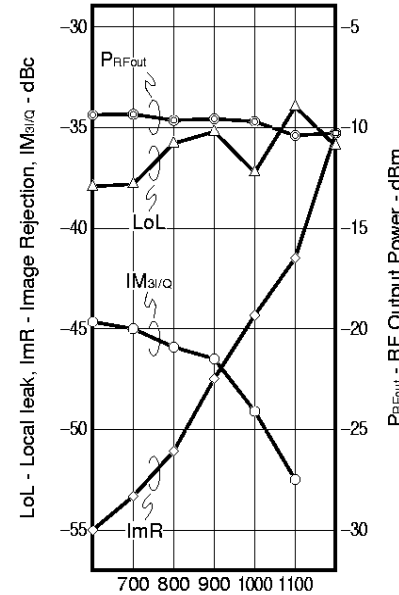
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/3/Q}
(at V_{CC} = 3.0 V, T_A = +25 °C)



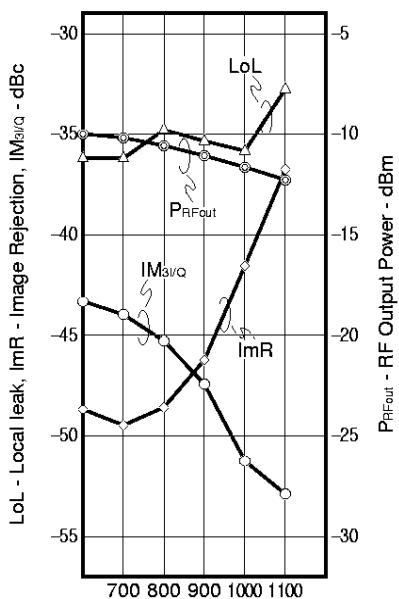
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/3/Q}
(at V_{CC} = 3.6 V, T_A = +25 °C)



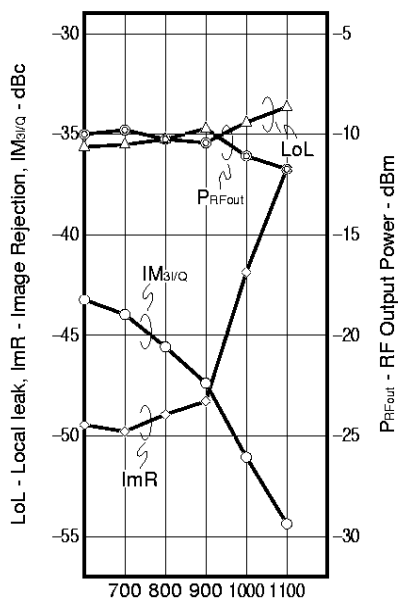
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
 P_{RFout} , LoL, ImR, $IM_{3/Q}$
 (at $V_{CC} = 2.7\text{ V}$, $T_A = +85\text{ }^{\circ}\text{C}$)



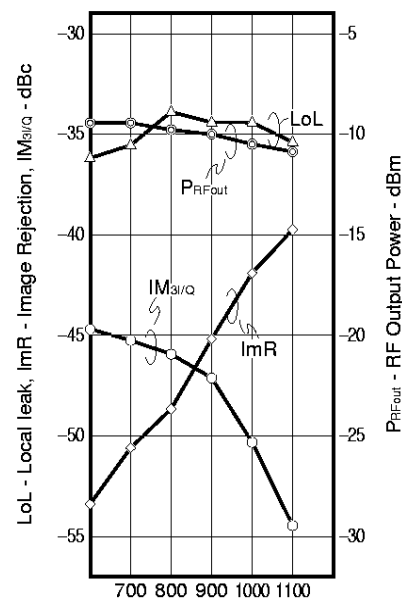
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
 P_{RFout} , LoL, ImR, $IM_{3/Q}$
 (at $V_{CC} = 3.0\text{ V}$, $T_A = +85\text{ }^{\circ}\text{C}$)



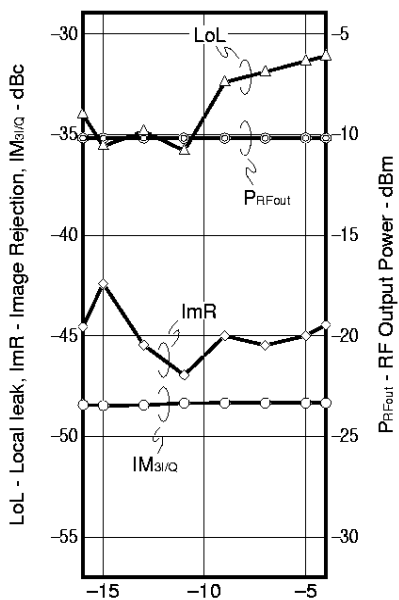
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
 P_{RFout} , LoL, ImR, $IM_{3/Q}$
 (at $V_{CC} = 3.6\text{ V}$, $T_A = +85\text{ }^{\circ}\text{C}$)



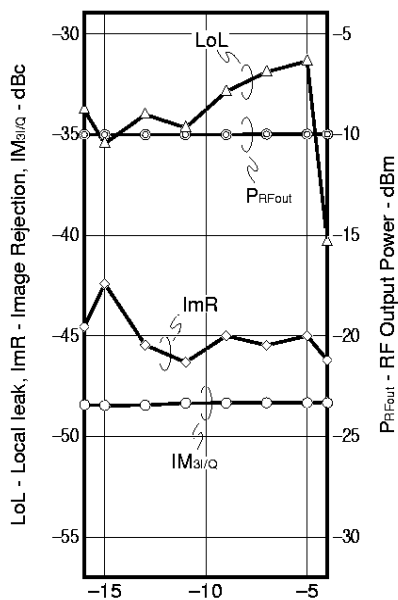
f_{LO} - Local Input Frequency - MHz

Lo INPUT POWER vs
 P_{RFout} , LoL, ImR, $IM_{3/Q}$
 (at $V_{CC} = 2.7\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$)



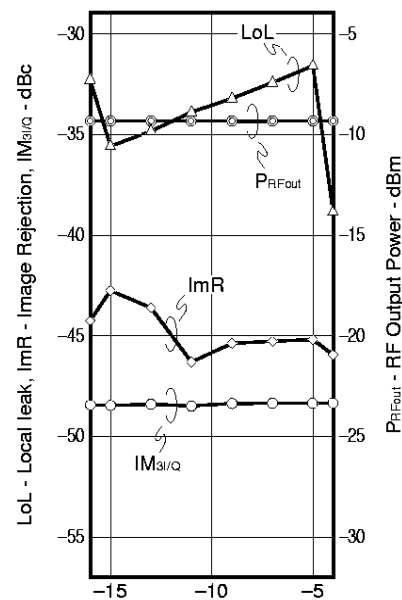
P_{Lo} - Local Input Power - dBm

Lo INPUT POWER vs
 P_{RFout} , LoL, ImR, $IM_{3/Q}$
 (at $V_{CC} = 3.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$)



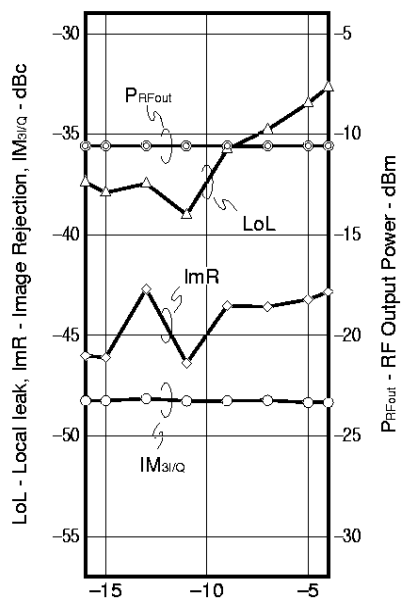
P_{Lo} - Local Input Power - dBm

Lo INPUT POWER vs
 P_{RFout} , LoL, ImR, $IM_{3/Q}$
 (at $V_{CC} = 3.6\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$)



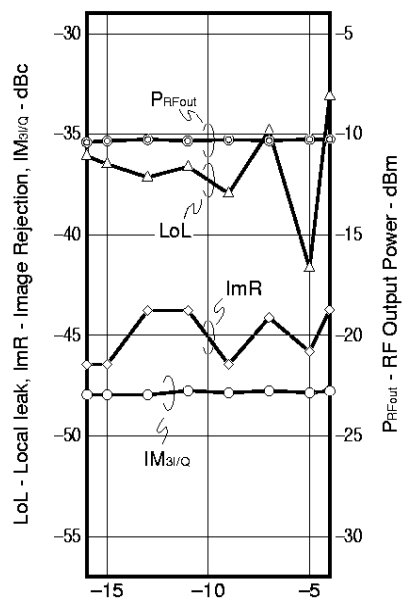
P_{Lo} - Local Input Power - dBm

Lo INPUT POWER vs
 P_{RFout} , LoL, ImR, IM_{3/3/Q}
(at $V_{CC} = 2.7\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$)



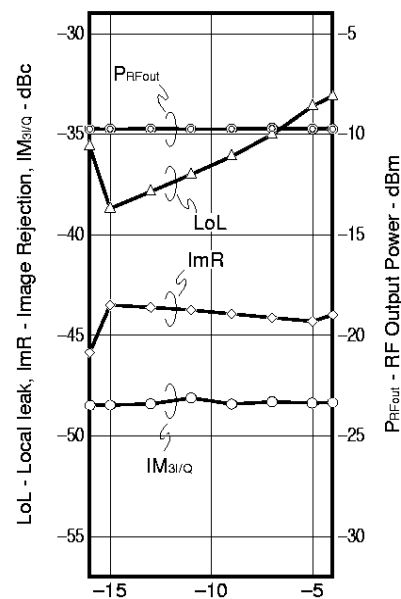
Lo - Local Input Power - dBm

Lo INPUT POWER vs
 P_{RFout} , LoL, ImR, IM_{3/3/Q}
(at $V_{CC} = 3.0\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$)



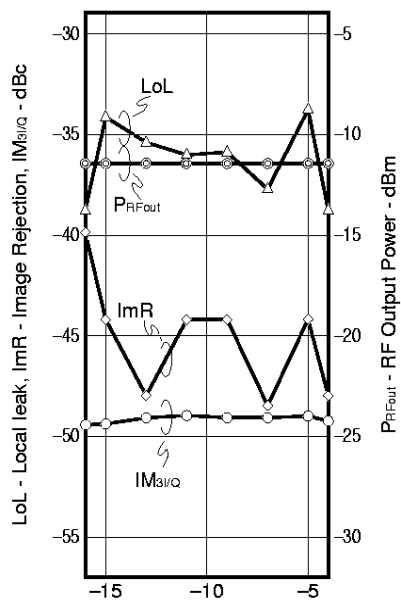
Lo - Local Input Power - dBm

Lo INPUT POWER vs
 P_{RFout} , LoL, ImR, IM_{3/3/Q}
(at $V_{CC} = 3.6\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$)



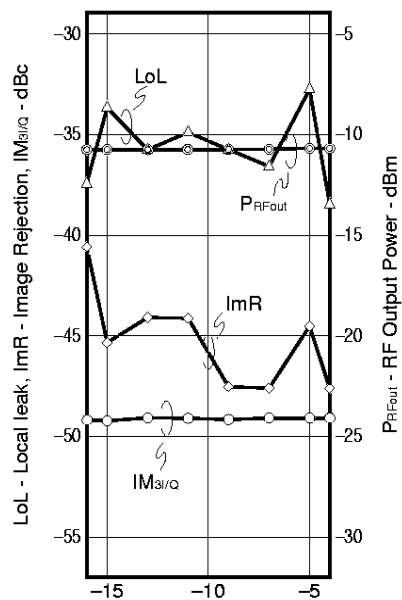
Lo - Local Input Power - dBm

Lo INPUT POWER vs
 P_{RFout} , LoL, ImR, IM_{3/3/Q}
(at $V_{CC} = 2.7\text{ V}$, $T_A = +85\text{ }^{\circ}\text{C}$)



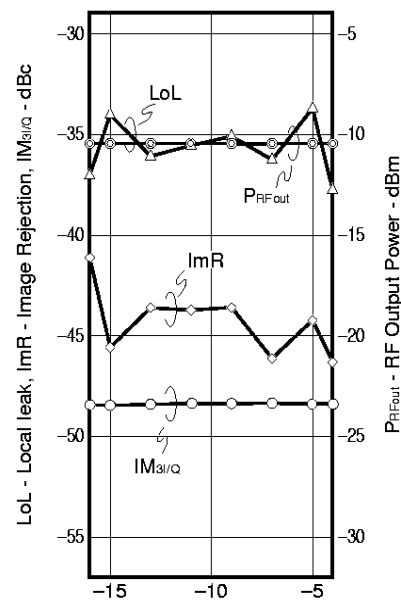
Lo - Local Input Power - dBm

Lo INPUT POWER vs
 P_{RFout} , LoL, ImR, IM_{3/3/Q}
(at $V_{CC} = 3.0\text{ V}$, $T_A = +85\text{ }^{\circ}\text{C}$)

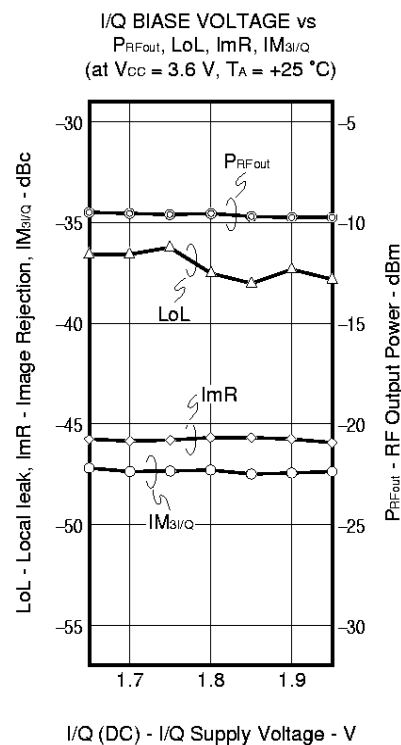
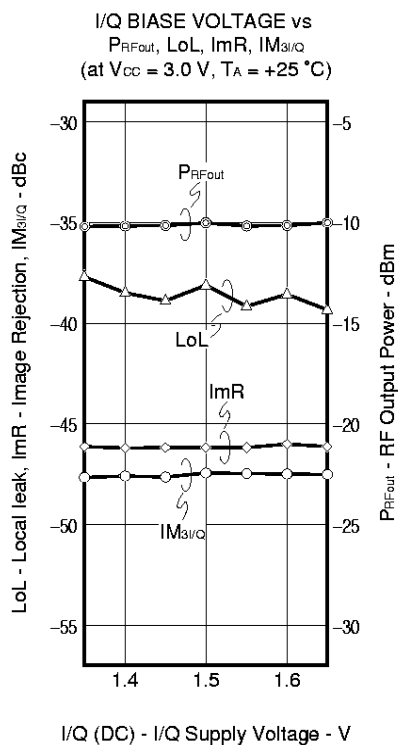
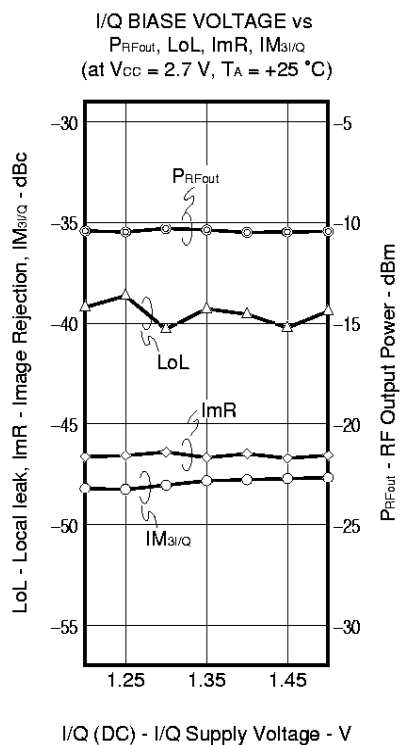
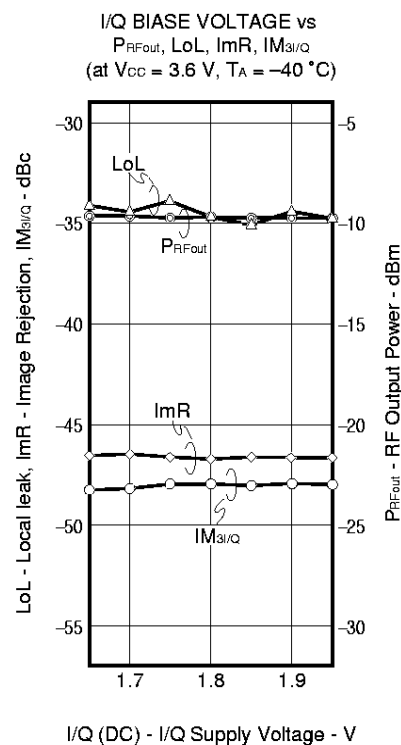
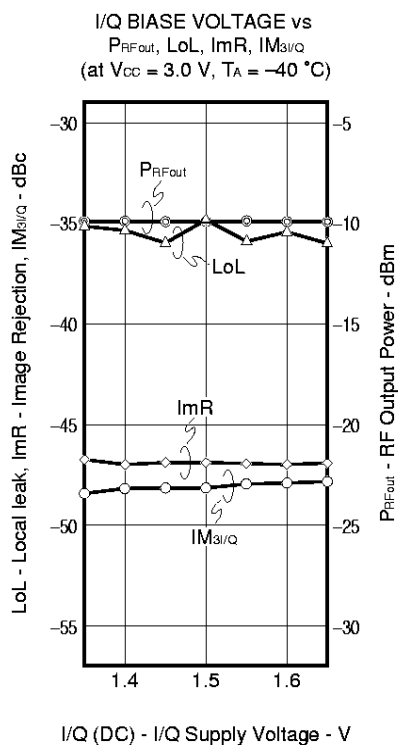
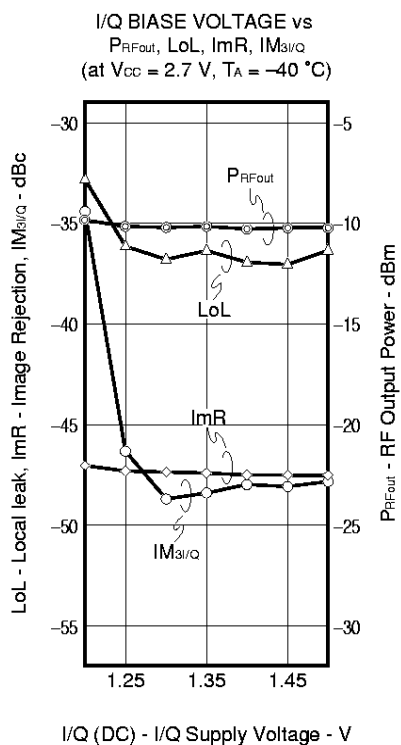


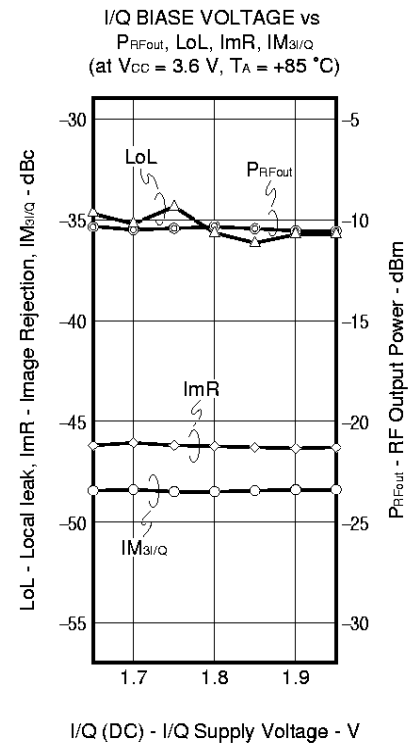
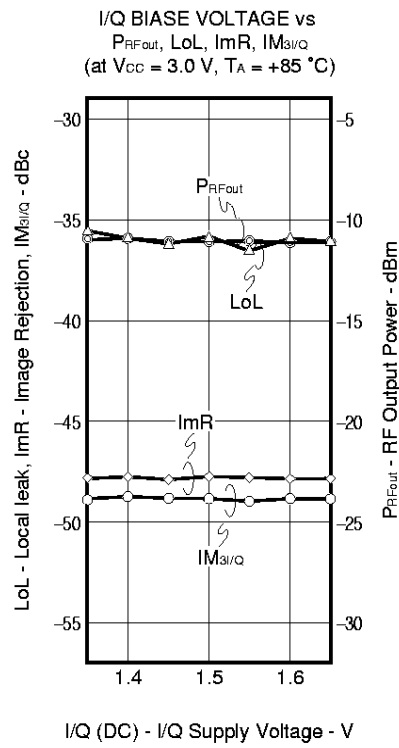
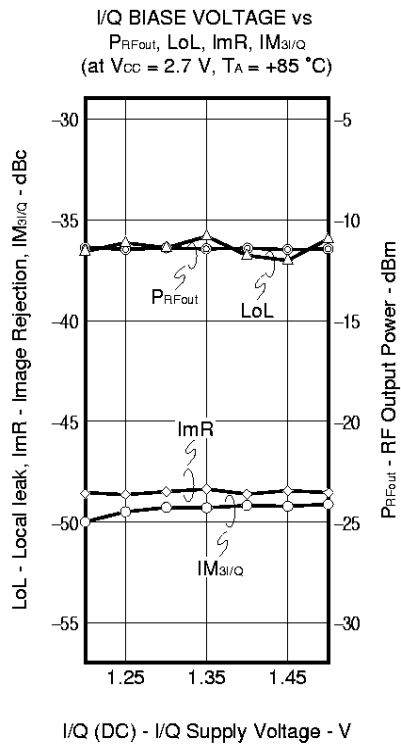
Lo - Local Input Power - dBm

Lo INPUT POWER vs
 P_{RFout} , LoL, ImR, IM_{3/3/Q}
(at $V_{CC} = 3.6\text{ V}$, $T_A = +85\text{ }^{\circ}\text{C}$)

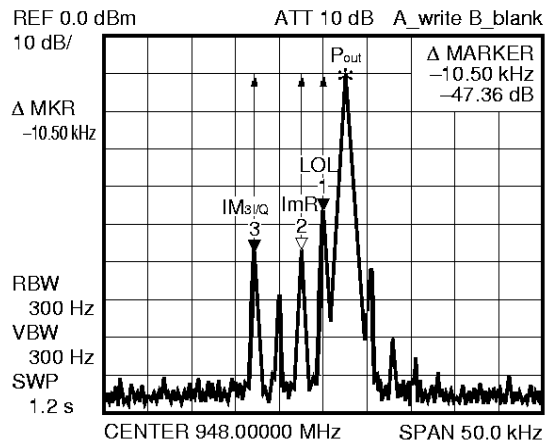


Lo - Local Input Power - dBm

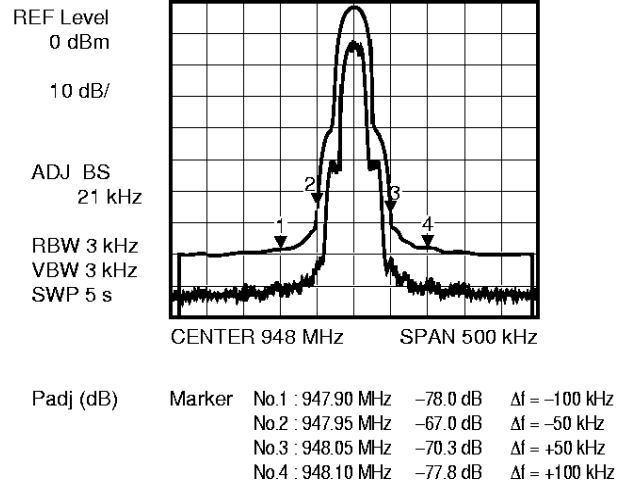




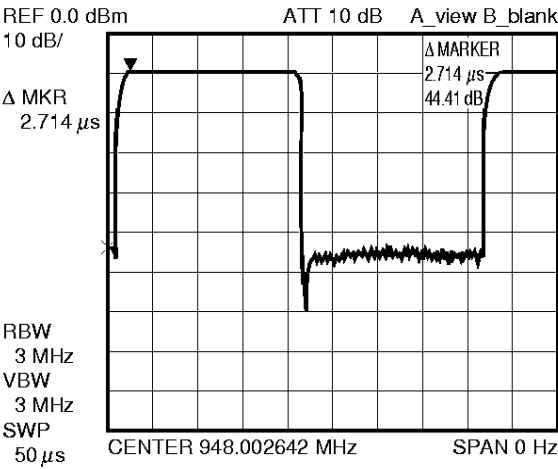
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM
<PDC> 42 kbps, RNYQ $\alpha = 0.5$, MOD Pattern [0000]



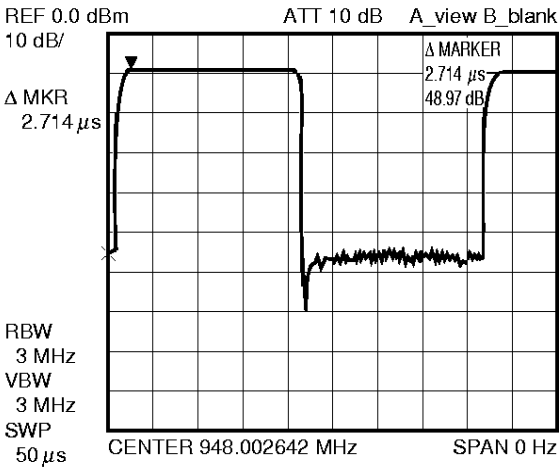
TYPICAL $\pi/4$ QPSK MODULATION OUTPUT SPECTRUM
<PDC> 42 kbps, RNYQ $\alpha = 0.5$, MOD Pattern [PN9]



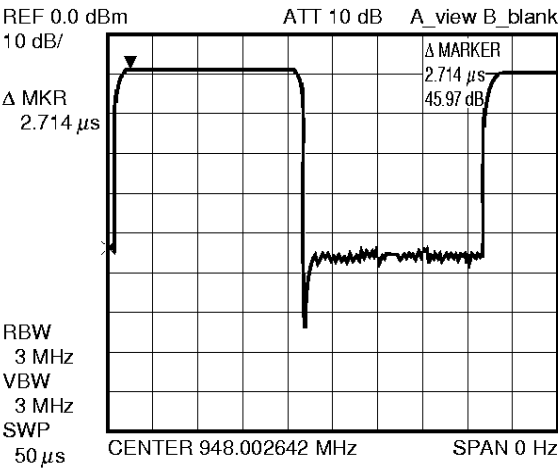
POWER SAVE RESPONSE
(at $V_{CC} = V_{PS} = 2.7\text{ V}$)



POWER SAVE RESPONSE
(at $V_{CC} = V_{PS} = 3.0\text{ V}$)

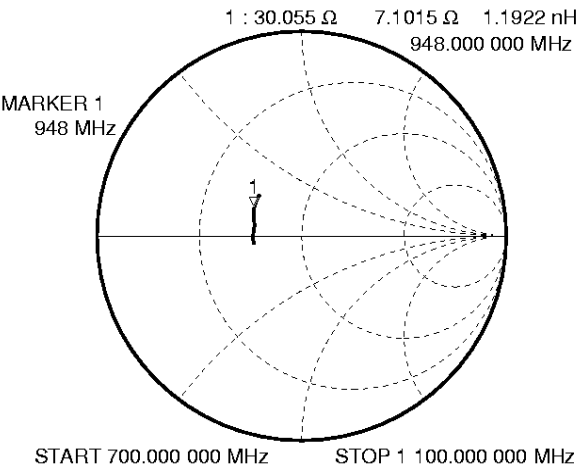


POWER SAVE RESPONSE
(at $V_{CC} = V_{PS} = 3.6\text{ V}$)

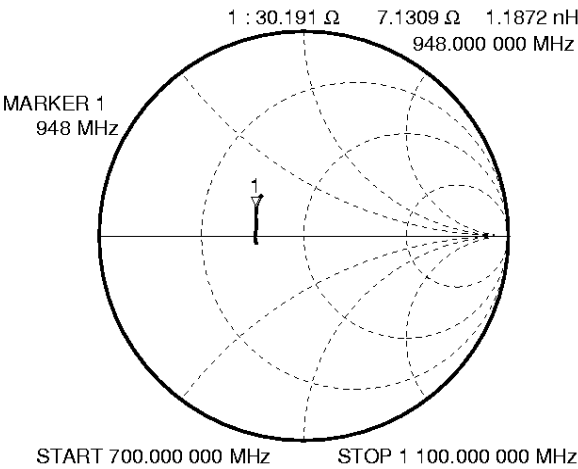


Lo INPUT (Loin) IMPEDANCE

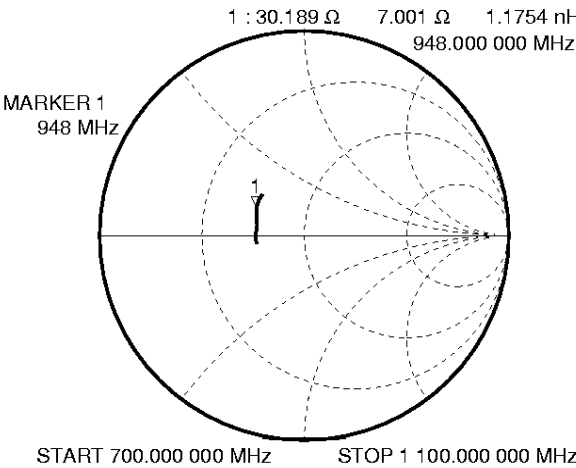
$V_{CC} = V_{PS} = 2.7\text{ V}$



$V_{CC} = V_{PS} = 3.0\text{ V}$

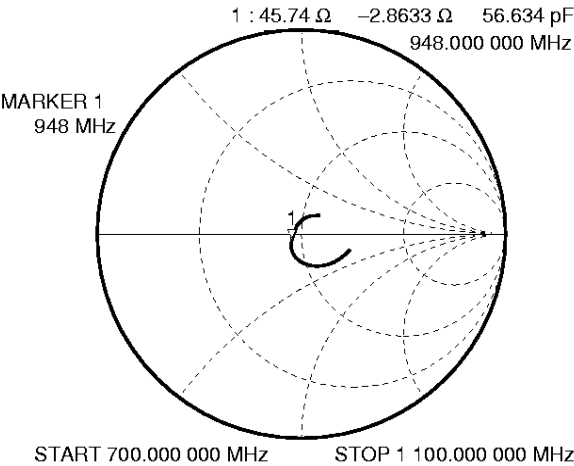


$V_{CC} = V_{PS} = 3.6\text{ V}$

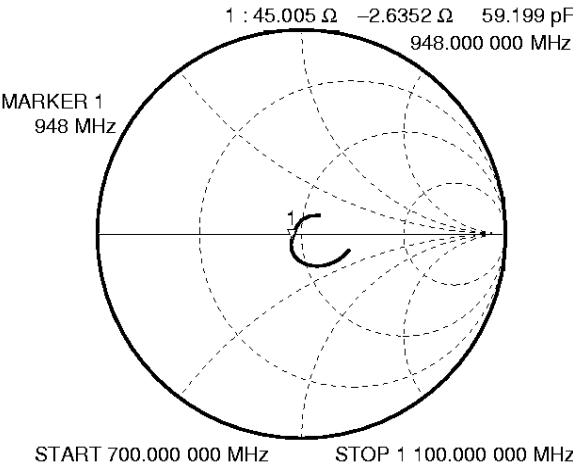


RF OUTPUT (RF_{out}) IMPEDANCE

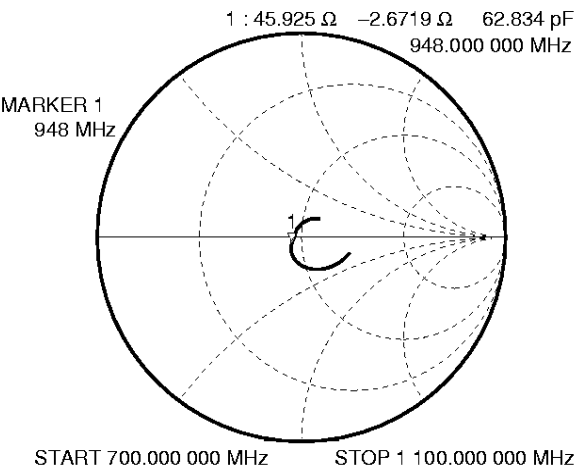
V_{CC} = V_{PS} = 2.7 V



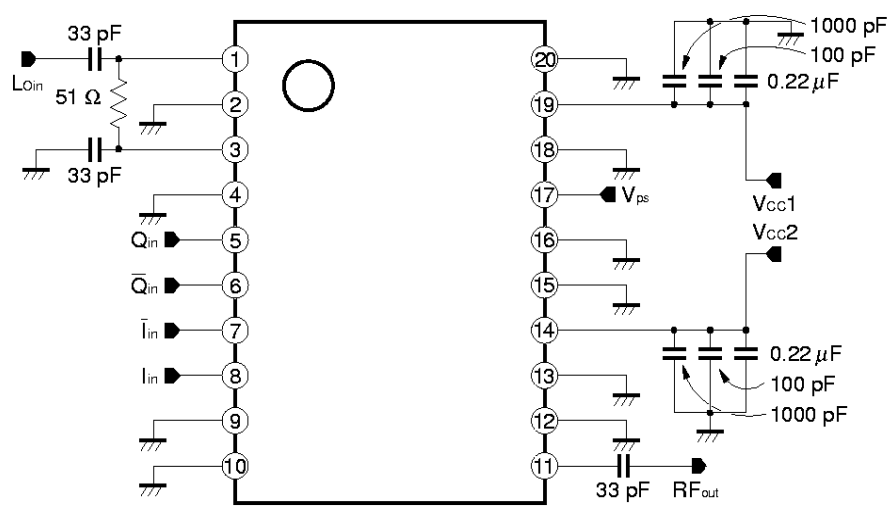
V_{CC} = V_{PS} = 3.0 V



V_{CC} = V_{PS} = 3.6 V

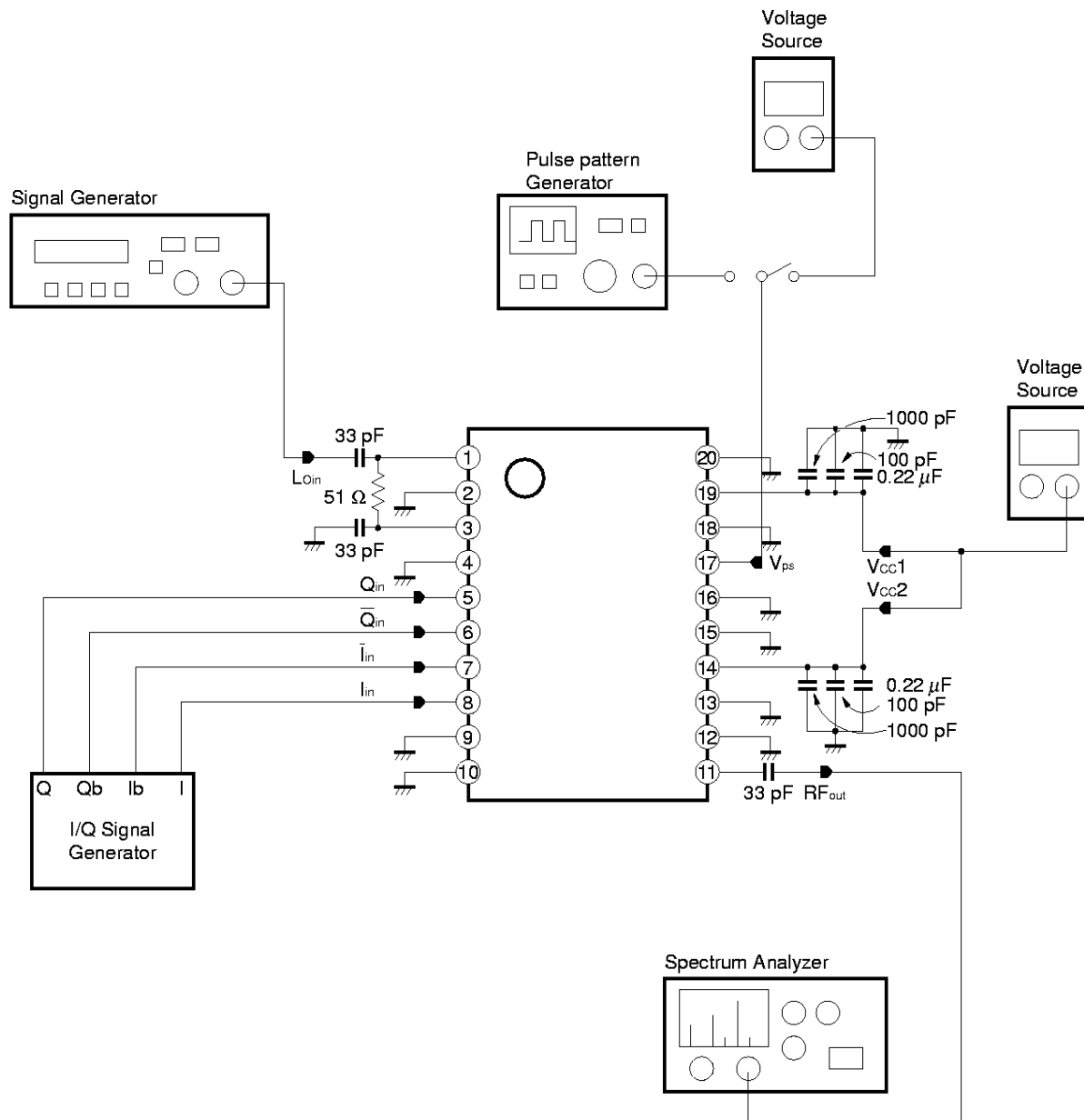


TEST CIRCUIT



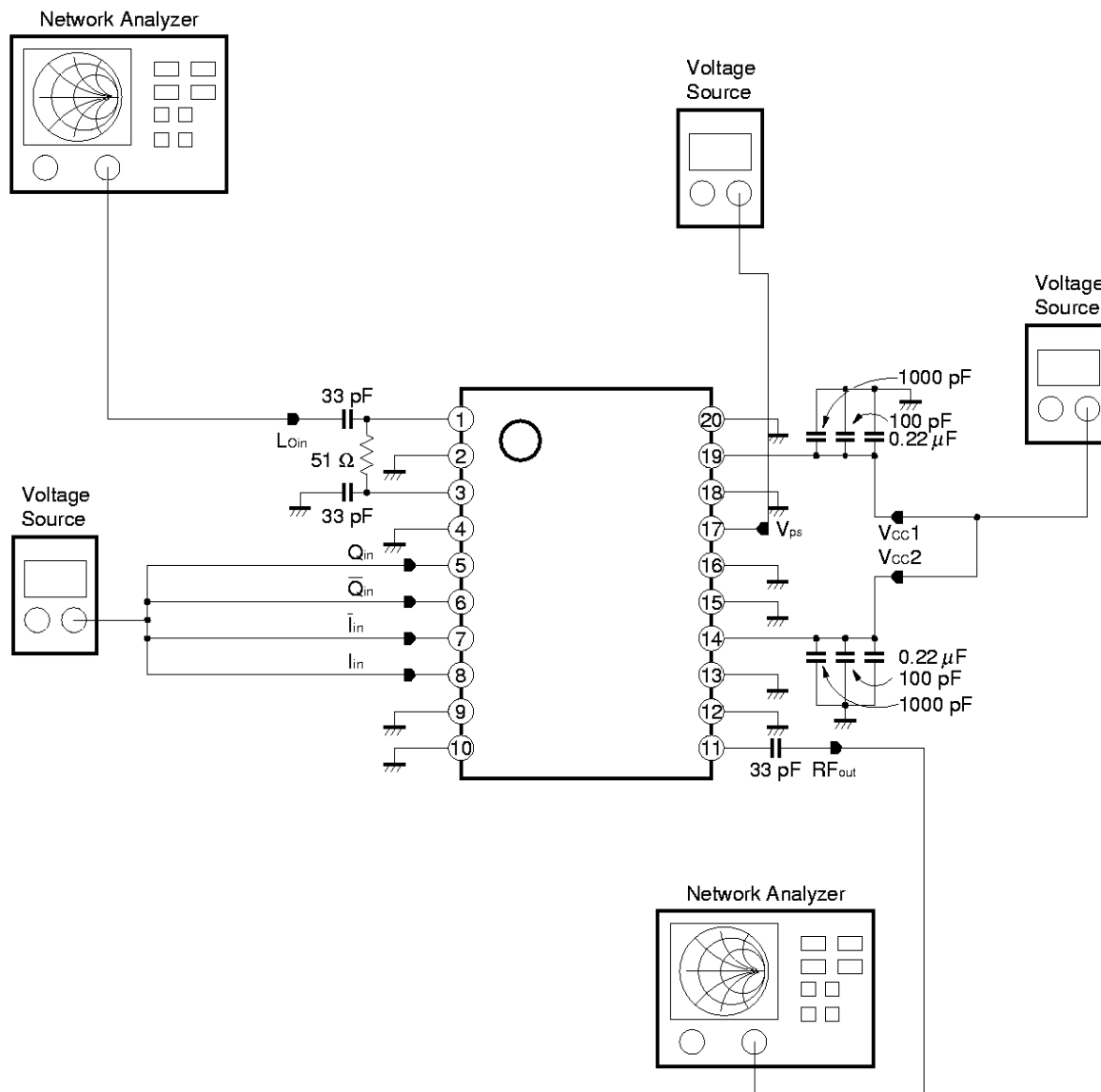
MEASUREMENT BLOCK DIAGRAM 1

(RF Output Power, Local Carrier Leak, Image Rejection, I/Q 3rd Order Intermodulation Distortion and Power Save Rise and Fall Time)

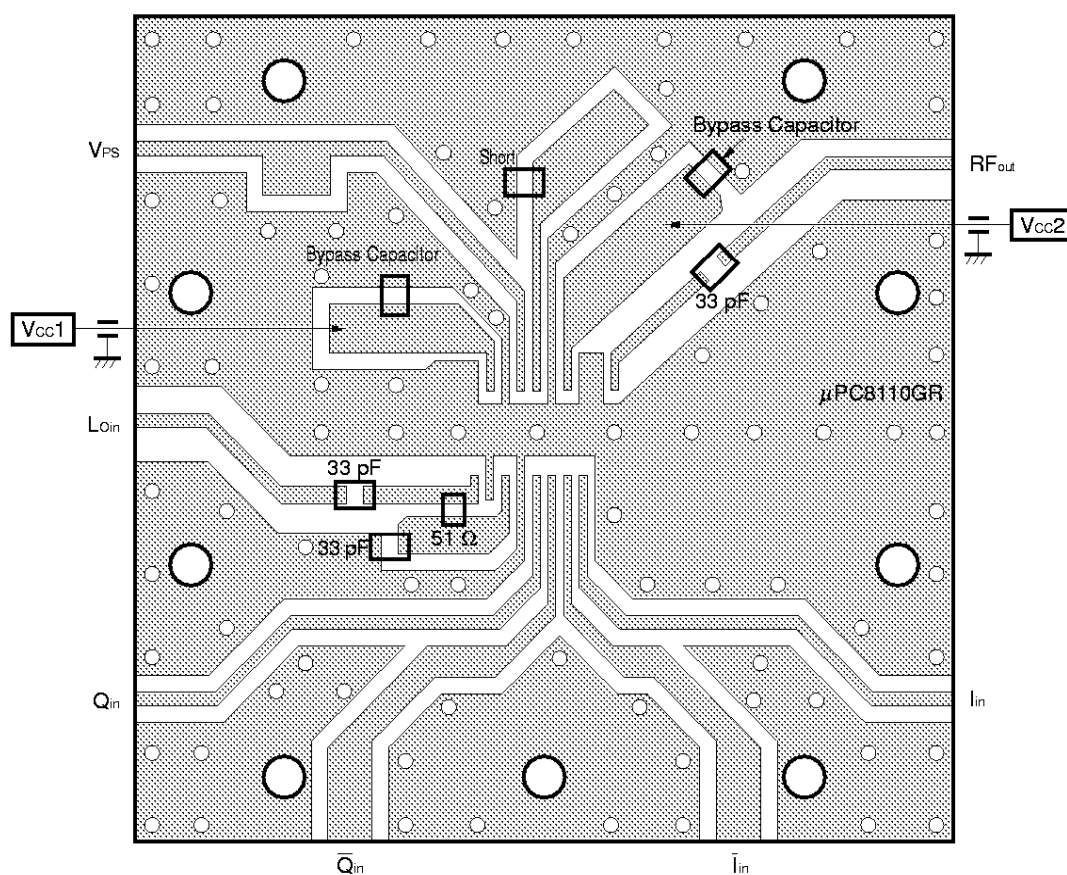


MEASUREMENT BLOCK DIAGRAM 2

(Local Input VSWR and RF Output VSWR)



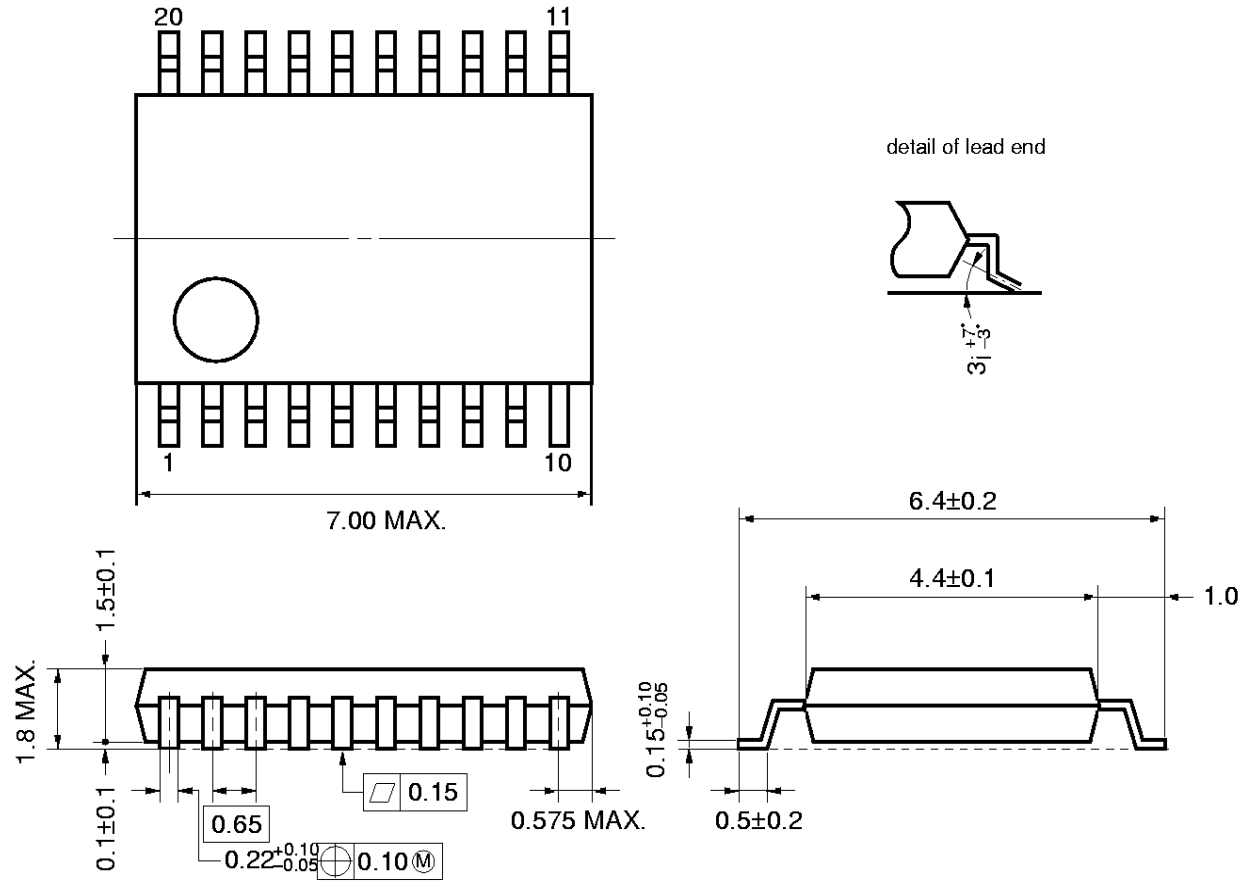
TEST BOARD



- Notes
1. Double-sided patterning with 35 μm thick copper on polyimide board sizing 50 u 50 u 0.4 mm.
 2. GND pattern on backside.
 3. Solder coating over patterns.
 4. { , $\bigcirc$ indicate through-holes.

PACKAGE DIMENSIONS (Unit: mm)

20 pin plastic SSOP (225 mil)



NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electrostatic sensitive devices.
- (2) Form a ground pattern as wide as possible to keep the minimum ground impedance (to prevent undesired oscillation).
- (3) Keep the track length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (e.x. 1 000 pF) to the Vcc pin.
- (5) $\overline{I}$, $\overline{Q}$ DC offset voltage should be same as the I, Q DC offset voltage (to prevent changing the local leak level with power save control.)

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering method and conditions than the recommended conditions are to be consulted with our sales representatives.

PPC8110GR

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 3, Exposure limit ^{Note} : None	IR35-00-3
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 3, Exposure limit ^{Note} : None	VP15-00-3
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit ^{Note} : None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 3 seconds/pin or below, Exposure limit ^{Note} : None	

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Apply only a single process at once, except for "Partial heating method".

[MEMO]

[MEMO]

[MEMO]

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.