EM 6620

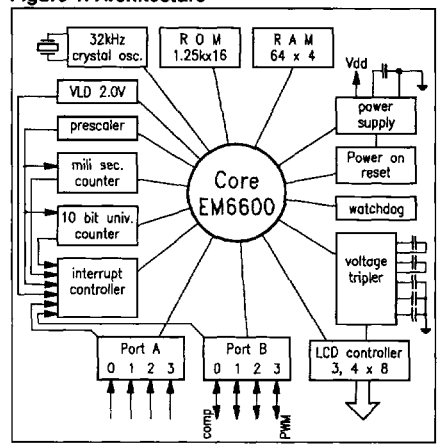
NEW!
MFP Version EM6520
(Multiple Field Programmable)

4-Bit Microcontroller

Features

- Low Power - 2.1 µ A active mode
  - 0.5 µ A standby mode (No LCD)
  - 0.15 µA sleep mode @ 1.5 V, 32 kHz, 20 °C
- Low Voltage - 1.2 to 3.6 V
- SVLD - metal mask programmable (2.0 V)
- ROM - 1280 × 16
- RAM - 64 × 4
- 2 clocks per instruction cycle
- 72 basic instructions
- Oscillation supervisor
- Timer watchdog (2 sec)
- Max. 8 inputs (2 ports)
- Max. 4 outputs (1 port)
- LCD 8 segments, 3 or 4 times multiplexed
- Universal 10-bit counter / PWM / event counter
- 1/1000 sec, 12 bit binary coded decimal counter
- Frequency output 1 Hz, 2048 Hz, 32 kHz, PWM
- 7 internal interrupt sources (1 × ms counter, 2 × counter, 3 × prescaler, SVLD)
- 5 external interrupt sources (port A, compare)

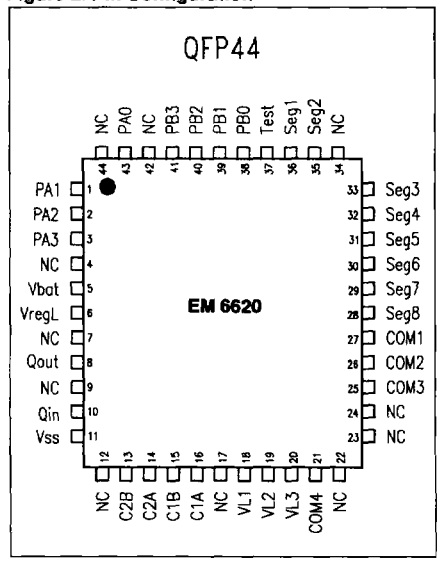
Figure 1. Architecture



Description

The EM66XX series is an advanced single-chip low-cost CMOS 4-bit microcontroller. It contains ROM, RAM, power on reset, watchdog timer, oscillation detection circuit, 10 bit up/down counter, 1 ms counter, prescaler, voltage level detector (SVLD), compare input, frequency output, LCD driver and several clock functions. The low voltage feature and low power consumption make it the most suitable controller for battery, stand alone and mobile equipment. The EM66XX series is manufactured using EM's Advanced Low-Power (ALP) CMOS Process.

Figure 2. Pin Configuration



Typical Applications

- Timing device
- Medical applications
- Domestic appliance
- Timer / sports timing devices
- Safety and security devices
- Automotive controls with display
- Measurement equipment
- Interactive system with display
- Bicycle computers

12

EM6620 at a glance

- **Power Supply**
- Low-voltage low-power architecture including internal voltage regulator
- 1.2 ... 3.6 V battery voltage
- 2.1 µA in active mode (25 °C)
- 0.50 µA in standby mode (LCD off, 25 °C)
- 0.15 µA in sleep mode (25 °C)
- 32 kHz oscillator

- **RAM**
- 64 x 4 bits, direct addressable

- **ROM**
- 1280 x 16 bits, metal mask programmable

- **CPU**
- 4 bit RISC architecture
- 2 clock cycles per instruction
- 72 basic instructions

- **Main Operating Modes and Resets**
- Active mode (CPU is running)
- Standby mode (CPU in Halt)
- Sleep mode (no clock, reset state)
- Initial reset on power on (POR)
- Watchdog reset (logic and oscillation watchdogs)
- Reset with input combination on port A (register selectable)

- **Liquid Crystal Display Driver (LCD)**
- 8 segments 3 or 4 times multiplexed
- Internal or external voltage tripler
- Free segment allocation architecture (metal 2 mask)
- LCD switch off for power save

- **4-Bit Input Port A**
- Direct input read on the port terminals
- Debounced or direct interrupt requests from each input
- Interrupt request on positive or negative edge
- Pull-up, pull-down or none, selectable by register
- Test variables (software) for conditional jumps
- PA[0] and PA[3] are inputs for the event counter
- PA[3] is start/stop input for the milli-second counter
- Reset with input combination (register selectable)

- **Prescaler**
- 15 stage system clock divider down to 1 Hz
- 3 Interrupt requests; 1 Hz, 32 Hz or 8 Hz, blink
- Prescaler reset (4 kHz to 1 Hz)

- **4-Bit Bi-Directional Port B**
- All different functions bit wise selectable
- Direct input read on the port terminals
- Data output latches
- CMOS or N-channel open drain outputs
- Pull-down or pull-up selectable
- Weak pull-up in N-channel open drain mode
- Selectable PWM, 32 kHz, 2 kHz and 1 Hz output
- Dynamic input comparator on PB[0] (SVLD level)

- **Voltage Level Detector**
- Mask selectable level, default 2.0 V
- Busy flag during measure
- Interrupt request at end of measure

- **10-Bit Universal Counter**
- 10, 8, 6 or 4 bit up/down counting
- Parallel load
- 8 different input clocks
- Event counting with PA[0] or PA[3] as input clocks
- Full 10 bit or limited (8, 6, 4 bit) compare function
- 2 interrupt requests (on compare and on 0)
- Hi-frequency input on PA[3] and PA[0]
- Pulse width modulation (**PWM**) output possible on PB[3]

- **Milli-Second Counter**
- 3 digits binary coded decimal counter (12 bits)
- Internal 1000 Hz clock generation
- PA[3] input signal pulse width and period measurement
- Hardware or software controlled start stop mode
- Interrupt request on either 1/10 s or 1 s

- **Interrupt Controller**
- 5 external and 7 internal interrupt request sources
- Each interrupt request individually maskable
- Each interrupt flag individually resettable
- Automatic reset of each interrupt request register read
- General interrupt request to CPU can be disabled
- Automatic enabling of general interrupt request flag when going into HALT mode