



3.3V CMOS 12-BIT SYNCHRONOUS BUS EXCHANGER WITH BUS-HOLD AND 5 VOLT TOLERANT I/O

IDT74LVCH16276A

FEATURES:

- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH16276A:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION

The LVCH16276A synchronous bus exchanger is built using advanced dual metal CMOS technology. The LVCH16276A is a high-speed, bidirectional, 12-bit, registered, bus multiplexer for use in synchronous memory interleaving applications. All registers have a common clock and use a clock enable ($\overline{CE}_{xx}$) on each data register to control data sequencing. The output enables and mux select ($\overline{OE}_A$, $\overline{OE}_B$ and SEL) are also under synchronous control allowing direction changes to be edge triggered events.

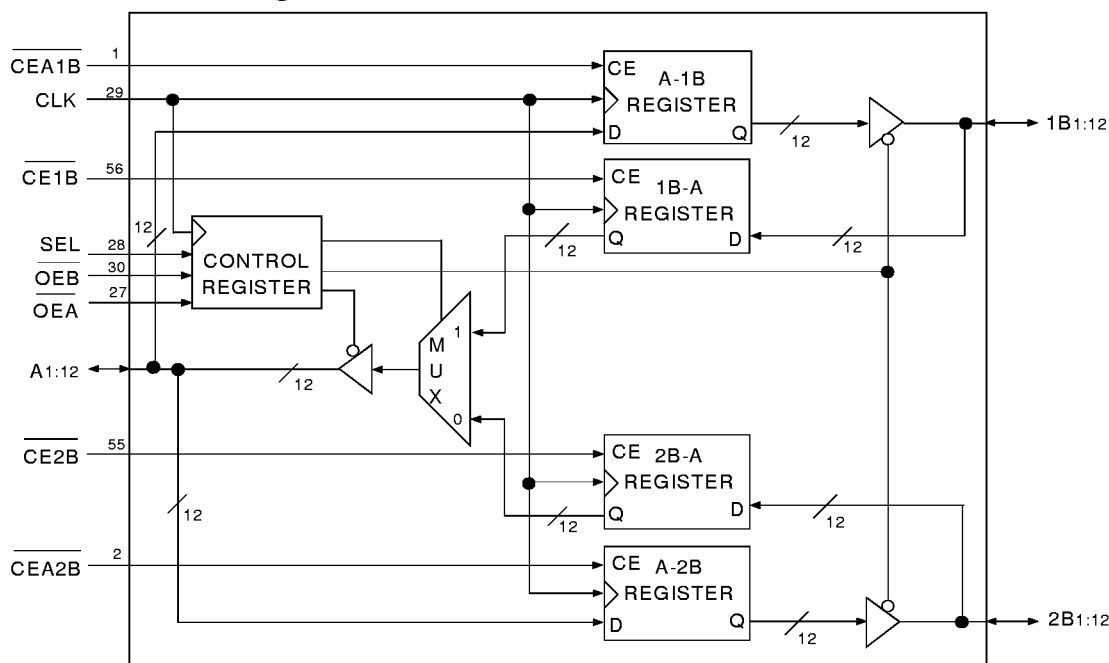
The tri-port bus exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The clock enable ($\overline{CE}_{1B}$, $\overline{CE}_{2B}$, $\overline{CE}_{A1B}$ and $\overline{CE}_{A2B}$) inputs control the data storage. Both B ports have a common output enable ($\overline{OE}_B$) to aid in synchronously loading the B registers from the B port.

All pins of the LVCH16276A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH16276A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16276A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

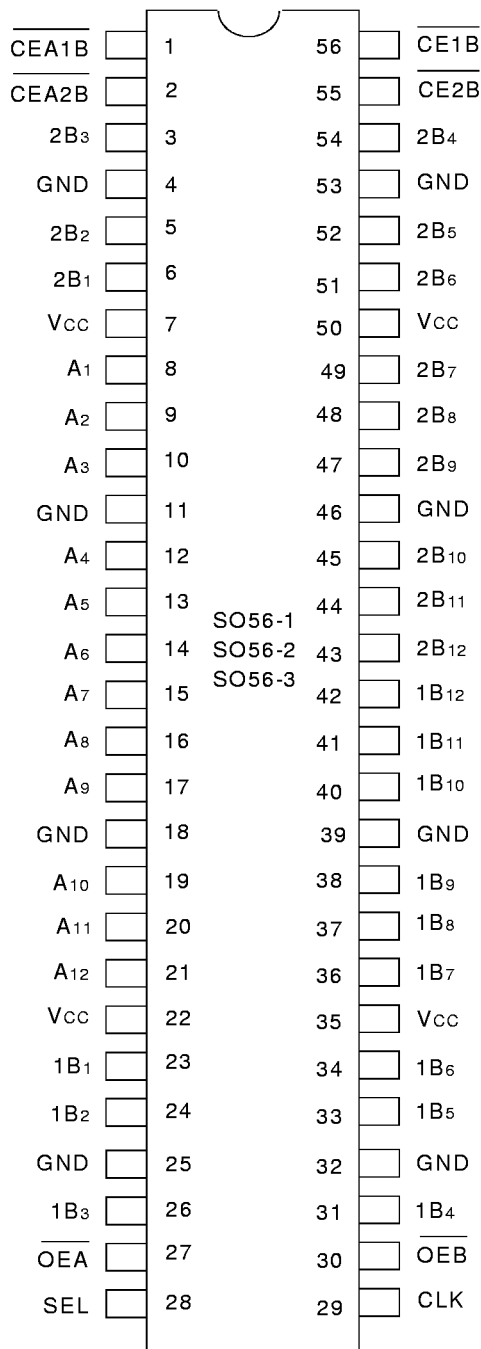
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

MARCH 1999

PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
TSTG	Storage Temperature	– 65 to +150	°C
IOUT	DC Output Current	– 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

LVC Link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

LVC Link

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

A(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. ⁽¹⁾
1B(1:12)	I/O	Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory. ⁽¹⁾
2B(1:12)	I/O	Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory. ⁽¹⁾
CLK	I	Clock Input.
$\overline{\text{CEA1B}}$	I	Clock Enable Input for the A-1B Register. If $\overline{\text{CEA1B}}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).
$\overline{\text{CEA2B}}$	I	Clock Enable Input for the A-2B Register. If $\overline{\text{CEA2B}}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).
$\overline{\text{CE1B}}$	I	Clock Enable Input for the 1B-A Register. If $\overline{\text{CE1B}}$ is LOW during the rising edge of CLK, data will be clocked into register 1B-A (Active LOW).
$\overline{\text{CE2B}}$	I	Clock Enable Input for the 2B-A Register. If $\overline{\text{CE2B}}$ is LOW during the rising edge of CLK, data will be clocked into register 2B-A (Active LOW).
SEL	I	1B or 2B Part Selection. When HIGH during the rising edge of CLK, SEL enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, SEL enables data transfer from 2B Port to A Port.
$\overline{\text{OE A}}$	I	Synchronous Output Enable for A Port (Active LOW).
$\overline{\text{OEB}}$	I	Synchronous Output Enable for 1B Port and 2B Port (Active LOW).

NOTE:

1. These pins have "Bus-hold". All other pins have inputs, outputs, or I/Os.

FUNCTION TABLES (1)

Inputs							Outputs
1Bx	2Bx	SEL	$\overline{\text{CE1B}}$	$\overline{\text{CE2B}}$	$\overline{\text{OE A}}$	CLK	Ax
H	X	H	L	X	L	↑	H
L	X	H	L	X	L	↑	L
X	X	H	H	X	L	↑	A ₀ ⁽²⁾
X	H	L	X	L	L	↑	H
X	L	L	X	L	L	↑	L
X	X	L	X	H	L	↑	A ₀ ⁽²⁾
X	X	X	X	X	H	↑	Z

Inputs					Outputs	
Ax	$\overline{\text{CEA1B}}$	$\overline{\text{CEA2B}}$	$\overline{\text{OEB}}$	CLK	1Bx	2Bx
H	L	L	L	↑	H	H
L	L	L	L	↑	L	L
H	L	H	L	↑	H	B ₀ ⁽²⁾
L	L	H	L	↑	L	B ₀ ⁽²⁾
H	H	L	L	↑	B ₀ ⁽²⁾	H
L	H	L	L	↑	B ₀ ⁽²⁾	L
X	H	H	L	↑	B ₀ ⁽²⁾	B ₀ ⁽²⁾
X	X	X	H	↑	Z	Z
X	X	X	L	↑	Active	Active

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
- A₀, B₀ = Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾	—	—	10	
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V other inputs at V _{CC} or GND		—	—	500	μA

LVC Link

NOTES:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	—	—	—	μA
			V _I = 0.7V	—	—	—	
I _{BHHO} I _{BHLO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

LVC Link

NOTES:

- Pins with Bus-hold are identified in the pin description.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = – 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

LVC Link

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to +85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per bus exchanger Outputs enabled	CL = 0pF, f = 10Mhz		pF
CPD	Power Dissipation Capacitance per bus exchanger Outputs disabled			pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter		V _{CC} = 2.7V		V _{CC} = 3.3V±0.3V		Unit
			Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay CLK to 1Bx or CLK to 2Bx		1.5	6.6	1.5	5.7	ns
t _{PLH} t _{PHL}	Propagation Delay CLK to Ax	SEL Stable $\overline{\text{CE}}\text{x}\overline{\text{B}}$ Enabled	1.5	7	1.5	5.8	ns
		SEL Changing $\overline{\text{CE}}\text{x}\overline{\text{B}}$ Disabled	1.5	7.5	1.5	6.5	ns
		SEL Changing $\overline{\text{CE}}\text{x}\overline{\text{B}}$ Enabled	1.5	7.6	1.5	6.6	ns
t _{PZH} t _{PZL}	Output Enable Time CLK to Ax, CLK to 1Bx, or CLK to 2Bx		1.5	6.8	1.5	5.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time CLK to Ax, CLK to 1Bx, or CLK to 2Bx		1.5	6.6	1.5	6.6	ns
t _{SU}	Set-Up Time, HIGH or LOW Data to CLK		1.5	—	1.5	—	ns
t _{SU}	Set-Up Time, $\overline{\text{OE}}\text{A}$ to CLK, $\overline{\text{OE}}\text{B}$ to CLK		1.5	—	1.5	—	ns
t _{SU}	Set-Up Time, SEL to CLK		1.5	—	1.5	—	ns
t _{SU}	Set-Up Time, $\overline{\text{CE}}\text{A}1\overline{\text{B}}$ to CLK, $\overline{\text{CE}}1\overline{\text{B}}$ to CLK $\overline{\text{CE}}2\overline{\text{B}}$ to CLK, or $\overline{\text{CE}}\text{A}2\overline{\text{B}}$ to CLK		1.8	—	1.8	—	ns
t _H	Hold Time, CLK to Data		1	—	1	—	ns
t _H	Hold Time, CLK to $\overline{\text{OE}}\text{A}$, CLK to $\overline{\text{OE}}\text{B}$, CLK to SEL		1	—	1	—	ns
t _H	Hold Time, CLK to $\overline{\text{CE}}\text{A}1\overline{\text{B}}$, CLK to $\overline{\text{CE}}1\overline{\text{B}}$, CLK to $\overline{\text{CE}}2\overline{\text{B}}$, CLK to $\overline{\text{CE}}\text{A}2\overline{\text{B}}$		0.7	—	0.7	—	ns
t _w	Pulse Width, CLK HIGH		2.5	—	2.5	—	ns
t _{sk(o)}	Output Skew ⁽²⁾		—	500	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

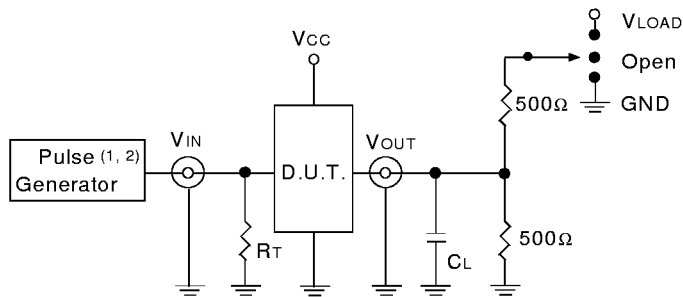
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1) = 3.3V ±0.3V	V _{CC} (1) = 2.7V	V _{CC} (2) = 2.5V ±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

LVC Link

TEST CIRCUITS FOR ALL OUTPUTS



LVC Link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

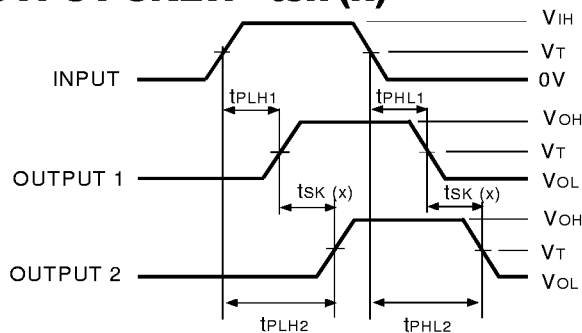
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

LVC Link

OUTPUT SKEW - t_{SK} (x)



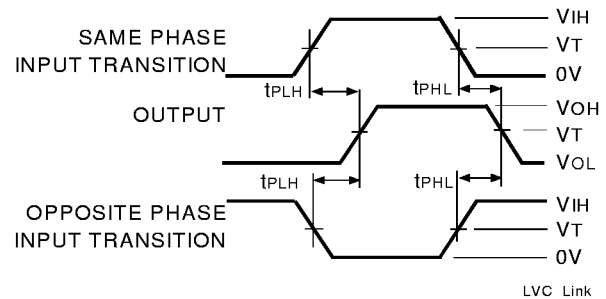
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

LVC Link

NOTES:

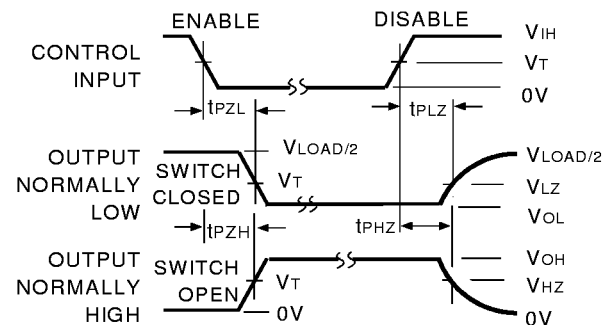
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



LVC Link

ENABLE AND DISABLE TIMES

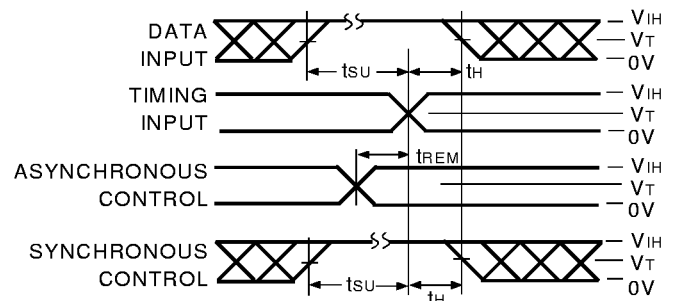


LVC Link

NOTE:

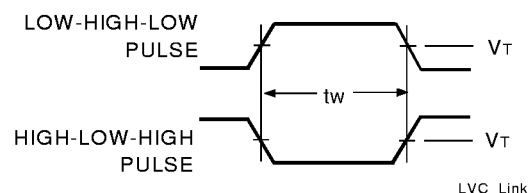
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



LVC Link

PULSE WIDTH



LVC Link

ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					276A		12-Bit Synchronous Bus Exchanger
				16			Double-Density with Resistors, $\pm 24\text{mA}$
			H				Bus-hold
	74						-40°C to +85°C



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

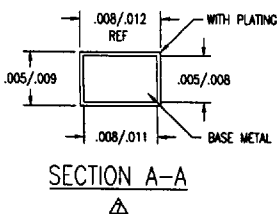
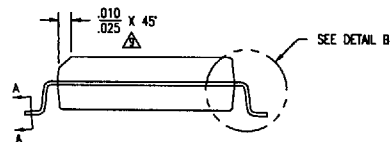
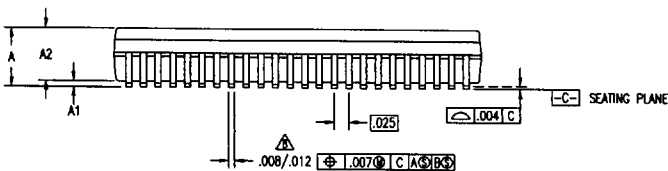
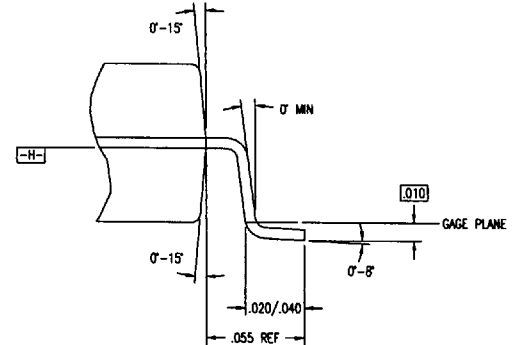
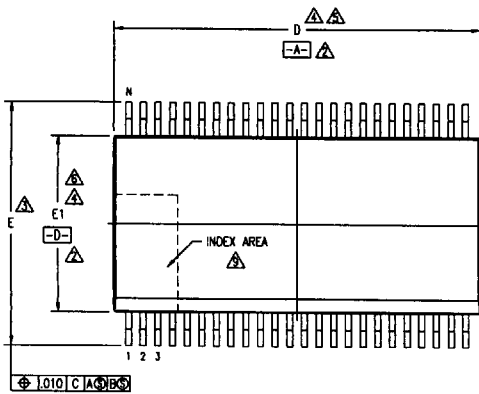
for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
www.idt.com*

*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.
 The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PACKAGE DIAGRAM OUTLINES

SSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	



TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2075 Slender Way, Santa Clara, CA 95054	
XXX	±	PHONE: (408) 727-8118	
XXX		FAX: (408) 482-8874	
XXX		TWC: 910-338-2070	
APPROVALS	DATE	TITLE	REV
DRAWN	08/15/90	PV PACKAGE OUTLINE	02
CHECKED		.300" BODY WIDTH SSOP	
		.025" PITCH	
		SIZE C	
		DRAWING No. PSC-4029	
		DO NOT SCALE DRAWING	

PACKAGE DIAGRAM OUTLINES SSOP (Continued)

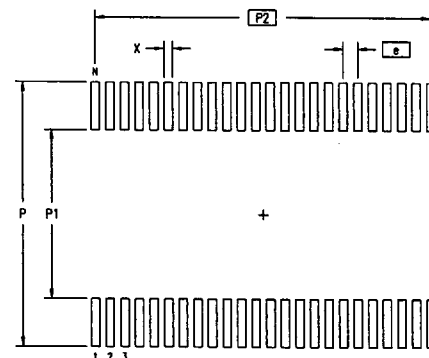
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. WJ
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

DWG #		S048-1				DWG #		S056-1			
SYMBOL	JEDEC VARIATION				NOTE	JEDEC VARIATION				NOTE	
	AA			AB							
	MIN	NOM	MAX	MIN		NOM	MAX				
A	.095	.102	.110			.095	.102	.110			
A1	.008	.012	.016			.008	.012	.016			
A2	.088	.090	.092			.088	.090	.092			
D	.620	.625	.630	4,5		.720	.725	.730	4,5		
E	.395	.405	.420	3		.395	.405	.420	3		
E1	.291	.295	.299	4,6		.291	.295	.299	4,6		
N	48					56					

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARIATION AA & AB

LAND PATTERN DIMENSIONS



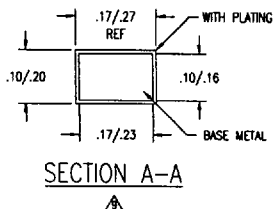
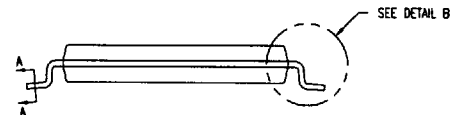
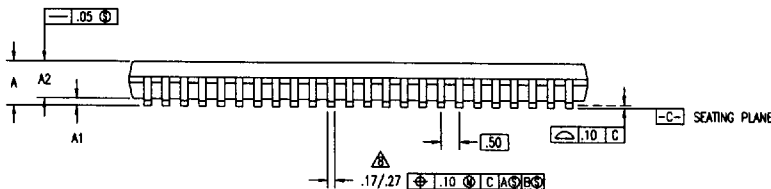
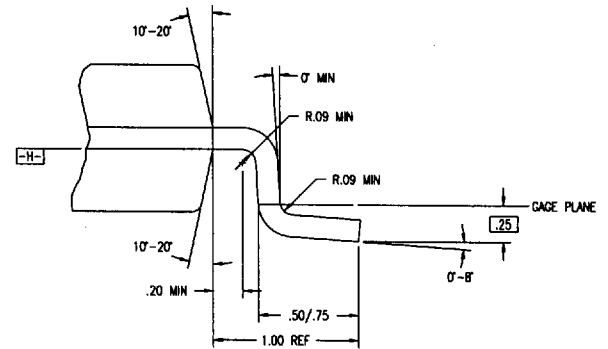
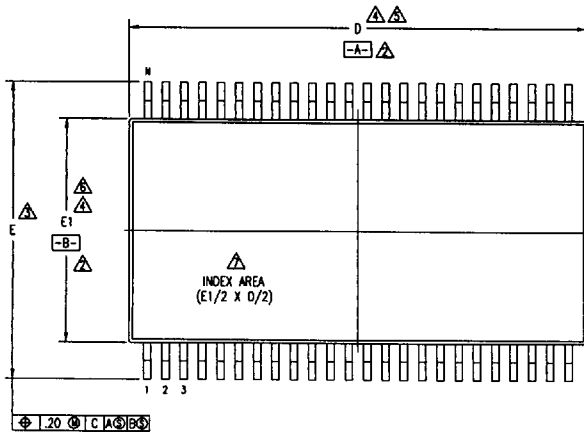
	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

TOLERANCES UNLESS SPECIFIED		INTEGRATED DEVICE TECHNOLOGY, INC.	
DECIMAL	ANGULAR	2075 Stoner Way, Santa Clara, CA 95054	
XXX.X	±	PHONE: (408) 727-8116	
XXXX.X		FAX: (408) 482-8874	
XXXX.X		TW: 810-338-2070	
APPROVALS	DATE	TITLE	REV
DRN	06/15/90	PV PACKAGE OUTLINE	
CHECKED		.300" BODY WIDTH SSOP	
		.025" PITCH	
		SIZE	REV
		C	02
		DRAWING No.	
		PSC-4029	
		DO NOT SCALE DRAWING	

PACKAGE DIAGRAM OUTLINES

TSSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	



TOLERANCES UNLESS SPECIFIED		INTEGRATED DEVICE TECHNOLOGY, Inc.	
DECIMAL	ANGULAR	2975 Slender Way, Santa Clara, CA 95054	
XXX.X	±	PHONE: (408) 727-8118	
XXXX.X		FAX: (408) 492-8674	
XXXX.X		TW: 910-336-2070	
APPROVALS	DATE	TITLE	REV
DRAWN	01/15/93	PA PACKAGE OUTLINE	
CHECKED		6.10 mm BODY WIDTH TSSOP	
		.50 mm PITCH	
		SIZE C	DRAWING No. PSC-4039
			REV 03
DO NOT SCALE DRAWING			

PACKAGE DIAGRAM OUTLINES TSSOP (Continued)

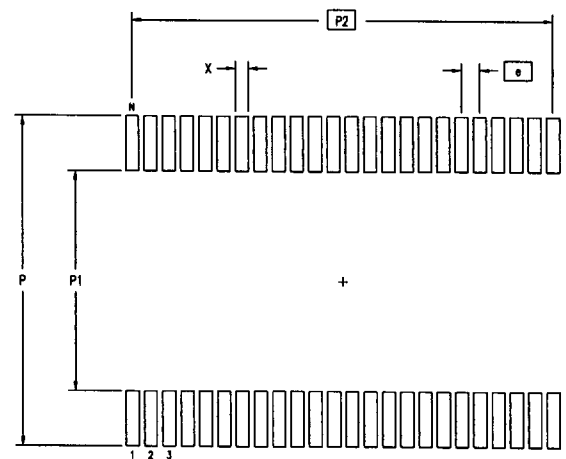
DWG #				S048-2		DWG #				S056-2	
SYMBOL	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE			
	ED				EE						
	MIN	NOM	MAX		MIN	NOM	MAX				
	A	-	-		1.10	-	-		1.10		
A1	.05	-	.15		.05	-	.15				
A2	.85	1.00	1.05		.85	1.00	1.05				
D	12.40	12.50	12.60	4,5	13.90	14.00	14.10	4,5			
E	7.95	8.10	8.25	3	7.95	8.10	8.25	3			
E1	6.00	6.10	6.20	4,6	6.00	6.10	6.20	4,6			
N	48				56						

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS $\square$ -A- and $\square$ -B- TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION E TO BE DETERMINED AT SEATING PLANE $\square$ -C-
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MQ-153, VARIATION ED & EE

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

LAND PATTERN DIMENSIONS



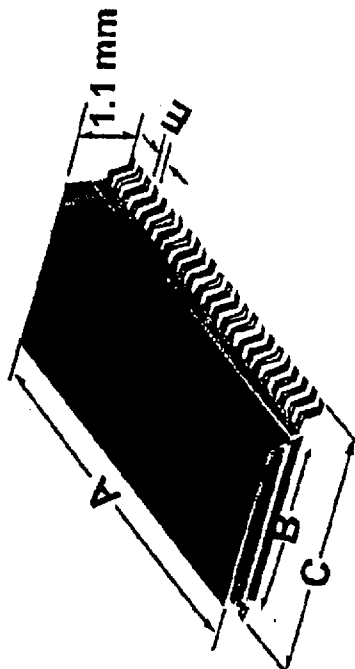
	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10
P2	11.50	BSC	13.50	BSC
X	.30	.40	.30	.40
e	.50	BSC	.50	BSC
N	48		56	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2975 Slender Way, Santa Clara, CA 95054	
±	±	PHONE: (408) 727-8118	
±	±	FAK: (408) 482-8874	
±	±	TWC: 910-338-2070	
APPROVALS	DATE	TITLE	PA PACKAGE OUTLINE
DRW	01/15/93	6.10 mm BODY WIDTH TSSOP	
CHECKED		.50 mm PITCH	
		SIZE	C
		DRAWING No.	PSC-4039
		REV	03
DO NOT SCALE DRAWING			



TVSOP

The Most Compact Double Density Package

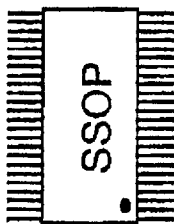


TVSOP Package	Typical Dimensions (in mm)				Area (mm ²)
	A	B	C	E	
48 Pin	9.80	4.40	6.40	0.40	63.00
56 Pin	11.30	4.40	6.40	0.40	72.30
80 Pin	17.00	6.10	8.10	0.40	137.80
100 Pin	20.80	6.10	8.10	0.40	168.50



Double Density Packaging

48-Pin



16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²

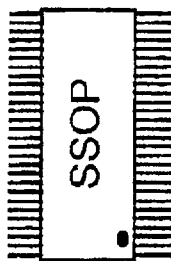


12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²



9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

56-Pin



18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²



14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²



11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

TVSOP	Area (mm ²)	%Smaller Than SSOP	%Smaller Than TSSOP
48 pin	63.00	61.9	38.0
56 pin	72.30	62.2	36.0