

MITSUBISHI <DIGITAL ASSP>
M74HCT245-1P/FP

**OCTAL 3-STATE
NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS**

DESCRIPTION

The M74HCT 245-1 is an integrated circuit chip consisting of eight transceivers with noninverted outputs.

FEATURES

- TTL level inputs $V_{IL}=0.8V$ max, $V_{IH}=2.0V$ min
- High-fanout 3-state output : ($I_{OL}=24mA$, $I_{OH}=-24mA$)
- High-speed : 11ns typ. ($C_L=50pF$, $V_{CC}=5V$)
- Low power dissipation : 25 μ W/package, max
($V_{CC}=5V$, $T_a=25^{\circ}C$, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : $T_a=-40\sim+85^{\circ}C$

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTION

Use of silicon gate technology allows the M74HCT245-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS245. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. When used as such, no pull-up resistors are required.

Two buffers with 3-state noninverted outputs have their inputs and outputs connected and can be used as buffers in both directions.

The input/output direction is controlled by directions input DIR.

When DIR is high, the A data ports will become input terminals and the B data ports will become output terminals.

When DIR is low, B will become input terminals and A will become output terminals.

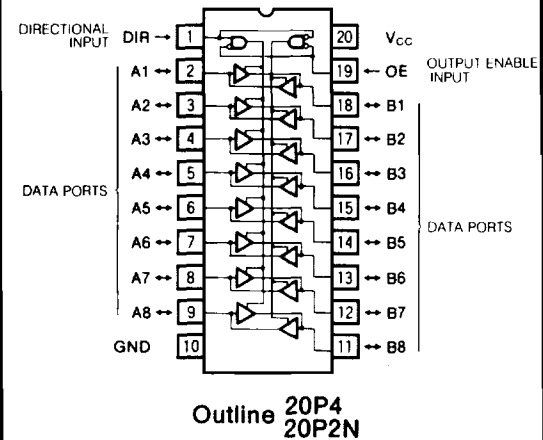
When output enable OE is high, A and B will both become high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

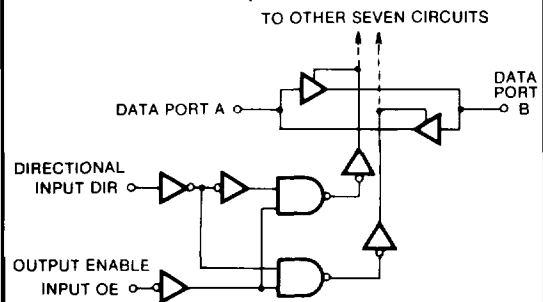
Inputs		Data ports	
OE	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1 : I : Input pin
O : Output pin
Z : High impedance (A and B are separated.)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



LOGIC DIAGRAM (EACH TRANSCEIVER)



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ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC} + 0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC} + 0.5$	V
I_{IK}	Input protection diode current	$V_I < 0\text{V}$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0\text{V}$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current		± 50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 200	mA
P_d	Power dissipation	(Note 2)	500	mW
T_{stg}	Storage temperature		$-65 \sim +150$	$^\circ\text{C}$

Note 2 : M74HCT245-1FP : $T_a = -40 \sim +75^\circ\text{C}$ and $T_a = 75 \sim 85^\circ\text{C}$ are derated at $-7\text{mW}/^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85^\circ\text{C}$)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature	-40		+85	$^\circ\text{C}$
t_r, t_f	Input rise time, fall time	$V_{CC}=4.5\text{V}$		25	ns/V
		$V_{CC}=5.5\text{V}$		15	

ELECTRICAL CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits					Unit
			25°C			-40~+85°C		
			Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	$V_O=0.1V, V_{CC}=0.1V$ $ I_O =20\mu A$	2.0			2.0		V
V_{IL}	Low-level input voltage	$V_O=0.1V, V_{CC}=0.1V$ $ I_O =20\mu A$			0.8		0.8	V
V_{OH}	High-level output voltage	$V_I=V_{IH}, V_{IL}$ $I_{OH}=-20\mu A$ $I_{OH}=-24mA, V_{CC}=4.5V$	$V_{CC}-0.1$ 3.83			$V_{CC}-0.1$ 3.70		V
V_{OL}	Low-level output voltage	$V_I=V_{IL}$ $I_{OL}=20\mu A$ $I_{OL}=24mA, V_{CC}=4.5V$			0.1 0.44		0.1 0.53	V
I_{IH}	High-level input current	$V_I=V_{CC}$			0.1		1.0	μA
I_{IL}	Low-level input current	$V_I=GND$			-0.1		-1.0	μA
I_{OZH}	Off-state high-level output current	$V_I=V_{IH}, V_{IL}, V_O=V_{CC}$			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I=V_{IH}, V_{IL}, V_O=GND$			-0.5		-5.0	μA
I_{CC}	Static supply current	$V_I=V_{CC}, GND, I_O=0\mu A$			5.0		50.0	μA
ΔI_{CC}	Maximum static supply current	$V_I=2.4V, 0.4V$ (Note 3)			2.7		2.9	mA

Note 3 : Only one input is set at this value. All others are fixed to V_{CC} and GND.

SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}, T_a=25^\circ\text{C}$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-to-high-level and high-to-low-level output transition time	$C_L=50\text{pF}$ (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-to-high-level and high-to-low-level output propagation time (A-B, B-A)	$C_L=5\text{pF}$ (Note 5)			18	ns
t_{PHL}	output propagation time (A-B, B-A)				20	ns
t_{PLZ}	Low-level and high-level output disable time (OE-A, B)	$C_L=50\text{pF}$ (Note 5)			27	ns
t_{PHZ}	disable time (OE-A, B)				27	ns
t_{PZL}	Low-level and high-level output enable time (OE-A, B)	$C_L=50\text{pF}$ (Note 5)			29	ns
t_{PZH}	enable time (OE-A, B)				29	ns

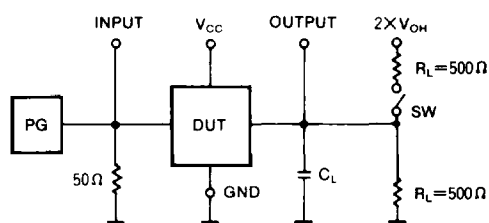
**OCTAL 3-STATE
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SWITCHING CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $T_a=-40\sim+85^\circ\text{C}$)

Symbol	Parameter	Test conditions	Limits					Unit
			25°C			−40~+85°C		
			Min	Typ	Max	Min	Max	
t _{TLH}	Low-to high-level and high-to low-level output transition time	C _L = 50pF (Note 5)		5	12		15	ns
t _{THL}				5	12		15	ns
t _{PLH}	Low-to high-level and high-to low-level output propagation time			9	19		24	ns
t _{PHL}	(A→B, B→A)			12	21		26	ns
t _{PLZ}	Low-level and high-level output disable time			10	30		38	ns
t _{PHZ}	(OE→A, B)			13	30		38	ns
t _{PZL}	Low-level and high-level output enable time			12	30		38	ns
t _{PZH}	(OE→A, B)			11	30		38	ns
C _i	Input capacitance				10		10	pF
C _O	Off-state output capacitance	OE=V _{CC}			15		15	pF
C _{PD}	Power dissipation capacitance (Note 4)		62.0					pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer). The power dissipated during operation under no-load condition is calculated using the following formula :
 $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}	Open
t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10%~90%) $t_r=3\text{ns}$, $t_f=3\text{ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM

