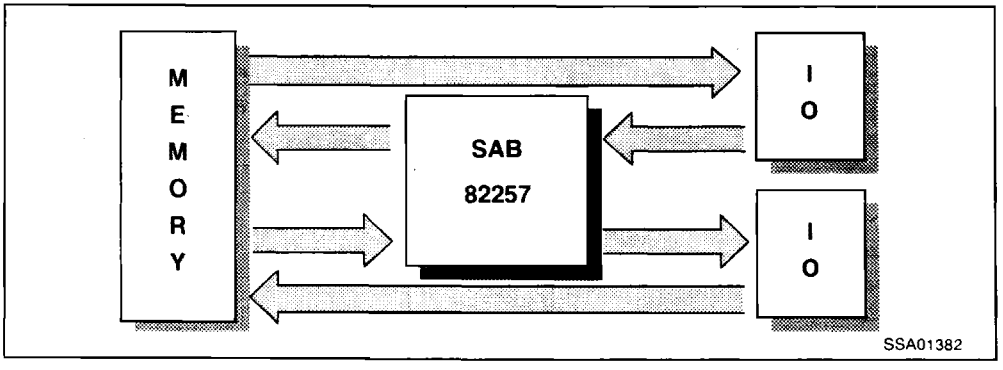
Advanced DMA Controller SAB 82257
for 8-/16-Bit Microcomputer Systems

8 MHz

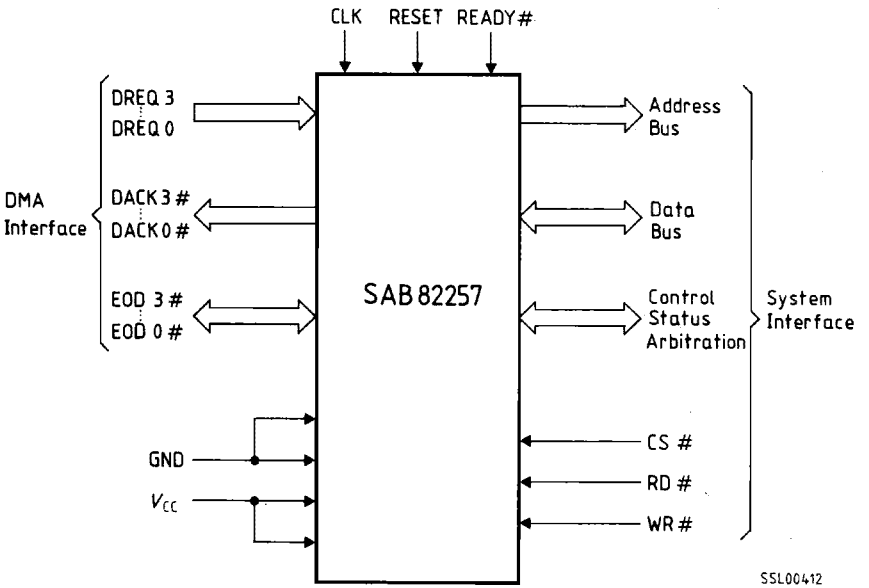
- High-performance 16-bit DMA controller for 16-bit family processors SAB 80286, SAB 80186/188, SAB 8086/88
- 4 independent high-speed DMA channels
- Adaptive on-chip bus interface for direct connection to 16/8-bit processors
- Standalone operation for modular systems
- Programmable bus loading
- Transfer rates up to 8 Mbytes/s (8 MHz system)
- 16 Mbytes addressing range
- 16 Mbytes maximum block size
- Command chaining for automatic processing
- Automatic data chaining (scattering/ gathering) for flexible data structures
- Single and double cycle transfers
- Automatic assembly/disassembly of data
- Memory-based communication scheme with CPU



The SAB 82257 is an advanced DMA (direct memory access) controller especially designed for the 16-bit microprocessors SAB 80286 and SAB 8086/186/88/188. In addition the operation with other processors is supported by the remote mode. The SAB 82257 has 4 independent DMA channels which can transfer data at rates up to 8 Mbytes/ s at 8 MHz clock frequency in an SAB 80286 system or up to 4 Mbytes/ s at 8 MHz in an SAB 8086/80186 system. This great bandwidth allows the user to handle very fast data transfers or a large number of concurrent peripherals.

The device is fabricated in advanced +5 V N-channel Siemens MYMOS technology and comes in a 68-pin plastic leaded chip carrier (PL-CC-68).

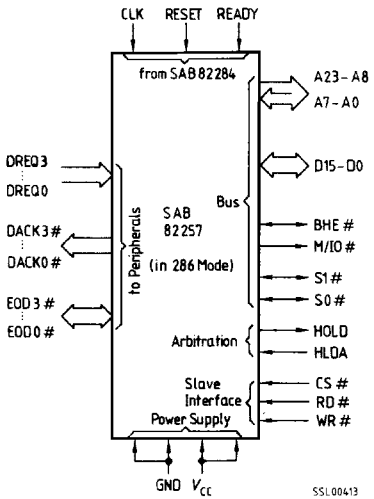
Logic Symbol



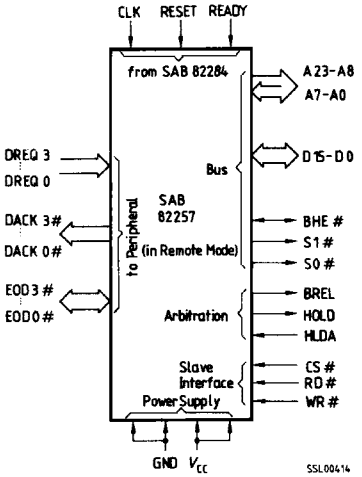
Modes of Operation, Adaptive Bus Interface

Like the advanced DMA controller SAB 82258A, the SAB 82257 has been defined to work with all 16-bit processors linke SAB 80286, SAB 80186/188 and SAB 8086/88 without additional support and interface logic. Hence the local buses of the above processors are different in signals, functions and timings, the SAB 82257 has an adaptive bus interface to meet the different requirements of these local buses.

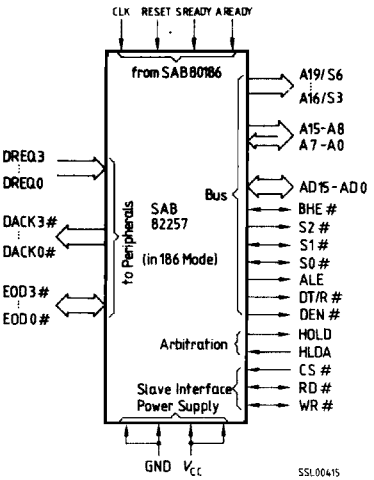
Logic Symbol in 286 Mode



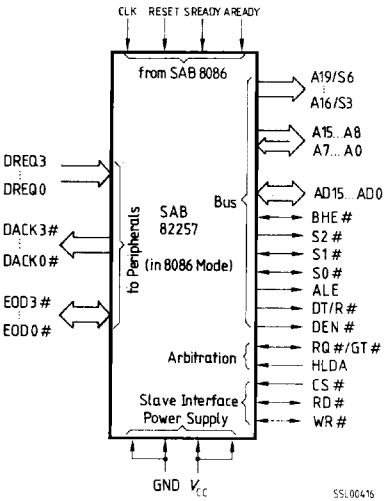
Logic Symbol in Remote Mode



Logic Symbol in 186 Mode



Logic Symbol in 8086 Mode

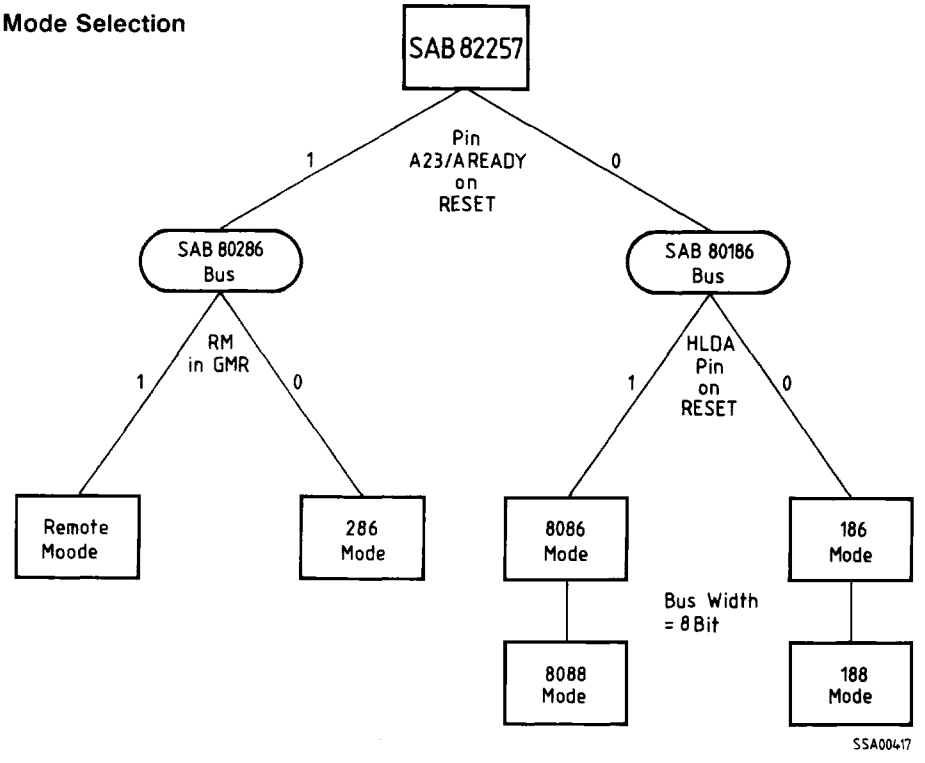


As a result of this, a bus compatibility with identical timing is attained with the processors SAB 80286, SAB 80186 and SAB 8086. A compatibility with the 8-bit bus versions of these processors, SAB 8088 and SAB 80188, is also guaranteed by defining the physical bus width of the SAB 82257 (per software) as 8 bits. The only difference in operation with SAB 8086 or SAB 80186 is that for SAB 8086 the HOLD pin functions as RQ#/GT# line (if HLDA is held high on reset).

The SAB 82257 can also be operated in remote or standalone mode, in which case it is not coupled directly to a processor. In remote mode, the SAB 82257 can be operated as sole bus master in a multimaster environment. The SAB 82257 is programmed to a specific mode of operation by applying defined logic levels to certain pins during reset and by setting the status of several control bits (see figure below).

Note: *Pin 57 (A21/DT/R# of the SAB 82257) must be high during reset in order to enable proper operation. This is provided, if pin A21 is connected to the SAB 80286's address bus. An internal pullup resistor supports applications where pin 57 is left open.*

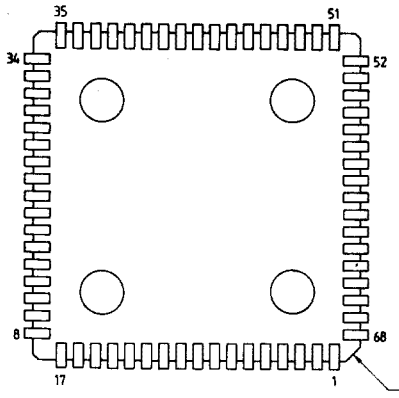
Mode Selection



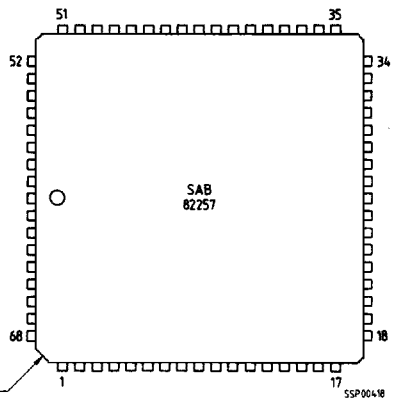
Pin 57 (A21 or DT/R#) must be high during Reset to enter the desired operating mode. An internal pullup pulls this pin high, if nothing is driving it.

Pin Configuration

PL-CC-68
Bottom view



PL-CC-68
Top view



Pin Definitions and Functions

Some pins of the SAB 82257 serve for different purposes according to the different modes of bus operation. The table below summarizes the pinouts of the SAB 82257 in the various modes. A detailed description of the general pin functions as well as the mode-specific pin functions is given in the following sections.

Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
16	HOLD	O	HOLD	O	HOLD or RQ#/GT#	O (186) I/O (8086)
17	HLDA	I	HLDA	I	HLDA	I
1	BHE#	I/O	BHE#	I/O	BHE#	I/O
14	M/IO#	O	BREL	O	S2#	O
11	S1#	I/O	S1#	O	S1#	I/O
13	S0#	I/O	S0#	O	S0#	I/O
8	CS#	I	CS#	I	CS#	I
2	RD#	I	RD#	I	RD#	I/O
3	WR#	I	WR#	I	WR#	I/O
10	READY#	I	READY#	I	SREADY	I
59	A23	O	A23	O	AREADY	I
59	A23	O	A23	O	AREADY	I
58	A22	O	A22	O	ALE	O
57	A21	O	A21	O	DT/R#	O
56	A20	O	A20	O	DEN#	O
55	A19	O	A19	O	A19/S6	O
54	A18	O	A18	O	A18/S5	O
53	A17	O	A17	O	A17/S4	O
52	A16	O	A16	O	A16/S3	O
51	A15	O	A15	O	A15	O
50	A14	O	A14	O	A14	O
49	A13	O	A13	O	A13	O
48	A12	O	A12	O	A12	O
47	A11	O	A11	O	A11	O
46	A10	O	A10	O	A10	O
45	A9	O	A9	O	A9	O
44	A8	O	A8	O	A8	O
42	A7	I/O	A7	I/O	A7	I/O
41	A6	I/O	A6	I/O	A6	I/O
40	A5	I/O	A5	I/O	A5	I/O
39	A4	I/O	A4	I/O	A4	I/O

Pin Definitions and Functions (cont'd)

Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
38	A3	I/O	A3	I/O	A3	I/O
37	A2	I/O	A2	I/O	A2	I/O
36	A1	I/O	A1	I/O	A1	I/O
35	A0	I/O	A0	I/O	AO	I/O
18	D15	I/O	D15	I/O	AD15	I/O
20	D14	I/O	D14	I/O	AD14	I/O
22	D13	I/O	D13	I/O	AD13	I/O
24	D12	I/O	D12	I/O	AD12	I/O
27	D11	I/O	D11	I/O	AD11	I/O
29	D10	I/O	D10	I/O	AD10	I/O
31	D9	I/O	D9	I/O	AD9	I/O
33	D8	I/O	D8	I/O	AD8	I/O
19	D7	I/O	D7	I/O	AD7	I/O
21	D6	I/O	D6	I/O	AD6	I/O
23	D5	I/O	D5	I/O	AD5	I/O
25	D4	I/O	D4	I/O	AD4	I/O
28	D3	I/O	D3	I/O	AD3	I/O
30	D2	I/O	D2	I/O	AD2	I/O
32	D1	I/O	D1	I/O	AD1	I/O
34	D0	I/O	D0	I/O	AD0	I/O
7	DREQ0	I	DREQ0	I	DREQ0	I
6	DREQ1	I	DREQ1	I	DREQ1	I
5	DREQ2	I	DREQ2	I	DREQ2	I
4	DREQ3	I	DREQ3	I	DREQ3	I
61	DACK0#	O	DACK0#	O	DACK0#	O
62	DACK1#	O	DACK1#	O	DACK1#	O
63	DACK2#	O	DACK2#	O	DACK2#	O
64	DACK3#	O	DACK3#	O	DACK3#	O
65	EOD0#	I/O	EOD0#	I/O	EOD0#	I/O
66	EOD1#	I/O	EOD1#	I/O	EOD1#	I/O
67	EOD2#	I/O	EOD2#	I/O	EOD2#	I/O
68	EOD3#	I/O	EOD3#	I/O	EOD3#	I/O
15	RESET	I	RESET	I	RESET	I
12	CLK	I	CLK	I	CLK	I
9,43	GND	–	GND	–	GND	–
26,60	V_{CC}	–	V_{CC}	–	V_{CC}	–

Pin Definitions for All Operating Modes

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>BHE#</td><td>1</td><td>I/O</td><td>BUS HIGH ENABLE
This active low input indicates transfer of data on the upper byte of the data bus, D15 to D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use BHE# to condition chip select functions. BHE# floats to tristate off when the SAB 82257 does not own the bus.
BHE# and A0 encodings
<table>
<tr><th>BHE#</th><th>A0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Word transfer (D15-D8)</td></tr>
<tr><td>0</td><td>1</td><td>Byte transfer on upper half of data bus (D15-D8)</td></tr>
<tr><td>1</td><td>0</td><td>Byte transfer on lower half of data bus (D7-D0)</td></tr>
<tr><td>1</td><td>1</td><td>Odd-addressed byte on 8-bit bus (D7-D0)</td></tr>
</table></td></tr>
<tr><td>RD#</td><td>2</td><td>I</td><td>READ
This active low input in conjunction with chip select enables reading the SAB 82257 register which is addressed by the address lines A7 to A0. This signal can be asynchronous to the SAB 82257 clock.</td></tr>
<tr><td>WR#</td><td>3</td><td>I</td><td>WRITE
This active low input in conjunction with chip select enables writing into the SAB 82257 registers which is addressed by the address lines A7 to A0. This signal can be asynchronous to the SAB 82257 clock.</td></tr>
<tr><td>DREQ0-
DREQ3</td><td>4-7</td><td>I</td><td>DMA REQUEST (0 TO 3)
These active high inputs are used for synchronized DMA transfers. DREQ3 has the meaning of I/O request (IOREQ) if channel 3 is a multiplexer channel. These signals can be asynchronous to the SAB 82257 clock.</td></tr>
</table>

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Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CS#	8	I	**CHIP SELECT** This active low input enables the access of a processor to SAB 82257 registers. This access is additionally controlled either by bus status signals or by the read or write command signals. Chip select can be asynchronous to the SAB 82257 clock.
CLK	12	I	**CLOCK** This input provides the fundamental timing. In 286 mode and remote mode it must be two times the system clock. It can be directly connected to the SAB 82284 CLK output. It is divided by two to generate the SAB 82257 internal clock. The on-chip divide-by-two circuitry can be synchronized to the external clock generator by a low-to-high transition on the RESET input, or by the first high-to-low transition on the status inputs S0# or S1# after reset. In 186/8086 mode no internal prescaling is done.
S0#, S1#	11, 13	I/O	**BUS STATUS LINES (0, 1)** These signals control the support circuits. The beginning of a bus cycle is indicated by S1# or S0# or both going active. The termination of a bus cycle is indicated by all status signals going inactive in 186 mode or bus ready signal (READY#) going active in 286 mode. The type of bus cycle is indicated by S0#, S1# and S2# (in 186 mode) or M/IO# (in 286 mode). S2# and M/IO# have the same meaning but in 186 mode the S2# signal can be active only when at least one of S1# or S0# is active, whereas in 286 mode the M/IO# signal is valid with the address on the address lines. The SAB 82257 can generate the following bus cycles by activating the status signals (and M/IO# in 286 mode):

Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function

S0#,S1# (cont'd) — 11, 13 — I/O

M/IO# or S2#	S1#	S0#	Cycle Type
0	0	0	Read I/O-vector (for multiplexer channel)
0	0	1	Read from I/O space
0	1	0	Write into I/O space
0	1	1	No bus cycle, does not occur in 186 mode
1	0	0	Does not occur
1	0	1	Read from memory space
1	1	0	Write into memory space
1	1	1	No bus cycle

When the SAB 82257 is not the master of the local bus the status signals are used as inputs for detection of synchronous accesses to the SAB 82257. The following table shows the bus status and CS# signals and their interpretation by the SAB 82258.

CS#	S1#	S0#	Description
1	X	X	SAB 82257 is not selected (no action)
0	0	0	No SAB 82257 access (no action)
0	0	1	Read from an SAB 82257 register
0	1	0	Write into an SAB 82257 register
0	1	1	No bus cycle[1)]

1) SAB 82257 is selected but no synchronous access is activated. In this case the SAB 82257 monitors RD# and WR# signals for detection of an asynchronous access.

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Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
RESET	15	I	**SYSTEM RESET** An activation of the reset signal forces the SAB 82257 to the initial state. The reset signal must be synchronous to CLK.
DACK0#-DACK3#	61-64	O	**DMA ACKNOWLEDGE (0 TO 3)** These active low inputs acknowledge the requests on the related DREQn signals. They are activated when the requested transfer(s) is (are) performed. If the channel 3 is a multiplexer channel the signal DACK3# has the meaning of I/O acknowledge (IOACK#).
EOD0#-EOD3#	65-68	I/O	**END OF DMA (0 TO 3)** These lines are implemented as open drain output drivers with a high impedance pullup resistor and thus can be used as bidirectional lines. As **outputs** the lines are activated for two system clock cycles at the end of the DMA transfer of the corresponding channel (if enabled) or they are activated under program control (EOD output or interrupt output). If the lines are held internally high but forced to low by external circuitry, they act as "End of DMA" **inputs.** The current transfer is aborted and the SAB 82257 continues with the next command. Additionally, a special function is possible with the EOD2# pin: this pin can also be used as common interrupt signal for all 4 channels. In this mode this line is not an open drain output but a pushpull output (output only). The other EOD# pins may be used as EOD# outputs/inputs as described above.
V_{CC}	26, 60		**POWER SUPPLY** (+ 5 V)
GND	9, 43		**GROUND** (0 V)

Pin Definitions for 286 Mode and Remote Mode

In 286 mode the SAB 82257 bus signals and bus timings are the same as for the SAB 80286 processor. Additional features of the SAB 82257 require a slight change in pin definitions. The processor can access internal registers of the SAB 82257. Therefore the bus signals must support these accesses. This means that some of the bus control signals must be bidirectional and some additional bus control signals are necessary. All additional pins and their functions are listed below.

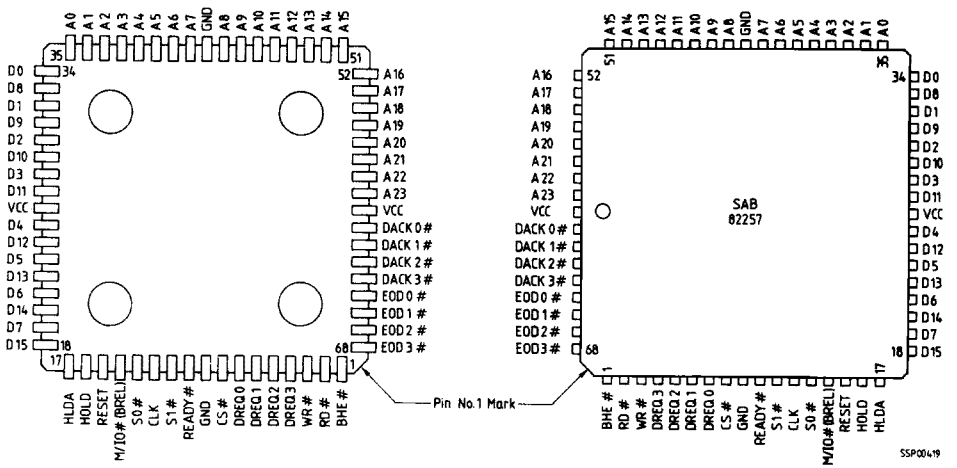
In **remote mode** most of the bus signals are the same as in 286 mode. Pin 14 (M/IO#) serves as BREL output. The HOLD/HLDA arbitration in remote mode is used only for system bus accesses, the resident bus is accessed directly.

The CS# input additionally requests access to the local bus of the SAB 82257. These accesses are enabled through the BREL output after the SAB 82257 has released the bus.

Pin Configuration in 286 Mode and Remote Mode

Component Pad View – As viewed from underside of component when mounted on the board

PC Board View – As viewed from the component side of the pc board



Pin Definitions for 286 Mode and Remote Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
READY#	10	I	**BUS READY** This active low input terminates a bus cycle. Bus cycles are extended without limit until terminated by READY# low. READY# is a synchronous input requiring setup and hold times relative to the system clock to be met for correct operation.
M/IO#	14 (286 mode)	O	**Memory / I/O SELECT** In 286 mode, pin 14 is used to distinguish between memory and I/O space addresses.
BREL	14 (remote mode)	O	**BUS RELEASE** In remote mode pin 14 is used to indicate when the SAB 82257 has released the control of the local bus.
HOLD	16	O	**BUS HOLD REQUEST** This active high output indicates a request for control of the local bus (286 mode) or the system bus (remote mode). When the SAB 82257 relinquishes the bus it drops the HOLD output. HOLD is connected to the bus arbiter in remote mode.
HLDA	17	I	**BUS HOLD ACKNOWLEDGE** This active high input indicates that the SAB 82257 can acquire the control of the bus. When it goes low SAB 82257 must relinquish the bus at the end of its current cycle. HLDA can be asynchronous to the SAB 82257 clock. HLDA is connected to the bus arbiter in remote mode.
D0-D15	18-25, 27-34	I/O	**DATA BUS (0 TO 15)** This is the bidirectional 16-bit data bus. For use with an 8-bit bus, only the lower 8 data lines D7-D0 are relevant.
A0-A7	35-42	I/O	**ADDRESS BUS (0 TO 7)** The lower 8 address lines for DMA transfers. They are also used to input the register address when the processor accesses an SAB 82257 register.
A8-A23	44-59	O	**ADDRESS BUS (8 TO 23)** Higher address outputs.

Pin Definitions for 186 Mode and 8086 Mode

In 186 mode and 8086 mode the SAB 82257 multiplexes the address with data and additional status lines.

Pins A0 to A15 retain their original function while pins A20 to A23 serve for different purposes (not used for address in 186/8086 mode).

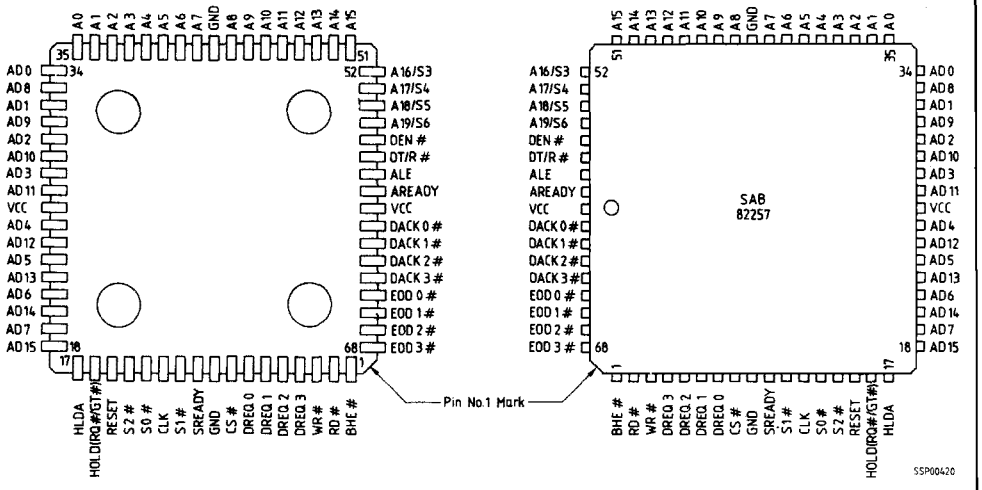
The RD# and WR# lines are additionally used as outputs in 186/8086 mode to support minimum mode systems.

Note that the HLDA input can be used to force the SAB 82257 off the bus in 8086 mode, even though the arbitration is done via the RQ#/GT# line!

Pin Configuration in 186 Mode and 8086 Mode

Component Pad View – As viewed from underside of component when mounted on the board

PC Board View – As viewed from the component side of the pc board



Pin Definitions for 186 Mode and 8086 Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ALE	58	O	**ADDRESS LATCH ENABLE** This active high output provides a strobe signal to separate the address information on the multiplexed AD lines.
DEN#	56	O	**DATA ENABLE** This active low output enables the data transceivers.
DT/R#	57	O	**DATA TRANSMIT/RECEIVE** This signal controls the direction of the data transceivers. When low, data is transferred to the SAB 82257, when high, the SAB 82257 places data onto the data bus.
S2#	14	O	**STATUS LINE 2** Signal as for SAB 186/8086/88 processors (see also S1#, S0# description in 286 mode).
AREADY	59	I	**ASYNCHRONOUS READY** The rising edge of this signal is internally synchronized, the falling edge must be synchronous to CLK. During reset this signal must be low to enter 186 mode.
SREADY	10	I	**SYNCHRONOUS READY** This signal must be synchronized externally. The use of this pin permits a relaxed system-timing specification by eliminating the clock phase which is required for resolving the signal level when using the AREADY input.
AD0-AD15	18-25 27-34	I/O	**ADDRESS/DATA BUS (0 to 15)** Lower address and data information is multiplexed on pin AD0 to AD15.
A0-A7 A8-A15	35-42 44-51	I/O O	**ADDRESS BUS (0 to 15)** Additionally the demultiplexed address information is available on address pin A0 to A15.

Pin Definitions for 186 Mode and 8086 Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
A16/S3-A19/S6	52–55	O	**ADDRESS BUS (16 TO 19)/ STATUS LINES (3 TO 6)** The higher address bits are multiplexed with additional status information.
HLDA	17	I	**BUS HOLD ACKNOWLEDGE** This active high input indicates that the SAB 82257 can acquire the control of the bus. When it goes low the SAB 82257 must relinquish the bus at the end of its current bus cycle. HLDA can be asynchronous to the SAB 82257 clock. In 8086 mode, HLDA can be used to force the SAB 82257 off the bus.
HOLD	16 (186 mode)	O	**BUS HOLD REQUEST** This active high output indicates a request for control of the bus. When the SAB 82257 relinquishes the bus, it drops the HOLD output.
RQ# GT#	16 (8086 mode)	I/O	**REQUEST/GRANT** In 8086 mode the HOLD output acts as RQ#/GT# line. The RQ#/GT# protocol implements a one-line communication dialog required to arbitrate the use of the system bus normally done via HOLD/HLDA. The RQ#/GT# signal is active low and has an internal pullup resistor.

Functional Description

General

The SAB 82257 is an advanced general-purpose DMA controller especially designed for efficient highspeed data transfers on an SAB 80286 bus as well as on an SAB 80186/188 or SAB 8086/88 bus.

It supports two basic operating modes:

- local mode (tightly coupled to a processor) and
- remote mode (loosely coupled to a processor).

In the first case the SAB 82257 is directly coupled to the CPU and uses the same system support/control devices as the CPU (see figure below). This mode is possible with the above-mentioned processors.

As a second basic operating mode remote (standalone) mode is supported (see figure below). Here the SAB 82257 has its own sets of bus interface circuits and thus can utilize its own local bus. This allows the DMA controller to work in parallel with the main CPU and therefore overall system performance can be increased. Besides, this mode is very useful for the design of modular systems and allows connecting the SAB 82257 to any other processor via the system bus independent of the processor's local bus.

The SAB 82257 has four independent DMA channels that can transfer up to 8 Mbytes/s in single cycle mode (2 clocks/transfer). In 2-cycle transfer mode the maximum rate is 4 Mbytes/s. Switching between channels induces no time penalty. Thus the overall maximum transfer rate of 8 Mbytes/s is also valid for multiple channel operation.

This fast operation is possible because of the pipelined architecture of the SAB 82257 which allows the different functional units to work in parallel.

The SAB 82257 supports two address spaces, memory space and I/O space, each with a maximum address range of 16 Mbytes. In addition, the maximum block length (byte count) is also 16 Mbytes to support applications where large blocks of data have to be transferred (e.g. graphics).

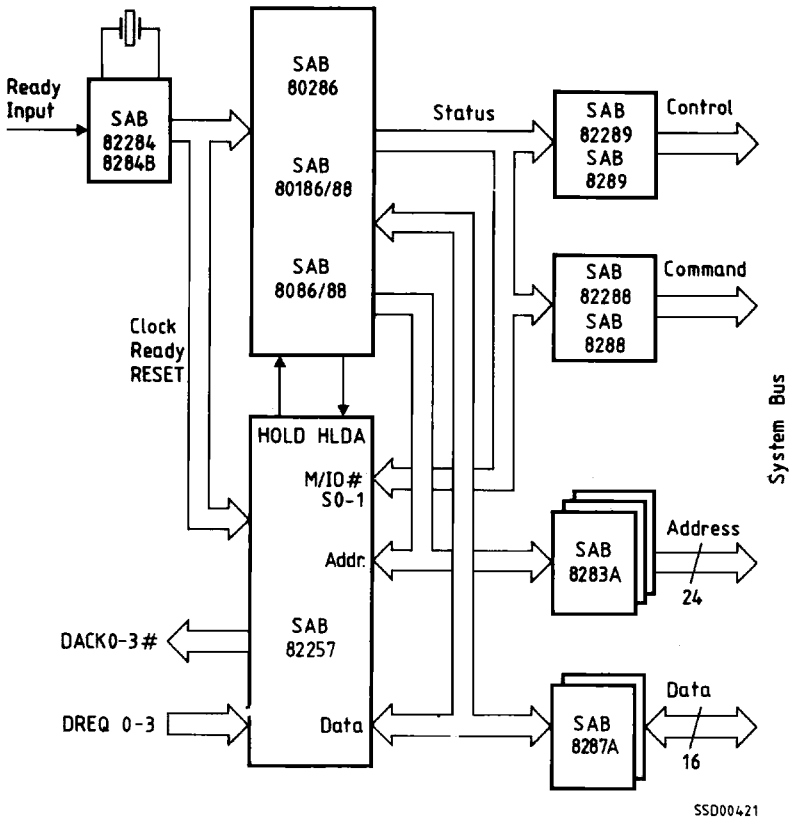
As source or as destination, four parameters can be selected independently:

- address space (memory or I/O)
- physical bus width (8 bits or 16 bits)
- logical bus width (same as physical bus width or 8 bits on a 16-bit physical bus) and
- transfer direction (increasing, decreasing, fixed pointer or constant value).

If the physical bus width of source or destination differs from the logical bus width, an automatic byte/word assembly (word/byte disassembly) takes place. The same is true, if the logical bus widths of source and destination are not identical.

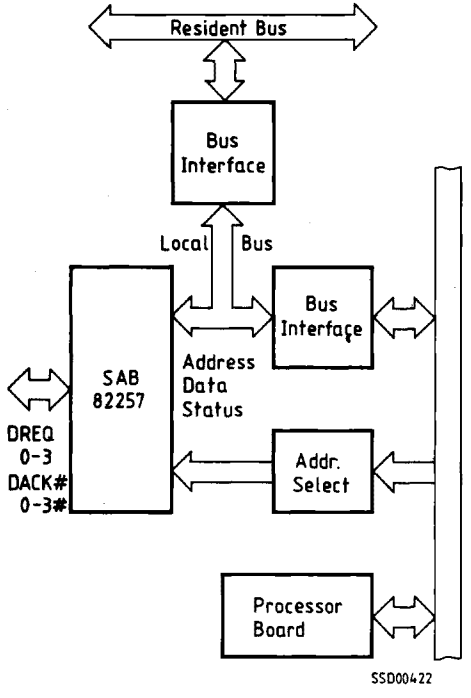
Basic SAB 82257 Operating Modes

a) Local Mode



Basic SAB 82257 Operating Modes

b) Remote Mode

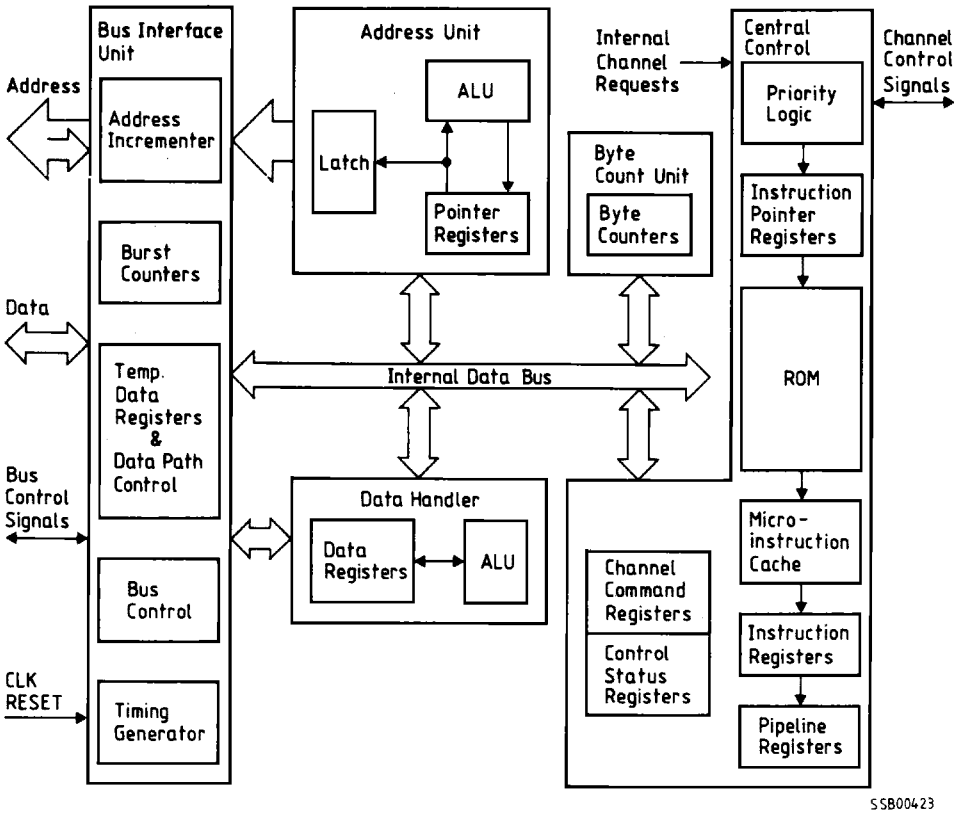


Transfers between different address spaces can be performed within one or two cycles, transfers within one address space can be performed only in two cycles.

The transfers can be executed free running or externally synchronized via DREQ where source or destination synchronization is possible.

In summary, this very symmetrical operation of the SAB 82257 gives the user a great amount of design flexibility.

Block Diagram of the SAB 82257



Adaptive Bus Interface

As shown in the figure on page 4, the SAB 82257 bus interface has two basic timing modes: the 286 mode and the 186 mode. In 286 mode the SAB 82257 is directly coupled to an SAB 80286, in 186 mode to an SAB 80186 or SAB 80188. For each of these two modes a slightly different variation exists:

- For the 286 mode the variation is the remote mode, where the SAB 82257 operates as a bus master on the system bus without being directly coupled to a processor. In this mode the SAB 82257 can utilize its own local bus and the communication with the main processor is done via the system bus. To enable access to SAB 82257 registers by the main processor, the SAB 82257 must release its local bus. This "local bus arbitration" in remote mode is done via the CS# and BREL lines.
- For the 186 mode the variation is the 8086 mode, where the SAB 82257 supports the RQ#/GT# protocol and thus can be directly coupled to an SAB 8086 or SAB 8088.

Memory-Based Communication

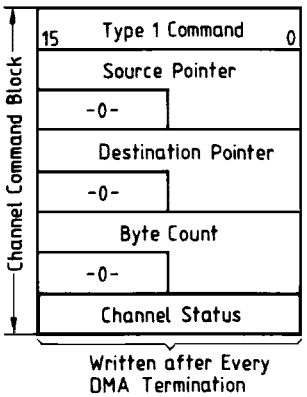
The normal communication between the SAB 82257 and the processor is memory-based. This means that all necessary data for a transfer is contained in a command block in memory accessible for CPU and SAB 82257 (see figure below). To start the transfer the CPU loads one of the command pointer registers of the SAB 82257 with the address of the command block and then issues a "start channel command". Getting the command the SAB 82257 loads the entire command block from memory into its on-chip channel registers and executes it. On completing the operation, channel status information is written back by the SAB 82257 into the channel status word contained in the command block in memory.
The command block structure of the SAB 82257 is identical with the structure of the SAB 82258A short command blocks. This allows to portate SAB 82257 software to the SAB 82258A and vice versa (in thise case with restrictions).

Command Chaining

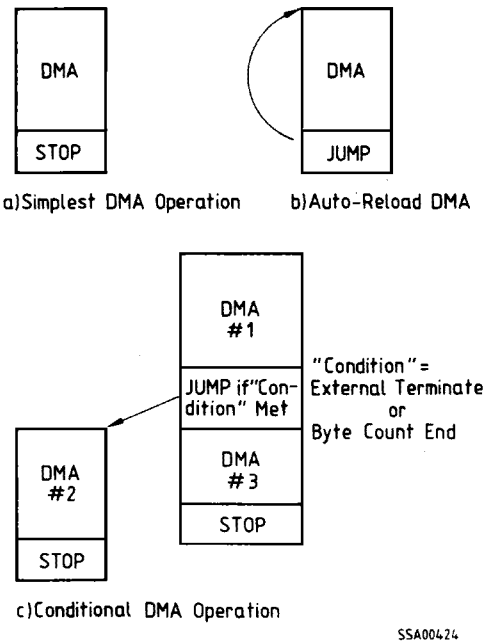
Command blocks for any channel can be chained for sequential execution (see figure). When the SAB 82257 has completed the execution of a command, it automatically increments the command pointer and starts to fetch and execute the next command block until a stop command is found. As a result a chain of command blocks can be executed by the SAB 82257 without any CPU intervention. Due to conditional and unconditional STOP and JUMP commands, quite complex sequences of DMA can be executed by the SAB 82257.

Memory-Based Communication and Command Chaining

Memory-Based Communication



Command Chaining



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Data Chaining

Data chaining allows an automatic, dynamic linking of data blocks scattered in memory. There are two types: list and linked-list data chaining.

If for a DMA the source blocks are to be dynamically linked during DMA, it is called source chaining and the effect is that of gathering data blocks and sending them out effectively as one block.

If one source block is dynamically broken up into multiple destination blocks, it is called destination chaining. This results in scattering of a block.

This dynamic linking and unlinking of data blocks makes the logical sequencing of data independent of its physical sequencing in memory.
In the case of linked list chaining (see figure a) each data block has a descriptor containing information on position of the data block in memory, length of the data block and a pointer to the next descriptor.

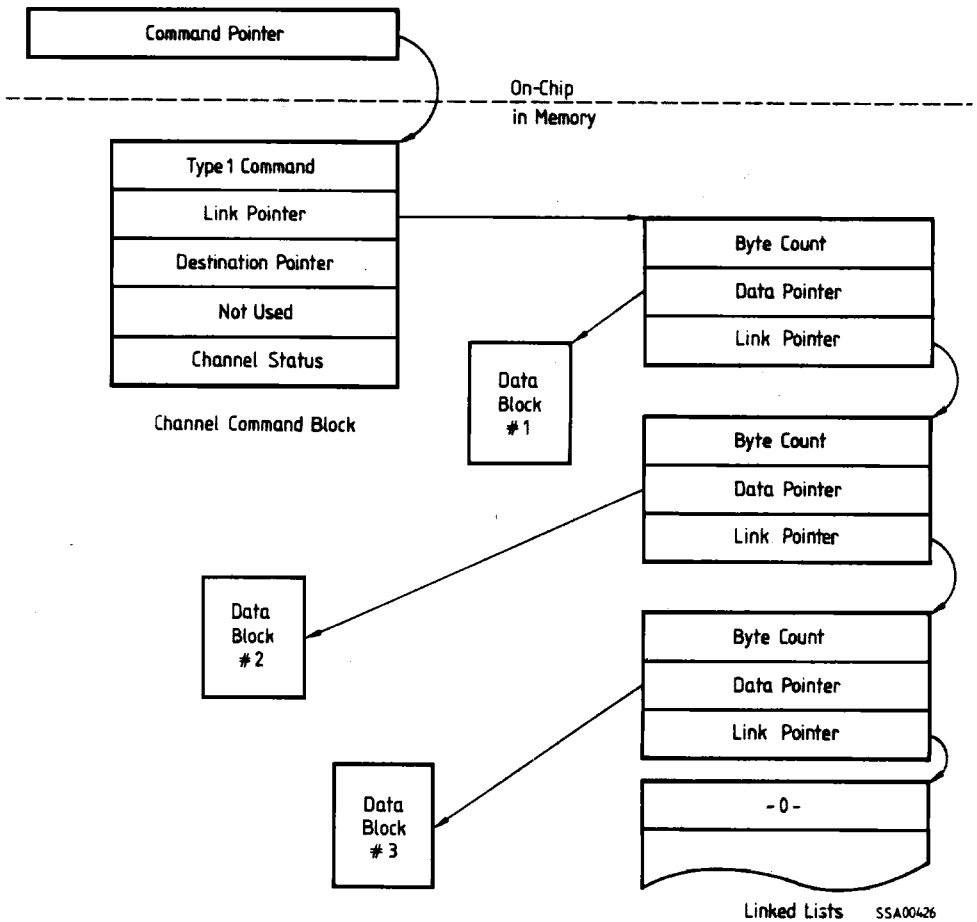
During data transfer the data block 1 is sent out first, then 2 and so on till a "0" is encountered in the byte count field.

The second type of data chaining is list chaining (see figure b).

Unlike linked list chaining, here the data block descriptors are continuous in a block and thus determine the sequence of data blocks. The flexibility lost in terms of predefined sequence is gained in terms of linking time.

Data Chaining

a) Linked List Chaining



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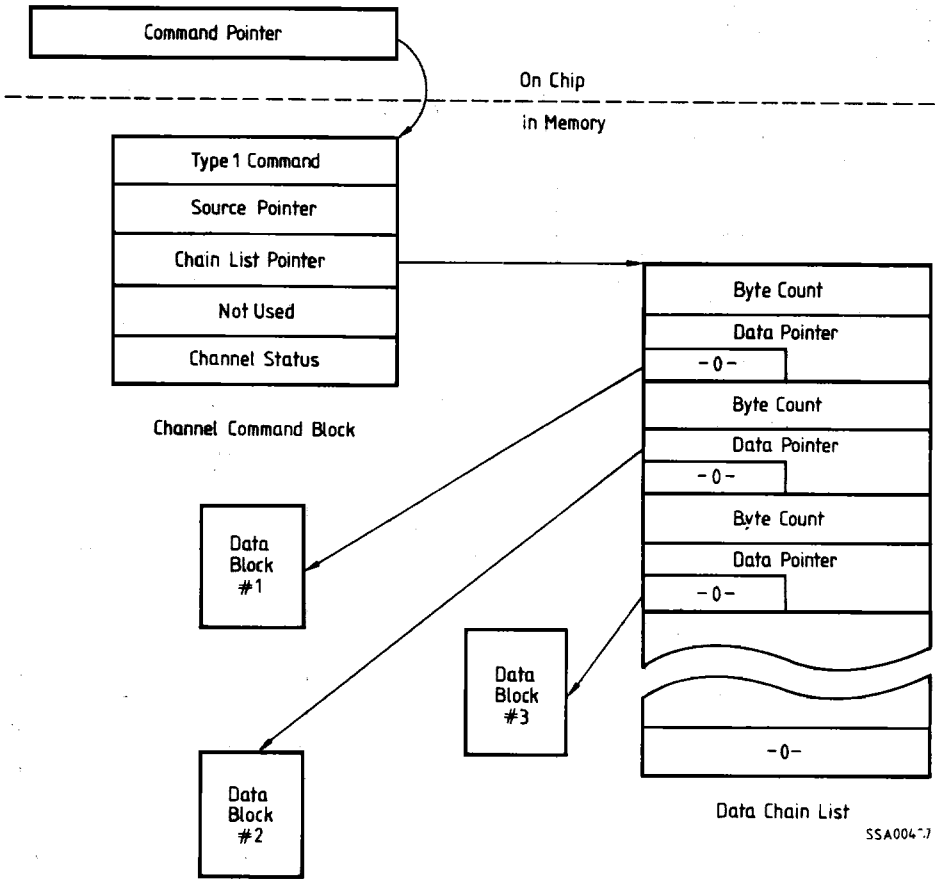
Data Chaining

b) List Chaining



Operating the SAB 82257

Reset

When activating the reset input, the SAB 82257 is forced into its initial state. All channels and bus activities are stopped, tristate lines are tristated and the others enter the inactive state. While the reset input is active, pin 57 must be held high and lines A23/AREADY and HLDA must be forced to the appropriate levels to select the desired bus interface mode (see figures on page 4, 41 and 52).
After deactivating reset the inactive state is maintained, in addition the state of the SAB 82257 registers is as follows:

- general mode register, general burst register, general delay register, general status register and the four channel status registers are set to zero,
- all other registers and bits are undefined.

Note: The general mode register (GMR) should be loaded first to select the mode of operation before any other activity is started on the SAB 82257.

DMA Interface

The DMA interface consists of three lines:

- DREQ – DMA request
- DACK# – DMA acknowledge and
- EOD# – End of DMA

The first two lines work as request and acknowledge lines to control synchronized DMA transfers as known from conventional DMA controllers.
A special feature of the SAB 82257 are the bidirectional EOD# lines . Firstly they can be used as inputs to receive an asynchronous external terminate signal to terminate a running DMA.
Secondly, as an output, they can be used to send out a pulse which interrupts the CPU and/or signals to the peripheral a specific status (e.g. transfer aborted, or end of a block, or send/receive next block ...).

The EOD# output signal can be generated synchronously to a transfer (during the last transfer) or asynchronously to the transfers by a specific command.

In addition the EOD# output of channel 2 can be used as a collective interrupt output for all DMA channels while the other three retain their normal function.

Slave Interface

The slave interface is used to access the SAB 82257 internal registers. Although nearly all of the communication between CPU and SAB 82257 is done via memory-based data blocks, some direct accesses to SAB 82257 registers are necessary.
For example during the initialization phase the general mode register must be written, or to start a channel the command pointer register and the general command register must be loaded. Also during the debugging phase it is of great benefit to have access to all of the SAB 82257 internal registers.

The slave interface is enabled by the CS# input and consists of the following lines:

- S0#, S1# – status lines (inputs)
- RD#, WR# – control lines (inputs)
- A0-A7 – register address (inputs)
- D0-D15 – data lines (inputs/outputs) or
- AD0-AD15 – data lines (inputs/outputs) for synchronous access in 186 mode

Note that all of these lines are outputs, if the SAB 82257 is an active bus master.

In 186 mode and 286 mode two types of accesses are possible:

- Synchronous access by means of the status lines. Processor and SAB 82257 are directly coupled and must use the same clock.
- Asynchronous access by using the control lines RD# and WR# (processor and SAB 82257may have different clocks).

In all modes except the synchronous access in 186 mode the register address must be supplied on address pins A0 to A7. Using synchronous access in 186 mode the address information is expected at address/data lines AD0 to AD7.
In remote mode only the asynchronous access is possible because the SAB 82257 first has to release its local bus to enable the register access. On receiving an access request (activation of CS# input) the SAB 82257 releases its local bus as soon as possible and signals this by activating the BREL line. Now the CPU can accomplish its access.

Bus Arbitration

To arbitrate access to the bus between the SAB 82257 and the processor, the signals HOLD and HLDA serve for communication. Normally the SAB 82257 competes for the bus via HOLD, the processor grants access to the bus via HLDA. The HLDA signal can also be deactivated in order to force the SAB 82257 off the bus for a certain reason (kick off). After reactivation of HLDA, the SAB 82257 will again get control of the bus.
In 8086 mode this communication is done by pulses via a single RQ#/GT# line which uses the HOLD pin. In this case normally the HLDA input has no function. Nevertheless, even in 8086 mode the HLDA input can be used for kick-off. This provides some kind of additional bus arbitration.

Register Set

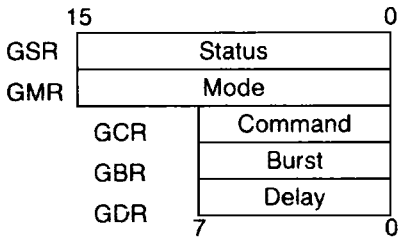
The following figure shows the user visible registers of the SAB 82257. A set of 5 registers, called the general registers, is used for all of the 4 channels. The mode register is being written to first after reset and it describes the SAB 82257 environment – bus widths, priorities, etc.

The general command register (GCR) is used to start and stop the DMA transfer on different channels. The general status register (GSR) shows the status of all of the 4 channels; if the channel is running, if interrupt is pending, etc. General burst register (GBR) and general delay register (GDR) are used to specify the bus load which is permissible for the SAB 82257.

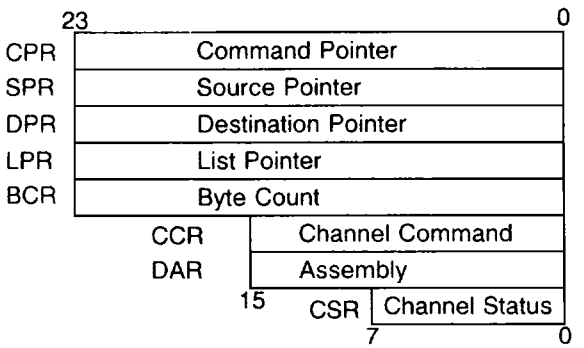
There is a set of channel registers for each of the 4 channels. Most channel registers serve as cache registers and need to be accessed only for debugging. During normal operation they are loaded automatically by the SAB 82257 (see next paragraph). The layout of register addresses shown in the figure on the next page. All register addresses are even. Locations not designated in that figure are reserved and should not be used.

SAB 82257 Register Set

General Register



Channel Register (4 sets; 1 per channel)



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Register Address Arrangement

Address Bits 0-5	Address Bits 7, 6			
	00	01	10	11
0	GCR			
2				
4	GSR			
6				
8	GMR			
A	GBR			
C	GDR			
E				
10	CSR 0	CSR 1	CSR 2	CSR 3
12	DAR 0	DAR 1	DAR 2	DAR 3
14				
16				
18				
1A				
1C				
1E				
20	CPR L0	CPR L1	CPR L2	CPR L3
22	CPR H0	CPR H1	CPR H2	CPR H3
24	SPR L0	SPR L1	SPR L2	SPR L3
26	SPR H0	SPR H1	SPR H2	SPR H3
28	DPR L0	DPR L1	DPR L2	DPR L3
2A	DPR H0	DPR H1	DPR H2	DPR H3
2C				
2E				
30	LPR L0	LPR L1	LPR L2	LPR L3
32	LPR H0	LPR H1	LPR H2	LPR H3
34				
36				
38	BCR L0	BCR L1	BCR L2	BCR L3
3A	BCR H0	BCR H1	BCR H2	BCR H3
3C	CCR L0	CCR L1	CCR L2	CCR L3
3E	CCR H0	CCR H1	CCR H2	CCR H3

GCR = General Command Register
GSR = General Status Register
GMR = General Mode Register
GBR = General Burst Register
GDR = General Delay Register
CSR = Channel Status Register
DAR = Data Assembly Register

CPR = Command Pointer Register
SPR = Source Pointer Register
DPR = Destination Pointer Register
LPR = List Pointer Register
BCR = Byte Count Register
CCR = Channel Command Register

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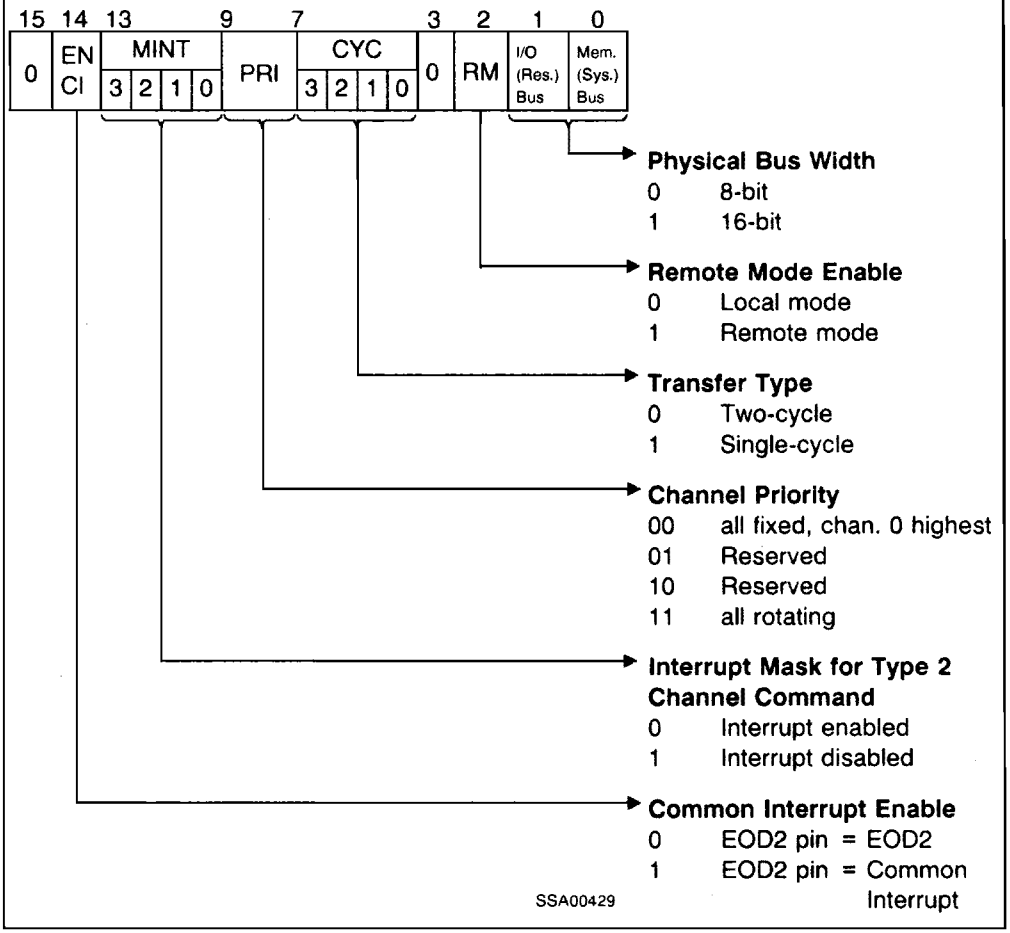
Register Description

General Mode Register

In the general mode register GMR (figure below) the system wide parameters are specified. This register should be programmed first after reset, with an 8-bit bus program low byte first.

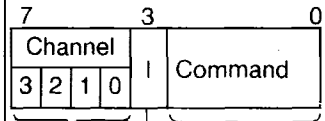
General Mode Register (GMR)



General Command Register

Individual channels are started and stopped by a command written to the general command register GCR (figure below). The GCR is directly loaded by the CPU.

General Command Register



Channel Command

000	NOP	
001	CONTINUE	Channel(s) after it has been stopped by the STOP command
010	START	Channel(s) = Command block at system/memory space
011	START	Channel(s) = Command block at resident I/O space
100	STOP	Channel(s)
101	---	Reserved
110	---	Reserved
111	HALT	Single-step channel(s): Start execution and stop before next command block will be loaded

Interrupt Command

0	NOP
1	Clear interrupt(s) of channel(s)

Channel Select

0	Channel not effected
1	Command refers to this channel

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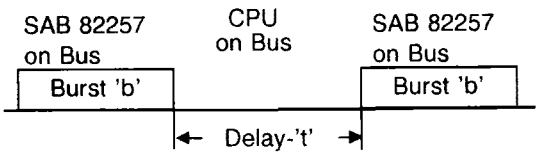
General Burst and Delay Register

It is possible to restrict the bus load generated by the SAB 82257 on the CPU bus by programming the burst and the delay register. The bus load is defined by the formula given in figure a) below. The factor b (burst) is programmed in the general burst register GBR, t (delay time) in the general delay register GDR (see figures b and c). Since the SAB 82257 can also execute locked bus cycles, the maximum burst length consists of b + 3 (8-bit bus) or b + 2 (16-bit bus) bus cycles. GBR and GDR must be directly loaded by the CPU. Loading GBR with 0 leads to no bus load limitations for the SAB 82257 (default after reset).

General Burst and Delay Register

a) Bus Loading

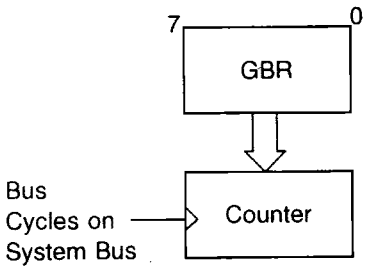


Bus Load due to the SAB 82257 $= \frac{b}{b+t}$

b) General Burst Register (GBR) – to Program 'b'

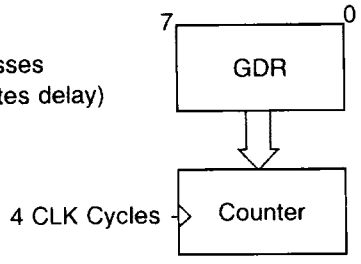
Determines max. number of contiguous bus cycles from the SAB 82257

If GBR = 0, No Limit



c) General Delay Register (GDR) – to Program 't'

Determines min. number of clock cycles between burst accesses (default after reset = 0,i.e. 4 T-states delay)



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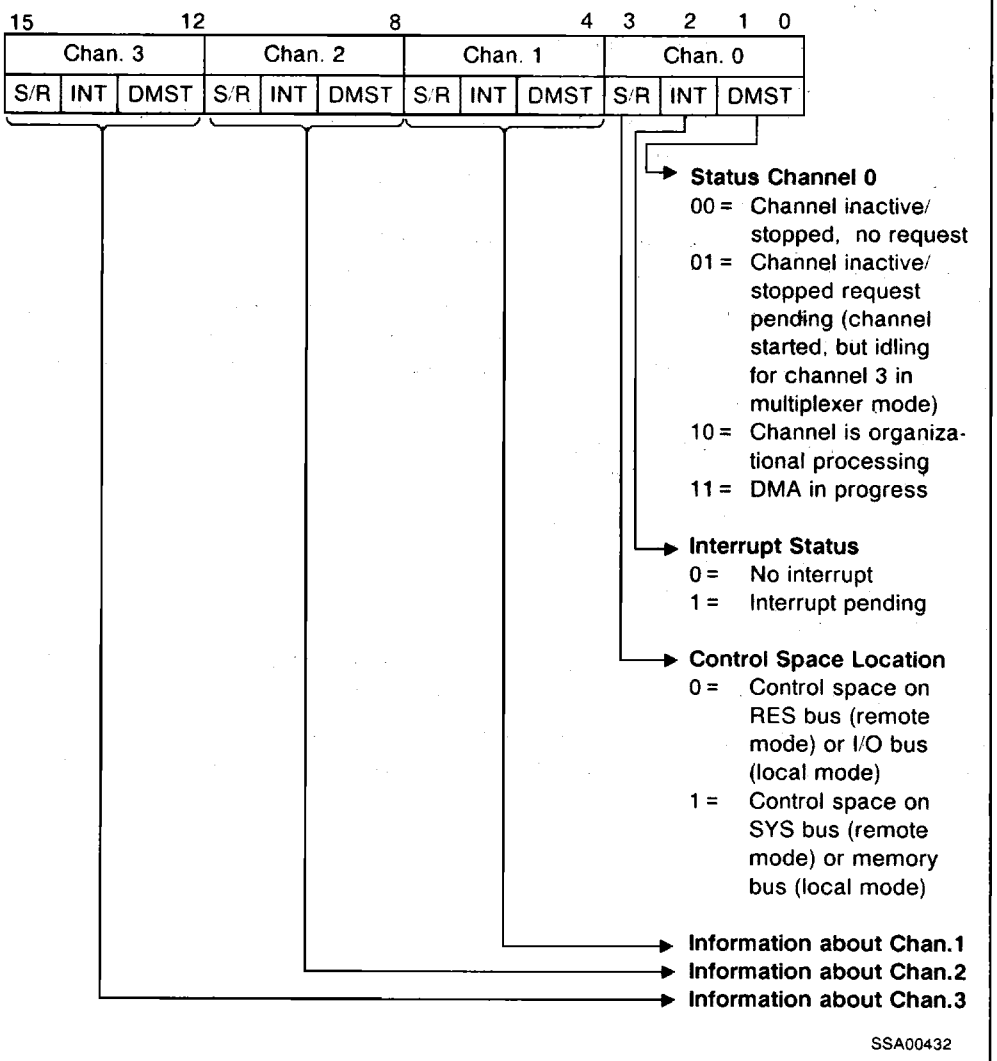
General Status Register

The general status register GSR (figure below) shows the current status of all the channels.

General Status Register (GSR)



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Channel Commands

The channel commands are contained in the channel command block. 15 bits are used to specify the command. There are two types of channel commands:

- Type 1: for data movement
- Type 2: for command chaining control

The command block for a type 1 command is 16 bytes long (see figure „Memory based Communication").

The type 1 command fields (see figures below) contain information on:

a. Bus width of source and destination
b. If source and/or destination address should be incremented or decremented or kept constant during the transfer
c. If source/destination is in memory or I/O space (local mode) or in system or resident space (remote mode)
d. If data chaining (list or linked-list) is to be performed
e. If the data transfer is synchronized (source or destination)

Type 2 command blocks are 6 bytes long (see figure „Type 2 Command Block") of which the first 2 bytes form the command and the rest is either a relative displacement or an absolute address for the JUMP operation. There are two basic type 2 commands (see figure „Type 2 Command Block"):

a. JUMP – conditional and non-conditional
b. STOP – conditional and non-conditional

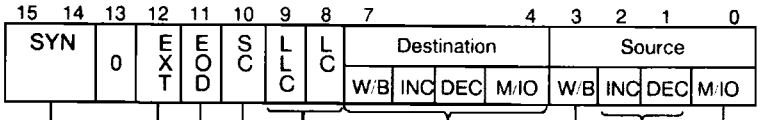
The conditional case tests for either of the 2 condition bits which are altered at the termination of any DMA operation:

- Termination due to byte count end
- Termination due to external terminate.

It is thus possible to JUMP or STOP further execution of commands based on any of these conditions and optionally generate an EOD# or interrupt signal.

The combination of type 1 and 2 commands gives the SAB 82257 a high degree of "programmability". It can thus execute quite complex algorithms with a fairly low demand for CPU service.

Type 1 (DMA) Channel Command



Source Description

Associated Space
0 I/O or resident
1 Memory or system

Source Pointer
00 Printer not modified
01 Decrement pointer
10 Increment pointer
11 No pointer (constant value)

Logical Bus Width
0 8-bit
1 16-bit

Destination Description
Same as source description

Data Chaining

LLC	LC	
0	0	No chaining
0	1	List chaining
1	0	Link list chaining
1	1	Not allowed

Select Chaining
0 Destination data chaining
1 Source data chaining

Enable EOD# Output

Enable External Terminate Input

Synchronization
00 Not valid(type 2 command)
01 Source synchronization
10 Destination synchronization
11 No synchronization (free running)

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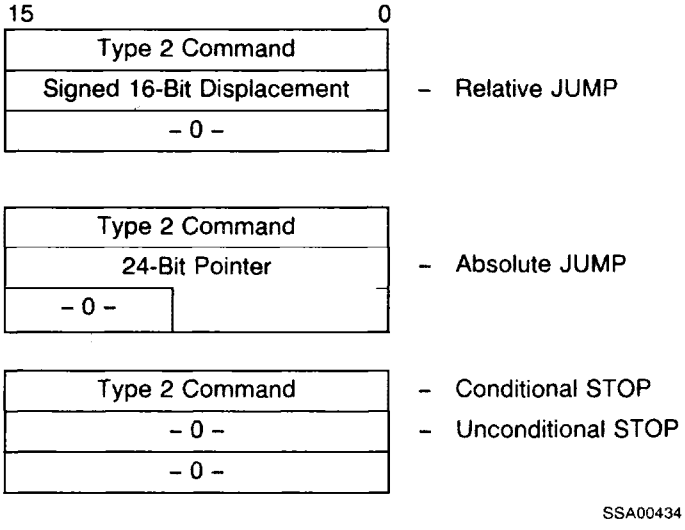
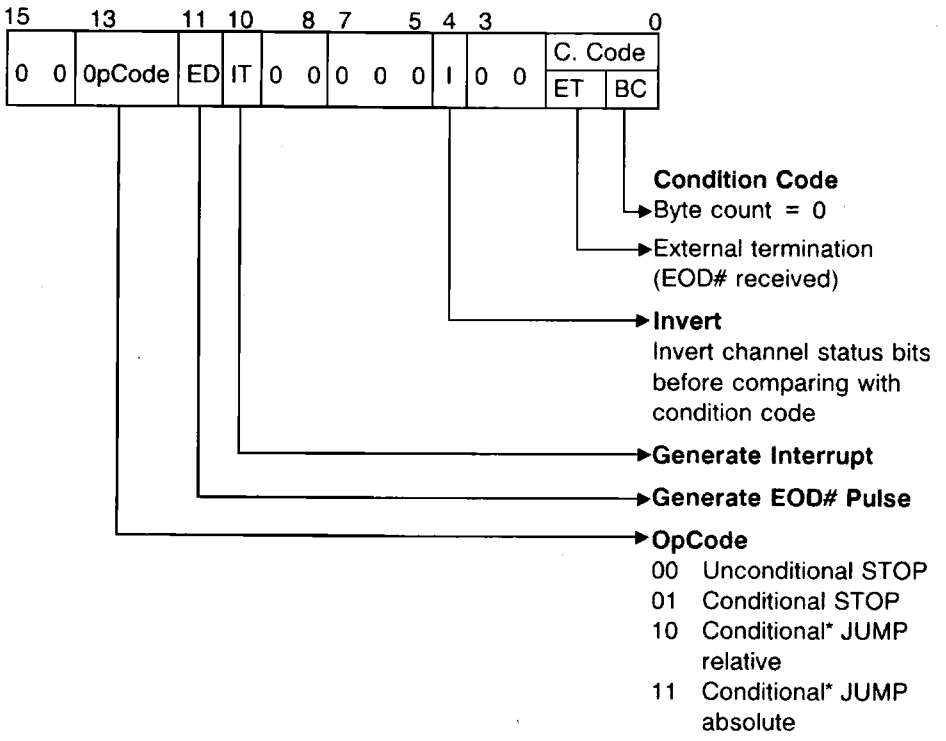
Type 2 Command Blocks (for command chaining control)



Type 2 Command Format



*) Unconditional JUMP when both condition code bits are set 1.

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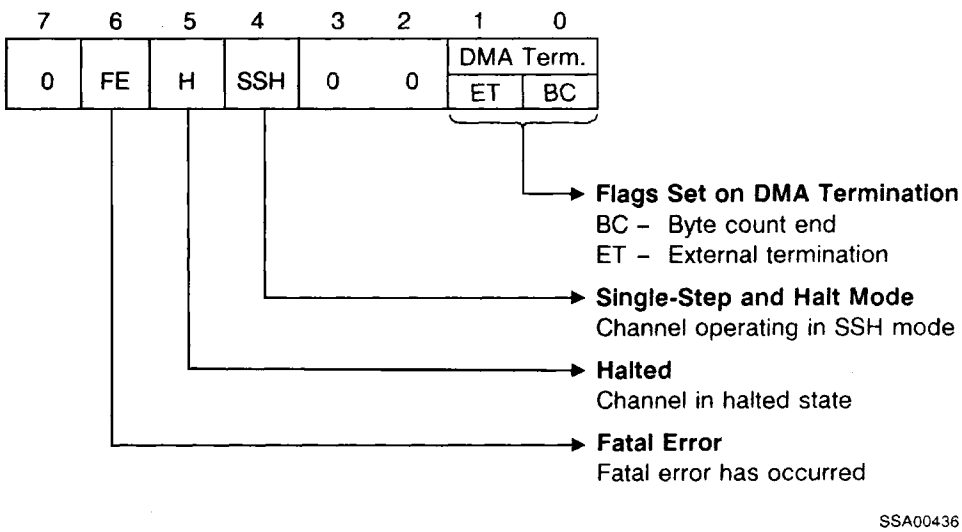
Channel Status Register

For each channel there is a channel status register (see figure below). This register shows the current state of the appropriate channel.

Channel Status Register



Timings

The bus timings in 286 and remote mode are identical to that for the SAB 80286, in 186 and 8086 mode the timings are identical to that for the SAB 80186. For exact timings see timing diagrams of AC Characteristics.

Asynchronous control inputs are specified with setup and hold times which are only important to determine whether the SAB 82257 responds to the signal in the current cycle or the next cycle.

The following pages hold two sections of AC characteristics and waveforms. The first section refers to 286 mode and remote mode, the second one to 186 mode and 8086 mode.

Absolute Maximum Ratings

Temperature under bias ..... 0 to 70°C
Storage temperature ..... – 65 to + 150°C
Voltage on any pin with respect to ground ..... – 0.5 to + 7 V
Power dissipation ..... 3.6 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics [1]

T_C = 0 to 100°C; V_{CC} = + 5 V ± 10%

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage (except CLK)	V_{IL}	– 0.5	+ 0.8	V	–
Input high voltage (except CLK)	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.45	V	I_{OL} = 3.0 mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = – 400 µA
Power supply current	I_{CC}	– –	550 385	mA mA	T_C = 0°C, (turn on) T_C = 100°C (steady operation) all outputs open
Input leakage current	I_{LI}				
S0#, S1#, S2#, BHE#, RD#, WR#, M/IO#		–	– 200	µA	0 V ≤ V_{IN} ≤ V_{CC}
HOLD (RQ#/GT# mode), EOD#		–	–1.5	mA	0 V ≤ V_{IN} ≤ V_{CC}
A23 (AREADY), A21 [2]		–	–1.5	mA	0 V ≤ V_{IN} ≤ V_{CC}
other pins		–	± 10	µA	0 V ≤ V_{IN} ≤ V_{CC}
Output leakage current	I_{LO}	–	± 10	µA	0.45 V ≤ V_{OUT} ≤ V_{CC}
Clock input low voltage	V_{CL}	– 0.5	+ 0.6	V	–
Clock input high voltage	V_{CH}	3.8	V_{CC} + 1.0	V	–

1) Clock must be applied.
2) This specification is valid only during RESET.

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Capacitance

$T_C = 25°C$; V_{CC} = GND = 0 V, $f_c = 1$ MHz

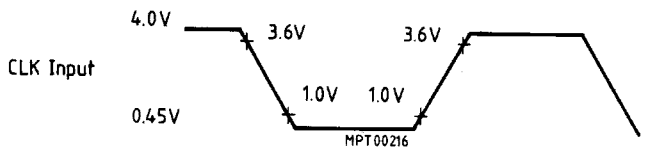
Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Capacitance of inputs (except CLK)	C_{IN}	–	10	pF	3)
Capacitance of I/O or outputs	C_{IO}	–	20	pF	3)
Capacitance of CLK input	C_{CLK}	–	12	pF	3)

3) Not 100% tested, guaranteed by design characterization.

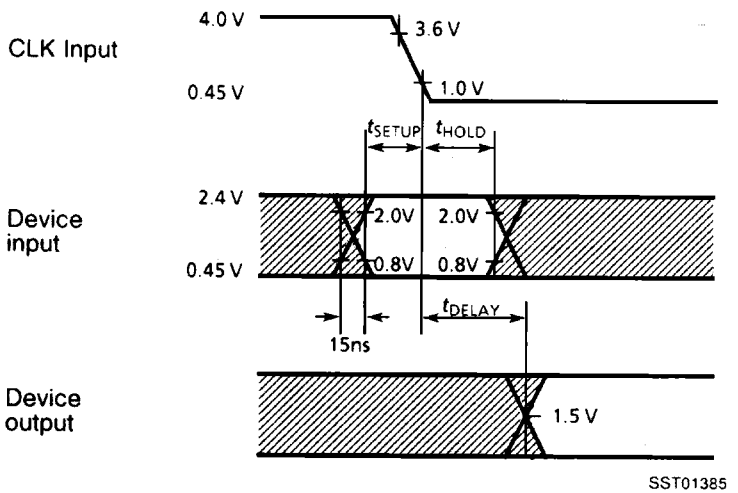
AC Testing Waveforms

Test Loading on Outputs

Drive and Measurement Points – CLK Input



Setup, Hold and Delay Time Measurement – General



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AC Characteristics SAB 82257 (286 mode)

T_C = 0 to 100°C; V_{CC} = +5 V ±10%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
CLK cycle period	t_1	62	250	ns	–
CLK low time	t_2	15	230	ns	at 1.0 V
CLK high time	t_3	20	235	ns	at 3.6 V
Address/control output delay	t_4	–	60	ns	C_L = 100 pF
Status output delay	t_5	–	40	ns	C_L = 100 pF
Sync data setup time	t_6	10	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync READY# setup time	t_8	38	–	ns	–
Sync READY# hold time	t_9	25	–	ns	–
Sync control input setup time	t_{10}	20	–	ns	–
Sync control/address input hold time	t_{11}	20	–	ns	–
Sync address setup time	t_{12}	2.5	–	ns	–
Data/control output delay	t_{13}	–	50	ns	C_L = 100 pF
Data/control float delay	t_{14}	–	50	ns	–
BHE# setup time	t_{15}	60	–	ns	–
Write command width	t_{16}	4CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	2CLK + t_6 + t_{44}	–	ns	–
Async address setup time	t_{18}	t_{43}	–	ns	–
Async data access time	t_{19}	–	5CLK + t_{43} + t_{13}	ns	–
Mode select setup time	t_{28}	2CLK + 20	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Command recovery time	t_{33}	4CLK + t_{43} + t_{44}	–	ns	–

AC Characteristics SAB 82257 (286 mode) cont'd

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
CLK rise time	t_{34}	–	15	ns	1.0 to 3.6 V
CLK fall time	t_{35}	–	15	ns	3.6 to 1.0 V
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
CS# active response time	t_{37}	2CLK	20CLK + t_{43} + t_{44}	ns	1)
CS# active after BREL inactive	t_{39}	0	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async input setup time	t_{43}	20	–	ns	2)
Async input hold time	t_{44}	20	–	ns	2)
Async HLDA high time	t_{47}	2CLK + t_{43} + t_{44}	–	ns	3)
HOLD output low time	t_{49}	4CLK – t_{13}	–	ns	–
HLDA low to HOLD low delay	t_{50}	6CLK	20CLK + t_{43} + t_{13}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	20	–	ns	–
Async access hold time	t_{55}	20	–	ns	–
CS# hold time	t_{56}	40	–	ns	–
DACK# output delay	t_{59}	–	50	ns	–

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- normal pointer transfer (3 bus cycles): 16 CLK
- splitted pointer transfer (4 bus cycles): 20 CLK

If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

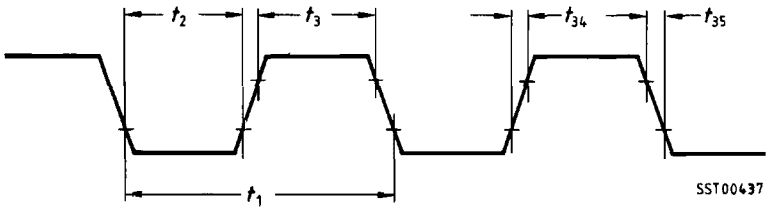
2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

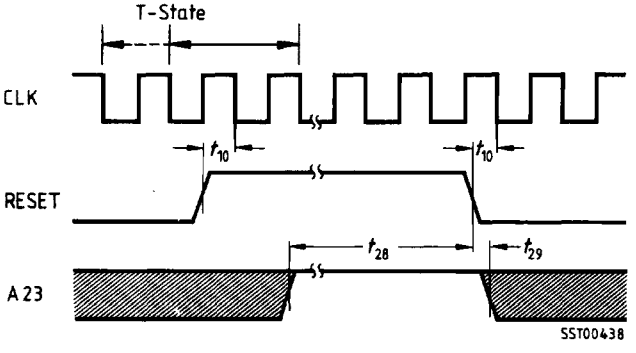
4

Waveforms

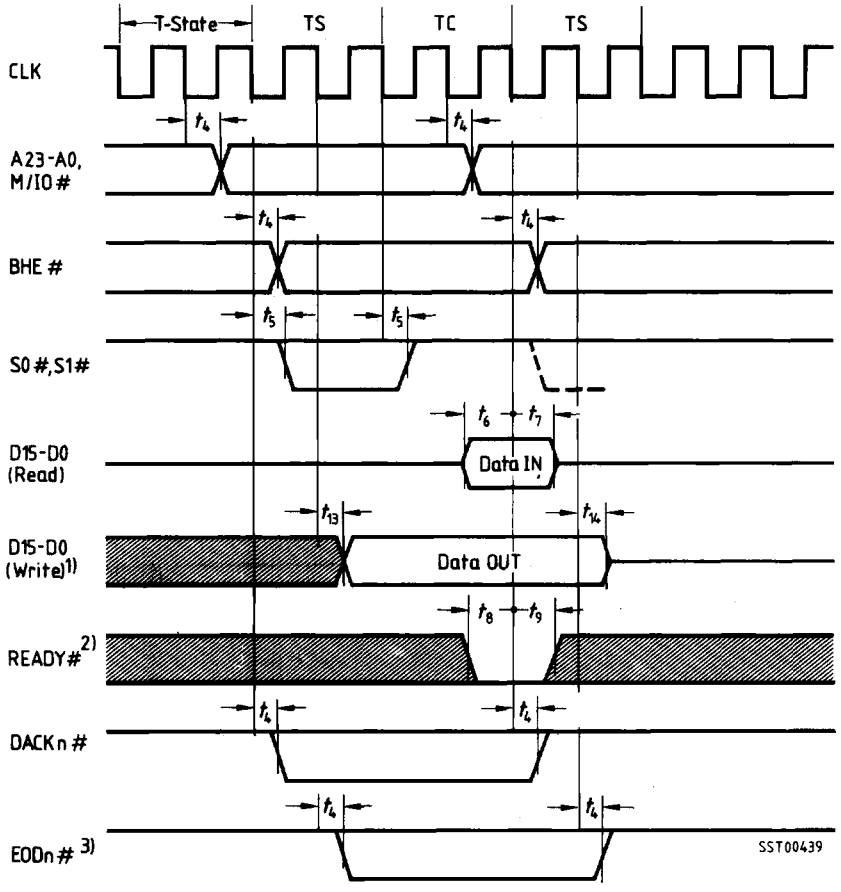
Clock Signal (286 mode)



Mode Selection on RESET (286 mode)



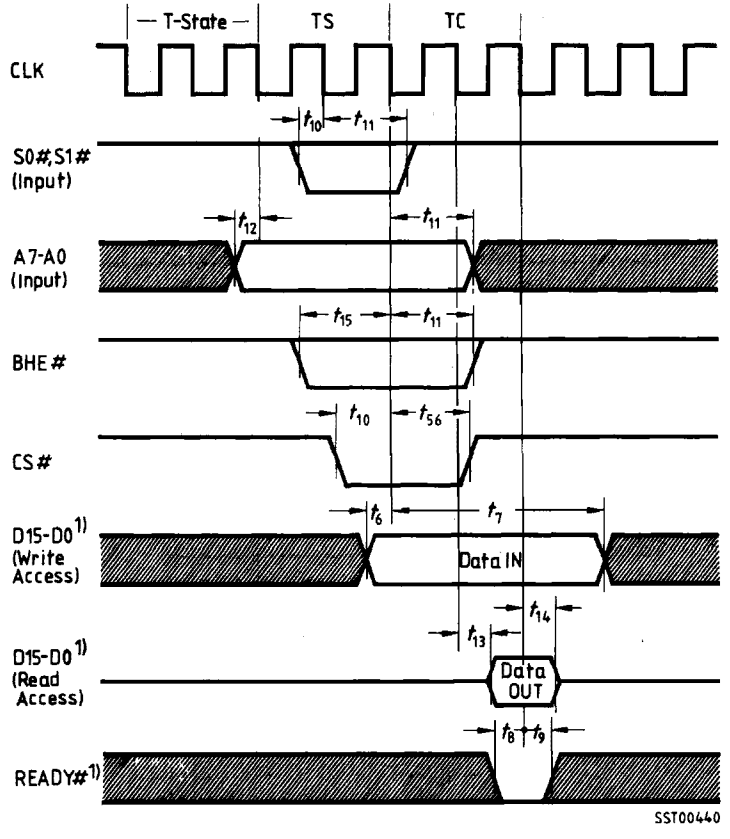
Major Timing for Active Bus Cycles (286 mode)



1) If executing a single cycle transfer, D15 to D0 float like during read cycles!
2) TC will be repeated, if READY# is inactive at the sampling point (end of current TC).
3) Initiated by terminal count.

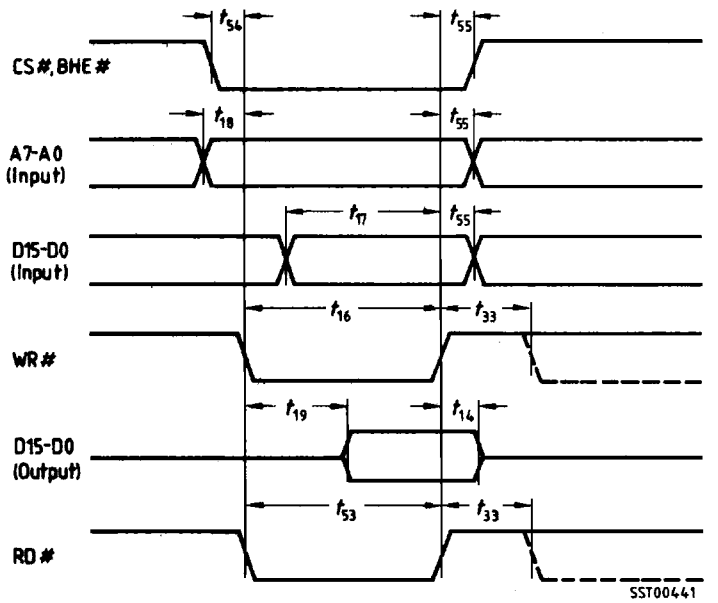
4

Synchronous Access (286 mode)



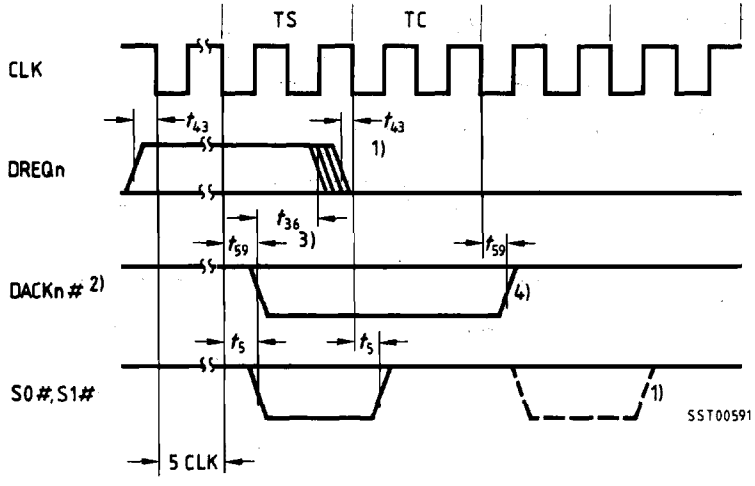
1) The processor will repeat TC, if READY# is not active at the sampling point (end of current TC). The SAB 82257 will output data until the end of the repeated TC (read access) or sample the data bus again at the beginning of the repeated TC (write access).

Asynchronous Access (286 mode)



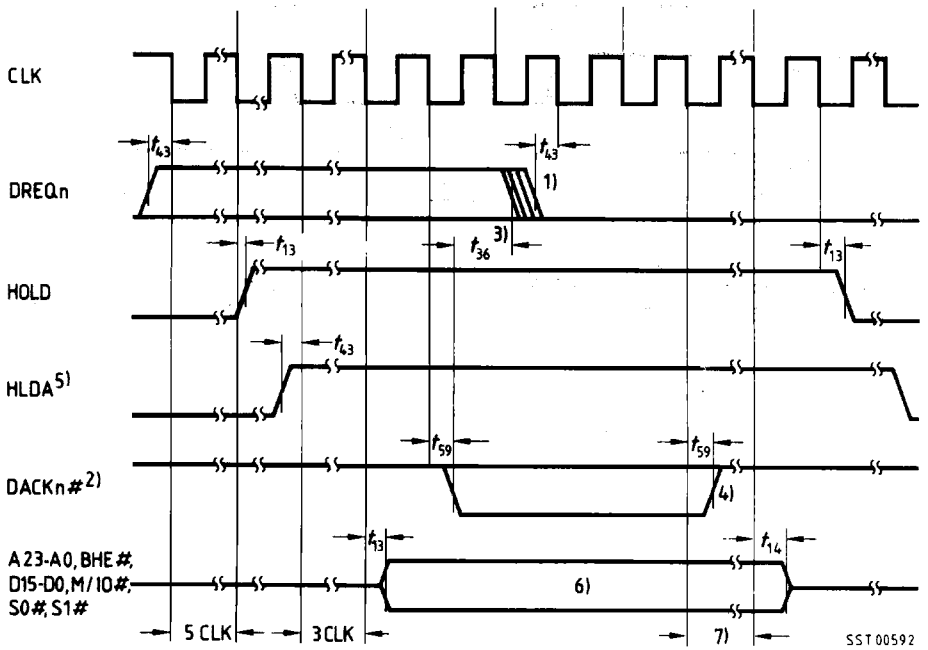
4

DMA Control Without Bus Arbitration (286 mode)



1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) Minimum time to execute bus cycle.
4) If the SAB 82257 does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

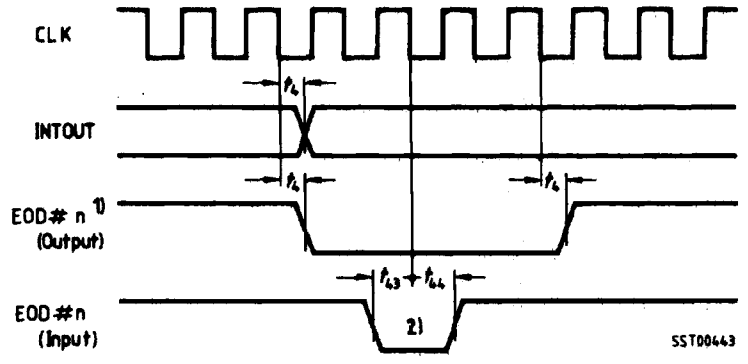
DMA Control With Bus Arbitration (286 mode)



1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) Minimum time to execute bus cycle.
4) If the SAB 82257 does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.
5) The SAB 82257 can be forced off the bus by driving HLDA inactive (see "Bus Arbitration").
6) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycle".
7) The SAB 82257 may execute additional bus cycles, e.g. for command chaining.

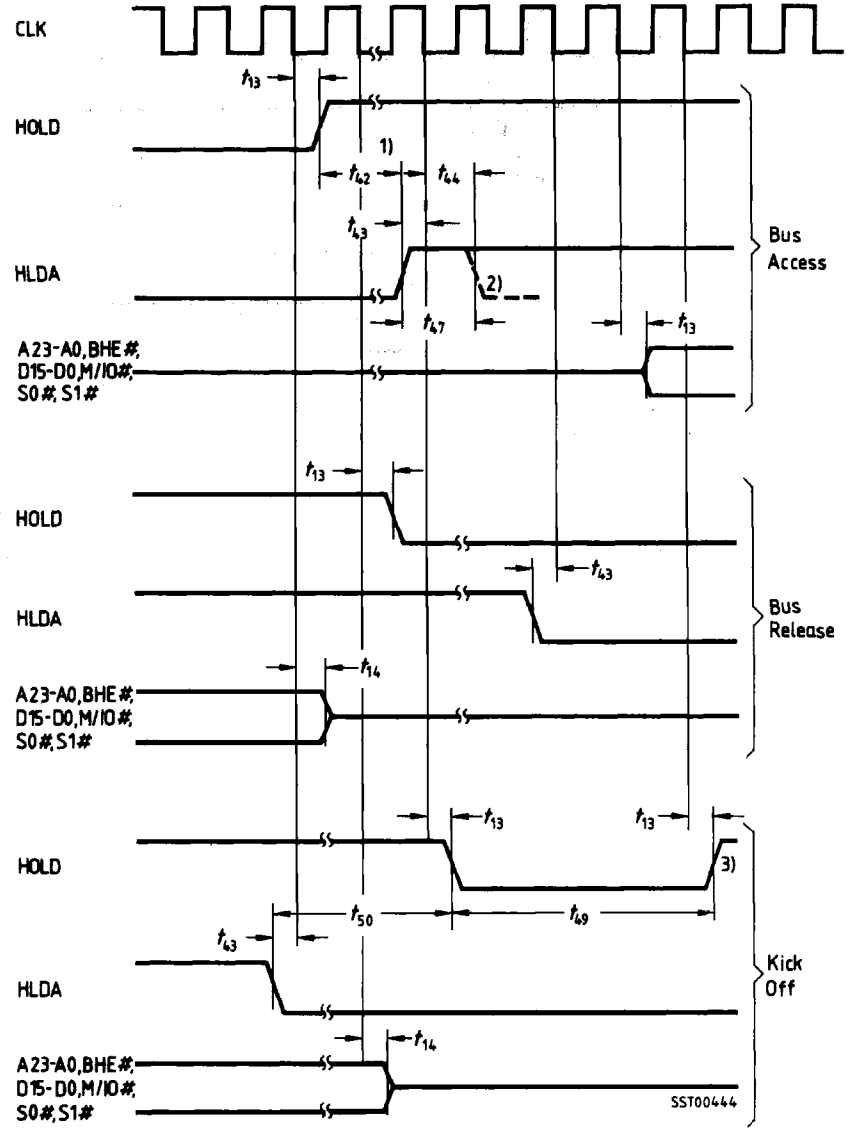
4

EOD#/INTOUT Timing (286 mode)



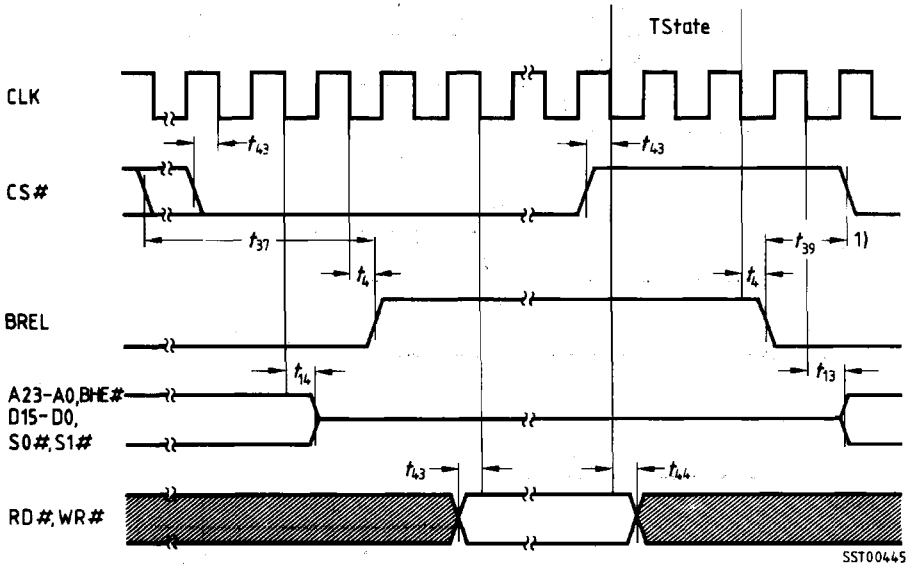
1) Initiated by type 2 command.
2) EOD# input minimum pulse width is 3 CLKs, if the signal is asynchronous.

Bus Arbitration (286 mode)



1) To avoid arbitration conflicts, HLDA should not become active before HOLD.
2) Minimum HLDA high time before kick-off to respond to HOLD signal.
3) Earliest possible reactivation of HOLD after deactivation of HLDA.

Access in Remote Mode



1) Required to avoid bus conflicts.

This diagram shows the times when the output signals are driven active and input signals are recognized, rather than the exact timing.

AC Characteristics SAB 82257 (186 mode)

T_C = 0 to 100°C; V_{CC} = +5 V ±10%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Control output delay	t_4	–	60	ns	–
Sync address/data setup time	t_6	10	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync control input setup time	t_{10}	20	–	ns	–
Sync control/address input hold time	t_{11}	20	–	ns	–
Data/control delay	t_{13}	–	50	ns	C_L = 100 pF
Data float delay	t_{14}	–	50	ns	–
Write command width	t_{16}	2CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	1CLK + 30	–	ns	–
Async address setup time	t_{18}	20	–	ns	–
Async data access time	t_{19}	–	2CLK + t_{22} + t_{43} + t_{13}	ns	–
CLK cycle period	t_{20}	125	500	ns	–
CLK low time	t_{21}	55	–	ns	at 1.5 V
CLK high time	t_{22}	55	–	ns	at 1.5 V
CLK rise time	t_{23}	–	15	ns	1.0 to 3.5 V
CLK fall time	t_{24}	–	15	ns	3.5 to 1.0 V
AREADY active setup time	t_{25}	20	–	ns	2)
AREADY hold time	t_{26}	15	–	ns	2)
AREADY inactive setup time	t_{27}	35	–	ns	–
Mode select setup time	t_{28}	2CLK + 20	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Address/data output delay	t_{30}	10	50	ns	C_L = 20 to 200 pF
Status output delay	t_{31}	10	55	ns	–
Float delay	t_{32}	10	50	ns	–

4

AC Characteristics SAB 82257 (186 mode) cont'd

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Command recovery time	t_{33}	2CLK + t_{43} + t_{44}	–	ns	–
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
ALE output delay	t_{38}	–	40	ns	–
Address/control input hold time	t_{40}	10	–	ns	–
Address input setup time	t_{41}	20	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async control input setup time	t_{43}	20	–	ns	2)
Async control input hold time	t_{44}	20	–	ns	2)
HLDA hold time	t_{45}	10	–	ns	–
Async HLDA high time	t_{46}	1CLK + t_{43} + t_{45}	–	ns	3)
HOLD output delay	t_{48}	5	70	ns	–
HLDA output low time	t_{51}	2CLK – t_{48max}	–	ns	–
HLDA low to HOLD low delay	t_{52}	3CLK	16CLK + t_{43} + t_{48}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	20	–	ns	–
Async access hold time	t_{55}	20	–	ns	–
SREADY hold time	t_{57}	15	–	ns	–
Status setup time	t_{58}	35	–	ns	–
DACK# output delay	t_{60}	–	60	ns	–
Status hold time	t_{61}	10			

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- normal pointer transfer (3 bus cycles): 12 CLK
- splitted pointer transfer (4 bus cycles): 16 CLK

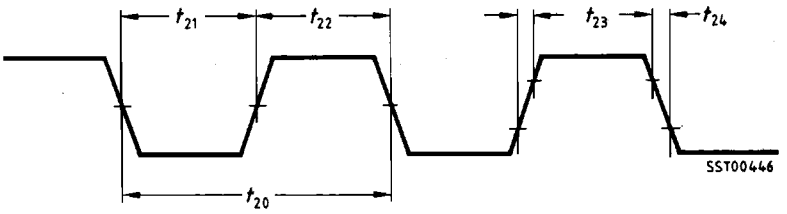
If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

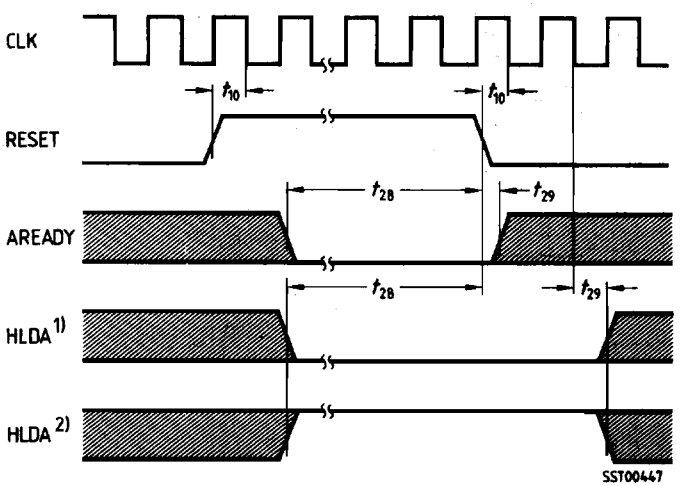
3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

Waveforms

Clock Signal (186 mode)



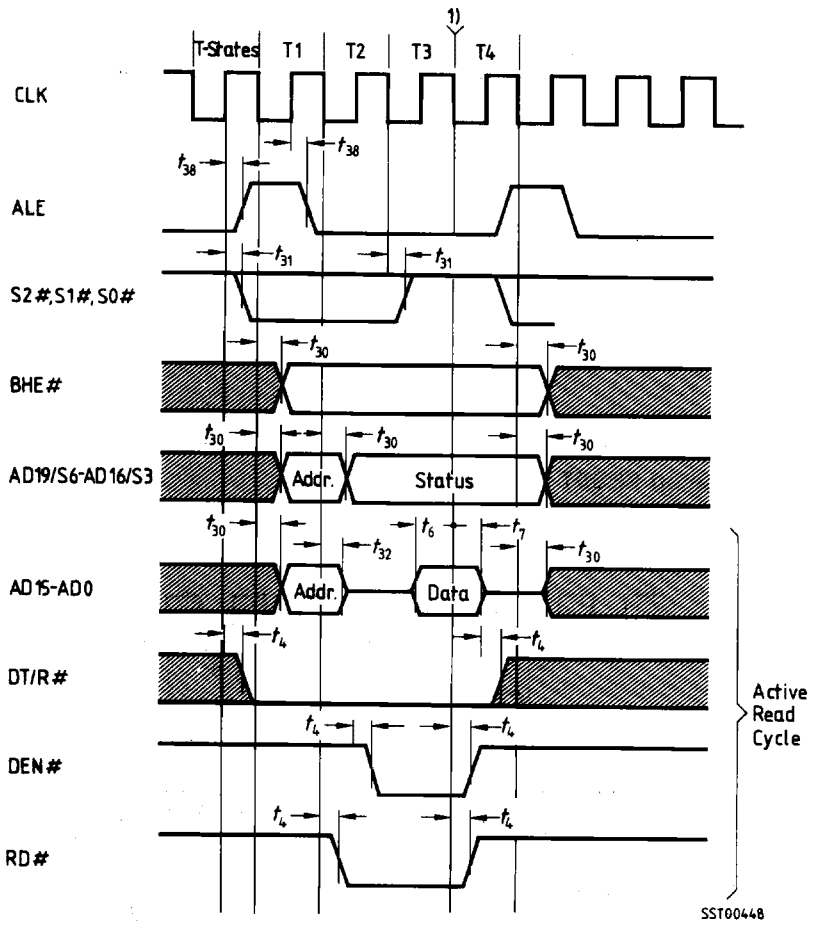
Mode Selection on RESET (186 mode)



1) To operate in 186 mode with HOLD/HLDA protocol.
2) To operate in 8086 mode with RQ#/GT# protocol.

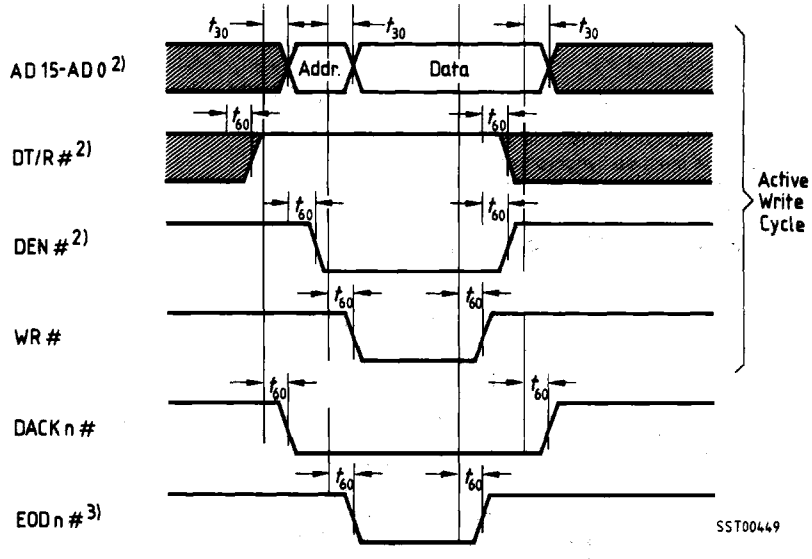
4

Major Timing for Active Bus Cycle (186 mode) a)



1) A wait state is inserted after T3 or TW, whenever the bus is not ready at the beginning of T3 or TW (see "Bus Cycle Termination"). The status must be valid just prior to T4.

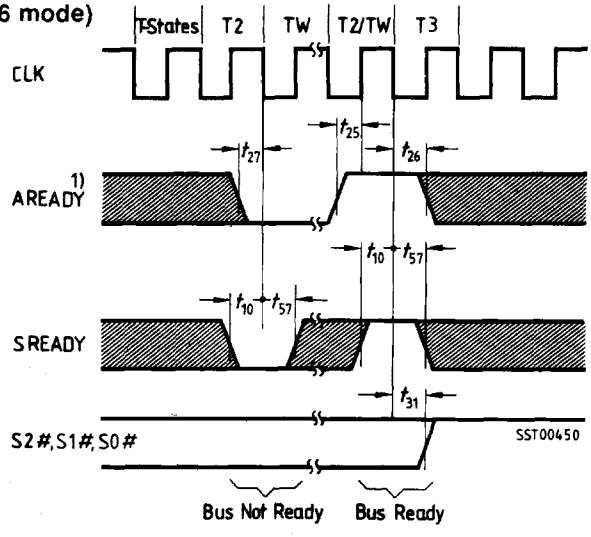
Major Timing for Active Bus Cycle (186 mode) b)



2) For a single-cycle transfer the timing of AD15-AD0,DT/R# and DEN# is identical to a read cycle. AD15-AD0 will float as during a read cycle.
3) Initiated by terminal count.

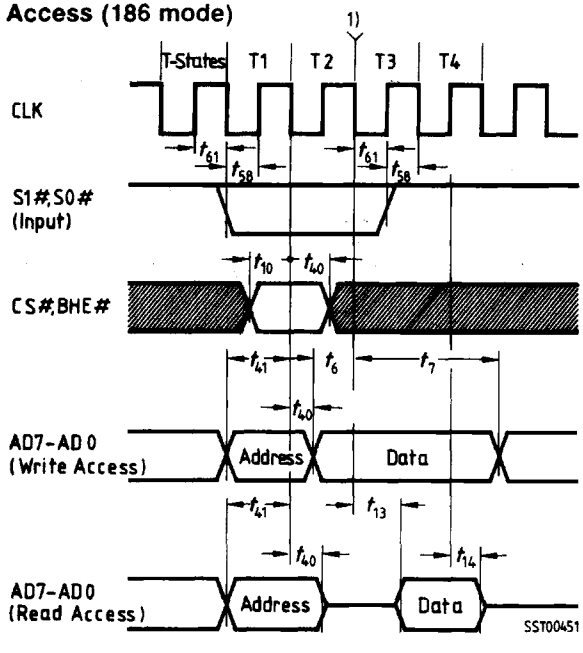
4

Bus Cycle Termination (186 mode)



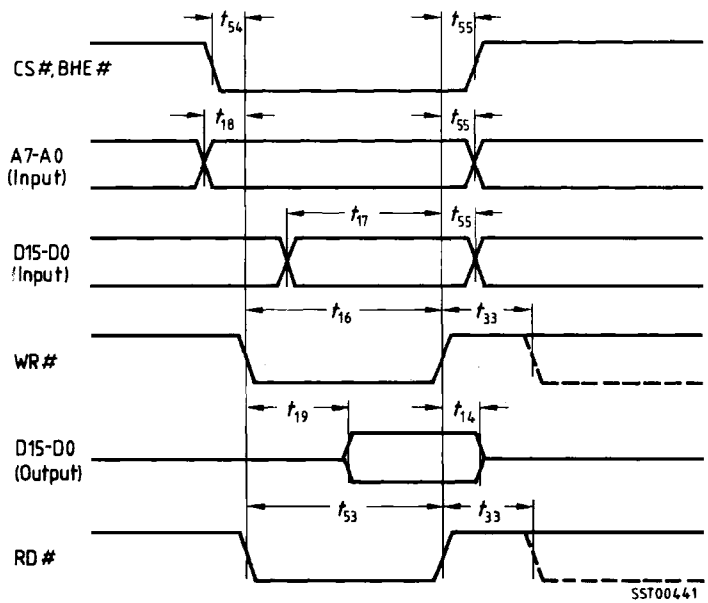
1) Only the rising edge of AREADY is synchronized internally to CLK. The falling edge must be synchronized externally.

Synchronous Access (186 mode)



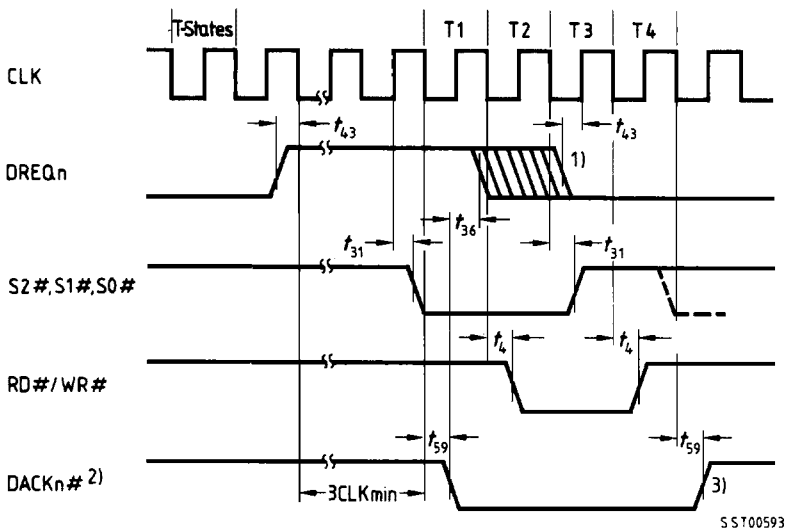
1) Additional wait cycles may be inserted. Status must be valid just prior to T4.

Asynchronous Access (186 mode)



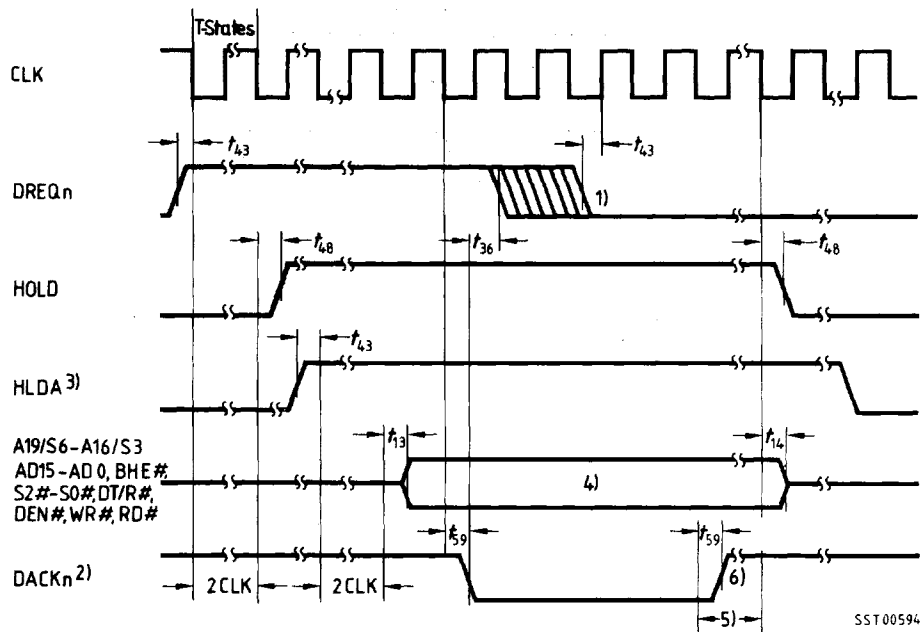
4

DMA Control Without Bus Arbitration (186 mode)



1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) If the SAB 82257 does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

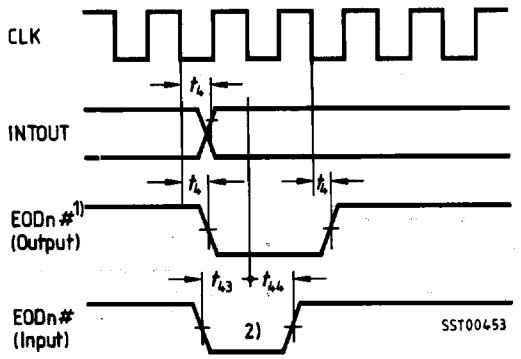
DMA Control With Bus Arbitration (186 mode)



1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) The SAB 82257 can be forced off the bus by driving HLDA inactive (see "Bus Arbitration").
4) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycle".
5) The SAB 82257 may execute additional bus cycles, e.g. for command chaining.
6) If the SAB 82257 does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

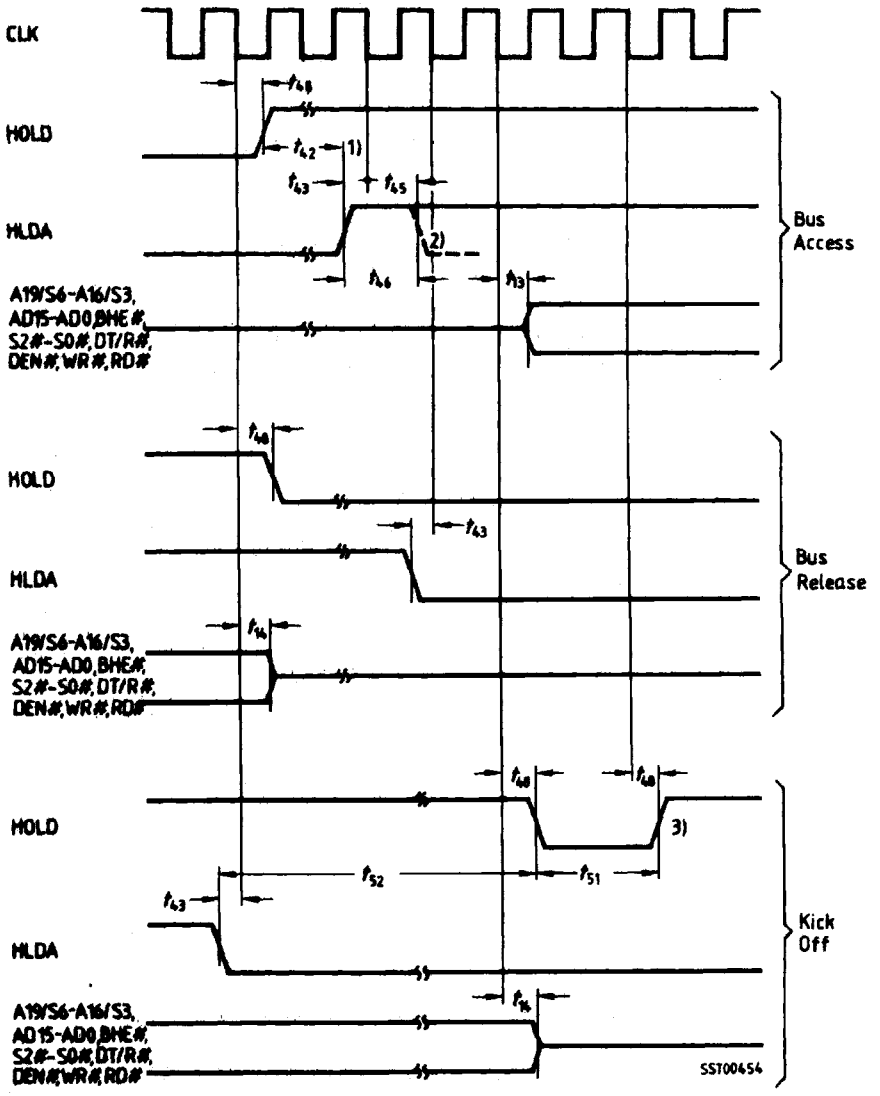
4

EOD#/INTOUT Timing (186 mode)



1) Initiated by type 2 command.
2) EOD# input minimum pulse width is 2 CLKs, if the signal is asynchronous.

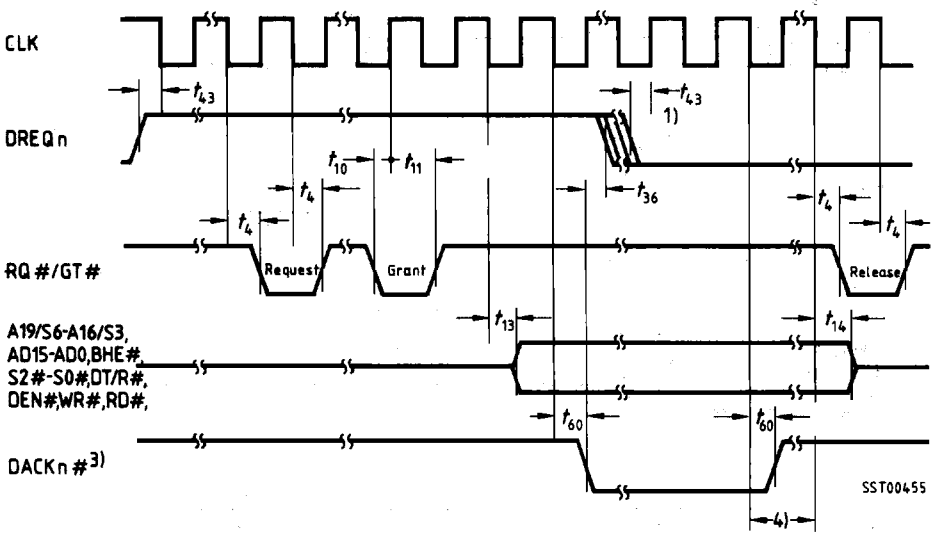
Bus Arbitration (186 mode)



1) To avoid arbitration conflicts, HLDA should not become active before HOLD.
2) Minimum HLDA high time before kick-off to respond to HOLD signal.
3) Earliest possible reactivation of HOLD after deactivation of HLDA.

4

DMA Control with RQ#/GT# Protocol (8086 mode)



1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent bus cycles are executed.
2) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycles".
3) Refers to the highest priority request. Acknowledge of lower priority requests may be delayed by higher priority requests.
4) The SAB 82257 may execute additional bus cycles, e.g. for command chaining.