

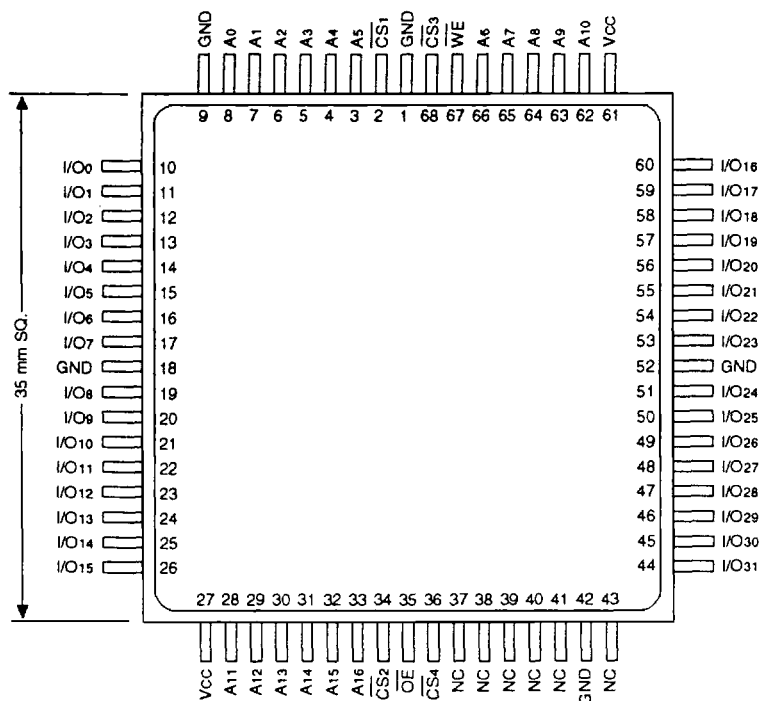


FIGURE 1 — Pin Configuration

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground

Pin Description

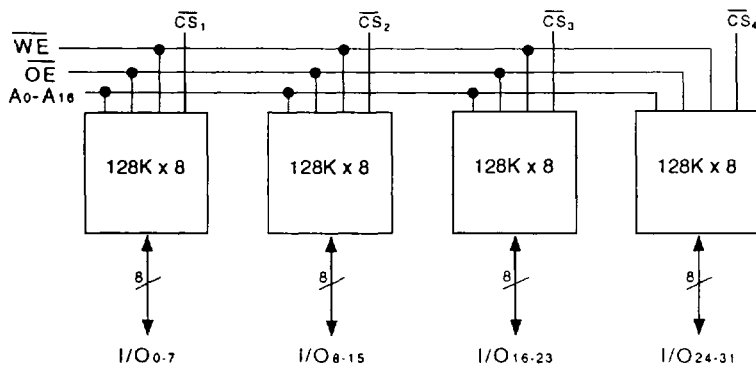


FIGURE 2 — Block Diagram

WS-128K32-XG4X

Advanced* 4 Megabit CMOS SRAM Module

FEATURES

- Access Times of 25nS to 120nS
- 68 lead, 35 mm Gull Wing Ceramic QFP
- User Configurable as 128Kx32, 256Kx16 or 512Kx8
- Battery Back-Up Operation
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Low Power CMOS Fully Static Design
- 5 Volt Power Supply
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

DESCRIPTION

The White Technology WS-128K32-XG4X is a 4-megabit CMOS SRAM module organized as 128K words by 32 bits; 256K x 16 or 512K x 8. The module is constructed on a ceramic substrate, hermetically sealed with a welded metal cover, on a 35mm square gull wing package, utilizing four 128K x 8 SRAM devices.

The WS-128K32-XG4X is available with access times of 25 to 120nS over the military temperature ranges.

* This data sheet describes a product under development and is subject to change without notice.

WH15012

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Commercial	Military	Unit
Operating Temperature	T _A	0 to +70	-55 to +125	°C
Storage Temperature	T _{stg}	-40 to +85	-65 to +150	°C
Signal Voltage Relative to GND	V _G	-0.5 to +7.0	-0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL} ⁽¹⁾	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

(1) V_{IL} (min.) = 3.0V for pulse width less than 20ns.

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby (deselect/power down)
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active (deselect)
L	X	L	Write	Data In	Active

CAPACITANCE

(@ T_A = 25°C)

Parameter	Symbol	Condition	Max	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	30	pF
Output Capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	30	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Sym	Conditions	-25		-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = Max, V _{IN} = GND or V _{CC}		15		15		15		15	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		15		15		15		15	μA
Operating Supply Current x 32 Mode	I _{CC} x 32	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , Duty Cycle = Max		400		400		350		350	mA
Operating Supply Current x 16 Mode	I _{CC} x 16	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , Duty Cycle = Max		280		280		250		250	mA
Operating Supply Current x 8 Mode	I _{CC} x 8	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , Duty Cycle = Max		150		150		130		130	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{CC} , $\overline{OE}$ = V _{IH} , Duty Cycle = Max		60		60		40		35	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = Min		0.4		0.4					V
		I _{OL} = 2.1mA, V _{CC} = Min						0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = Min	2.4		2.4						V
		I _{OH} = -1.0mA, V _{CC} = Min					2.4		2.4		V

Parameter	Sym	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = Max, V _{IN} = GND or V _{CC}		15		15		15		15	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		15		15		15		15	μA
Operating Supply Current x 32 Mode	I _{CC} x 32	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , Duty Cycle = Max		300		300		250		250	mA
Operating Supply Current x 16 Mode	I _{CC} x 16	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , Duty Cycle = Max		225		225		200		200	mA
Operating Supply Current x 8 Mode	I _{CC} x 8	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , Duty Cycle = Max		120		80		70		70	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{CC} , $\overline{OE}$ = V _{IH} , Duty Cycle = Max		7		7		5		5	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA		0.4		0.4		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0mA	2.4		2.4		2.4		2.4		V

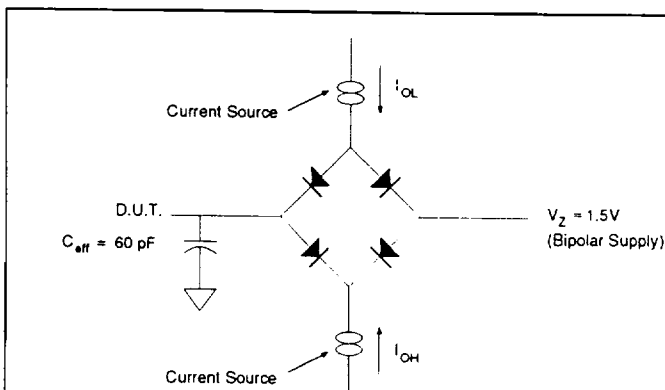


FIGURE 3 — AC Test Circuit

AC TEST CONDITIONS

Parameter	Typ.	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

V_Z is programmable from -2V to +7V

I_{OL} & I_{OH} programmable from 0 to 16mA

Tester Impedance Z₀ = 75 Ω

V_Z is typically the midpoint of V_{OH} and V_{OL} (i.e. (2.4 + 0.4)/2 = 1.4V)

I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE Tester Includes Jig Capacitance

AC ELECTRICAL CHARACTERISTICS

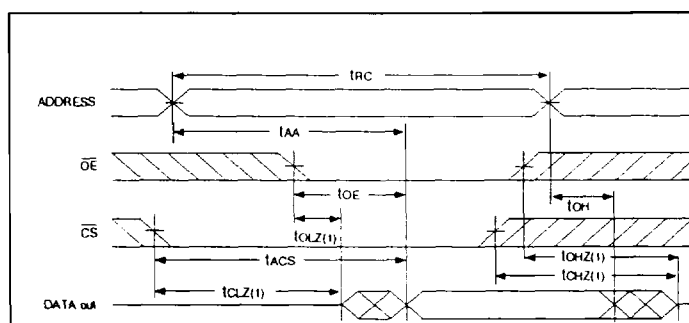
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	-25		-35		-45		-55		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	25		35		45		55		nS
Address Access Time	t _{AA}		25		35		45		55	nS
Data Hold from Address Change	t _{OH}	4		4		4		4		nS
Chip Select Access	t _{ACS}		25		35		45		55	nS
Output Enable to Output Valid	t _{OE}		15		20		25		30	nS
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		5		5		nS
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		nS
Chip Deselect to Output in High Z	t _{CHZ} ¹		12		15		20		25	nS
Output Disable to Output in High Z	t _{OHZ} ¹		12		15		20		25	nS

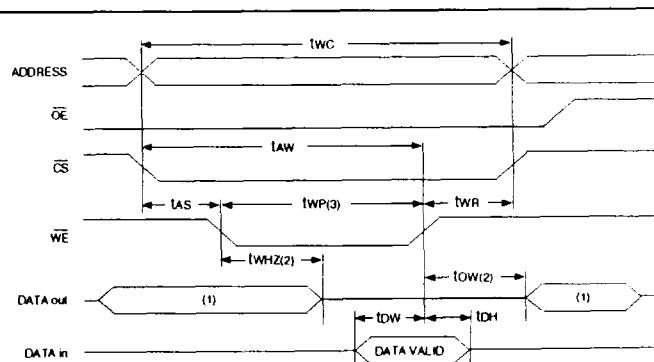
1. This parameter is guaranteed by design but not tested.

Parameter	Symbol	-70		-85		-100		-120		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	70		85		100		120		nS
Address Access Time	t _{AA}		70		85		100		120	nS
Data Hold from Address Change	t _{OH}	5		5		5		5		nS
Chip Select Access	t _{ACS}		70		85		100		120	nS
Output Enable to Output Valid	t _{OE}		35		40		45		50	nS
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		5		5		nS
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		nS
Chip Deselect to Output in High Z	t _{CHZ} ¹		30		35		40		50	nS
Output Disable to Output in High Z	t _{OHZ} ¹		30		35		40		50	nS

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORMS

FIGURE 4 — Read Cycle Timing

1. Measured ± 200mV steady state; guaranteed by design but not tested.


FIGURE 5 — Write Cycle Timing $\overline{WE}$ Controlled

- I/O pins are in their output state, input signals must not be applied.
- This parameter is guaranteed by design but not tested.
- A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle										
Write Cycle Time	t _{WC}	25		35		45		55		nS
Chip Select to End of Write	t _{CW}	20		30		40		45		nS
Address Valid to End of Write	t _{AW}	20		30		40		45		nS
Data to Write-Time Overlap	t _{DW}	15		18		20		25		nS
Write Pulse Width	t _{WP}	20		25		35		40		nS
Address Setup Time	t _{AS}	0		0		0		0		nS
Write Recovery Time	t _{WR}	0		0		0		0		nS
Output Active from End of Write	t _{OW} ¹	5		5		5		5		nS
Write to Output in High Z	t _{WHZ} ¹		10		15		15		20	nS
Data Hold from Write Time	t _{DH}	3		3		3		5		nS

1. This parameter is guaranteed by design but not tested.

Parameter	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle										
Write Cycle Time	t _{WC}	70		85		100		120		nS
Chip Select to End of Write	t _{CW}	65		80		90		110		nS
Address Valid to End of Write	t _{AW}	65		80		90		110		nS
Data to Write-Time Overlap	t _{DW}	30		35		40		55		nS
Write Pulse Width	t _{WP}	45		50		55		65		nS
Address Setup Time	t _{AS}	5		5		5		5		nS
Write Recovery Time	t _{WR}	0		0		0		0		nS
Output Active from End of Write	t _{OW} ¹	5		5		5		5		nS
Write to Output in High Z	t _{WHZ} ¹		30		35		40		50	nS
Data Hold from Write Time	t _{DH}	5		5		5		5		nS

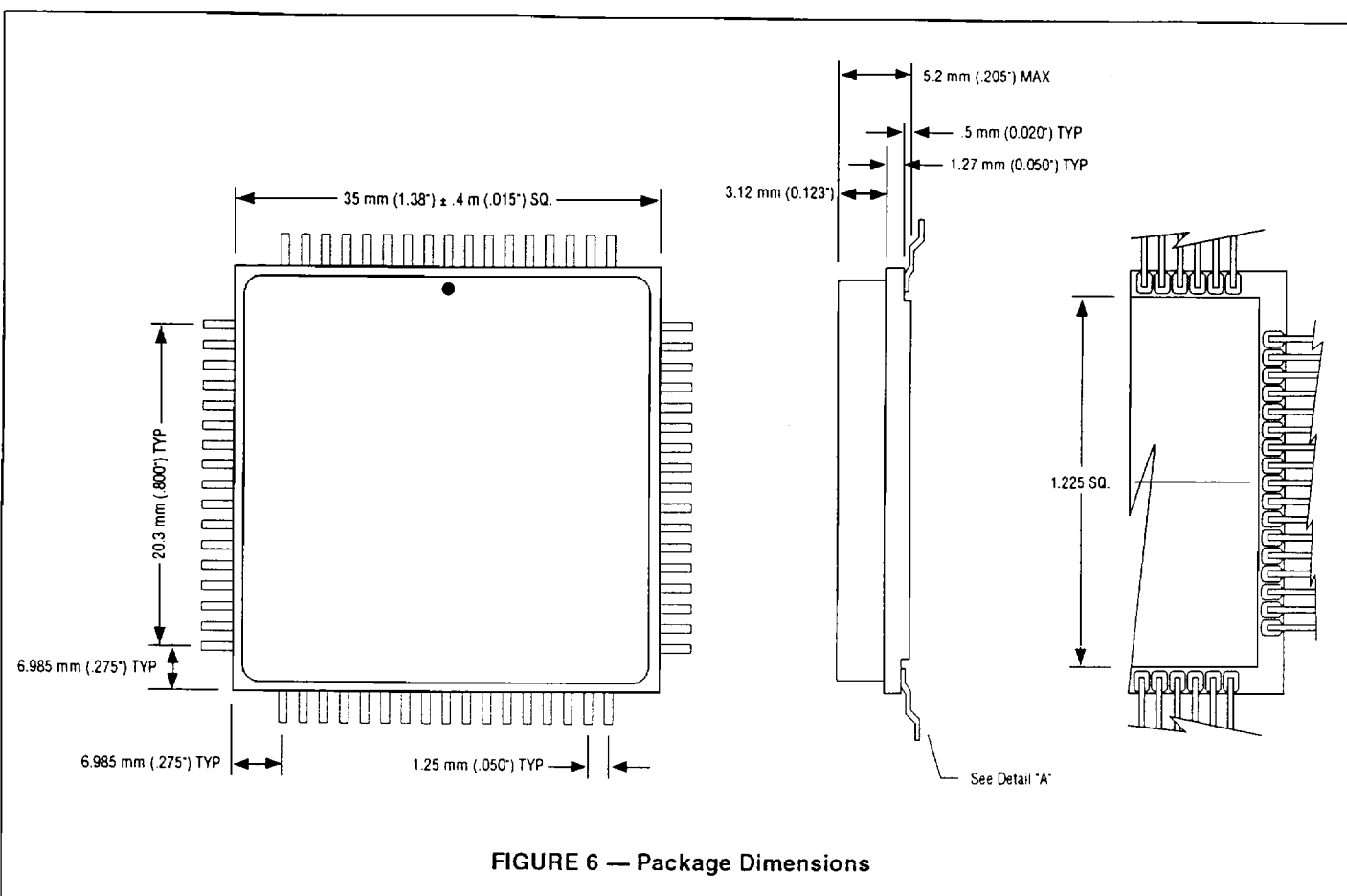
1. This parameter is guaranteed by design but not tested.

DATA RETENTION CHARACTERISTICS

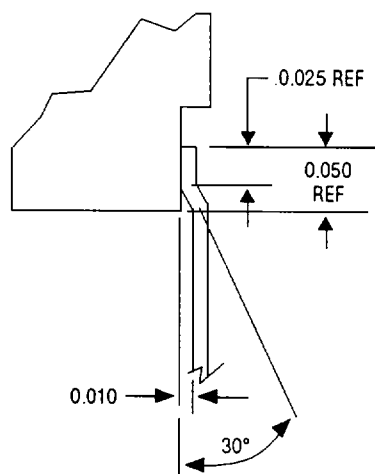
(T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	-25			-35			-45			-55			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \geq V_{CC} - .2V$	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		.3	6.0		.3	6.0		.5	6.0		.03	3.2	mA
	I _{CCDR2}	V _{CC} = 2V		.15	4		.15	4		.25	2.5		.02	2.0	mA

Parameter	Symbol	Conditions	-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \geq V_{CC} - .2V$	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		30	1500		30	1500		10	1100		10	1500	μA
	I _{CCDR2}	V _{CC} = 2V		20	1000		20	1000		7	750		7	1000	μA



DETAIL "A"



ORDERING INFORMATION

W S - 128K 32 - XXX G4 X X

SPECIAL PROCESSING:

E = Rad Tolerant Die

DEVICE GRADE:

C = Commercial, 0 to 70°C

I = Industrial, -40°C to 85°C

M = Military, -55°C to 125°C

PACKAGE TYPE:

G4 = Ceramic 35 mm Quad Flat Pack - Gull Wing

ACCESS TIME IN nS

ORGANIZATION, 128Kx32

User configurable as 256Kx16 or 512Kx8

SRAM

WHITE TECHNOLOGY

This data has been carefully checked and is believed to be accurate. The information contained herein is not intended to and does not create any warranty of merchantability or fitness for a particular purpose. White Technology reserves the right to change specifications at any time without notice.

White Technology, Inc.

A wholly owned subsidiary of Bowmar Instrument Corporation

4246 East Wood Street

Tel: 602-437-1520

Phoenix, Arizona 85040

Fax: 602-437-9120