Standard Products

MIP 7965
64-Bit Superscaler Microprocessor

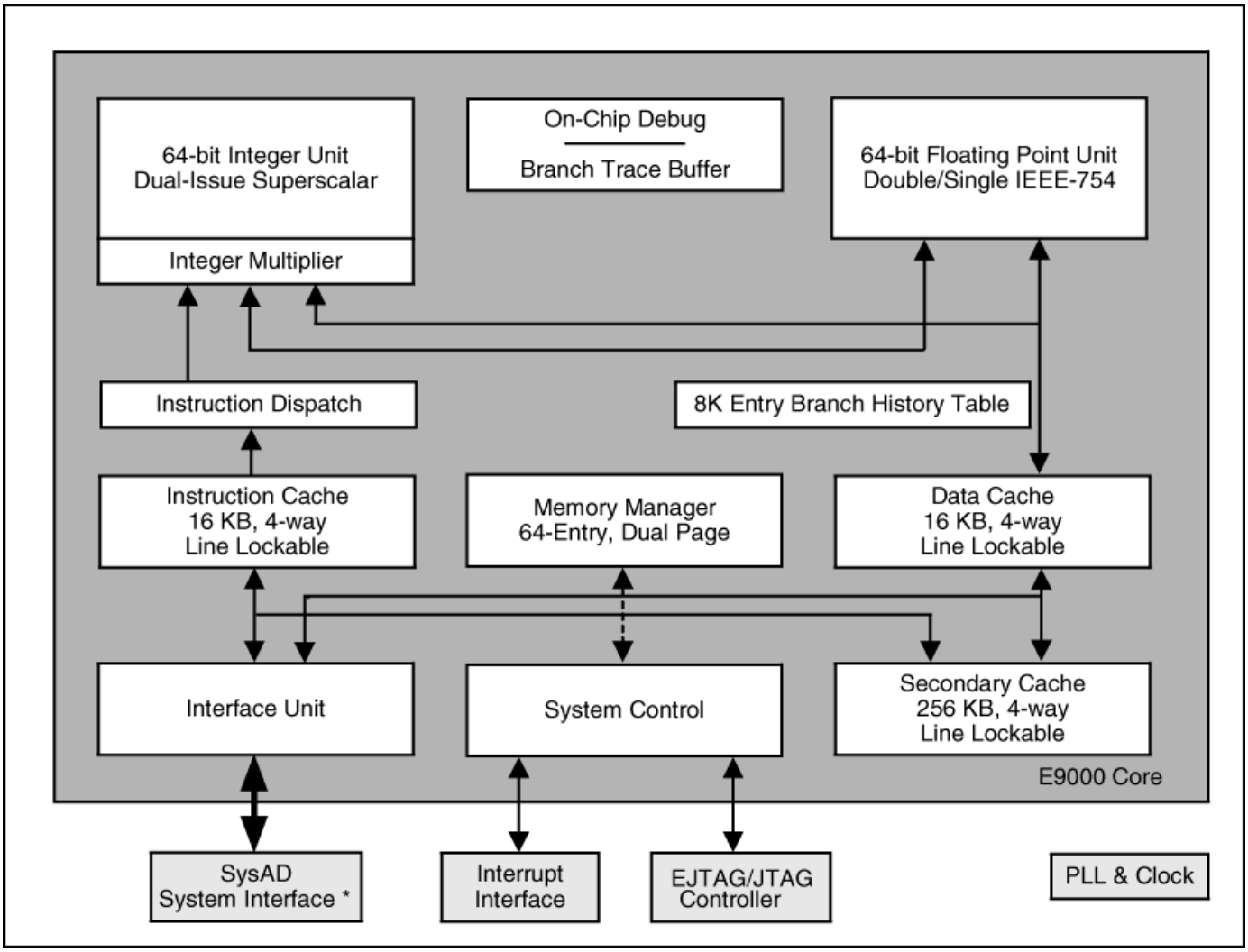
Preliminary

November 16, 2005

FEATURES

- Upscreened PMC-Sierra RM7965
- Military and Industrial Grades Available
- CPU core with MIPS64™ compatible Instruction Set Architecture that features:
  - 668 & 750 MHz
  - Dual-issue superscalar 7-stage pipeline
  - 16-KB, 4-way set associative L1 Instruction cache
  - 16-KB, 4-way set associative L1 Data cache
  - 256-KB, 4-way set associative L2 cache with industry best 5-cycle access latency
  - Error Checking and Correcting (ECC) on L2 cache
  - Fast Packet Cache™ to assist processing of packet data
  - 8K-entry branch prediction table
  - Fully associative 64-entry TLB with dual pages
  - High performance Floating Point unit (IEEE 754)
  - Fixed-point DSP instructions such as Multiply/Add, Multiply/Subtract and 3 Operand Multiply
- High-performance system interface:
  - Multiple outstanding reads with out of order return
  - 1600 MB/s peak throughput
  - Multiplexed address/data bus (SysAD) supports 2.5V and 3.3V I/logic
  - Processor clock multipliers 2, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 8.5, 9, 10, 11, 12, 13, 14, 15, 16, 17
- Integrated on-chip EJTAG controller
- 64-entry dynamic Trace Buffer for use in real-time trace and debug
- Two 32-bit virtually addressed Watch registers
- Integrated performance counters:
  - Contains 2 independent 32-bit counters
  - Counts over 30 processor events including mispredicted branches
  - Enables full characterization and analysis of application software
- MIP7965 is available in a 256-TBGA package (27x27 mm), or a *216-ExposedPad™ (24x24 mm) package:
  - MIP7965 (256-TBGA) is pin compatible with RM7065C and RM7065A TBGA products.
  - MIP7965 (*216-ExposedPad™) is pin compatible with the RM7065C and RM5261A ExposedPad™ products
  - MIP7965 (208-lead CQFP, cavity-up package (F17)) is pin compatible with the ACT7000ASC
  - MIP7965 (208-lead CQFP, inverted footprint (F24)), is pin compatible and with the same pin rotation as the commercial PMC-Sierra RM5261A

*NOTE: *216-ExposedPad package, MIPS64 and Fast Packet Cache are Trademarks of PMC-Sierra*
Contact factory for availability



BLOCK DIAGRAM

INTRODUCTION

The MIP7965 comprise a new family of high-performance 64-bit microprocessors. This product is optimized for performance with features including a seven-stage dual-issue pipeline, tightly coupled L1 and L2 caches, and sophisticated branch prediction for maintaining pipeline efficiency.

A 200 MHz 64-bit multiplexed system address and data bus (SysAD) enables a high-bandwidth I/O interface to a variety of system controllers providing connectivity to a wide range of networking peripherals. All products also contain vectored and prioritized interrupt controllers for versatile interrupt configurations.

On-chip EJTAG debug modules ensure smooth and easy debugging for both hardware and software by allowing single-step and state examination. The inclusion of a pipeline-rate branch instruction trace buffer facilitates debugging under operating conditions.

For access of up to 64 MB of L3 external SRAM cache, the MIP7965 microprocessor also features an integrated L3 cache controller and a user selectable EZ cache protocol, which eliminates the need for external Tag RAMs.

The MIP7965 is available in either a 256-TBGA package or a *216-ExposedPad™ package. The 256-TBGA package is pin compatible with previous RM7065x devices, and the *216-ExposedPad package is pin compatible with the RM7065C and the RM5261A ExposedPad products. Both RM7965 products offer a cost advantage by eliminating the L3 cache controller functionality available with the RM7900.

**Contact factory for availability*

For additional Detail Information regarding the operation of the PMC-Sierra see the latest PMC-Sierra datasheet for the RM79xx Family Microprocessors Data Sheet, Issue No. 4: March, 2004

PIN DESCRIPTIONS

The following is a list of control, data, clock, interrupt, and miscellaneous pins of MIP7965.

System Interface

PIN NAME	TYPE	DESCRIPTION
ExtRqst*	Input	External request Signals that the external agent is submitting an external request.
Release*	Output	Release interface Signals that the processor is releasing the system interface to slave state
RdRdy*	Input	Read Ready Signals that an external agent can now accept a processor read.
WrRdy*	Input	Write Ready Signals that an external agent can now accept a processor write request.
ValidIn*	Input	Valid Input Signals that an external agent is now driving a valid address or data on the bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
PRqst*	Output	Processor Request When asserted this signal requests that control of the system interface be returned to the processor.
PAck*	Input	Processor Acknowledge When asserted, in response to PRqst*, this signal indicates to the processor that it has been granted control of the system interface.
RspSwap*	Input	Response Swap RspSwap* is used by the external agent to signal the processor when it is about to return a memory reference out of order; i.e., of two outstanding memory references, the data for the second reference is being returned ahead of the data for the first reference. In order that the processor will have time to switch the address to the tertiary cache, this signal must be asserted a minimum of two cycles prior to the data itself being presented. Note that this signal works as a toggle; i.e., for each cycle that it is held asserted the order of return is reversed. By default, anytime the processor issues a second read it is assumed that the reads will be returned in order; i.e., no action is required if the reads are indeed returned in order.
RdType	Output	Read Type During the address cycle of a read request, RdType indicates whether the read request is an instruction read or a data read.
SysAD[63:0]	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC[7:0]	Input/Output	System address/data check bus An 8-bit bus containing parity check bits for the SysAD bus during data cycles.
SysCmd[8:0]	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	System Command/Data Identifier Bus Parity For the RM79xx, unused on input and zero on output.

Clock/Control Interface

PIN NAME	TYPE	DESCRIPTION
SysClock	Input	System clock Master clock input used as the system interface reference clock. All output timings are relative to this input clock. Pipeline operation frequency is derived by multiplying this clock up by the factor selected during boot initialization.

Power Supply

PIN NAME	TYPE	DESCRIPTION
VccInt	Input	Power supply for core.
VccIO	Input	Power supply for I/O.
VccP	Input	Vcc for PLL Quiet VccInt for the internal phase locked loop. Must be connected to VccInt through a filter circuit.
VccJ	Input	Power supply used for JTAG.
Vss	Input	Ground Return.
VssP	Input	Vss for PLL Quiet Vss for the internal phase locked loop. Must be connected to Vss through a filter circuit.

Interrupt Interface

PIN NAME	TYPE	DESCRIPTION
INT[9:0]*	Input	Interrupt Ten general processor interrupts, bit-wise ORed with bits 9:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 15 of the interrupt register..

JTAG Interface

PIN NAME	TYPE	DESCRIPTION
JTDI/DBDI	Input	JTAG/EJTAG data in JTAG/EJTAG serial data in.
JTCK/DBCK	Input	JTAG/EJTAG clock input JTAG/EJTAG serial clock input.
JTDO/DBDO	Output	JTAG/EJTAG data out JTAG/EJTAG serial data out.
JTMS/DBMS	Input	JTAG/EJTAG command JTAG/EJTAG command signal, signals that the incoming serial data is command data.
JTRST*/DBRST*	Input	JTAG/EJTAG reset.
JTAGSEL	Input	JTAG/EJTAG select Selects JTAG when JTAGSEL=1 ; selects EJTAG when JTAGSEL=0

Initialization Interface

PIN NAME	TYPE	DESCRIPTION
BigEndian	Input	Big Endian / Little Endian Control Allows the system to change the processor addressing
VccOK	Input	Vcc is OK When asserted, this signal indicates to the MIP7965 that the VccInt power supply has been above the recommended value for more than 100 milliseconds and will remain stable. The assertion of VccOK initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	Cold Reset This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with SysClock.
Reset*	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with SysClock.
ModeClock	Output	Boot Mode Clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
Modein	Input	Boot Mode Data In Serial boot-mode data input.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	RANGE	UNITS
V_{TERM}	Terminal Voltage with respect to Vss	-0.5[2] to 3.9	V
Tc	Operating Temperature I = Industrial R = Extended T = Military M = Military, Screened	 -40 to +85 -55 to +110 -55 to +125 -55 to +125	 °C °C °C °C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{IN}	DC Input Current	±20	mA
I_{OUT}	DC Output Current [4]	±20	mA

Notes:

1. Stresses above those listed under "*AbsoluteMaximums Rating*" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VIN minimum = -2.0V for pulse width less than 15nS. VIN maximum should not exceed +3.95 Volts.
3. When VIN < 0V or VIN > VccIO.
4. No more than one output should be shorted at one time. Duration of the short should not exceed more than 30 second.

RECOMMENDED OPERATING CONDITIONS

GRADE	CPU SPEED	TEMP (CASE)	Vss	VccInt	VccIO	VccP	VccJ
Industrial	750 MHz	-40°C to+85°C	0 V	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV
	668 MHz			1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV
Extended	750 MHz	-55°C to +110°C	0 V	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV
	668 MHz			1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV
Military	750 MHz	-55°C to +125°C Note 5	0 V	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV
	668 MHz			1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV

Notes

1. VccIO should not exceed VccInt by greater than 2.5 V during the power-up sequence.
2. Applying a logic high state to any I/O pin before VccInt becomes stable is not recommended.
3. As specified in IEEE 1149.1 (JTAG), the JTMS pin must be held high during reset to avoid entering JTAG test mode. Refer to the RM79xx User Manual.
4. VccP must be connected to VccInt through a passive filter circuit. See RM79xx User Manual fo rrecommended circuit.
5. Contact factory for military temperature range products (CQFP hermetic MCM packages will be screened at -55°C to + 125°C).

DC ELECTRICAL CHARACTERISTICS

VccIO = 3.15 - 3.45V

PARAMETER	MINIMUM	MAXIMUM	CONDITIONS
V_{OL}	-	0.2V	$\|I_{OUT}\|$ = 100µA
V_{OH}	VccIO - 0.2V	-	
V_{OL}	-	0.4V	$\|I_{OUT}\|$ = 2mA
V_{OH}	2.4V	-	
V_{IL}	-0.3V	0.8V	
V_{IH}	2.0V	VccIO + 0.3V	
I_{IN}	- -	±15µA ±15µA	V_{IN} = 0 V_{IN} = VccIO

VccIO = 2.3V – 2.7V

PARAMETER	MINIMUM	MAXIMUM	CONDITIONS
V_{OL}	-	0.2V	$\|I_{OUT}\|$ = 100µA
V_{OH}	2.1V	-	
V_{OL}	-	0.4V	$\|I_{OUT}\|$ = 1mA
V_{OH}	2.0V	-	
V_{OL}	-	0.7V	$\|I_{OUT}\|$ = 2mA
V_{OH}	1.7V	-	
V_{IL}	-0.3V	0.7V	
V_{IH}	1.7V	VccIO + 0.3V	
I_{IN}	- -	±15µA ±15µA	V_{IN} = 0 V_{IN} = VccIO

POWER CONSUMPTION

PARAMETER		CONDITIONS	CPU SPEED			
			750MHz (IND)	668MHz (IND)	750MHz (MIL)	668MHz (MIL)
			MAX	MAX	MAX	MAX
V_{CCINT} Power (mWatts)	Standby		3000	3000	3000	3000
	Active	Maximum with no FPU operation [2]	5000	4500	5000	4500
		Maximum worst case instruction mix	5000	4500	5000	4500

Notes:
1. Worst case supply voltage (maximum VccInt) with worst case temperature (maximum T_{CASE}).
2. Dhrystone 2.1 instruction mix.
3. I/O supply power is application dependant, but typically <20% of VccInt.

AC CHARACTERISTICS

CAPACITIVE LOAD DERATION

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS	Mode
C_{LD}	Load Derate	-	2	ns/25pF	LVTTL

CLOCK PARAMETERS

PARAMETER	SYMBOL	TEST CONDITIONS	BUS SPEED		UNITS
			LVTTL		
			MIN	MAX	
SysClock High	t_{SCHigh}	Transition ≤ 2ns	3	-	ns
SysClock Low	t_{SCLow}	Transition ≤ 2ns	3	-	ns
SysClock Frequency[1]			33.3	133	MHz
SysClock Period	t_{SCP}		7.5	30	ns
Clock Jitter for SysClock	$t_{JitterIn}$		-	±150	ps
SysClock Rise Time	t_{SCRise}		-	2	ns
SysClock Fall Time	t_{SCFall}		-	2	ns
ModeClock Period	$t_{ModeCKP}$		-	256	ns
JTAG Clock Period	$t_{JTAGCKP}$		4	-	ns

Notes:
1. Operation of the MIP7965 is only guaranteed with the Phase Loop enabled.

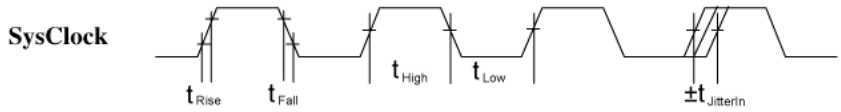
SYSTEM INTERFACE PARAMETERS

PARAMETER[1]	SYM	TEST CONDITIONS	BUS SPEED		UNITS
			LVTTL I/O		
			MIN	MAX	
Data Output[2,3,7]	t_{DO}	LVTTL (VccIO = 3.3V): mode[15:14] = 10 (fastest)[5,6,7]	0.75	4.5	ns
		LVTTL (VccIO = 3.3V): mode[15:14] = 01 (slowest)[5,6,7]	0.75	5.5	ns
Data Setup[4]	t_{DS}[6]	t_{RISE} = See above table	2.5	-	ns
Data Hold[4]	t_{DH}	t_{FALL}= See above table	1.0	-	ns

Notes
1. In LVTTL mode, timings are measured from 0.425 x VccIO of clock to 0.425 x VccIO of signal for 3.3V I/O, and from 0.48 x VccIO of clock to 0.48 x VccIO of signal for 2.5V I/O.
2. Capacitive load for all LVTTL maximum output timings is 50 pF. Minimum output timings are for theoretical no load conditions.
4. Data Output timing applies to all signal pins whether tristate I/O or output only.
5. Setup and Hold parameters apply to all signal pins whether tristate I/O or input only.
6. Only mode [15:14] = 10 is tested and guaranteed.
7. Data shown is for 3.3V I/O. For 2.5V I/O derate t_{DO} Max by 0.5 nS, and t_{DO} Min by 0.25 ns.

TIMING DIAGRAMS

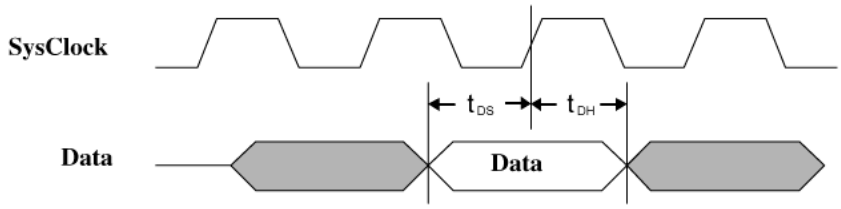
CLOCK TIMING



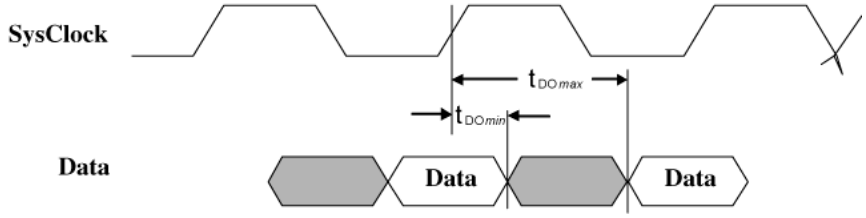
SYSTEM INTERFACE TIMING

(SysAD, SysCmd, ValidIn*, ValidOut*, etc.)

INPUT TIMING



OUTPUT TIMING

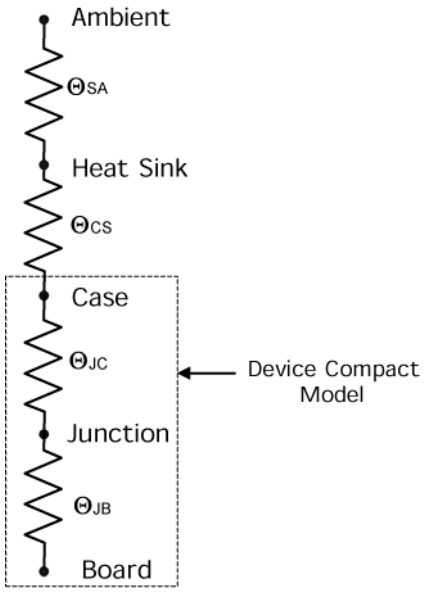


THERMAL INFORMATION

This product is designed to operate over a wide temperature range when used with a heat sink.

Maximum long-term operating junction temperature to ensure adequate long-term life	TBD at 750 MHz
	TBD at 668 MHz
Maximum junction temperature for short-term excursions with guaranteed continued functional performance	TBD at 750 MHz
	TBD at 668 MHz
Minimum ambient temperature	TBD

Device Compact Model [2]	
256-TBGA	
θ_{JC} (°C/W)	0.43
θ_{JB} (°C/W)	2.92
θ_{JA} (°C/W)	15.85
216-ExposedPad	
θ_{JC} (°C/W)	0.28
θ_{JB} (°C/W)	2.10
θ_{JA} (°C/W)	9.50
208-Lead CQFP F17 & F24	
θ_{JC} (°C/W)	TBA
θ_{JB} (°C/W)	TBA
θ_{JA} (°C/W)	TBA

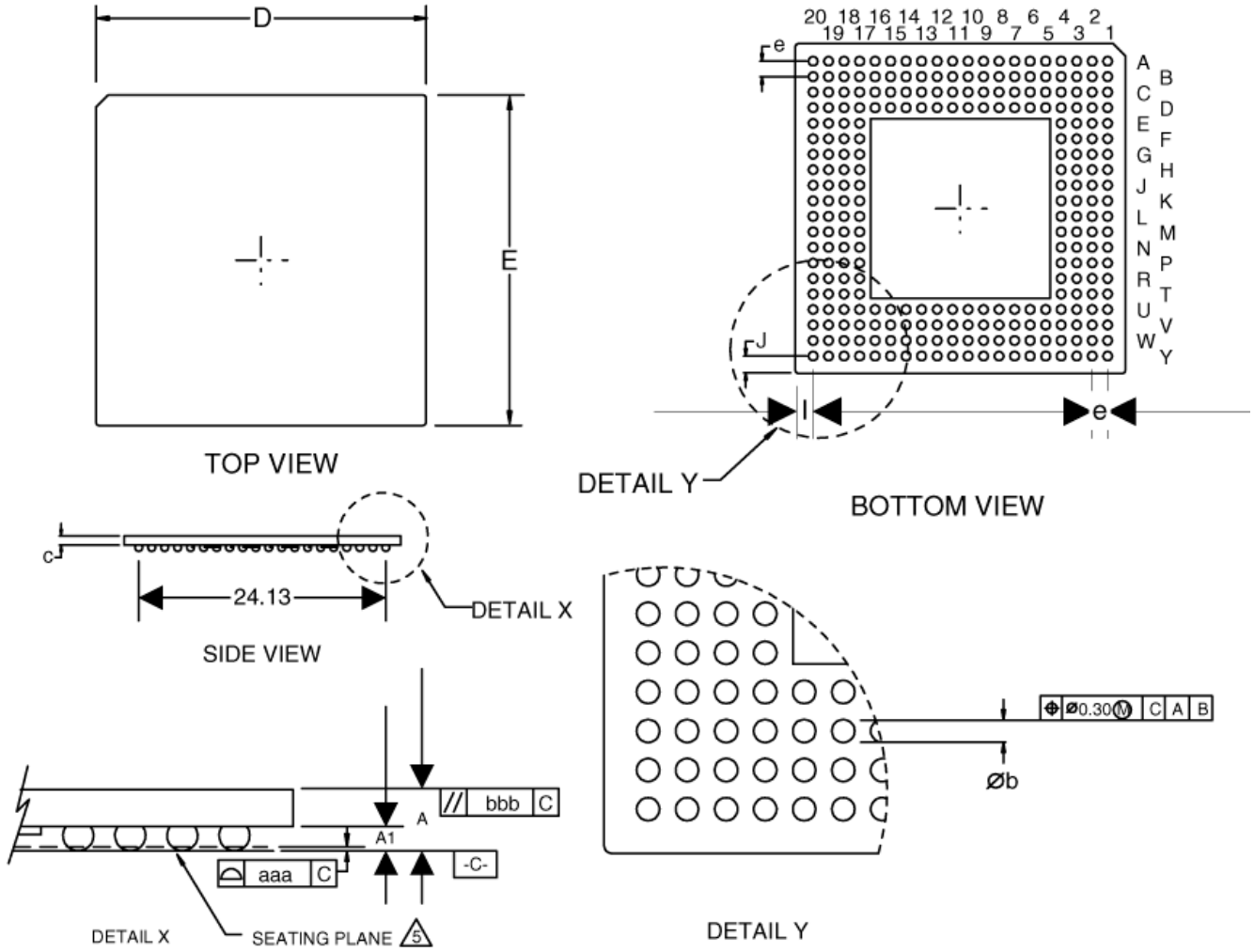


Operating power is dissipated in any package (watts) offered at worst case power supply		
Power at 750 MHz	VccInt = 1.3 V, VccIO = 3.3 V	5.0W
Power at 668 MHz	VccInt = 1.3 V, VccIO = 3.3 V	4.5W

Notes

1. Short-term is understood as the definition stated in Telcordia Generic Requirements GR-63-Core.
2. θ_{JC}, the junction-to-case thermal resistance, θ_{JB}, the junction-to-board thermal resistance are obtained from Package vendor.
3. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material.

MIP7965 256-TBGA PACKAGE OUTLINE



Symbol	Min	Nom	Max
A8	—	—	1.70
A1	0.50	0.60	0.70
D		27.00	
E		27.00	
I	1.435 REF.		
J	1.435 REF.		
M	20 <PERIMETER>		
aaa			0.20
bbb			0.25
b	0.60	0.75	0.90
c	0.80	0.90	1.00
e	1.27 TYP.		

Notes

1. Package Dimensions conform to JEDEC Registration MO-149(BG-2X).
2. “e" represents the basic solder ball grid pitch.
3. "M" represents the maximum solder ball matrix size.
4. "Dimension "b" is measured at the maximum solder ball diameter parallel to the primary datum "c".
5. The Primary datum "c" and the seating plane are defined by the spherical crowns of the solder balls.
6. All dimensions are in millimeters.
7. Dimensioning and tolerancing per ASME Y14.5M-1994.
8. After surface mount assembly, solder ball will have 0.15 mm (TYP) collapse in "A" dimension.
9. Substrate base material is copper.
10. Package top surface color shall be black.
11. Cavity depth maximum is 0.50 mm.

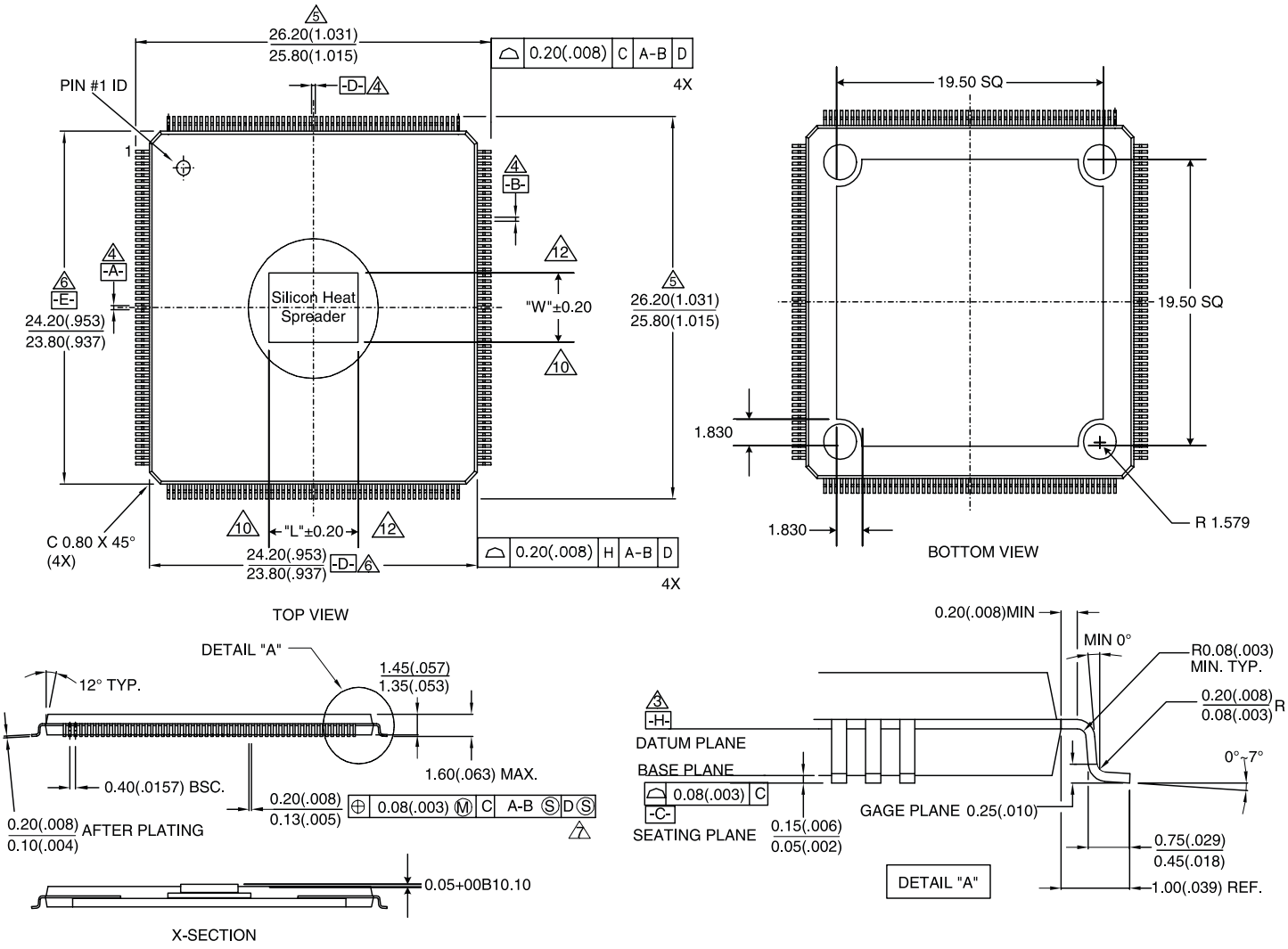
MIP7965 256-TBGA ALPHANUMERICAL PINOUT

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A1	VccIO	B19	VccIO	D17	VccIO	J3	VccInt
A2	Vss	B20	Vss	D18	Do Not Connect	J4	VccIO
A3	Vss	C1	Vss	D19	Vss	J17	VccIO
A4	Do Not Connect	C2	Vss	D20	Do Not Connect	J18	SysAD54
A5	SysAD35	C3	VccIO	E1	SysAD5	J19	SysAD22
A6	Vss	C4	Do Not Connect	E2	Do Not Connect	J20	Vss
A7	SysAD33	C5	Do Not Connect	E3	VccInt	K1	SysAD41
A8	SysAD32	C6	Do Not Connect	E4	VccIO	K2	SysAD10
A9	Vss	C7	SysAD34	E17	VccIO	K3	SysAD42
A10	SysADC1	C8	VccInt	E18	Do Not Connect	K4	SysAD11
A11	Do Not Connect	C9	SysAD0	E19	Do Not Connect	K17	SysAD53
A12	Vss	C10	SysADC4	E20	SysAD59	K18	SysAD21
A13	SysADC2	C11	SysADC7	F1	Vss	K19	SysAD52
A14	SysAD62	C12	VccInt	F2	SysAD36	K20	SysAD20
A15	Vss	C13	SysAD31	F3	SysAD4	L1	SysAD43
A16	SysAD60	C14	SysAD61	F4	VccInt	L2	SysAD44
A17	Do Not Connect	C15	VccInt	F17	VccInt	L3	SysAD12
A18	Vss	C16	Do Not Connect	F18	SysAD27	L4	VccInt
A19	Vss	C17	Do Not Connect	F19	SysAD58	L17	VccInt
A20	VccIO	C18	VccIO	F20	Vss	L18	SysAD51
B1	Vss	C19	Vss	G1	SysAD38	L19	SysAD19
B2	VccIO	C20	Vss	G2	SysAD6	L20	SysAD50
B3	Vss	D1	Do Not Connect	G3	SysAD37	M1	Vss
B4	Vss	D2	Vss	G4	VccInt	M2	SysAD13
B5	Do Not Connect	D3	Do Not Connect	G17	VccInt	M3	SysAD45
B6	SysAD3	D4	VccIO	G18	SysAD26	M4	VccIO
B7	SysAD2	D5	VccIO	G19	SysAD57	M17	VccIO
B8	SysAD1	D6	Do Not Connect	G20	SysAD25	M18	SysAD18
B9	SysADC5	D7	VccInt	H1	SysAD7	M19	SysAD49
B10	SysADC0	D8	VccInt	H2	SysAD39	M20	Vss
B11	SysADC3	D9	VccIO	H3	SysAD40	N1	SysAD14
B12	SysADC6	D10	VccInt	H4	SysAD8	N2	SysAD46
B13	Do Not Connect	D11	VccInt	H17	SysAD24	N3	VccInt
B14	SysAD30	D12	VccIO	H18	SysAD56	N4	SysAD47
B15	SysAD29	D13	SysAD63	H19	SysAD55	N17	VccInt
B16	Do Not Connect	D14	VccInt	H20	SysAD23	N18	SysAD48
B17	Vss	D15	SysAD28	J1	Vss	N19	SysAD16
B18	Vss	D16	VccIO	J2	SysAD9	N20	SysAD17

MIP7965 256-TBGA ALPHANUMERICAL PINOUT CON'T

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
P1	SysAD15	U15	INT3*	W13	SysCmd5
P2	RspSwap*	U16	VccIO	W14	SysCmdP
P3	PAck*	U17	VccIO	W15	VccInt
P4	VccInt	U18	INT6*	W16	INT1*
P17	ColdReset*	U19	Vss	W17	Vss
P18	VccOK	U20	INT7*	W18	Vss
P19	BigEndian	V1	Vss	W19	VccIO
P20	Reset*	V2	Vss	W20	Vss
R1	Vss	V3	VccIO	Y1	VccIO
R2	Do Not Connect	V4	RDType	Y2	Vss
R3	JTDI	V5	RdRdy*	Y3	Vss
R4	JTCK	V6	VccP	Y4	ModeIn
R17	VccInt	V7	Do Not Connect	Y5	ValidOut*
R18	ExtRqst*	V8	VccInt	Y6	Vss
R19	NMI*	V9	Do Not Connect	Y7	VccP
R20	Vss	V10	Do Not Connect	Y8	Do Not Connect
T1	PRqst*	V11	VccInt	Y9	Vss
T2	JTDO	V12	SysCmd3	Y10	Do Not Connect
T3	VccIO	V13	SysCmd6	Y11	SysCmd0
T4	JTRST*	V14	VccInt	Y12	Vss
T17	VccIO	V15	INT2*	Y13	SysCmd4
T18	VccInt	V16	INT5*	Y14	SysCmd8
T19	INT9*	V17	INT4*	Y15	Vss
T20	INT8*	V18	VccIO	Y16	VccJ
U1	ModeClock	V19	Vss	Y17	INT0*
U2	Vss	V20	Vss	Y18	Vss
U3	JTMS	W1	Vss	Y19	Vss
U4	VccIO	W2	VccIO	Y20	VccIO
U5	JTAGSEL	W3	VSS		
U6	ValidIn*	W4	Vss		
U7	VssP	W5	WrRdy*		
U8	VccInt	W6	Release*		
U9	VccIO	W7	SysClock		
U10	VccInt	W8	VccInt		
U11	VccInt	W9	Do Not Connect		
U12	VccIO	W10	Do Not Connect		
U13	SysCmd7	W11	SysCmd1		
U14	VccInt	W12	SysCmd2		

MIP7965 216-ExposedPad PACKAGE OUTLINE



Notes

1. Controlling dimensions: millimeters. Inches are shown in parentheses. [] is reference.
2. Dimensions and tolderancing per ASME Y 14.5M01994.
3. Datum plane “H” is located at mold parting line and is coincident where the lead exits the plastic body at the bottom of the parting line.
4. Datums “A-B” and “D” to be determined at datum plane “H”.
5. To be determined at the seating plane “C”.
6. These dimensions to be determined at datum plane “H”. These dimensions to do not include mold protrusion. Allowable protrusion is 0.25 mm (.010”) per side.
7. Lead width does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm/0.003” total in excess of these dimensions at maximum material condition.
8. Top heat spreader is silicon.
9. Bottom heat spreader is copper, CDA-110.
10. Dimension is silicon heat slug. Die type RM7965: W=4.72, L=6.52.
11. Leads plating: 85/15 Sn/Pb Alloy (standard), 99/1 Sn/Bi Alloy (lead-free).
12. Bottom slug plating: 85/15 Sn/Pb Alloy (standard), 99/1 Sn/Bi Alloy (lead-free).

MIP7965 216-ExposedPad NUMERICAL PINOUT vs FUNCTION [1,2]

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	VccIO	39	SysAD48	77	VccIO	115	JTDO
2	Do Not Connect	40	SysAD16	78	SysCmd5	116	VccIO
3	Do Not Connect	41	VccInt	79	SysCmd4	117	ModeClock
4	Do Not Connect	42	BigEndian	80	SysCmd3	118	VccInt
5	Do Not Connect	43	VccIO	81	SysCmd2	119	PRQST*
6	VccInt	44	VccOK	82	VccInt	120	PACK*
7	SysAD59	45	ColdReset*	83	SysCmd1	121	RspSwap*
8	SysAD27	46	Reset*	84	SysCmd0	122	VccIO
9	SysAD58	47	ExtRqst*	85	Do Not Connect	123	VccInt
10	VccInt	48	NMI*	86	Do Not Connect	124	SysAD47
11	VccIO	49	VccInt	87	Do Not Connect	125	SysAD15
12	SysAD26	50	INT9*	88	VccInt	126	VccInt
13	VccInt	51	INT8*	89	Do Not Connect	127	SysAD46
14	SysAD57	52	INT7*	90	Do Not Connect	128	SysAD14
15	SysAD25	53	VccJ	91	VccInt	129	SysAD45
16	SysAD56	54	VccIO	92	Do Not Connect	130	SysAD13
17	SysAD24	55	VccJ	93	Do Not Connect	131	SysAD44
18	SysAD55	56	VccIO	94	Do Not Connect	132	SysAD12
19	SysAD23	57	INT5*	95	VccInt	133	VccInt
20	VccInt	58	INT4*	96	Do Not Connect	134	SysAD43
21	SysAD54	59	INT3*	97	SysClock	135	SysAD11
22	SysAD22	60	INT2*	98	VssP	136	VccIO
23	SysAD53	61	INT1*	99	VccP	137	VccIO
24	SysAD21	62	INT0*	100	Release*	138	SysAD42
25	VccIO	63	VccInt	101	ValidOut*	139	SysAD10
26	VccIO	64	VccInt	102	ValidIn*	140	SysAD41
27	VccIO	65	Do Not Connect	103	WrRdy*	141	SysAD9
28	SysAD52	66	Do Not Connect	104	RdRdy*	142	VccInt
29	SysAD20	67	Do Not Connect	105	Do Not Connect	143	SysAD40
30	VccInt	68	VccIO	106	ModeIn	144	SysAD8
31	SysAD51	69	Do Not Connect	107	RdType	145	SysAD39
32	SysAD19	70	Do Not Connect	108	JTAGSEL	146	SysAD7
33	SysAD50	71	Do Not Connect	109	VccJ	147	SysAD38
34	SysAD18	72	VccInt	110	JTRST*	148	SysAD6
35	SysAD49	73	SysCmdP	111	VccIO	149	VccInt
36	SysAD17	74	SysCmd8	112	JTMS	150	SysAD37
37	VccIO	75	SysCmd7	113	JTCK	151	SysAD5
38	VccInt	76	SysCmd6	114	JTDI	152	SysAD36

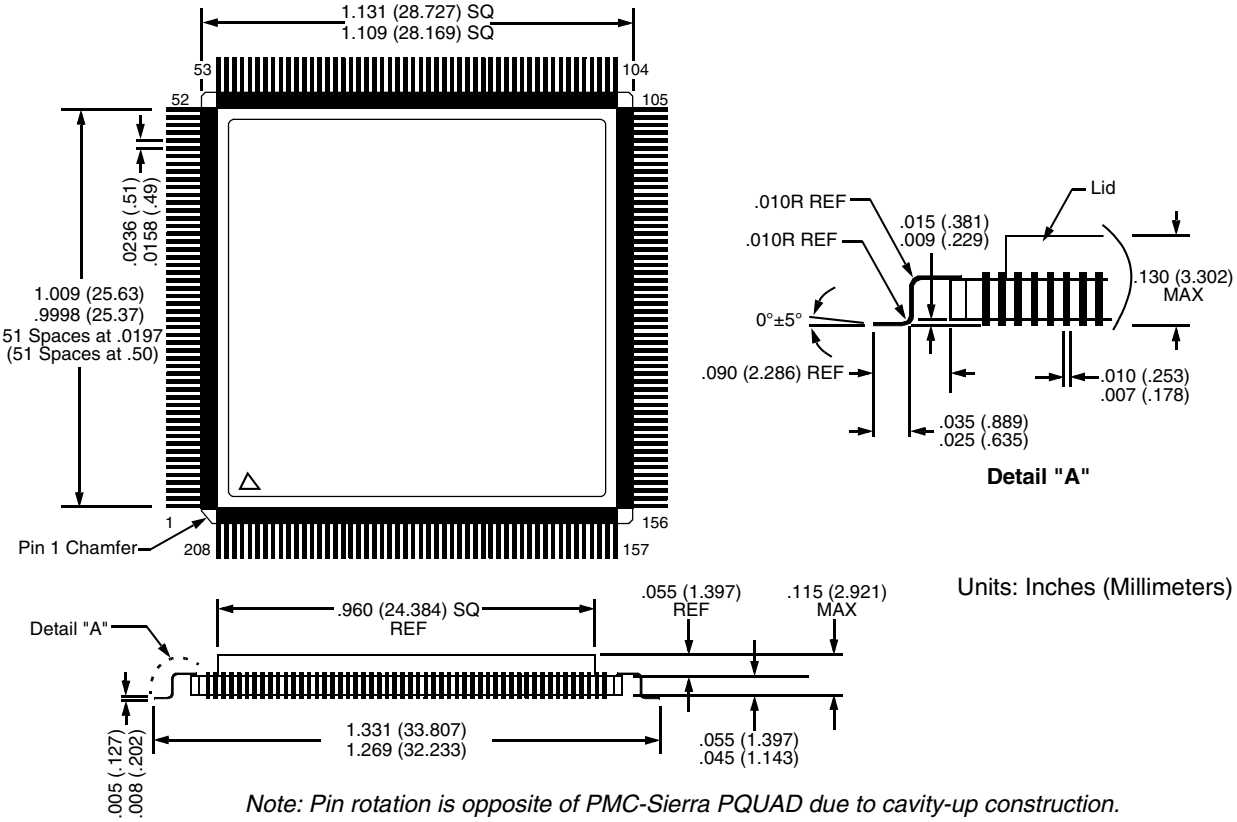
MIP7965 216-ExposedPad NUMERICAL PINOUT vs FUNCTION [1,2] CON'T

PIN	FUNCTION	PIN	FUNCTION
153	SysAD4	191	VccIO
154	VccInt	192	SysADC7
155	Do Not Connect	193	SysADC3
156	Do Not Connect	194	VccInt
157	VccInt	195	SysADC6
158	Do Not Connect	196	VccIO
159	Do Not Connect	197	SysADC2
160	Do Not Connect	198	SysAD63
161	Do Not Connect	199	SysAD31
162	VccIO	200	Do Not Connect
163	Do Not Connect	201	SysAD62
164	VccIO	202	SysAD30
165	VccIO	203	VccIO
166	Do Not Connect	204	VccIO
167	Do Not Connect	205	VccInt
168	Do Not Connect	206	SysAD61
169	Do Not Connect	207	SysAD29
170	SysAD35	208	VccInt
171	SysAD3	209	SysAD60
172	VccInt	210	SysAD28
173	SysAD34	211	Do Not Connect
174	SysAD2	212	Do Not Connect
175	VccInt	213	Do Not Connect
176	VccIO	214	Do Not Connect
177	VccInt	215	VccIO
178	SysAD33	216	VccIO
179	SysAD1		
180	SysAD32		
181	SysAD0		
182	SysADC5		
183	SysADC1		
184	VccIO		
185	VccInt		
186	SysADC4		
187	SysADC0		
188	Do Not Connect		
189	VccInt		
190	VccIO		

Notes:

1. The exposed pad on the bottom of the ExposedPad package acts as the sole device ground and as the primary heat conduction path. As such, it must be soldered to the printed circuit board.
2. See PMC-2030256, 216-ExposedPad Design Guidelines Application Note for details.

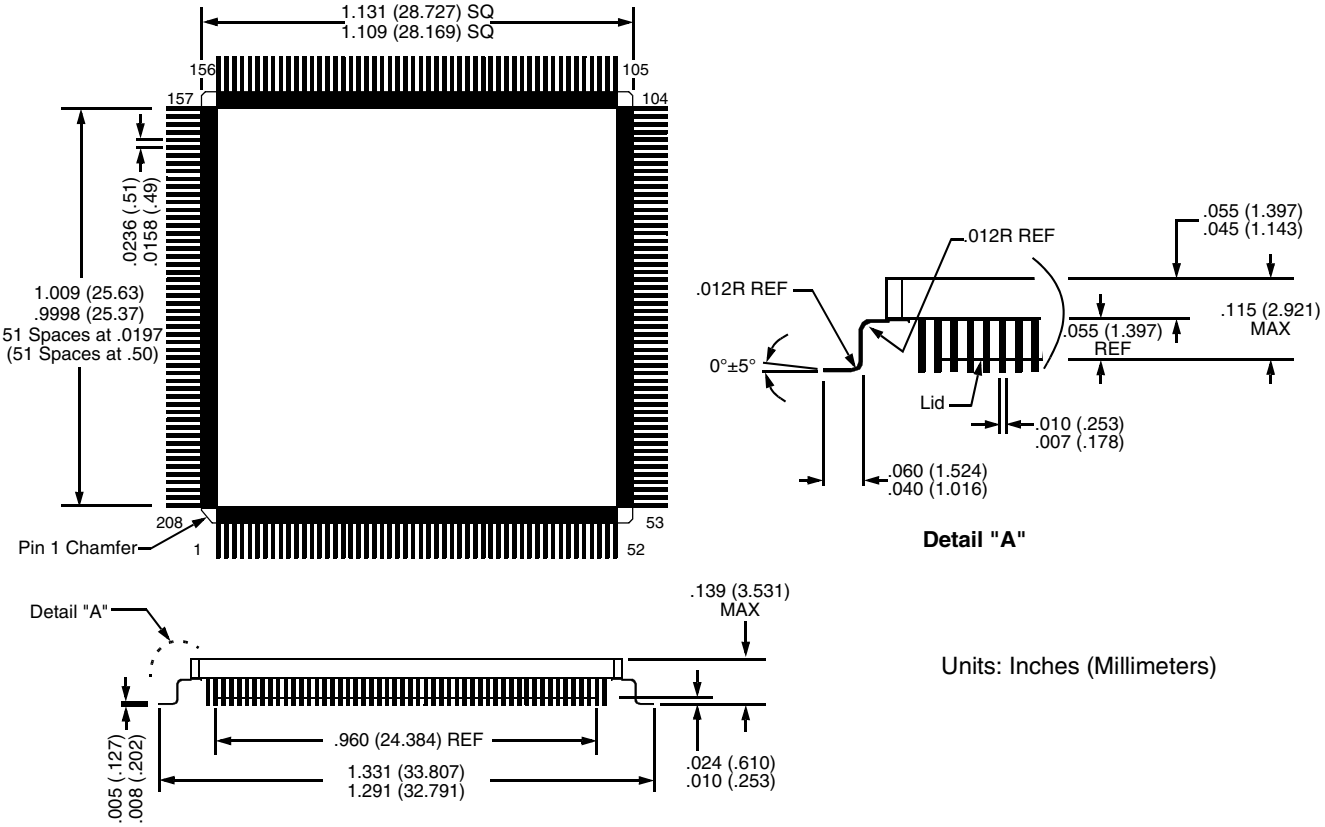
MIP7965 "F17" – CQFP 208 Leads PACKAGE OUTLINE



Units: Inches (Millimeters)

Note: Pin rotation is opposite of PMC-Sierra PQUAD due to cavity-up construction.

MIP7965 "F24" – Inverted QFP 208 Leads PACKAGE OUTLINE



Units: Inches (Millimeters)

Note: Pin rotation is Identical to PMC-Sierra PQUAD due to cavity-down construction.

MIP7965 208-Lead CQFP PINOUTS – "F17" & "F24"

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	VccIO	53	Do Not Connect	105	VccIO	157	Do Not Connect
2	Do Not Connect	54	Do Not Connect	106	NMI*	158	Do Not Connect
3	Do Not Connect	55	Do Not Connect	107	ExtRqst*	159	Do Not Connect
4	VccIO	56	VccIO	108	Reset*	160	Do Not Connect
5	Vss	57	Vss	109	ColdReset*	161	VccIO
6	SysAD4	58	ModeIn	110	VccOK	162	Vss
7	SysAD36	59	RdRdy*	111	BigEndian	163	SysAD28
8	SysAD5	60	WrRdy*	112	VccIO	164	SysAD60
9	SysAD37	61	ValidIn*	113	Vss	165	SysAD29
10	VccInt	62	ValidOut*	114	SysAD16	166	SysAD61
11	Vss	63	Release*	115	SysAD48	167	VccInt
12	SysAD6	64	VccP	116	VccInt	168	Vss
13	SysAD38	65	VssP	117	Vss	169	SysAD30
14	VccIO	66	SysClock	118	SysAD17	170	SysAD62
15	Vss	67	VccInt	119	SysAD49	171	VccIO
16	SysAD7	68	Vss	120	SysAD18	172	Vss
17	SysAD39	69	VccIO	121	SysAD50	173	SysAD31
18	SysAD8	70	Vss	122	VccIO	174	SysAD63
19	SysAD40	71	VccInt	123	Vss	175	SysADC2
20	VccInt	72	Vss	124	SysAD19	176	SysADC6
21	Vss	73	SysCmd0	125	SysAD51	177	VccInt
22	SysAD9	74	SysCmd1	126	VccInt	178	Vss
23	SysAD41	75	SysCmd2	127	Vss	179	SysADC3
24	VccIO	76	SysCmd3	128	SysAD20	180	SysADC7
25	Vss	77	VccIO	129	SysAD52	181	VccIO
26	SysAD10	78	Vss	130	SysAD21	182	Vss
27	SysAD42	79	SysCmd4	131	SysAD53	183	SysADC0
28	SysAD11	80	SysCmd5	132	VccIO	184	SysADC4
29	SysAD43	81	VccIO	133	Vss	185	VccInt
30	VccInt	82	Vss	134	SysAD22	186	Vss
31	Vss	83	SysCmd6	135	SysAD54	187	SysADC1
32	SysAD12	84	SysCmd7	136	VccInt	188	SysADC5
33	SysAD44	85	SysCmd8	137	Vss	189	SysAD0
34	VccIO	86	SysCmdP	138	SysAD23	190	SysAD32
35	Vss	87	VccInt	139	SysAD55	191	VccIO
36	SysAD13	88	Vss	140	SysAD24	192	Vss
37	SysAD45	89	VccInt	141	SysAD56	193	SysAD1
38	SysAD14	90	Vss	142	VccIO	194	SysAD33
39	SysAD46	91	VccIO	143	Vss	195	VccInt
40	VccInt	92	Vss	144	SysAD25	196	Vss
41	Vss	93	Int0*	145	SysAD57	197	SysAD2
42	SysAD15	94	Int1*	146	VccInt	198	SysAD34
43	SysAD47	95	Int2*	147	Vss	199	SysAD3
44	VccIO	96	Int3*	148	SysAD26	200	SysAD35
45	Vss	97	Int4*	149	SysAD58	201	VccIO
46	ModeClock	98	Int5*	150	SysAD27	202	Vss
47	JTDO	99	VccIO	151	SysAD59	203	Do Not Connect
48	JTDI	100	Vss	152	VccIO	204	Do Not Connect
49	JTCK	101	Do Not Connect	153	Vss	205	Do Not Connect
50	JTMS	102	Do Not Connect	154	Do Not Connect	206	Do Not Connect
51	VccIO	103	Do Not Connect	155	Do Not Connect	207	VccIO
52	Vss	104	Do Not Connect	156	Vss	208	Vss

SAMPLE ORDERING INFORMATION

PART NUMBER	SCREENING	PIPELINE FREQ (MHZ) Note 3	PACKAGE
MIP7965-750B1I	Industrial Temperature Range -40°C to +85°C Testing	750	256-TBGA
MIP7965-668MI Note 1 (AP7965-668MI - Custom Part)		668	216-ExposedPad
MIP7965-750F17I		750	208 Lead, CQFP, F17
MIP7965-668F24I		668	208 Lead, CQFP, F24
MIP7965-668B1R	Extended Temperature Range -55°C to +110°C Testing Note 2	668	256-TBGA
MIP7965-750MR Note 1		750	216-ExposedPad
(AP7965-750MT - Custom Part)	Military Temperature Range -55°C to +125°C Testing	750	216-ExposedPad
MIP7965-750F17T Note 1	Military Temperature Range, -55°C to +125°C Testing	750	208 Lead, CQFP, F17
MIP7965-668F24T Note 1		668	208 Lead, CQFP, F24
MIP7965-750F17M Note 1	Military Temperature Screened, -55°C to +125°C Testing Note 2	750	208 Lead, CQFP, F17
MIP7965-668F24M Note 1		668	208 Lead, CQFP, F24

Notes
1. Contact Factory for Availability
2. Contact factory for military temperature range products (CQFP hermetic MCM package will be screened at -55°C to + 125°C).
3. Contact factory for higher speed product options.

PART NUMBER BREAKDOWN

MIP 7965 – 750 B1 I

MIPS Series (AP Custom Series)

Base Processor Type

Maximum Pipeline Frequency

750 = 750MHz
668 = 668MHz

Screening

I = Industrial Temp, -40°C to +85°C
R = Extended Temp, -55°C to +110°C
T = Military Temp, -55°C to +125°C, Note 2
M = Military Temp, -55°C to +125°C, Screened * Note 2

Package Type & Size

B1 = 26mm Sq, 256-TBGA
M = 26mm Sq, 216-ExposedPad™ Lead, Note 1
F17 = 1.120" Sq, 208 Lead CQFP, Note 2
F24 = 1.120" Sq, Inverted 208 Lead CQFP, Note 2

Formerly released as AP7965

* **Screened to the individual test methods of MIL-STD-883**

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