Integrated Circuit Systems, Inc.

ICS8523
LOW SKEW, 1-TO-4 LVHSTL FANOUT BUFFER

GENERAL DESCRIPTION

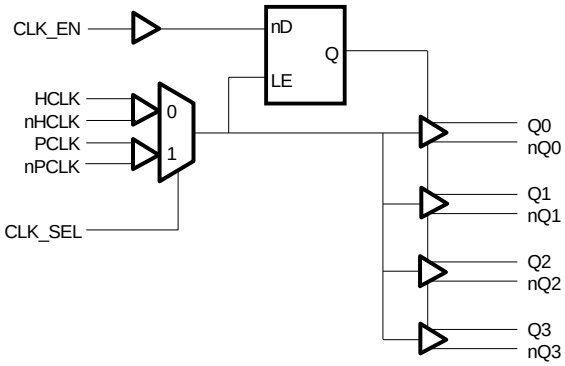
The ICS8523 is a low skew, high performance, 1-to-4 LVHSTL clock fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8523 has selectable clock inputs that accept either HSTL or PECL input levels. The clock enable is synchronous which eliminates the runt clock pulses which occur during asynchronous enabling and disabling of the outputs.

Guaranteed output and part-to-part skew characteristics make the ICS8523 ideal for those applications demanding well defined performance and repeatability.

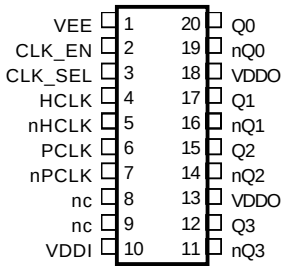
FEATURES

- 4 LVHSTL outputs each with the ability to drive 50Ω to ground
- Selectable differential HSTL or PECL clock inputs
- Voh (max) = 1.2V
- Input crossover voltage, Vx, 0.68V ≤ Vx ≤ 0.9V
- Output frequency up to 500MHz
- 30ps output skew
- 3.3V input, 1.8V output operating supply voltages
- LVCMOS / LVTTL control inputs
- 20 lead TSSOP
- 0°C to 70°C ambient operating temperature
- Industrial temperature version available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8523

20-Lead TSSOP
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	VEE	Power		Negative power supply pin. Connect to power supply ground.
2	CLK_EN	Input	Pullup	Synchronous clock enable. When HIGH clock outputs follows clock input. When LOW, Q outputs are force low, nQ outputs are force high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH selects differential HSTL inputs. When LOW selects differential PECL inputs. LVCMOS / LVTTL interface levels.
4	HCLK	Input	Pulldown	Non-inverting differential HSTL clock input.
5	nHCLK	Input	Pullup	Inverting differential HSTL clock input.
6	PCLK	Input	Pulldown	Non-inverting differential PECL clock input.
7	nPCLK	Input	Pullup	Inverting differential PECL clock input.
8, 9	nc	Unused		Unused pins.
10	VDDI	Power		Input power supply pin. Connect to 3.3V.
11, 12	nQ3, Q3	Output		Differential clock outputs. LVHSTL interface levels.
13, 18	VDDO	Power		Output power supply. Connect to 1.8V.
14, 15	nQ2, Q2	Output		Differential clock outputs. LVHSTL interface levels.
16, 17	nQ1, Q1	Output		Differential clock outputs. LVHSTL interface levels.
19, 20	nQ0, Q0	Output		Differential clock outputs. LVHSTL interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	HCLK, nHCLK					pF
		PCLK, nPCLK					pF
		CLK_EN, CLK_SEL					pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ

TABLE 3A. CONTROL INPUTS FUNCTION TABLE

Inputs		Outputs	
CLK_EN	**CLK_SEL**	**Q0 thru Q3**	**nQ0 thru nQ3**
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	Active	Active
1	1	Active	Active

In the active mode the state of the output is a function of the HCLK , nHCLK and PCLK, nPCLK inputs as described in Table 3B.

TABLE 3B. CLOCK INPUTS FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
HCLK or PCLK	**nHCLK or nPCLK**	**Q0 thru Q3**	**nQ0 thru nQ3**		
0	0	LOW	HIGH	Differential to Differential	Non Inverting
1	1	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Single ended use requires that one of the differential input be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTL levels the recommended input bias network is a 10KΩ resistor from the input pin to VDD, 10KΩ resistor from the input pin to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is VDD/2 ± 300mV.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDDI + 0.5V
Outputs	-0.5V to VDDO + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VDDI = 3.3V±5%, VDDO = 1.8V±10%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Ouptut Power Supply Voltage		1.6	1.8	2.0	V
IEE	Power Supply Current				50	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, VDDI = 3.3V±5%, VDDO = 1.8V±10%, T_A=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	CLK_EN, CLK_SEL		2		3.765	V
VIL	Input Low Voltage	CLK_EN, CLK_SEL		-0.3		0.8	V
IIH	Input High Current	CLK_EN				5	µA
		CLK_SEL				150	µA
IIL	Input Low Current	CLK_EN		-150			µA
		CLK_SEL		-5			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, VDDI = 3.3V±5%, VDDO = 1.8V±10%, T_A=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	PCLK				150	µA
		nPCLK				5	µA
IIL	Input Low Current	PCLK		-5			µA
		nPCLK		-150			µA
VPP	Peak-to-Peak Input Voltage			0.1		1.3	V
VCMR	Common Mode Input Voltage; NOTE 1			0.13		1.3	V

NOTE 1: Common mode voltage for PECL is defined as the minimum VIH. VCMR is compatible with DCM, LVDS, LVPECL and SSTL input levels.

TABLE 4D. LVHSTL DC CHARACTERISTICS, VDDI = 3.3V±5%, VDDO = 1.8V±10%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	HCLK				150	µA
		nHCLK				5	µA
IIL	Input Low Current	HCLK		-5			µA
		nHCLK		-150			µA
VPP	Peak-to-Peak Input Voltage			0.1		1.3	V
VCMR	Common Mode Input Voltage; NOTE 1, 2			0.13		1.3	V
VOH	Output High Voltage; NOTE 3			1.0		1.2	V
VOL	Output Low Voltage; NOTE 3			0		0.4	V
VOX	Output Crossover Voltage			40% x (VOH-VOL) + VOL		60% x (VOH-VOL) + VOL	V

NOTE 1: Common mode voltage for HSTL is defined as the crossover voltage. VCMR is compatible with DCM, LVDS, LVPECL and SSTL input levels.
NOTE 2: For single ended applications the maximum input voltage for HCLK and nHCLK is VDD + 0.3V.
NOTE 3: Outputs terminated with 50Ω to ground. The power dissipation of a terminated output pair is 32mW.

TABLE 5. ELECTRICAL AC CHARACTERISTICS, VCC=3.3V±5%, VCCO=1.8V±10%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				650	MHz
tpLH	Propagation Delay, Low-to-High; NOTE 2		1.0		2.0	ns
tpHL	Propagation Delay, High-to-Low; NOTE 2		1.0		2.0	ns
tsk(o)	Output Skew; NOTE 3				30	ps
tsk(pp)	Part-to-Part; NOTE 4				150	ps
tjit(Ø)	Input-to-Output Jitter; NOTE 5				0	ps
tR	Output Rise Time	30% to 70%	100		800	ps
tF	Output Fall Time	30% to 70%	100		800	ps
tPW	Output Pulse Width		tCYCLE/2 -TBD	tCYCLE/2	tCYCLE/2 +TBD	ns
tS	Clock Enable Setup Time		1.0			ns
tH	Clock Enable Hold Time		1.0			ns

NOTE 1: All parameters measured at 500Mhz unless noted otherwise.
NOTE 2: Measured from the 50% point to the differential output crossing point.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured from the 50% point of the input to the differential output crossing point.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Measured from the 50% point of like inputs to the differential output crossing point.
NOTE 5: Measured by triggering on input signal and measuring the largest displacement between output cycles.

PACKAGE OUTLINE - G SUFFIX

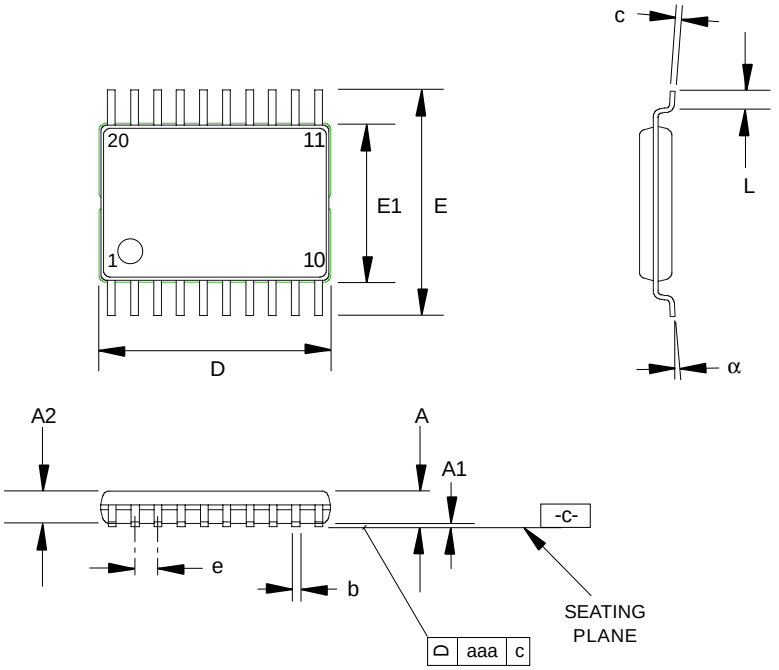


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
N	20			
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	6.40	6.60	.252	.260
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		.0256 BASIC	
L	0.45	0.75	.018	.030
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

Reference Document: JEDEC Publication 95, MO-153

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8523AG	ICS8523AG	20 lead TSSOP	75	0°C to 70°C
ICS8523AGT	ICS8523AG	20 lead TSSOP on Tape and Reel	2500	0°C to 70°C