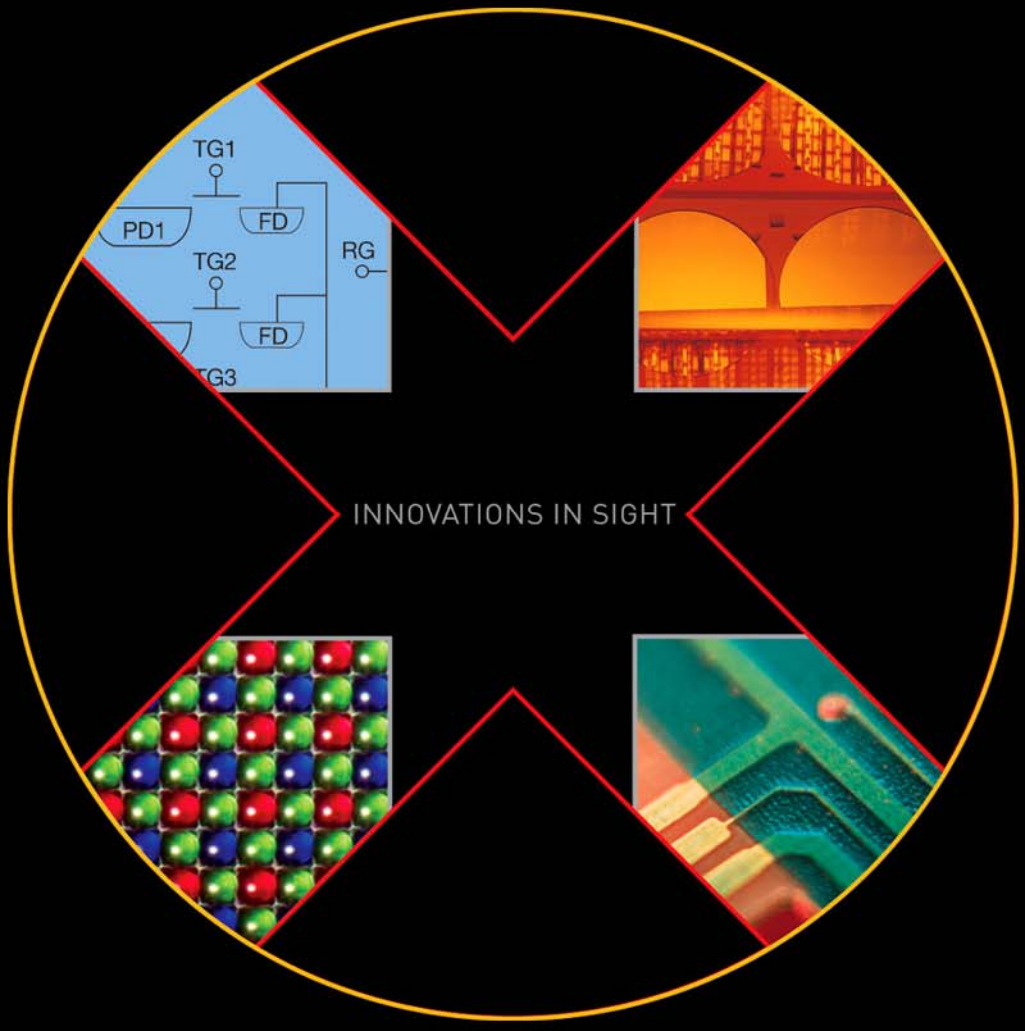
DEVICE PERFORMANCE SPECIFICATION

Revision 5.1 MTD/PS-0229

September 12, 2008



KODAK KLI-2113 IMAGE SENSOR

2098 X 3 TRI-LINEAR CCD IMAGE SENSOR

Kodak

Image Sensor Solutions

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SUMMARY SPECIFICATION

KODAK KLI-2113 IMAGE SENSOR

2098 X 3 TRI-LINEAR CCD IMAGE SENSOR

DESCRIPTION

The KODAK KLI-2113 Image Sensor is a high dynamic range, multispectral, linear CCD image sensor ideally suited for demanding color scanner applications.

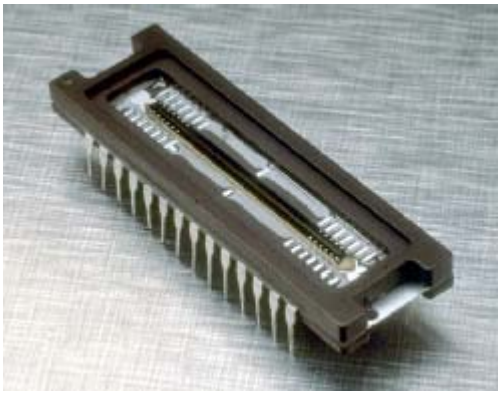
The imager consists of three parallel 2098-element photodiode arrays—one for each primary color. The KLI-2113 sensor offers high sensitivity, a high data rate, low noise and negligible lag. Independent exposure control for each channel allows color balancing at the front end. CMOS-compatible 5V clocks, and single 12V DC supply are all that are required to drive the KLI-2113 sensor, simplifying the design of interface electronics.

FEATURES

- High Resolution
- Wide Dynamic Range
- High Sensitivity
- High Operating Speed
- High Charge Transfer Efficiency
- No Image Lag
- Electronic Exposure Control
- Pixel Summing Capability
- Up to 2.0V peak-peak Output
- 5.0V Clock Inputs
- Two-Phase Register Clocking
- On-chip Dark Reference

APPLICATIONS

- Photography
- Industrial Imaging
- Scientific Imaging



Parameter	Typical Value
Architecture	3 Channel, RGB Tri-linear CCD
Pixels Count	2098 x 3
Pixel Size	14 µm (H) x 14 µm (V)
Pixel Pitch	14 µm
Inter-Array Spacing	112 mm (8 lines effective)
Imager Size	29.37 mm (H) x 0.24 mm (V)
Saturation Signal	170,000 electrons
Dynamic Range	76 dB
Responsivity (Wavelength = 460, 540, 650 nm)	25, 32, 50 V/µJ/cm^2
Output Sensitivity	11.5 µV/electron
Dark Current	0.02 pA/pixel
Dark Current Doubling Rate	9° C
Charge Transfer Efficiency	0.99999/Transfer
Photoresponse Non-uniformity	5% Peak-Peak
Lag (First Field)	0.6%
Maximum Data Rate	20 MHz/Channel
Package	CERDIP (Sidebrazed, CuW)
Cover Glass	AR coated, 2 sides

Parameters above are specified at T = 23° C (junction temperature) and 2 MHz clock rates unless otherwise noted

ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H0602	KLI- 2113-AAA-ER-AA	Monochrome, No Microlens, CERDIP Package (leadframe), Taped Clear Cover Glass with AR coating (2 sides), Standard Grade	KLI-2113-AAA (Serial Number)
4H0605	KLI- 2113-AAA-ER-AE	Monochrome, No Microlens, CERDIP Package (leadframe), Taped Clear Cover Glass with AR coating (2 sides), Engineering Sample	
4H0601	KLI- 2113-AAB-ED-AA	Monochrome, No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Standard Grade	KLI-2113-AAB (Serial Number)
4H0604	KLI- 2113-AAB-ED-AE	Monochrome, No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0600	KLI- 2113-DAA-ED-AA	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Standard Grade	KLI-2113-DAA (Serial Number)
4H0603	KLI- 2113-DAA-ED-AE	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0096	KEK-4H0096-KLI-2113-12-5	Evaluation Board (Complete Kit)	N/A

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

Please address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010

Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

DEVICE DESCRIPTION

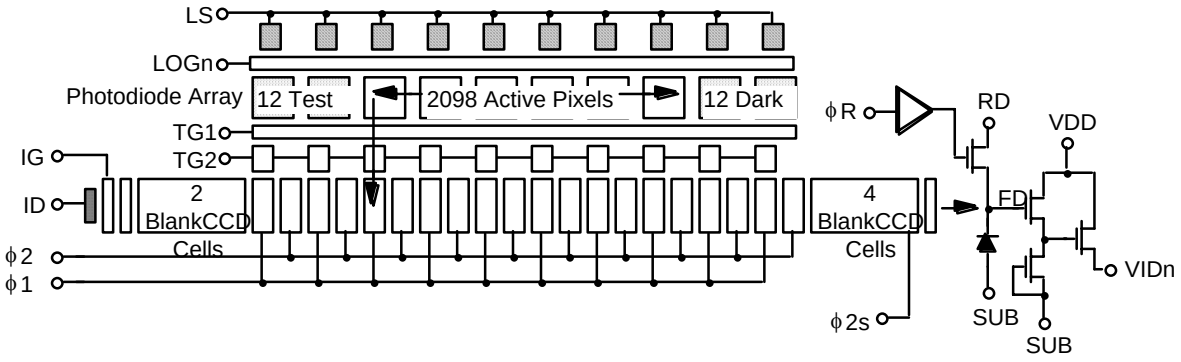


Figure 1: Single Channel Schematic

Exposure Control

Exposure control is implemented by selectively clocking the LOG gates during portions of the scanning line time. By applying a large enough positive bias to the LOG gate, the channel potential is increased to a level beyond the 'pinning level' of the photodiode. (The 'pinning' level is the maximum channel potential that the photodiode can achieve and is fixed by the doping levels of the structure.) With TG1 in an 'off' state and LOG strongly biased, all of the photocurrent will be drawn off to the LS drain. Referring to the timing diagrams, one notes that the exposure can be controlled by pulsing the LOG gate to a 'high' level while TG1 is turning 'off' and then returning the LOG gate to a 'low' bias level sometime during the line scan. The effective exposure (texp) is net time between the falling edge of the LOG gate and the falling edge of the TG1 gate (end of the line). Separate LOG connections for each channel are provided enabling on-chip light source and image spectral color balancing. As a cautionary note, the switching transients of the LOG gates during line readout may inject an artifact at the sensor output. Rising edge artifacts can be avoided by switching LOG during the photodiode-to-CCD transfer period, preferably, during the TG1 falling edge. Depending on clocking speeds, the falling edge of the LOG should be synchronous with the ϕ1/ϕ2 shift register readout clocks. For very fast applications, the falling edge of the LOG gate may be limited by on-chip RC delays across the array. In this case artifacts may extend across one or more pixels. Correlated double sampling (CDS) processing of the output waveform can remove the first order magnitude of such artifacts. In high dynamic range applications, it may be advisable to limit the LOG fall times to minimize the current transients in the device substrate and limit the magnitude of the artifact to an acceptable level.

Pixel Summing

The effective resolution of this sensor can be varied by enabling the pixel summing feature. A separate pin is provided for the last shift register gate labeled ϕ2s. This gate, when clocked appropriately, stores the summation of signal from adjacent pixels. This combined charge packet is then transferred onto the sense node. As an example, the sensor can be operated in 2-pixel summing mode (1049 pixels), by supplying a ϕ2s clock which is a 75% duty cycle signal at 1/2 the frequency of the ϕ2 signal, and modifying the ϕR clock as depicted in the timing diagram section. Applications that require full resolution mode (2098 pixels), must tie the ϕ2s pin to the ϕ2 pin. Refer to the timing diagram section for additional details.

IMAGE ACQUISITION

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode itself and is isolated from the CCD shift registers during the integration period by the transfer gates TG1 and TG2, which are held at barrier potentials. At the end of the integration period, the CCD register clocking is stopped with the ϕ1 and ϕ2 gates being held in a 'high' and 'low' state respectively. Next, the TG gates are turned 'on' causing the charge to drain from the photo-diode into the TG1 storage region. As TG1 is turned back 'off', charge is transferred through TG2 and into the ϕ1 storage region. The TG2 gate is then turned 'off', isolating the shift registers from the accumulation region once again. Complementary clocking of the ϕ1 and ϕ2 phases now resumes for readout of the current line of data while the next line of data is integrated.

CHARGE TRANSPORT

Readout of the signal charge is accomplished by two-phase, complementary clocking of the ϕ1 and ϕ2 gates. The register architecture has been designed for high speed clocking with minimal transport and output signal degradation, while still maintaining low (4.75Vp-p min) clock swings for reduced power dissipation, lower clock noise and simpler driver design. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the ϕ2 clock. Resettable floating diffusions are used for the charge to voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by $\Delta VFD = \Delta Q/CFD$. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock, ϕR.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

Pin	Name	Description
1	VIDR	Red Output Video
2	SUB	Substrate
3	RD	Reset Drain
4	ϕR	Reset Clock
5	LOGR	Red Overflow Gate
6	LOGG	Green Overflow Gate
7	SUB	Substrate
8	N/C	No Connection
9	LS	Light Shield/Exposure Drain
10	IG	Input Gate/LOG Test Pin
11	TG2	Outer Transfer Gate
12	N/C	No Connection
13	ϕ2s	Phase 2 Shift Register Summing Gate Clock
14	ϕ2	Phase 2 Shift Register Clock

Pin	Name	Description
28	VIDG	Green Output Video
27	SUB	Substrate
26	VDD	Amplifier Supply
25	VIDB	Blue Output Video
24	SUB	Substrate
23	N/C	No Connection
22	LOGB	Blue Overflow Gate
21	N/C	No Connection
20	N/C	No Connection
19	ID	Input Diode Test Pin
18	TG1	Inner Transfer Gate
17	N/C	No Connection
16	N/C	No Connection
15	ϕ1	Phase 1 Shift Register Clock

IMAGING PERFORMANCE

TYPICAL OPERATIONAL CONDITIONS

Specifications given under nominal operating conditions @ 25oC ambient, fCLK =2 MHz and nominal external VIDn load resistors unless otherwise specified.

SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Saturation Output Voltage	V_{sat}		2.0		V_{p-p}	1, 7	die[8]
Output Sensitivity	$\Delta V_o/\Delta N_e$		11.5		$\mu V/e^-$	7	design[9]
Saturation Signal Charge	$N_{e,sat}$		170k		electrons		design[9]
Responsivity (@ 650nm) (@ 540nm) (@ 460nm)	R		50 32 25		$V/\mu J/cm^2$	2, 7	design[9]
Output Buffer Bandwidth	f_{-3dB}		75		MHz	@ C_{LOAD} = 10 pF	design[9]
Dynamic Range	DR		76		dB	3	design[9]
Dark Current	I_{dark}		0.02		pA/pixel	4	die[8]
Charge Transfer Efficiency	CTE, η		.99999		-	5	design[9]
Lag	L		0.6	1	%	1st Field	design[9]
DC Output Offset	$V_{o,dc}$	6	7	9	Volts	7	design[9]
Photoresponse Uniformity	PRNU		5	10	% p-p	6	die[8]
Register Clock Capacitance	C_ϕ		500		pF	/phase	design[9]
Transfer Gate Capacitance	C_{TG}		400		pF		design[9]

Notes:

1. Defined as the maximum output level achievable before linearity or PRNU performance is degraded.
2. With color filter. Values specified at filter peaks. 50% bandwidth = ±30 nm.
3. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between $\phi 1$ and $\phi 2$ phases must be maintained to minimize clock noise.
4. Dark current doubles approximately every +9°C.
5. Measured per transfer. For total line h < $(.99999)^{4256} = 0.96$
6. Low frequency response across array with color filter array.
7. Decreasing external VIDn load resistors to improve signal bandwidth will decrease these parameters.
8. A parameter that is measured on every sensor during production testing.
9. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

(2 MHz Operation, Emitter Follower Buffered, 3/4 Vsat, Dark to Bright Transition)

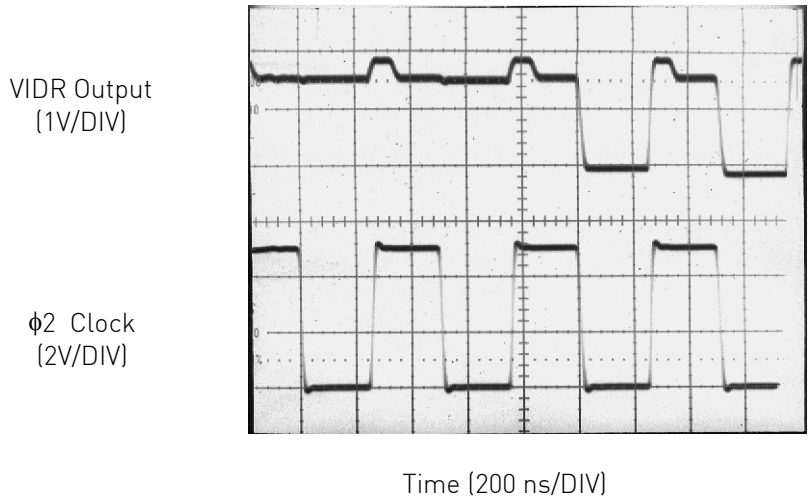


Figure 2: Output Waveforms

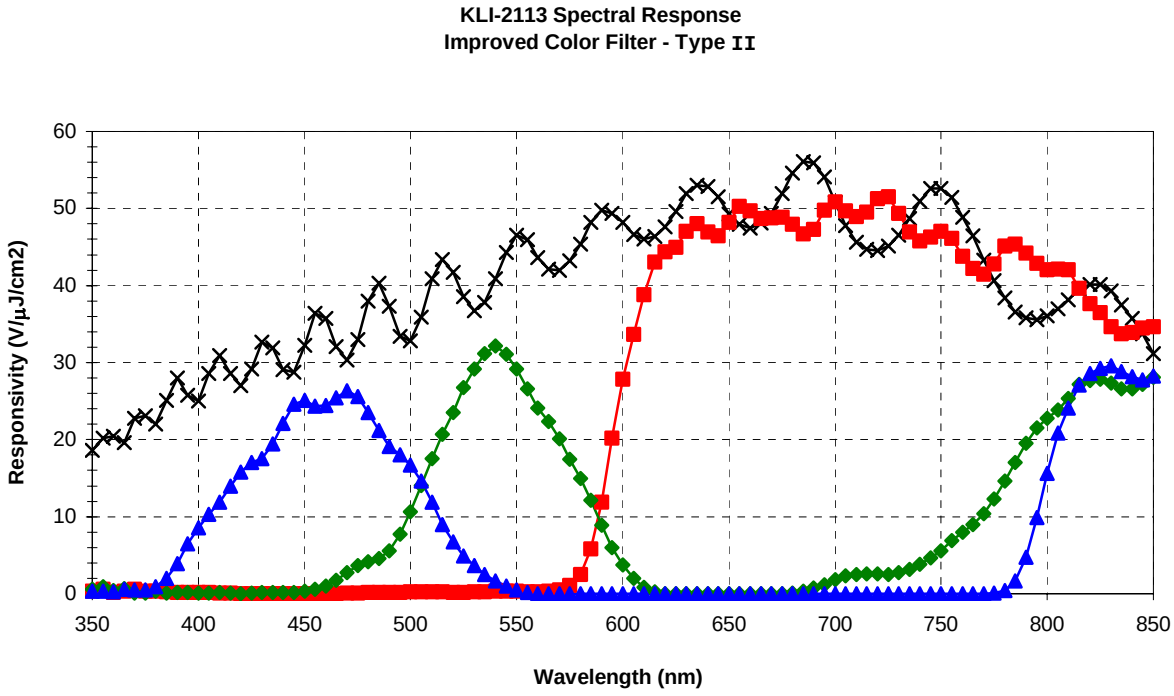


Figure 3: Typical Responsivity

DEFECT DEFINITIONS

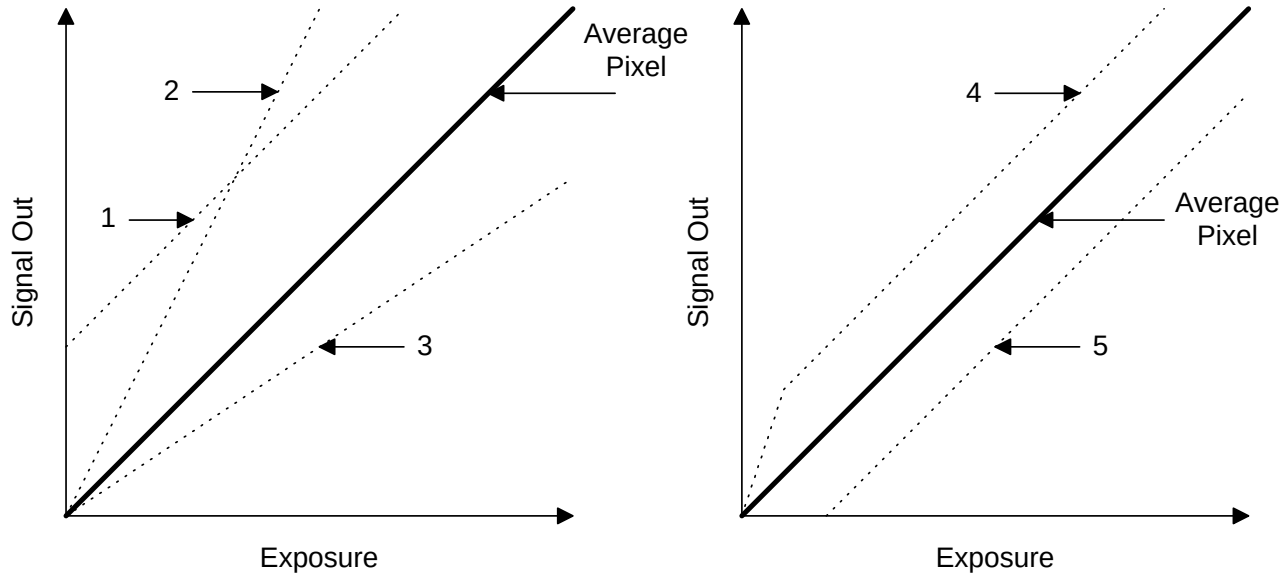
OPERATIONING CONDITIONS

Test conditions: T=25ºC, f_{CLK}=2MHz, t_{int}=1.066msec Specifications

Field	Defect Type	Threshold	Units	Notes	Number
Dark	Bright	8.0	mV	1, 2	0
Bright	Bright/Dark	10	%	1, 3	0
Bright	Exposure Control	4.0	mV	1, 4, 5	≤16

Notes:

1. Defective pixels will be separated by at least one non-defective pixel within and across channels.
2. Pixels whose response is greater than the average response by the specified threshold. See line 1 in figure below.
3. Pixels whose response is greater or less than the average response by the specified threshold. See lines 2 and 3 in figure below.
4. Pixels whose response deviates from the average pixel response by the specified threshold when operating in exposure control mode. See lines 4 and 5 in the figure below.
5. Defect coordinates are available upon request.



OPERATION

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Gate Pin Voltages	V_{GATE}	-0.5	+16	V	1, 2
Pin to Pin Voltage	$V_{PIN-PIN}$		16	V	1, 3
Diode Pin Voltages	V_{DIODE}	-0.5	+16	V	1,4
Output Bias Current	I_{DD}		-10	mA	5
Output Load Capacitance	$C_{VID,LOAD}$		15	pF	
CCD Clocking Frequency	f_C		20	MHz	6

Notes:

1. Referenced to substrate voltage.
2. Includes pins: ϕ1, ϕ2, ϕ2s, TG1, TG2, ϕR, IG, and LOGn.
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDn, RD, VDD, LS and ID.
5. Care must be taken not to short output pins to ground during operation as this may cause serious damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the nominal (2MHz) clocking frequency. VIDn load resistor values may need to be decreased as well to achieve required output bandwidths.

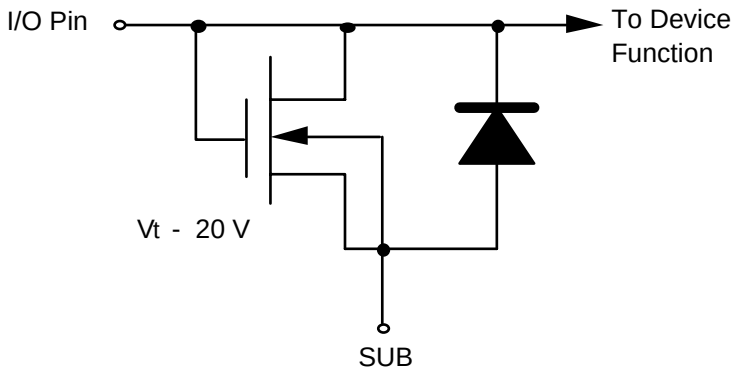


Figure 4: ESD Protection Circuit

CAUTION:

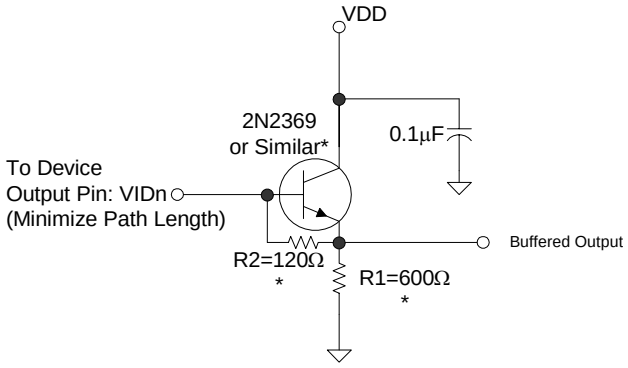
To allow for maximum performance, this device contains limited i/o protection and may be sensitive to electrostatic induced damage. Devices should be installed in accordance with strict ESD handling procedures!

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Substrate	V_{SUB}		0		V	
Reset Drain Bias	V_{RD}	+11.5	+12.0	+12.5	V	
Output Buffer Supply	VDD	+11.5	+12.0	+12.5	V	
Light Shield/Drain Bias	VLS	+11.5	+12.0	+12.5	V	
Output Bias Current/Ch.	I_{DDn}	-4.0	-6.0	-8.0	mA	1
Test Pin-Input Gate/LOG	V_{IG}		+12.0		V	
Test Pin-Input Diode	V_{ID}		+12.0		V	

Notes:

A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. See example below.



*Choose values optimized for specific operating frequency. R2 should not be less than 75Ω

Figure 5: Typical Output Bias/Buffer Circuit

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CCD Readout Clocks High	$V\phi_{1H}$,$V\phi_{2nH}$	+4.75	+5.0	+5.25	V	
CCD Readout Clocks Low	$V\phi_{1L}$,$V\phi_{2nL}$	-0.1	0	+0.1	V	
Transfer Clocks High	V_{TGnH}	+4.75	+5.0	+5.25	V	
Transfer Clocks Low	V_{TGnL}	-0.1	0	+0.1	V	
Reset Clock High	$V\phi_{RH}$	+4.75	+5.0	+5.25	V	
Reset Clock Low	$V\phi_{RL}$	-0.1	0	+0.1	V	
Exposure Clocks High	V_{LOGnH}	+4.75	+5.0	+5.25	V	1
Exposure Clocks Low	V_{LOGnL}	-0.1	0	+0.1	V	1

Note:

1. Tie pin to 0V for applications where exposure control is not used.

AC Timing Levels

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CCD Element Duration	$1e = 1/f_{CLK}$	50	500		ns	
Line/Integration Period	$1L = t_{int}$	0.108	1.066		ms	
PD-CCD Transfer Period	t_{pd}	1.0			µs	
Transfer Gate 1 Clear	t_{tg1}	500			ns	
Transfer Gate 2 Clear	t_{tg2}	500			ns	
Log Gate Duration	t_{LOG1}	1			µs	
Log Gate Clear	t_{LOG2}	1			µs	
Reset Pulse Duration	t_{rst}	9			ns	
Clamp to ϕ2 Delay	t_{cd}	5			ns	1
Sample to Reset Edge Delay	t_{sd}	5			ns	1
CCD Clock Rise Time	t_r		30		ns	Typical

Note:

1. Recommended delays for correlated double sampling of output.

TIMING

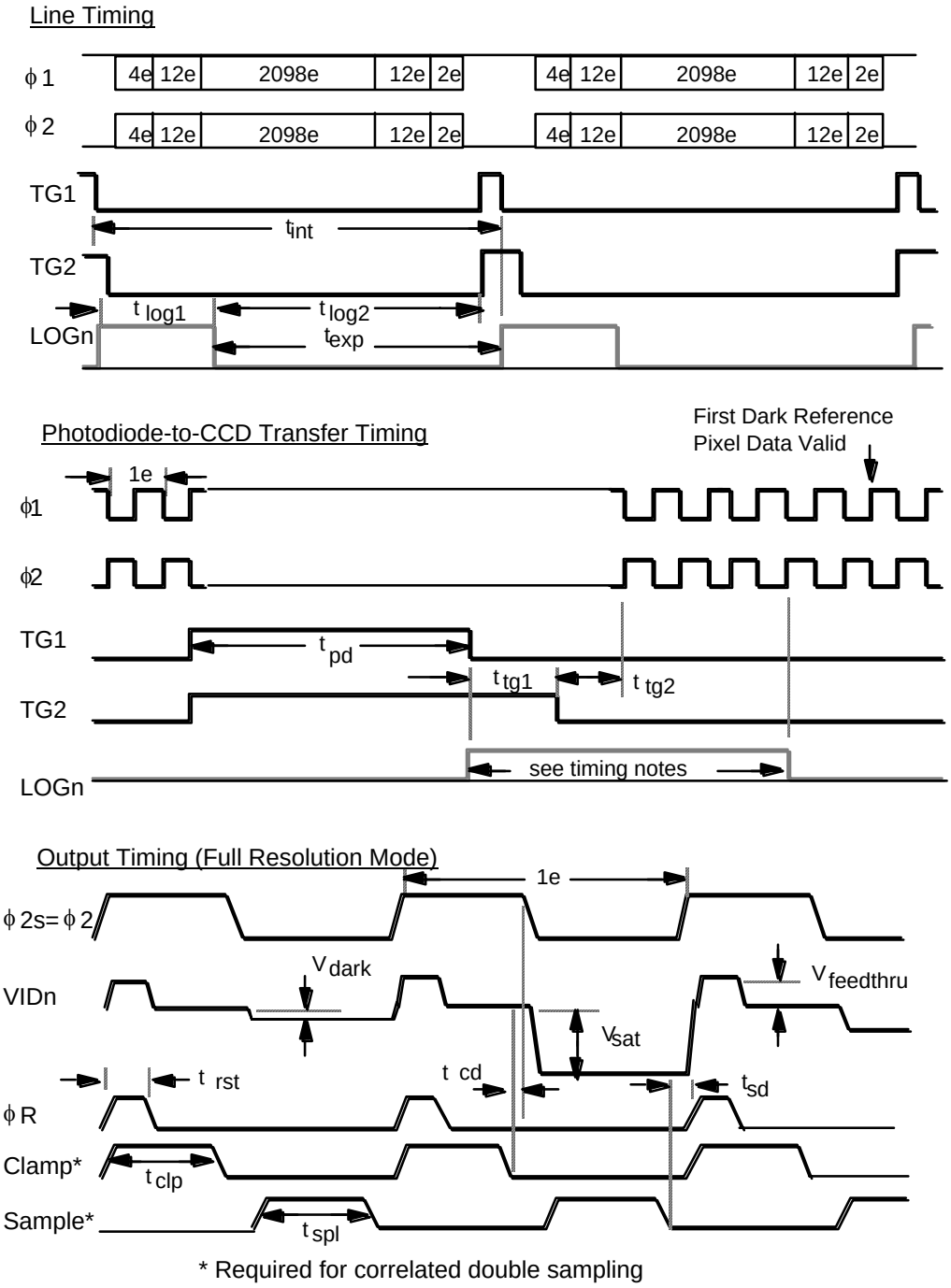


Figure 6: Line Timing

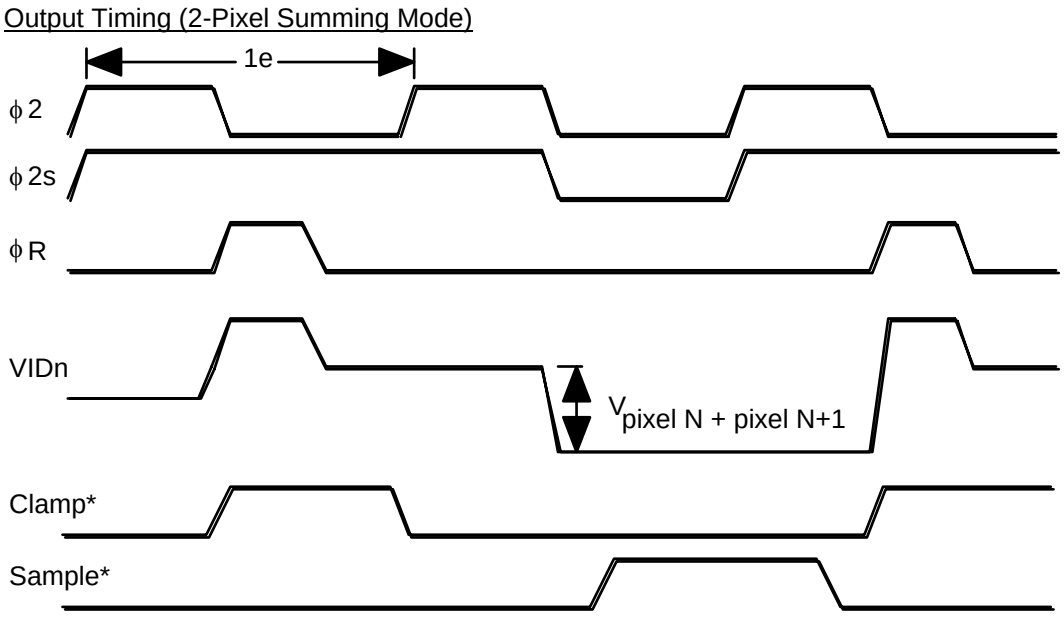


Figure 7: Output Timing

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	0	70	°C	1
Operating Teperature	T_{OP}	-25	+80	°C	2

Notes:
1. Noise performance will degrade with increasing temperatures.
2. Long term storage at these temperatures will accelerate color filter degradation.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices".

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. The color filters and/or microlenses may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter/microlens aging. (This condition applies to color parts only.)
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370ºC. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

MECHANICAL INFORMATION

COMPLETED ASSEMBLY

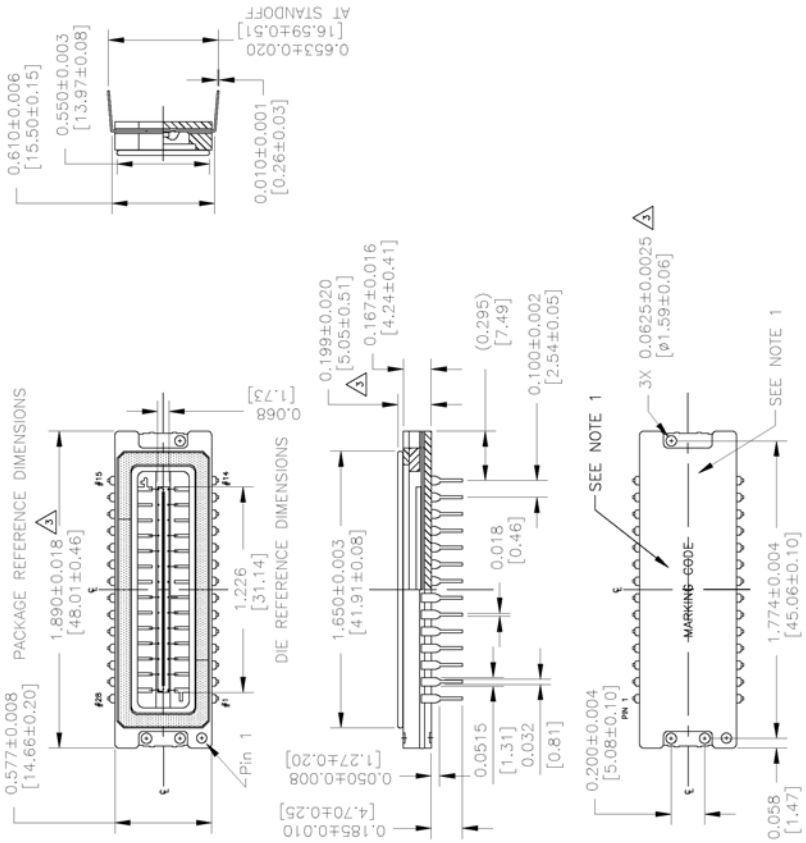


Figure 8: Completed Assembly Drawing (1 of 2)

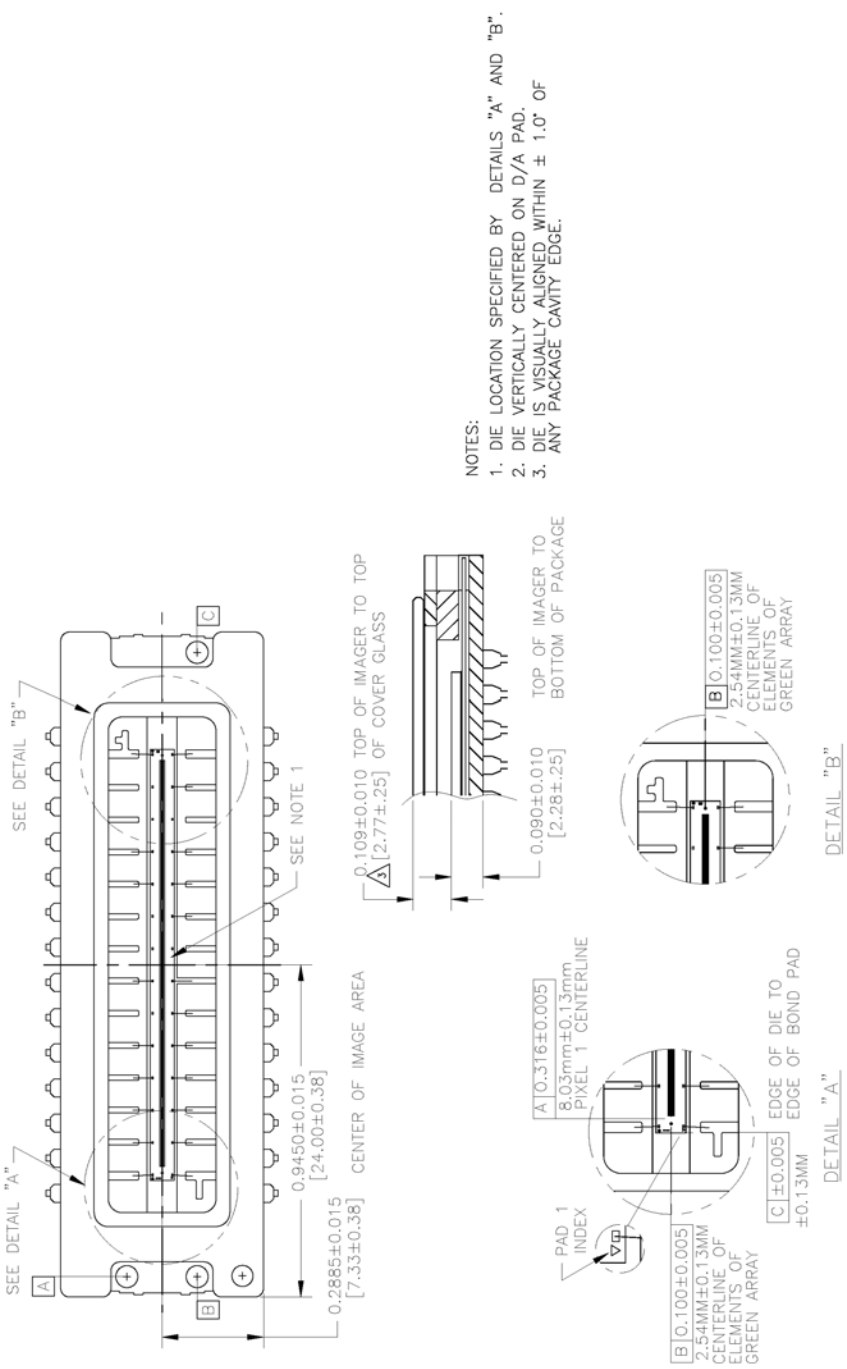


Figure 9: Completed Assembly Drawing (2 of 2)

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
4	New Color Filter materials implemented.
5	Updated format. Added Serial Numbers to Package Drawings
5.1	Corrected responsivity in Table on p.4

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