Data Sheet
December 1991

AT&T Microelectronics

T7275C Quad Differential Line Receiver

Features

- Four line receivers per package
- Low pulse-width distortion
- CMOS level outputs
- 7 ns minimum input pulse width
- 8.0 ns maximum propagation delay
- 140 Mbits/s data rate at 50% duty cycle
- 0.6 V input sensitivity
- 0.8 V minimum common-mode range
- Single 5 V supply
- Low-power CMOS technology
- −40 ° C to +85 ° C operating temperature available

Description

The T7275C Quad Differential Line Receiver integrated circuit is a quad differential input to CMOS output line receiver. It is functionally an ECL-level-to-CMOS converter. Direct interfacing to ECL signals is possible by ac coupling through a capacitor. The CMOS technology device is similar to the general-trade 26LS32 device; however, it has increased speed and decreased power consumption. By having four receivers in one T7275C device, circuit-board package count is reduced.

The typical propagation delay is 5 ns, and the typical common-mode operating range is 1.5 V. Input dc offset is less than 50 mV. The inputs typically have 10 mV of hysteresis.

The T7275C Line Receiver is compatible with many line drivers, including the AT&T T7274B and 41LG devices, and the general-trade 26LS31 device. The quad differential line receiver is available in a 16-pin, plastic DIP and a 16-pin, plastic SOJ package for surface mounting.

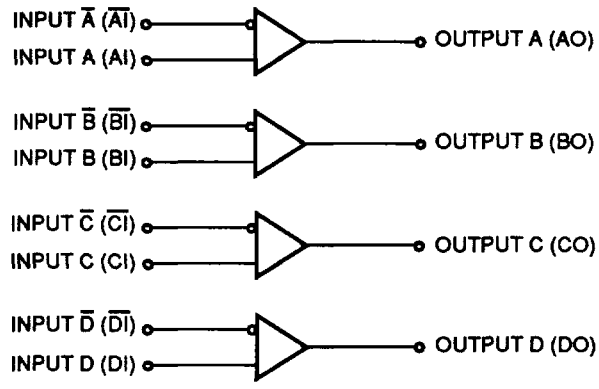


Figure 1. Block Diagram

Pin Information

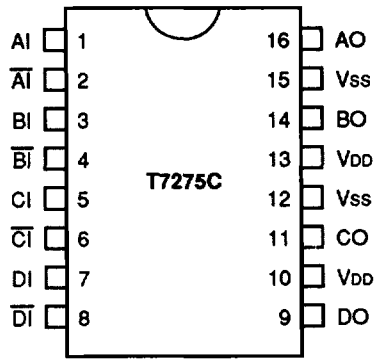


Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	AI	I	A-Line Driver Input.
2	$\overline{AI}$	I	Inverted A-Line Driver Input.
3	BI	I	B-Line Driver Input.
4	$\overline{BI}$	I	Inverted B-Line Driver Input.
5	CI	I	C-Line Driver Input.
6	$\overline{CI}$	I	Inverted C-Line Driver Input.
7	DI	I	D-Line Driver Input.
8	$\overline{DI}$	I	Inverted D-Line Driver Input.
9	DO	O	D-Line Driver Output.
10	V_{DD}	—	5 V Supply Pin.
11	CO	O	C-Line Driver Output.
12	V_{SS}	—	Ground Pin.
13	V_{DD}	—	5 V Supply Pin.
14	BO	O	B-Line Driver Output.
15	V_{SS}	—	Ground Pin.
16	AO	O	A-Line Driver Output.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability. External leads can be bonded or soldered safely at temperatures up to 300 ° C.

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{DD}	—	7.0	V
Ambient Operating Temperature Range	T_A	−40	85	°C
Storage Temperature Range	T_{stg}	−40	125	°C
Power Dissipation	P_{dis}	—	500	mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

HBM ESD Threshold	
Device	Voltage
T7275C	>2000 V

Typical Application

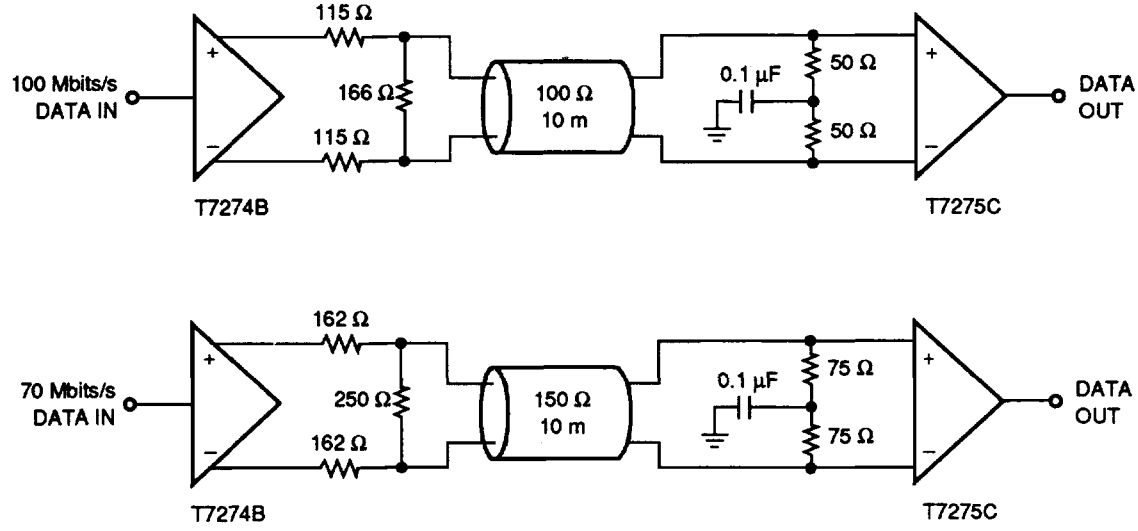


Figure 3. T7274B and T7275C in 100 Ω and 150 Ω Systems

Electrical Characteristics

T_A = −40 ° C to +85 ° C, (except as specified), or 0 ° C to 85 ° C (see the Ordering Information section), V_{DD} = 5.0 V ± 0.25 V

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages:					
Low, I_{OL} = 12.5 mA	V_{OL}	—	—	0.5	V
Low, I_{OL} = 25 mA	V_{OL}	—	—	0.9	V
High, I_{OH} = −12.5 mA	V_{OH}	4.25	—	—	V
High, I_{OH} = −25 mA	V_{OH}	3.85	—	—	V
Output Impedance	—	—	15	30	Ω
Differential Input Voltages:					
V_O = V_{OL} or V_{OH}; 2.1 V < V_{CM} < 2.9 V*	$V_{TH_{dc}}$†	50	—	—	mV
	$V_{TH_{ac}}$‡	0.6	—	—	V
Input Voltages Applied to Any Output:					
Low	V_{IL}	−0.5	—	—	V
High	V_{IH}	—	—	V_{DD} + 0.5	V
Input Currents (−0.5 V ≤ V_{IN} ≤ V_{DD} + 0.5 V):					
Differential	I_{ILD}	—	—	±2.0	μA
Any Input	I_{ILD}	—	—	±10	μA
Power Supply Current:					
dc Conditions§ (T_A = −40 ° C to +85 ° C)	I_{DD}	—	12.0	23.0	mA
dc Conditions§ (T_A = 0 ° C to 85 ° C)	I_{DD}	—	12.0	20.0	mA
100 Mbits/s (including load in Figure 4), Data = . . .0101. . .	I_{DD}	—	80.0	95.0	mA
Power Dissipation Capacitance per Channel	C_{PD}	—	32.0	—	pF
Input Capacitance	C_I	—	5.0	—	pF
Input Hysteresis	V_{HYST}	—	10	—	mV

* Operation with 1 V < V_{CM} < 4 V is possible, but with relaxed propagation delay and pulse-width distortion characteristics.
† dc threshold voltage. The minimum input differential voltage has zero noise immunity. This should be tested only in a static, noise-free environment.
‡ To meet timing specifications.
§ Pulling both differential inputs below 0.6 V powers down the device. The corresponding outputs go high.

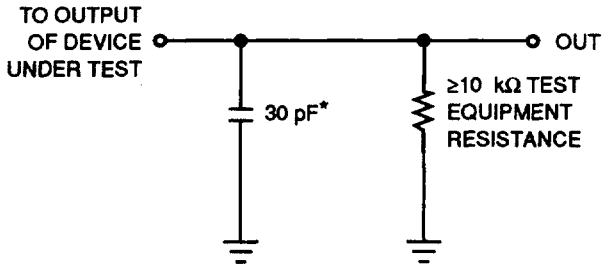
Timing Characteristics

T_A = −40 ° C to +85 ° C for T7275C-PL/EL (except as specified), V_{DD} = 5.0 V ± 0.25 V, 0 ° C to 85 ° C for T7275C-PE/EE, Figure 4, test circuit connected to output. The characteristics in this table apply to Figures 6 and 7. Input rise and fall times (10% to 90%) of less than 4 ns are necessary to meet maximum propagation delay and pulse-width distortion specifications.

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t_{PHL} t_{PLH}	Propagation delay input to output For all input configurations	3.5	5.0	8.0	ns	0 ° C to 85 ° C
t_{PHL} t_{PLH}	For all input configurations	2.5	5.0	8.0	ns	−40 ° C to +85 ° C
t_{PWD}	Pulse-width Distortion, $\lvert t_{IN} - t_{OUT} \rvert$	—	100	500	ps	—
t_R, t_F	Rise and Fall Times (10% to 90%)	—	1.5	3.0	ns	—
t_{IN}	Input Pulse Width	7	—	—	ns	—

Timing Characteristics (continued)

Timing Diagrams



* Includes jig and measurement equipment capacitance. See Figure 7 for variation in propagation delay with capacitance.

Figure 4. Output Voltage and Propagation Delay Test Circuit

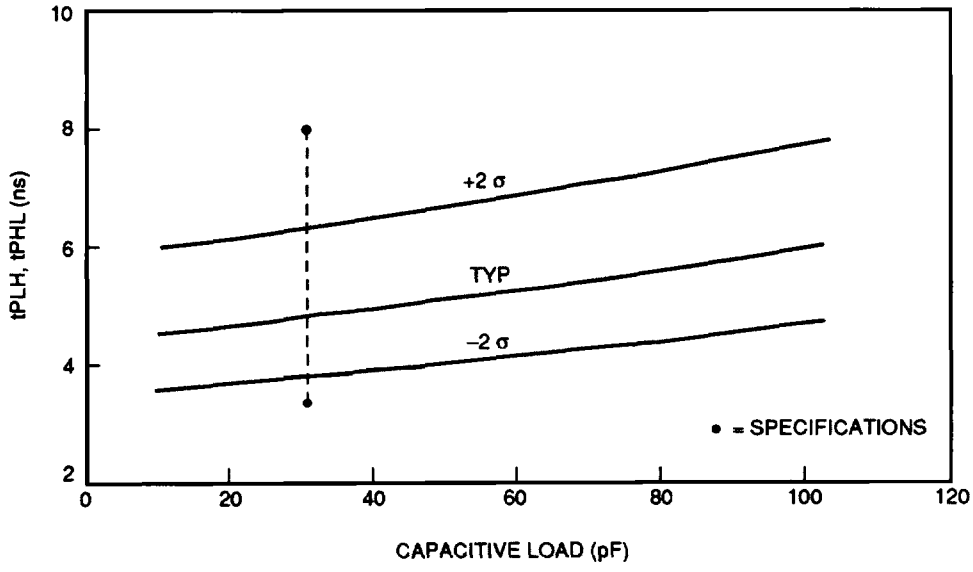


Figure 5. Propagation Delay vs. Loading Capacitance

Timing Characteristics (continued)

Timing Diagrams (continued)

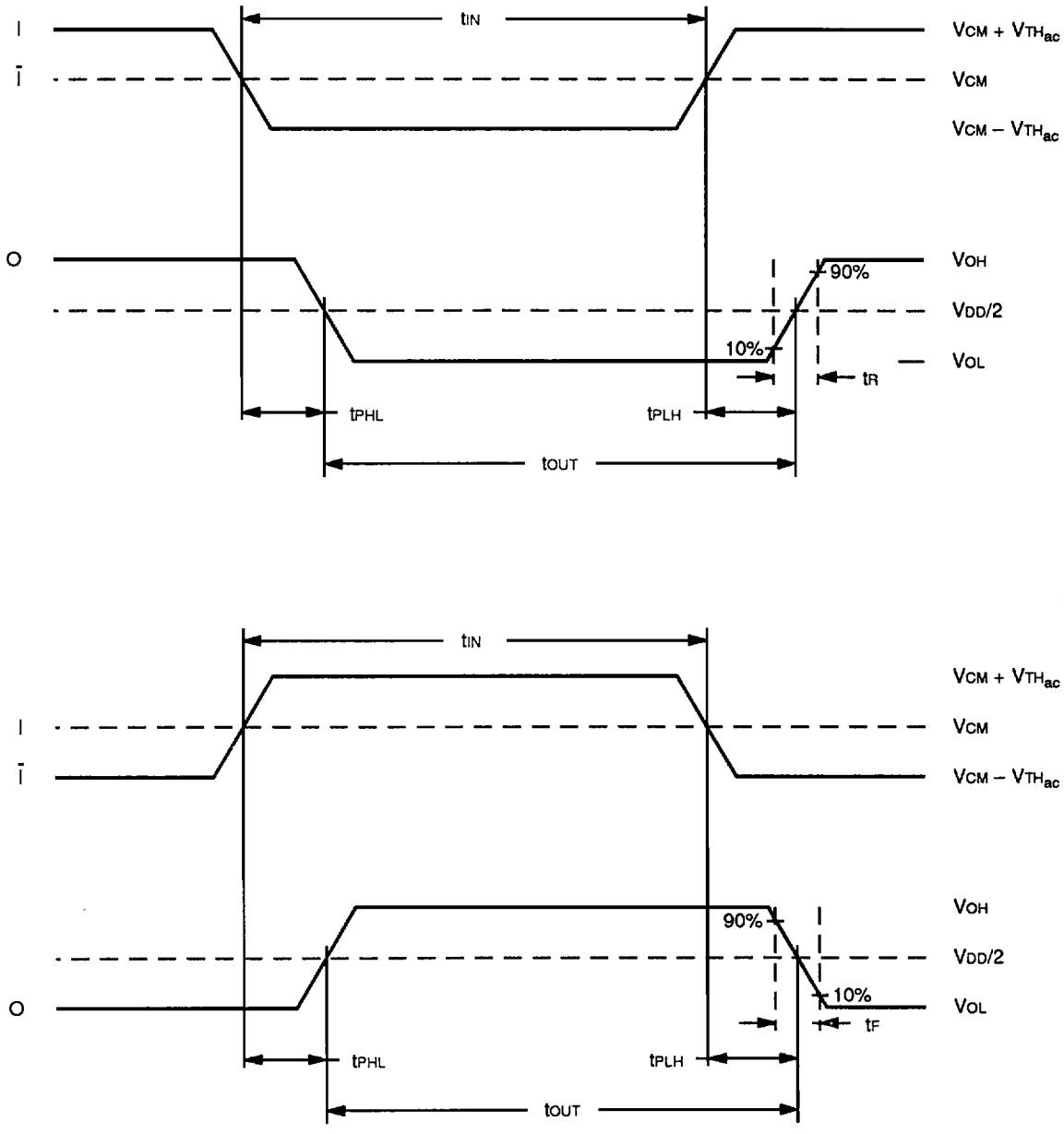


Figure 6. Timing Waveforms, Single-Ended Mode

Timing Characteristics (continued)

Timing Diagrams (continued)

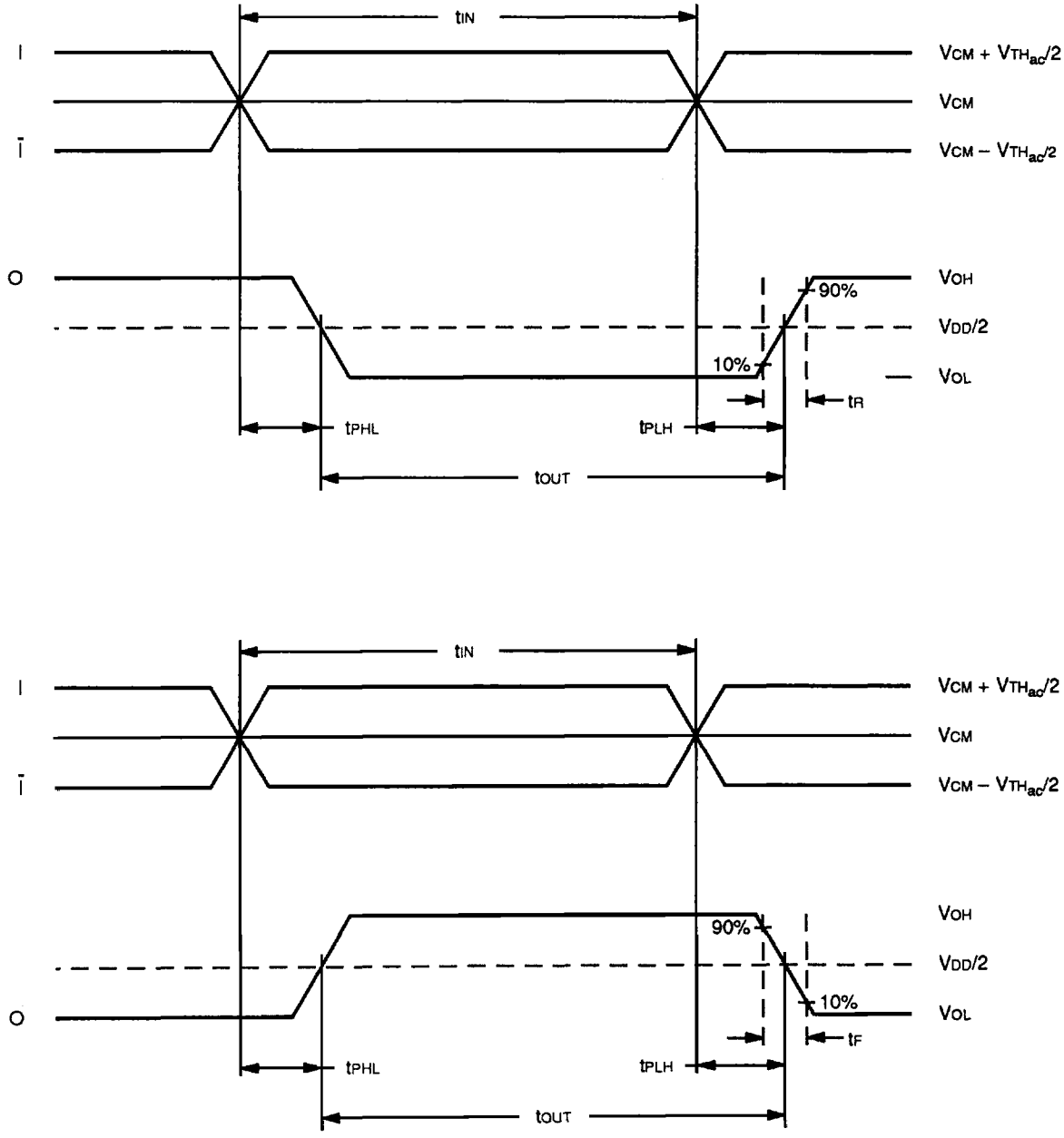
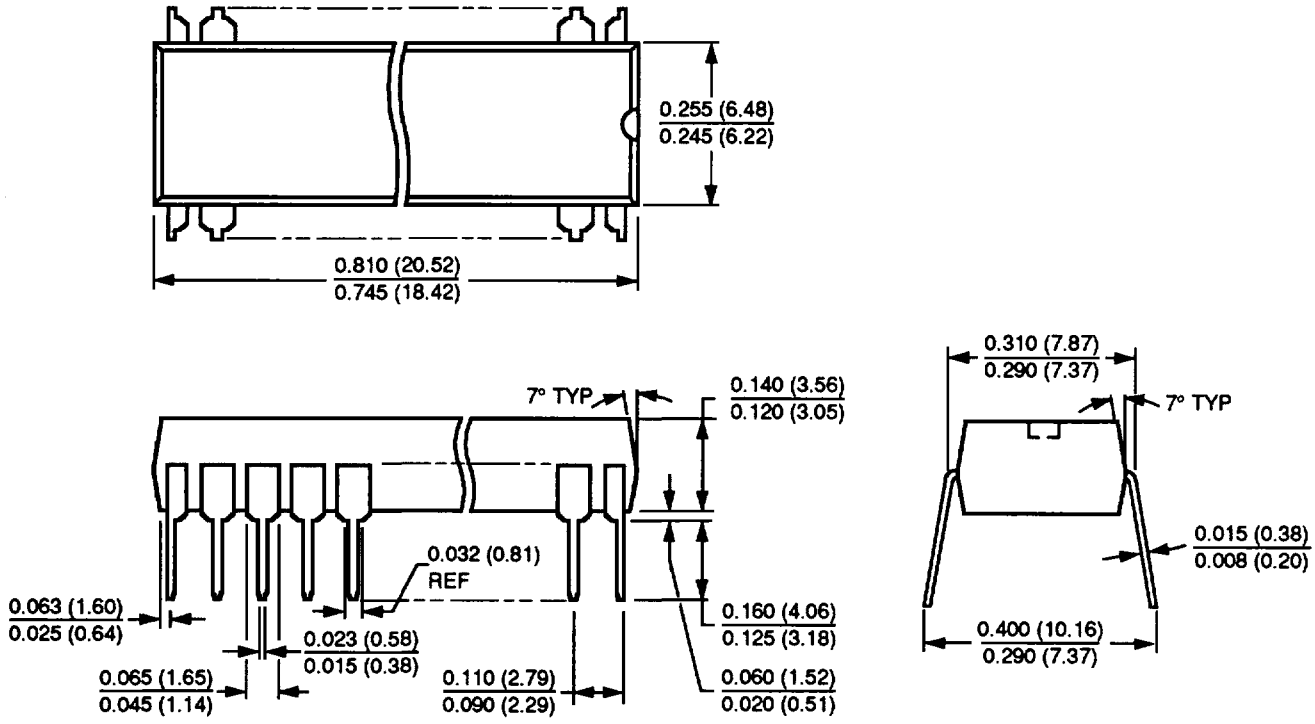


Figure 7. Timing Waveforms, Differential Mode

Outline Diagrams

16-Pin, Plastic DIP

Dimensions are in inches and (millimeters).



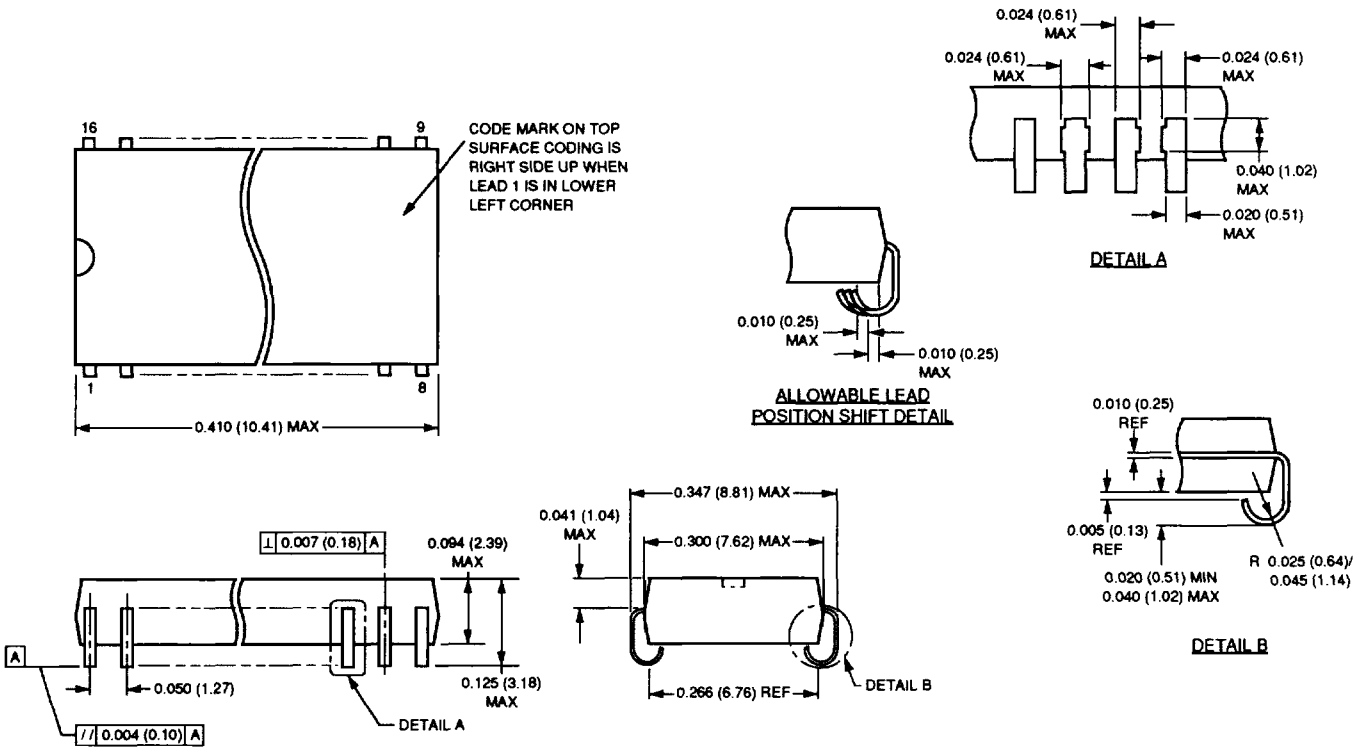
Notes:
Meets JEDEC standards.

Index mark may be semicircular notch or circular dimple located in index area.

Outline Diagrams (continued)

16-Pin, Plastic SOJ, Surface Mounting

Dimensions are in inches and (millimeters).



Ordering Information

Device Code	Package	Temperature	Comcode
T7275C-PE	16-Pin, Plastic DIP	0 ° C to 85 ° C	106279755
T7275C-EE	16-Pin, Plastic SOJ	0 ° C to 85 ° C	106279730
T7275C-PL	16-Pin, Plastic DIP	−40 ° C to +85 ° C	106601321
T7275C-EL	16-Pin, Plastic SOJ	−40 ° C to +85 ° C	106279748

Notes

For additional information, contact your AT&T Account Manager or the following:
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