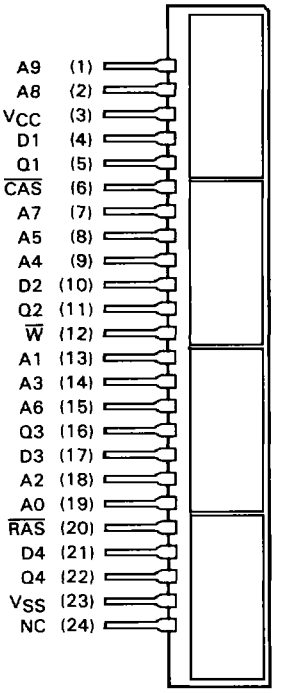
MAY 1987—REVISED MAY 1988

- 1,048,576 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- 24-Pin Single-In-line Package (SIP)
- Utilizes Four 1 Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages
- Long Refresh Period . . . 8 ms (512 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4C1024-10	100 ns	45 ns	190 ns
TMS4C1024-12	120 ns	55 ns	220 ns
TMS4C1024-15	150 ns	70 ns	260 ns

- Common $\overline{CAS}$ Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C

AC SINGLE-IN-LINE PACKAGE
(TOP VIEW)



description

The TM024HAC4 is a 4,096K dynamic random-access memory module, organized as 1,048,576 × 4 bits in a 24-pin single-in-line package (SIP). The SIP is composed of four TMS4C1024DJ, 1,048,576 × 1 bit dynamic RAMs, each in a 26/20-lead plastic small outline J-lead package (SOJ), mounted on top of a substrate together with decoupling capacitors mounted beneath the SOJs. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized. Each TMS4C1024DJ is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

PIN NOMENCLATURE TM024HAC4	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D4	Data Inputs
NC	No Connection
Q1-Q4	Data Outputs
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

The TM024HAC4 features $\overline{RAS}$ access times of 100 ns, 120 ns, and 150 ns maximum.

The refresh period is extended to 8 milliseconds, and during this period each of the 512 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

description (continued)

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM024HAC4 is rated for operation from 0°C to 70°C.

operation

The TM024HAC4 operates as four TMS4C1024s connected as shown in the functional block diagram on the following page. Refer to the TMS4C1024 data sheet for details of its operation.

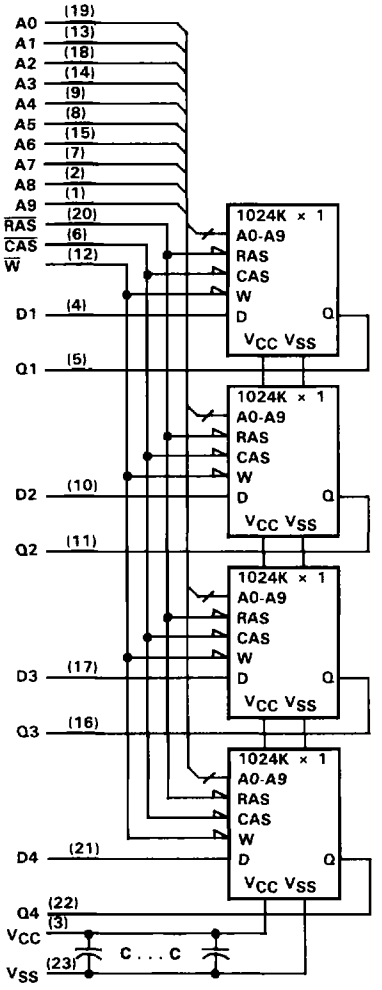
specifications

For TMS4C1024DJ electrical specifications, refer to the TMS4C1024 data sheet.

single-in-line package and components

PC substrate: 1,27 mm (0.05 in) nominal thickness; 0.005 in/in maximum warpage
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . . −1 V to 7 V
Voltage range on V_{CC} (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM024HAC4-10		TM024HAC4-12		TM024HAC4-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		280		240		220	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		12		12		12	mA
I_{CC3}	Average refresh current	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		260		220		200	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		180		140		120	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		24	pF
$C_{i(D)}$	Input capacitance, data inputs		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		28	pF
$C_{i(W)}$	Input capacitance, write-enable input		28	pF
C_o	Output capacitance		7	pF

NOTE 3: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0.0 V.