

## CMOS Strobed Hex Inverter/Buffer

High-Voltage Types (20-Volt Rating)

■ CD4502B consists of six inverter/buffers with 3-state outputs. A logic "1" on the OUTPUT DISABLE input produces a high-impedance state in all six outputs. This feature permits common bussing of the outputs, thus simplifying system design. A Logic "1" on the INHIBIT input switches all six outputs to logic "0" if the OUTPUT DISABLE input is a logic "0". This device is capable of driving two standard TTL loads, which is equivalent to six times the JEDEC "B"-series I<sub>OL</sub> standard.

The CD4502B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix). This device is similar to the MC14502.

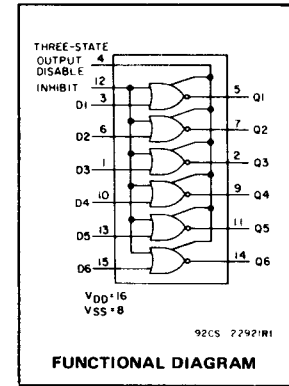
### Features:

- 2 TTL-load output drive capability
- 3-state outputs
- Common output-disable control
- Inhibit control
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Noise margin (full package-temperature range) =

1 V at V<sub>DD</sub> = 5 V  
 2 V at V<sub>DD</sub> = 10 V  
 2.5 V at V<sub>DD</sub> = 15 V

### Applications:

- 3-state hex inverter for interfacing IC's with data buses
- COS/MOS to TTL hex buffer



### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )	-0.5V to +20V
Voltages referenced to V <sub>SS</sub> Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V <sub>DD</sub> +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P <sub>D</sub> ):	
For T <sub>A</sub> = -55°C to +100°C	500mW
For T <sub>A</sub> = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

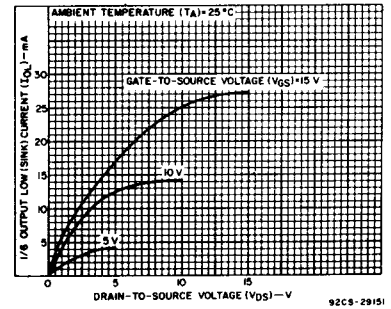


Fig.2 — Typical output low (sink) current characteristics.

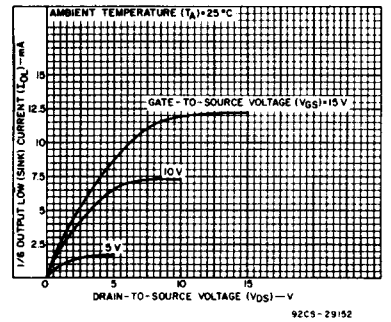


Fig.3 — Minimum output low (sink) current characteristics.

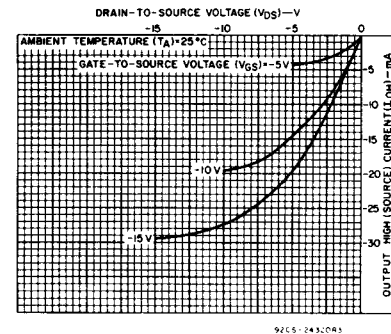


Fig.4 — Typical output high (source) current characteristics.

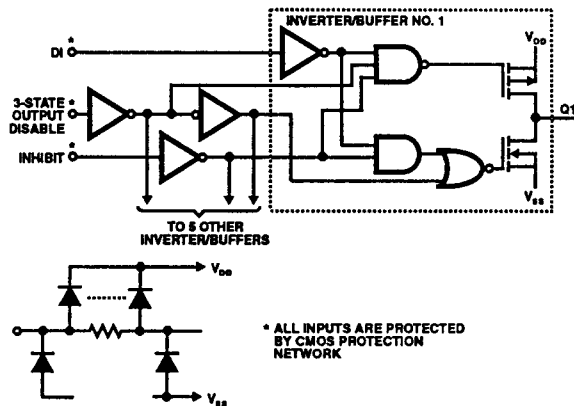
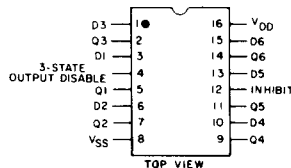


Fig.1 — Logic diagram of 1 of 6 identical inverter/buffers.

TRUTH TABLE			
DISABLE	INHIBIT	D <sub>n</sub>	Q <sub>n</sub>
0	0	0	1
0	0	1	0
0	1	X	0
1	X	X	Z

Logic 0 = Low  
 Z = High Impedance  
 X = Don't Care  
 Logic 1 = High



### TERMINAL ASSIGNMENT

# CD4502B Types

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range)	3	18	V

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	+25							
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, $I_{DD}$ Max.	-	0,5	5	1	1	30	30	-	0.02	1	$\mu A$
	-	0,10	10	2	2	60	60	-	0.02	2	
	-	0,15	15	4	4	120	120	-	0.02	4	
	-	0,20	20	20	20	600	600	-	0.04	20	
Output Low (Sink) Current $I_{OL}$ Min.	0.4	0,5	5	3.84	3.66	2.52	2.16	3.06	6	-	mA
	0.5	0,10	10	9.6	9	6.6	5.4	7.8	15.6	-	
Output High (Source) Current, $I_{OH}$ Min.	1.5	0,15	15	25.2	24	16.8	14.4	20.4	40.8	-	mA
	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
Output Voltage: Low-Level, $V_{OL}$ Max.	-	0,5	5			0.05			0	0.05	V
	-	0,10	10			0.05			0	0.05	
	-	0,15	15			0.05			0	0.05	
	-	0,5	5			4.95			4.95	5	
Output Voltage: High-Level, $V_{OH}$ Min.	-	0,5	5			4.95			4.95	10	V
	-	0,10	10			9.95			9.95	15	
	-	0,15	15			14.95			14.95	15	
	-	0,5	5			1.5			-	1.5	
Input Low Voltage, $V_{IL}$ Max.	0.5, 4.5	-	5			1.5			-	1.5	V
	1, 9	-	10			3			-	3	
	1.5, 13.5	-	15			4			-	4	
Input High Voltage, $V_{IH}$ Min.	4.5	-	5			3.5			3.5	-	V
	9	-	10			7			7	-	
	13.5	-	15			11			11	-	
Input Current $I_{IN}$ Max.		0,18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu A$
3-State Output Leakage Current $I_{OUT}$ Max.	0,18	0,18	18	$\pm 0.4$	$\pm 0.4$	$\pm 12$	$\pm 12$	-	$\pm 10^{-4}$	$\pm 0.4$	$\mu A$

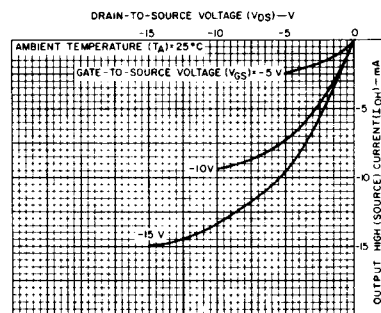


Fig. 5 - Minimum output high (source) current characteristics.

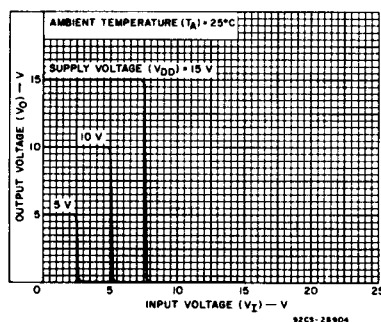


Fig. 6 - Typical voltage transfer characteristics.

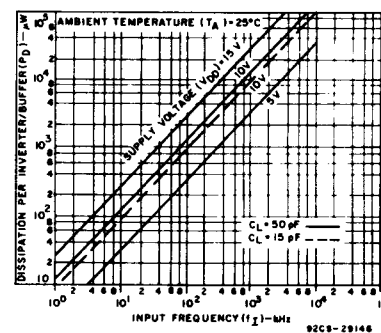


Fig. 7 - Typical power dissipation as a function of input frequency.

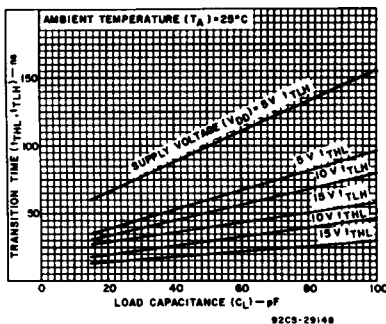


Fig. 8 - Typical transition time as a function of load capacitance.

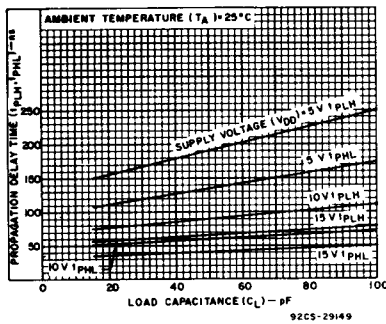


Fig. 9 - Typical propagation delay time as a function of load capacitance.

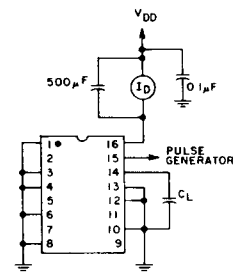


Fig. 10 - Power-dissipation test circuit.

## CD4502B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ K}\Omega$  Unless otherwise specified.**

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		VDD (V)	TYP		MAX
Data or Inhibit Delay Times: High to Low, $t_{PHL}$		5	135	270	ns
		10	60	120	
		15	40	80	
Low to High, $t_{PLH}$		5	190	380	ns
		10	90	180	
		15	65	130	
Disable Delay Times: $R_L = 1 \text{ K}\Omega$ Output High to High Impedance, $t_{PHZ}$	See Fig. 14	5	60	120	ns
		10	40	80	
		15	30	60	
High-Impedance to Output High, $t_{PZH}$	See Fig. 14	5	110	220	ns
		10	50	100	
		15	40	80	
Output Low to High Impedance, $t_{PLZ}$	See Fig. 14	5	125	250	ns
		10	65	130	
		15	55	110	
High Impedance to Output Low, $t_{PZL}$	See Fig. 14	5	125	250	ns
		10	55	110	
		15	40	80	
Transition Times: Low to High, $t_{TLH}$		5	100	200	ns
		10	50	100	
		15	40	80	
High to Low, $t_{THL}$		5	60	120	ns
		10	30	60	
		15	20	40	
Input Capacitance, $C_{IN}$	Any Input	5	7.5	pF	
Output Capacitance, $C_{OUT}$		7-8	15	pF	

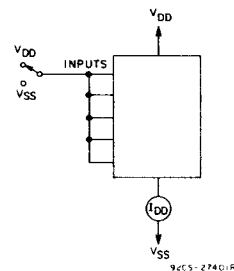


Fig. 11 - Quiescent device current test circuit.

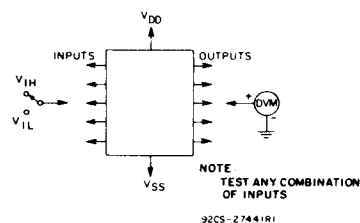


Fig. 12 - Input voltage test circuit.

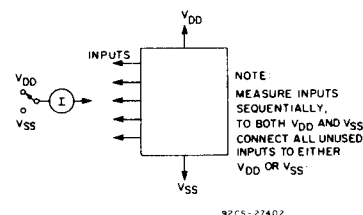


Fig. 13 - Input leakage current test circuit.

**3**  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

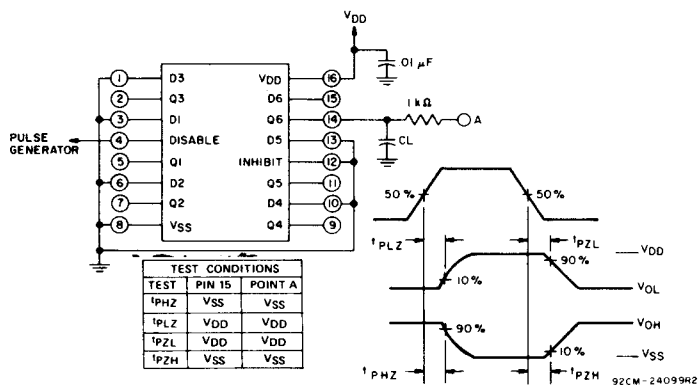
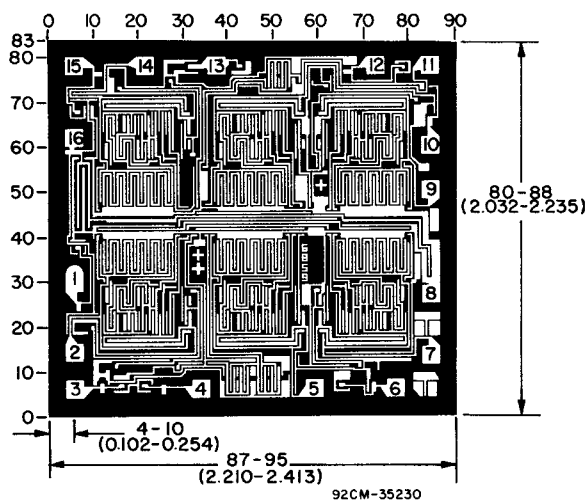


Fig. 14 - Disable delay times test circuit and waveforms.



Dimensions and Pad Layout for CD4502BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).