HOLT INTEGRATED CIRCUITS INC.

# HI-15530

October 2008

## 5V / 3.3V Manchester Encoder / Decoder

## GENERAL DESCRIPTION

The HI-15530 is a high performance CMOS integrated circuit designed to meet the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. The HI-15530 contains both an Encoder and Decoder, which operate independently.

The HI-15530 is fully compatible with either 5V or 3.3V logic and transceivers.

The device generates MIL-STD-1553 sync pulses, parity bits as well as the Manchester II encoding of the data bits. The decoder recognizes and identifies sync pulses, decodes data bits, and performs parity checking.

The HI-15530 supports the 1Mbit/s data rate of MIL-STD-1553 over the full temperature and voltage range.

For applications requiring small footprints and low cost, the HI-15530 is available in a 24-pin plastic SSOP package. Ceramic DIP and LCC packages are also available to achieve the highest level of reliability and to provide drop-in replacements for obsolete parts from other manufacturers.

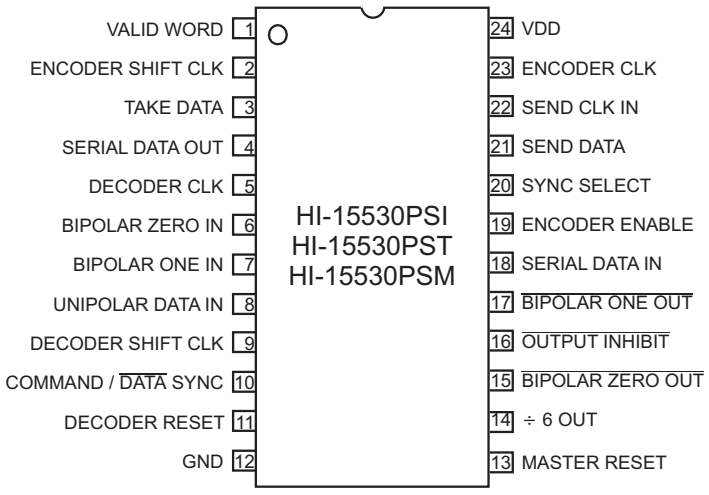
## APPLICATIONS

- MIL-STD-1553 Interfaces
- Smart Munitions
- Stores Management
- Sensor Interfaces
- Instrumentation

## FEATURES

- MIL-STD-1553 compatible
- 5V or 3.3V operation
- Interfaces to HI-1567 Transceiver Family
- Small footprint 24-pin plastic SSOP package option
- Direct replacement for:
  Harris/Intersil HD15530
  GEC Plessey Semiconductors MAS15530
  Aeroflex ACT15530
- 1.25 Mbit/s Maximum Data Rate
- Manchester II Encode and Decode
- Sync identification and Lock-in

## PIN CONFIGURATION (Top View)




**24 Pin SSOP package**

(Additional package pin configurations shown inside data sheet)

# PIN DESCRIPTIONS

| SIGNAL | SECTION | FUNCTION | DESCRIPTION |
|---|---|---|---|
| VALID WORD | DECODER | OUTPUT | A high output signals the receipt of a valid word |
| ENCODER SHIFT CLOCK | ENCODER | OUTPUT | Shifts data into the encoder on a low to high transition |
| TAKE DATA | DECODER | OUTPUT | Output is high during receipt of data after identification of a Sync Pulse and two valid Manchester data bits. |
| SERIAL DATA OUT | DECODER | OUTPUT | Received Data output in NRZ format |
| DECODER CLOCK | DECODER | INPUT | 12x the data rate. Clock for the transition finder and synchronizer, which generates the internal clock for the remainder of the decoder |
| BIPOLAR ZERO IN | DECODER | INPUT | A high input indicates the 1553 bus is in its negative state. This pin must be held high when the Unipolar input is used |
| BIPOLAR ONE IN | DECODER | INPUT | A high input indicates the 1553 bus is in the positive state. This pin must be held low when the Unipolar input is used |
| UNIPOLAR DATA IN | DECODER | INPUT | Input for unipolar data to the transition finder. Must be held low when Not in use |
| DECODER SHIFT CLOCK | DECODER | OUTPUT | Provides the DECODER CLOCK divided by 12, synchronized by the recovered serial data |
| COMMAND / $\overline{\text{DATA}}$ SYNC | DECODER | OUTPUT | A high on this pin occurs during the output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character |
| DECODER RESET | DECODER | INPUT | A high applied to this pin during a DECODER SHIFT CLOCK rising edge resets the bit counter |
| GND | BOTH | POWER | 0V supply |
| MASTER RESET | BOTH | INPUT | A high on this pin clears the 2:1 counters in both Encoder and Decoder and resets the divide-by-6 circuit |
| ÷6 OUT | ENCODER | OUTPUT | Provides ENCODER CLOCK divided by 6 |
| $\overline{\text{BIPOLAR ZERO OUT}}$ | ENCODER | OUTPUT | An active low output intended to drive the zero or negative sense of a MIL-STD-1553 Line Driver |
| $\overline{\text{OUTPUT INHIBIT}}$ | ENCODER | INPUT | A low inhibits the $\overline{\text{BIPOLAR ZERO OUT}}$ and $\overline{\text{BIPOLAR ONE OUT}}$ by forcing them to inactive high states |
| $\overline{\text{BIPOLAR ONE OUT}}$ | ENCODER | OUTPUT | An active low output intended to drive the one or positive sense on a MIL-STD-1553 Line Driver |
| SERIAL DATA IN | ENCODER | INPUT | Accepts serial data at the rate of the ENCODER SHIFT CLOCK |
| ENCODER ENABLE | ENCODER | INPUT | A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete) |
| SYNC SELECT | ENCODER | INPUT | Actuates a Command Sync for an input high and a Data Sync for a low |
| SEND DATA | ENCODER | OUTPUT | An active high output which enables the external source of serial Data |
| SEND CLOCK IN | ENCODER | INPUT | Clock input at 2 times the Data rate, usually driven by ÷6 OUT |
| ENCODER CLOCK | ENCODER | INPUT | Input to the divide by 6 circuit. Normal frequency is Data rate x12 |
| VDD | BOTH | POWER | 3.0 V to 5.5 V power supply pin |

# ENCODER OPERATION

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide-by-six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the ENCODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK (1). This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word (2). When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods (3). During these sixteen periods the data should be clocked into the SERIAL DATA IN input with every low-to-high transition of the ENCODER SHIFT CLOCK (3) - (4). After the sync and the Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word (5). If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time (5) as shown to prevent a consecutive word from being encoded. At any time a low on the $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

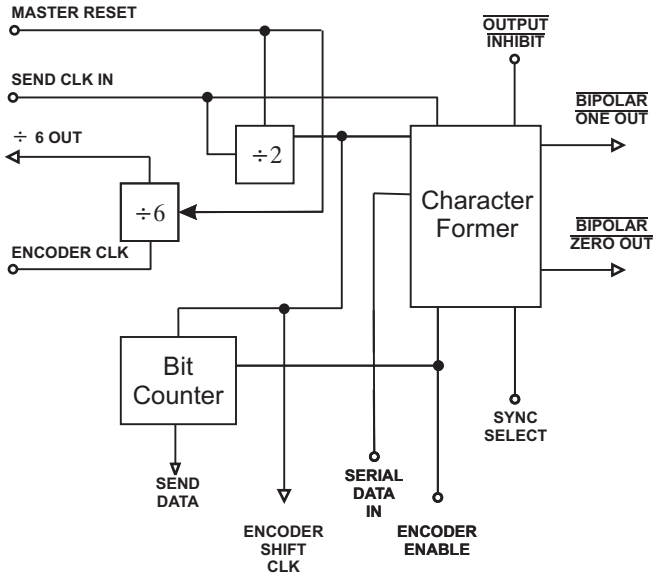



FIGURE 1. ENCODER

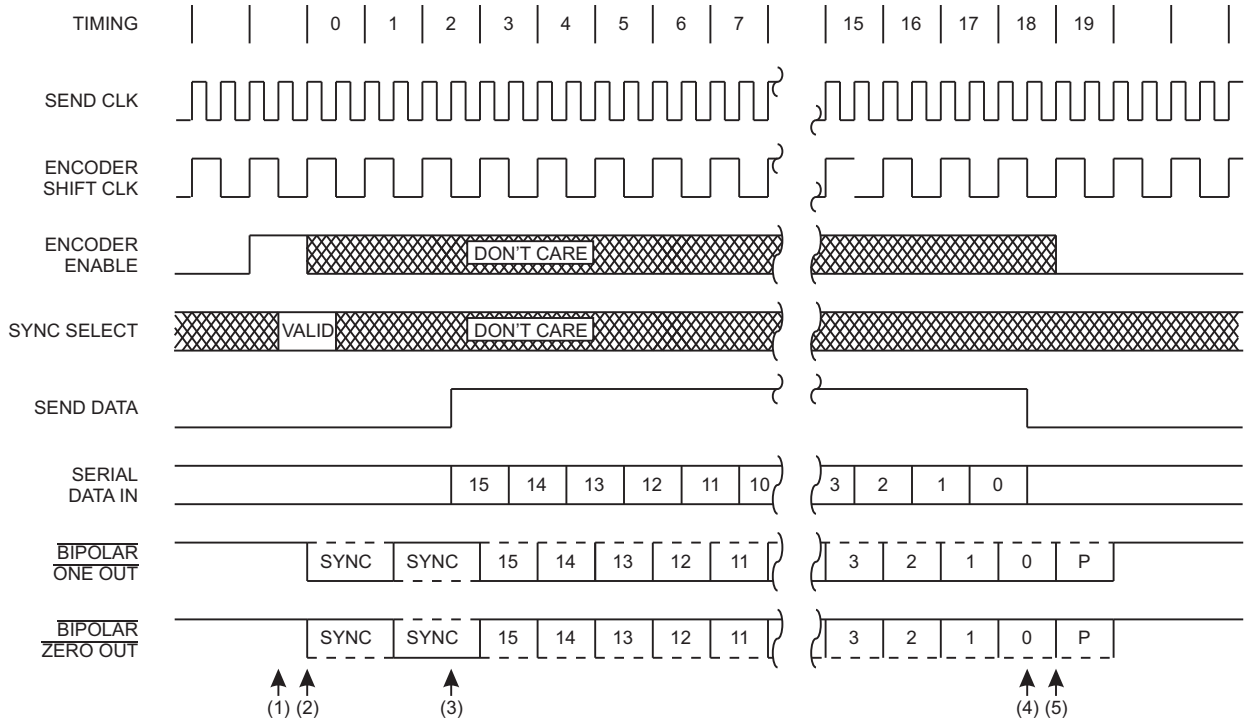



FIGURE 2. ENCODER OPERATION

# DECODER OPERATION

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in MIL-STD-1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ of an Encoder). The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized (1), the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high (2) and remain high for sixteen DECODER SHIFT CLOCK periods (3), otherwise it will remain low. The TAKE DATA output will go high and remain high (2) - (3) while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in an NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock (2) - (3). After all sixteen decoded bits have been transmitted (3) the data is checked for odd parity. A high on VALID WORD output (4) indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown (1). At any time in the above sequence, a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

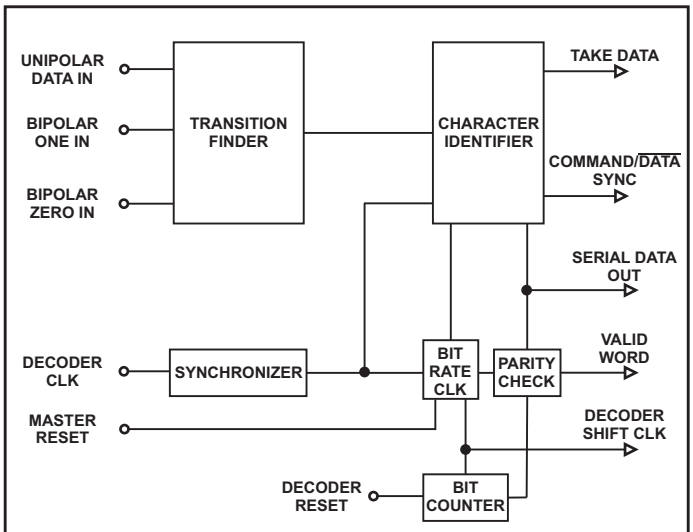



FIGURE 3. DECODER

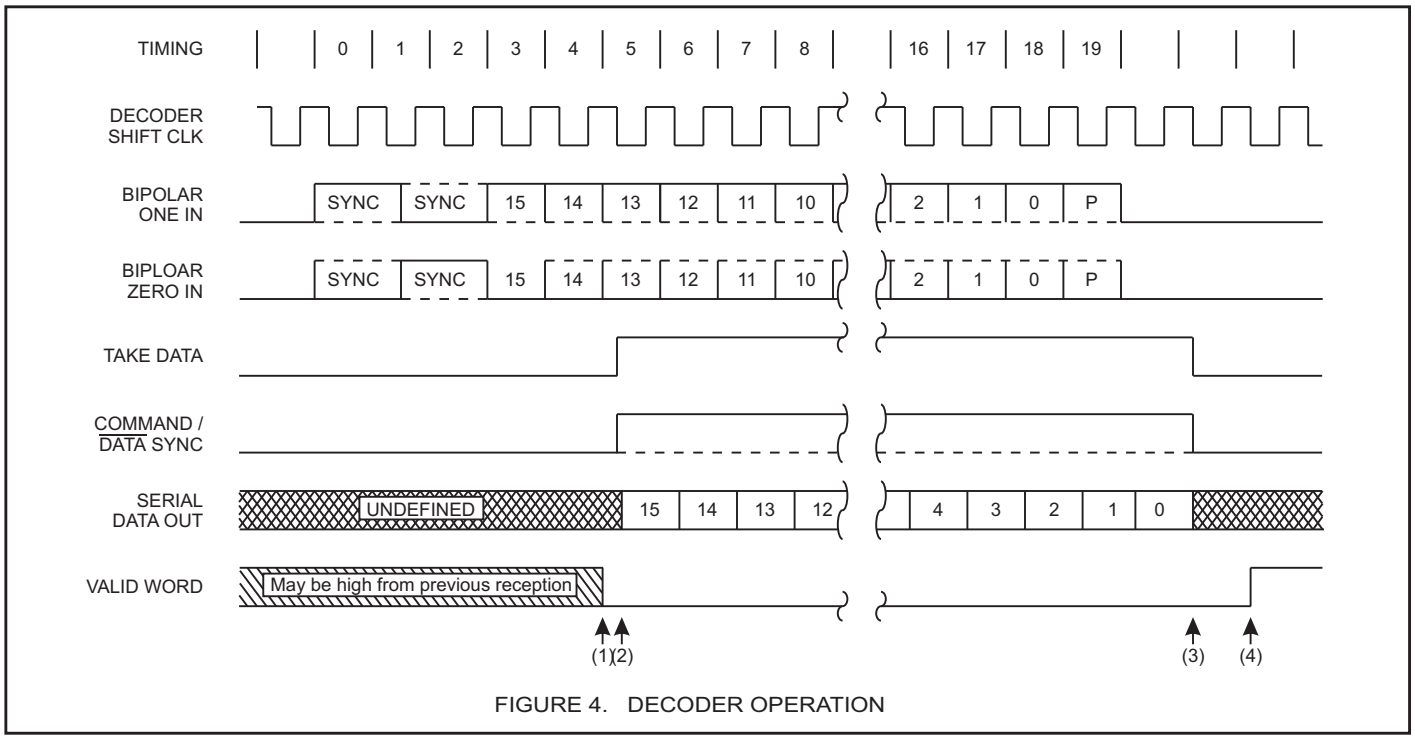
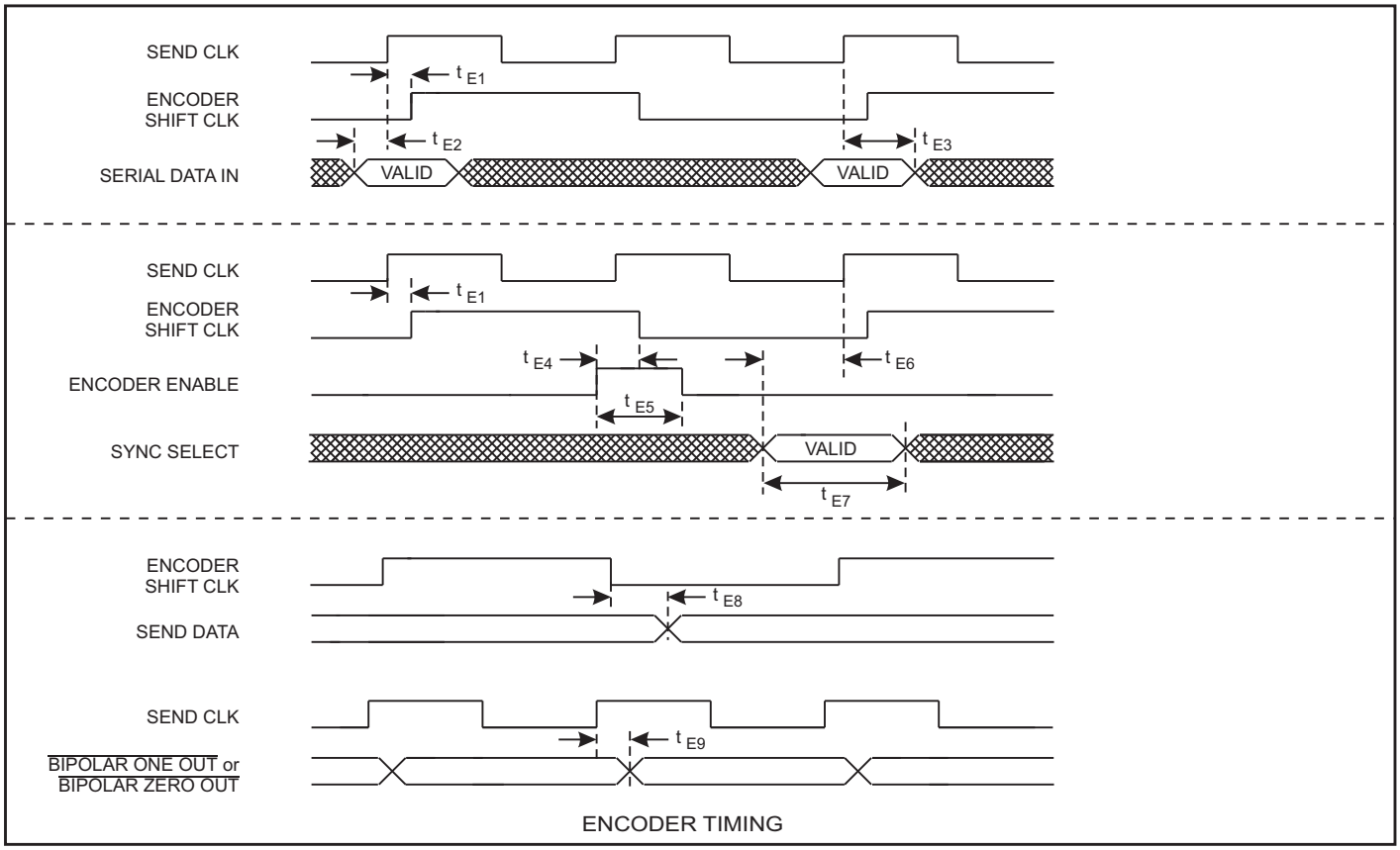
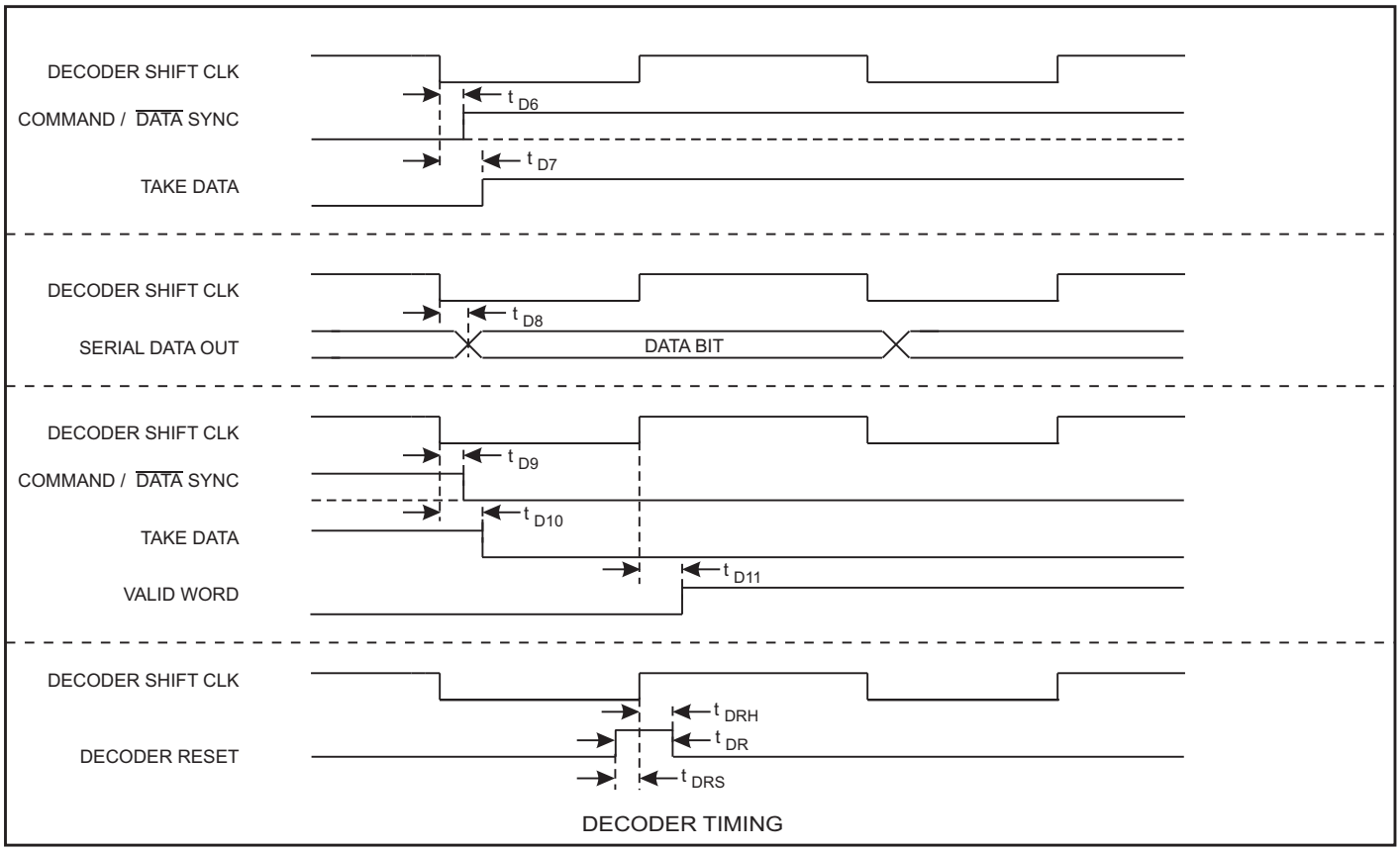



FIGURE 4. DECODER OPERATION

# TIMING DIAGRAMS

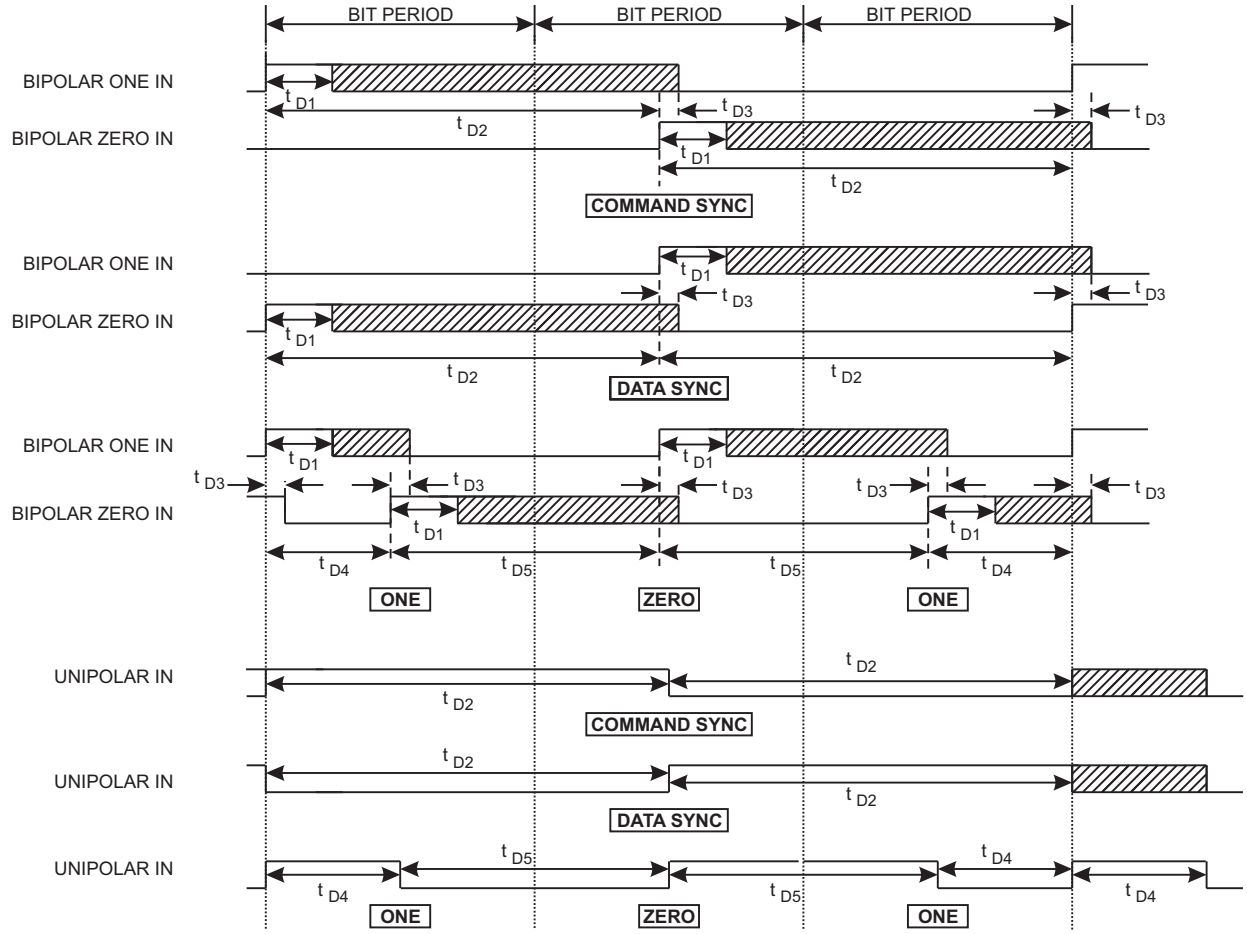



ENCODER TIMING

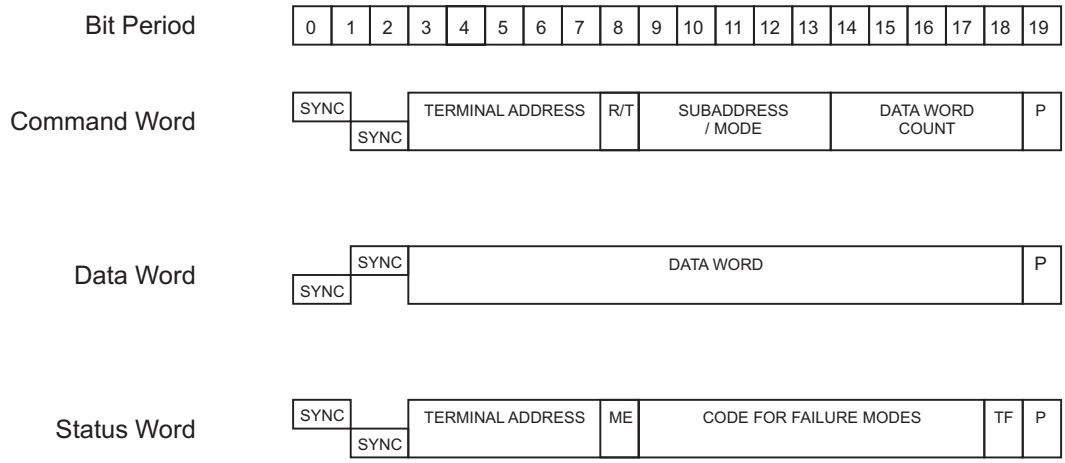



DECODER TIMING

# TIMING DIAGRAMS (cont.)




DECODER TIMING




MIL-STD-1553 WORD FORMATS

# ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage $V_{DD}$ . . . . . -0.3V to +7V | Power Dissipation at 25°C<br>Plastic SSOP . . . . . 1.5 W, derate10mW/°C<br>Ceramic DIP . . . . . 1.0 W, derate 7mW/°C |
| Voltage at any pin . . . . . -0.3V to Vcc +0.3V | DC Current Drain per pin . . . . . ±10mA |
| Operating Temperature Range:<br>Industrial . . . . . -40°C to +85°C<br>Hi-Temp . . . . . -55°C to +125°C | Storage Temperature Range: . . . . . -65°C to +150°C |

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# DC ELECTRICAL CHARACTERISTICS

$V_{DD}$ = 3.0 V to 5.5 V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

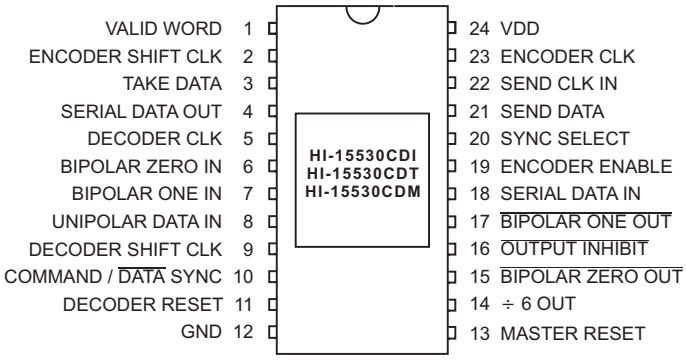
| PARAMETER | | SYMBOL | CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| Input Voltage | Input Voltage HI<br>Input Voltage LO | $V_{IH}$<br>$V_{IL}$ | | 70% $V_{DD}$ | | <br>30% $V_{DD}$ | V<br>V |
| Clock Input Voltage | Input Voltage HI<br>Input Voltage LO | $V_{IHC}$<br>$V_{ILC}$ | | $V_{DD}$-0.5 | | <br>0.5V | V<br>V |
| Input Leakage Current | Input Sink<br>Input Source | $I_{IH}$<br>$I_{IL}$ | | <br>-1.0 | | 1.0 | µA<br>µA |
| Output Voltage | Logic “1” Output Voltage | $V_{OH1}$<br>$V_{OH2}$ | $V_{DD}$=5V±10%, $I_{OH}$=-3mA<br>$V_{DD}$=3.3V±10%, $I_{OH}$=-1mA | 2.4<br>90% $V_{DD}$ | | | V<br>V |
| | Logic “0” Output Voltage | $V_{OL1}$<br>$V_{OL2}$ | $V_{DD}$=5V±10%, $I_{OL}$=1.8mA<br>$V_{DD}$=3.3V±10%, $I_{OH}$=1mA | | | 0.4<br>10% $V_{DD}$ | V<br>V |
| Standby Supply Current | | $I_{DDSB}$ | $V_{IN}$=$V_{DD}$, Outputs Open | | | 2.0 | mA |
| Operating Supply Current | | $I_{DD}$ | f=1MHz, Outputs Open | | | 10.0 | mA |
| Input Capacitance | | $C_{IN}$ | | | | 7.0 | pF |
| Output Capacitance | | $C_{OUT}$ | | | | 10.0 | pF |

# AC ELECTRICAL CHARACTERISTICS

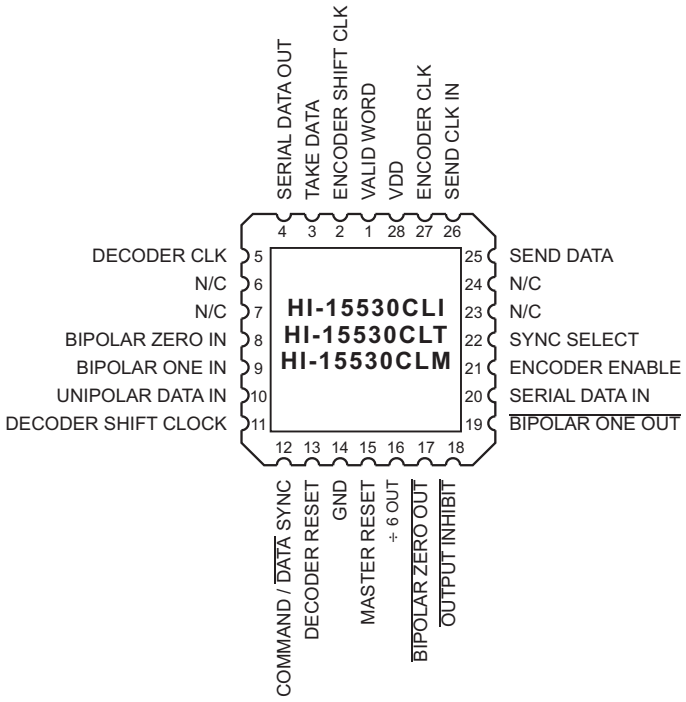
VDD = 3.0V to 5.5V, GND = 0V, TA = Operating Temperature Range, CL=50pF

| PARAMETER | SYMBOL | LIMITS | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **Encoder Timing** | | | | | |
| Encoder Clock Frequency | fEC | 0 | | 15 | MHz |
| Send Clock Frequency | fESC | 0 | | 2.5 | MHz |
| Encoder Clock Rise Time | tECR | | | 8 | ns |
| Encoder Clock Fall Time | tECF | | | 8 | ns |
| Encoder Data Rate | fED | 0 | | 1.25 | MHz |
| Master Reset Pulse Width | tMR | 150 | | | ns |
| Shift Clock Delay | tE1 | | | 125 | ns |
| Serial Data Setup Time | tE2 | 75 | | | ns |
| Serial Data Hold Time | tE3 | 75 | | | ns |
| Enable Setup Time | tE4 | 90 | | | ns |
| Enable Pulse Width | tE5 | 80 | | | ns |
| Sync Setup Time | tE6 | 55 | | | ns |
| Sync Pulse Width | tE7 | 150 | | | ns |
| Send Data Delay | tE8 | 0 | | 50 | ns |
| Bipolar Output Delay | tE9 | | | 130 | ns |
| Enable Hold Time | tE10 | 10 | | | ns |
| Sync Hold Time | tE11 | 95 | | | ns |
| **Decoder Timing** | | | | | |
| Decoder Clock Frequency | fDC | 0 | | 15 | MHz |
| Decoder Clock Rise Time | tDCR | | | 8 | ns |
| Decoder Clock Fall Time | tDCF | | | 8 | ns |
| Decoder Data Rate | fDD | 0 | | 1.25 | MHz |
| Decoder Reset Pulse Width | tDR | 150 | | | ns |
| Decoder Reset Setup Time | tDRS | 75 | | | ns |
| Decoder Reset Hold Time | tDRH | 10 | | | ns |
| Master Reset Pulse Width | tMR | 150 | | | ns |
| Bipolar Data Pulse Width | tD1 | tDC+10 | | | ns |
| Sync Transition Span | tD2 | | 18tDC | | ns |
| One-Zero Overlap | tD3 | | | tDC-10 | ns |
| Short Data Transition Span | tD4 | | 6tDC | | ns |
| Long Data Transition Span | tD5 | | 12tDC | | ns |
| Sync Delay (On) | tD6 | -20 | | 110 | ns |
| Take Data Delay (On) | tD7 | 0 | | 110 | ns |
| Serial Data Out Delay | tD8 | | | 80 | ns |
| Sync Delay (Off) | tD9 | 0 | | 110 | ns |
| Take Data Delay (Off) | tD10 | 0 | | 110 | ns |
| Valid Word Delay | tD11 | 0 | | 110 | ns |

# ADDITIONAL PIN CONFIGURATIONS (See data sheet page 1 for 24-Pin Small Outline SSOP)




**24 - Pin Ceramic Side-Brazed DIP**




**28 - Pin Ceramic LCC**

# ORDERING INFORMATION

**HI - 15530PS x x (Plastic)**

| PART NUMBER | LEAD FINISH |
|---|---|
| Blank | Tin / Lead (Sn / Pb) Solder |
| F | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|---|---|---|---|
| I | -40°C TO +85°C | I | No |
| T | -55°C TO +125°C | T | No |
| M | -55°C TO +125°C | M | Yes |

| PART NUMBER | PACKAGE DESCRIPTION |
|---|---|
| 15530PS | 24 PIN PLASTIC SSOP (24HS) |

See next page for Ceramic package style Ordering Information

# ORDERING INFORMATION (cont.)

## HI - 15530Cx x (Ceramic)

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN | LEAD FINISH |
|---|---|---|---|---|
| I | -40°C TO +85°C | I | No | Gold (Pb-free, RoHS compliant) |
| T | -55°C TO +125°C | T | No | Gold (Pb-free, RoHS compliant) |
| M | -55°C TO +125°C | M | Yes | Tin / Lead (Sn / Pb) Solder |

| PART NUMBER | PACKAGE DESCRIPTION |
|---|---|
| 15530CD | 24 PIN CERAMIC SIDE BRAZED DIP (24C) |
| 15530CL | 28 PIN CERAMIC LEADLESS CHIP CARRIER (28S) |

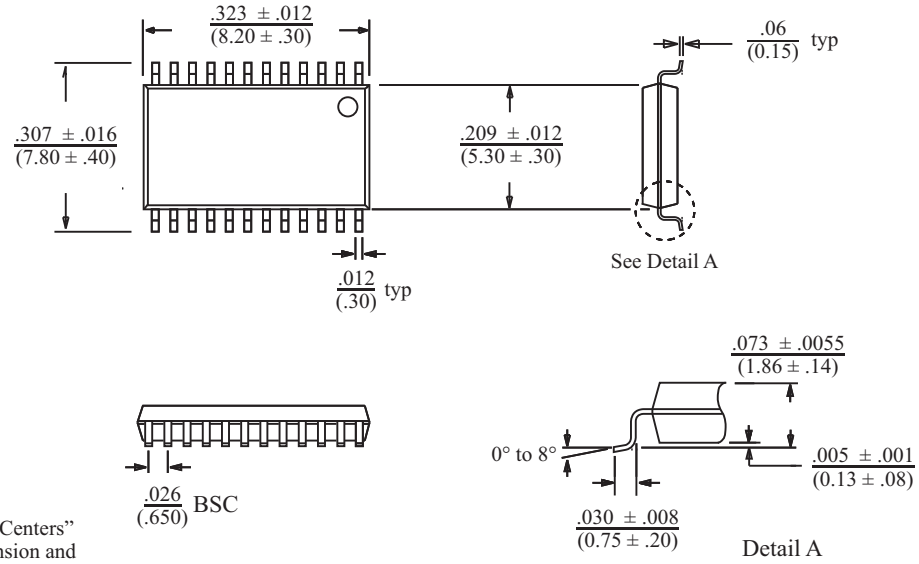
# REVISION HISTORY

| Revision | Date | Description of Change |
|---|---|---|
| DS15530, Rev. J | 10/16/08 | Corrected package height in Package Dimension drawing for 24-pin ceramic side-brazed DIP and clarified temperature ranges. |

## 24-PIN PLASTIC SSOP

*inches (millimeters)*

Package Type: 24HS

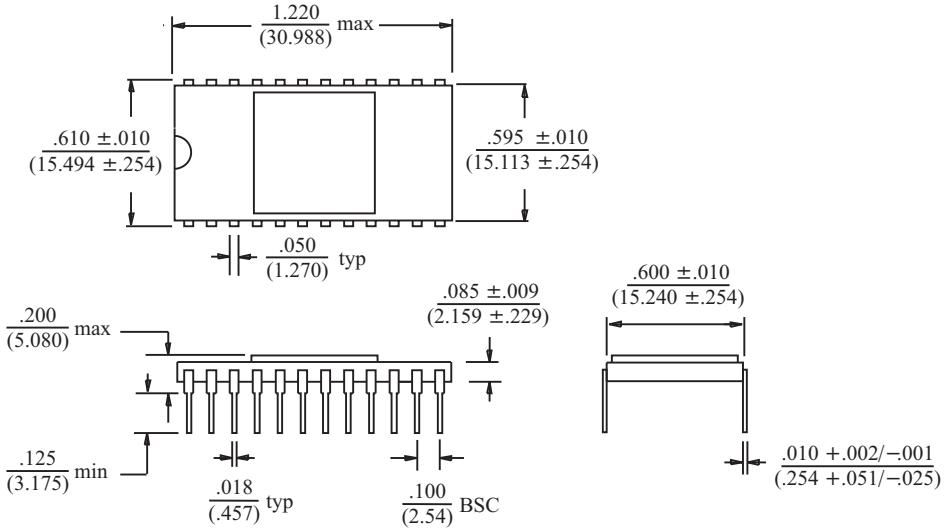



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

## 24-PIN CERAMIC SIDE-BRAZED DIP

*inches (millimeters)*

Package Type: 24C

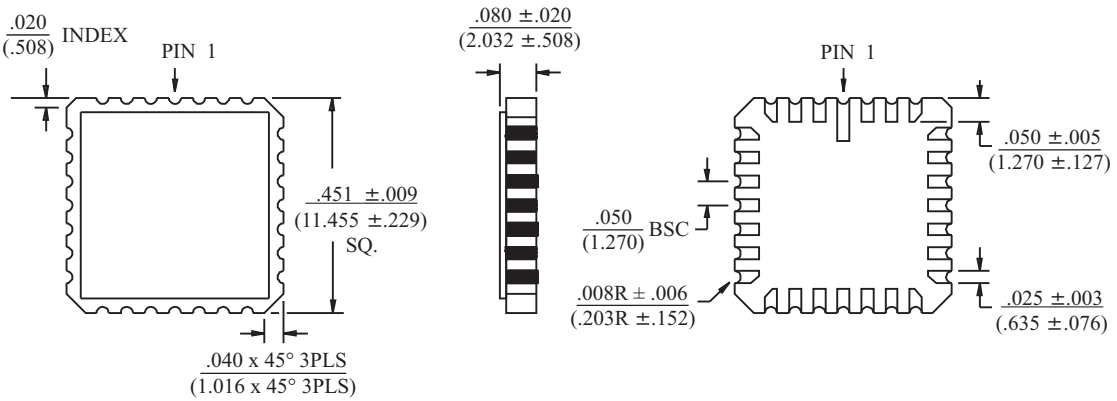



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

## 28-PIN CERAMIC LEADLESS CHIP CARRIER

*inches (millimeters)*

Package Type: 28S

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