Functional Description

The AT&T High-Speed Modem HSM Complete Modem Chip Sets consist of a ROM-coded AT&T DSP16A Digital Signal Processor, a AT&T V.32 Interface Device, an AT&T T7525 or CSP1027 Linear Codec, and a AT&T BMC microcontroller. See Figure 1.

AT&T DSP16A Digital Signal Processor

A ROM-coded AT&T DSP16A Digital Signal Processor performs the signal processing and control functions needed to implement the following signal modulations: V.32terbo, V.32bis, V.32, V.22bis, V.22, V.21, V.23, and Bell 212A and 103. It also implements Group 3 FAX modulations: V.17, V.29, V.27ter, and V.21 ch. 2.

AT&T Linear Codecs

The AT&T T7525 Linear Codec comes in a 28-pin SOJ package. It is the analog front-end of the data pump and incorporates sigma-delta technology.

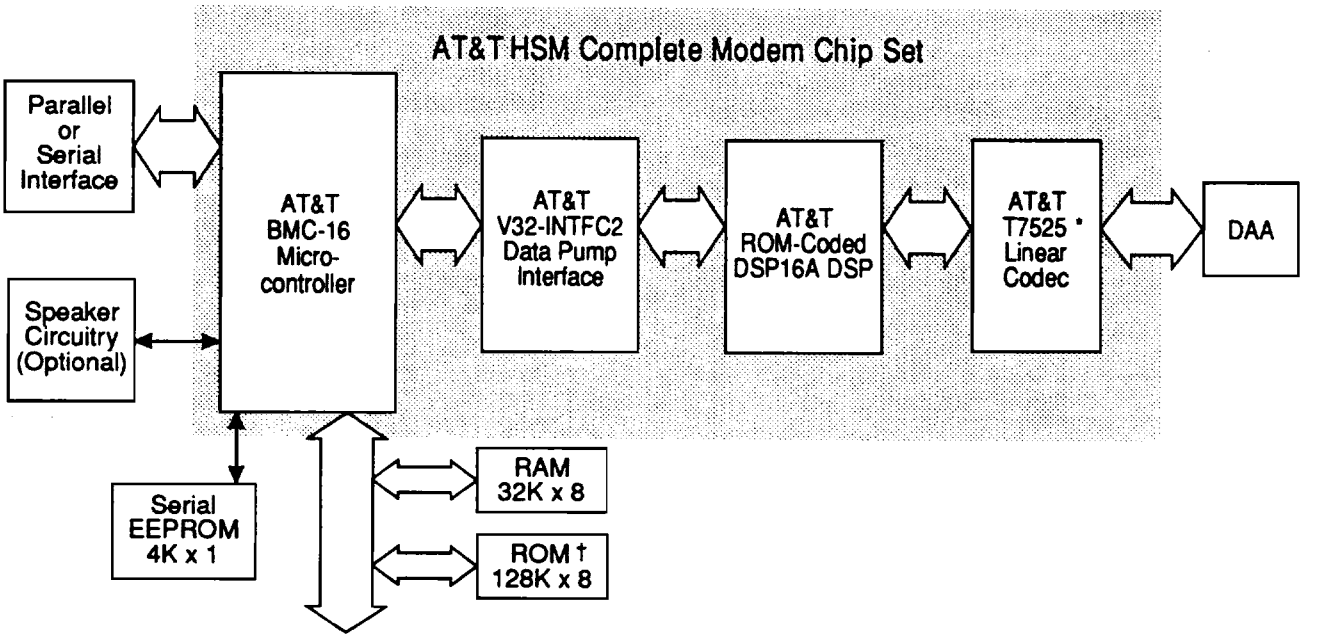
The AT&T CSP1027 Linear Codec comes in a 48-pin TQFP or a 44-pin QFP package. It is the analog front-end of the data pump and incorporates sigma-delta technology. The AT&T CSP1027 is a completely static device, resulting in lower power consumption. This codec provides two internal op amps so that no external op amps are required for the hybrid circuit.

AT&T V.32 Interface2 Device

The AT&T V32-INTFC2 device provides the V.24, eye pattern, and line interfaces. The AT&T V32-INTFC2 device also performs the clock generation.

AT&T BMC Micro Controller

The AT&T BMC microcontroller is an integrated 8-bit microcontroller, enhanced SCC, 550 UART emulation, low-power manager. The BMC connects to the data pump via dedicated lines and an external bus. The external bus also connects to an OEM-supplied ROM and RAM (see below).



* The AT&T T7525 Codec is replaced with a AT&T CSP1027 Codec in the PCMCIA version.

† 256K x 8 of ROM is required for the Data/FAX/Voice and Data/FAX/Cell feature sets.

Figure 1. AT&T HSM Complete Modem Chip Set Block Diagram

Functional Description (continued)

ROM and RAM Requirements
The BMC firmware performs the processing of general modem control, AT command set, error correction, data compression, host interface, low power management, and external memory interface functions. The firmware is provided by AT&T in object code for the OEM to program into external ROM. Data/FAX Features described in this document require 128K x 8 ROM and 32K x 8 RAM. Data/FAX/Voice Features and Data/FAX/Cell Features described in this document require 256K x 8 ROM and 32K x 8 RAM.

Serial EEPROM

A 4K x 1-bit serial EEPROM must be used for nonvolatile storage. The EEPROM may be used to store two user-selectable configurations.

Parallel or Serial Interface

The HSM interface provides a V.24 (RS-232-D) compatible serial interface to the DTE. This V.24 interface is also multiplexed with a 550 UART emulation interface for PC parallel bus applications. These pins are CMOS logic levels.

Speaker Interface

The AT&T HSM Complete Modem Chip Set supplies two speaker output signals: SPKRH and SPKRL (refer to schematics). These signals control the speaker as follows:

Volume	SPKRH	SPKRL
Off	Low	Low
Low	Low	High
Medium	High	Low
High	High	High

Environmental Requirements

Parameter	Value
Operating Temperature	0 °C to 70 °C
Storage Temperature	–25 °C to +70 °C

User Information

AT Commands

A summary of the commands implemented by the modem are shown in Table 2. Commands may be executed when the modem is in COMMAND mode. COMMAND mode is entered upon one of the following conditions:

- After powerup.
- At the termination of a connection.
- After the execution of a command other than dial or answer commands.
- Upon the receipt of the ESCAPE SEQUENCE (three contiguous characters matching the contents of S register 2) while on-line mode.
- Upon the on-to-off transition of DTR if &D1, &D2, or &D3 has been set.
- Upon the receipt of a break from the DTE if \K0, \K2, or \K4 has been set.
- Upon the receipt of a break-escape if % O2 or % O3 has been set.

Table 1. Complete Chip Set Power Dissipation (Active Typical)

Device	DeskTop	LapTop			PCMCIA			Units
	Active	Active	Idle	Sleep	Active	Idle	Sleep	
DSP16A DSP	565	270	0	0	270	0	0	mW
V32-INTFC2	260	120	0	0	120	0	0	mW
Linear Codec	125	60	0	0	72	0	0	mW
BMC Controller	180	250	25	.05	250	25	.05	mW
Total:	1120	700	25	.05	712	25	.05	mW

User Information (continued)

Table 2. AT Command Set Summary

Command	Description	Command	Description
A/	Repeat last command	&Un	Disable trellis coding
A	Answer command	&Vn	View active configuration/user profiles/telephone numbers
Bn	Communication standard	&Wn	Store active configuration
Cn	Carrier control option	&Xn	Synch transmit clock source option
D	Dial command	&Yn	Select stored profile on powerup
En	Off-line echo command	&Zn=x	Store telephone number
Fn	On-line echo command	%An	Set autoreliable fallback character
Hn	Switchhook control	%Cn	Data compression
In	ID/checksum option	%D	V.25 bis operating mode
Ln	Speaker volume	%En	Autoretrain
Mn	Speaker control	%Fn	V.25 bis character framing
Nn	Select negotiate handshake	%Gn	Auto fall forward/fallback enable
On	Go on-line	%On	Escape method
P	Enable pulse dialing	%Vn	Switch to V.25 bis
Qn	Result code display option	\ An	Block size
Sn	Select an S register	\ Bn	Transmit break
Sn=	Write to an S register	\Cn	Set autoreliable buffer
Sn?	Read an S register	\Gn	Select serial port flow control
T	Enable tone dialing	\Jn	Bits/s rate adjust
Vn	Result code form	\Kn	Set break control
Wn	Select extended result code	\Ln	Block *MNP* link
Xn	Result codes/call progress options	\Nn	Set operating mode
n	Long-space disconnect	\Qn	Set serial port flow control
Zn	Reset and recall stored profile	\Tn	Set inactivity timer
&Bn	V.32 autoretrain	\Vn	Modify result code form
&Cn	DCD option	\Xn	Set XON/XOFF pass through
&Dn	DTR option	–Cn	Set calling tone in data mode
&Fn	Load factory settings	–Jn	Set V.42 detect phase
&Gn	Guard tone option	–Kn	*MNP* extended services
&Kn	Select serial port flow control	–Qn	Fallback modulation speeds (*MNP* 10)
&Ln	Dial up/leased line option	–V	Display version
&Mn	Communications mode option	"Hn	V.42 bis compression control
&Pn	Dial pulse ratio	"Mn	*MNP* 10 control
&Qn	Communications mode option	"No	V.42 bis dictionary size
&Rn	RTS/CTS option	*H	Starting line speed for *MNP*10
&Sn	DSR option	)M	Set adjustable transmit level for *MNP* 10
&Tn	Self-test commands		

User Information (continued)

Table 3. FAX Commands Table

Command/ Response	Description	Command/ Response	Description
+FCLASS	Service class selection	+FMDL	Request model identification
+FTS	Stop transmission and pause	+FMFR	Manufacturer identification
+FRS	Wait for silence	+FREV	Request product revision identification
+FTM	FAX data transmit	+FMINSP	Minimum phase C speed
+FRM	FAX data receive	+FPHCTO	DTE phase C response time-out
+FTH	FAX HDLC frame transmit	+FRBC	Phase C receive data block size
+FRH	FAX HDLC frame receive	+FREL	Phase C received EOL alignment
+FCERROR	Reports error condition	+FSPL	Request to poll
+FAA	FAX autoanswer enable	+FTBC	Phase C transmit data block size
+FAXERR	T.30 session error report	+FCIG	Reports the remote ID
+FBADLIN	Bad line threshold	+FCFR	Indicate confirmation to receive
+BADMUL	Error threshold multiplier	+FCON	Facsimile connection response
+FBOR	Data bit order selection	+FCSI	Reports the remote ID
+FBUG	Session message reporting	+FDIS	Reports DIS frame information
+FCQ	Copy quality checking	+FDTC	Reports DTC frame information
+FCR	Capability to receive	+FET	Post page message response
+FCTCRTY	ECM retry count	+FHNG	Call termination with status
+FDCC	FAX capability parameters	+FHR	Report received HDLC frames
+FDCS	Current session results	+FHT	Report transmitted HDLC frames
+FDFFC	Data compression format conversion	+FNSC	Report received nonstandard neg. frames
+FDR	Begin or continue phase C receive data	+FNSF	Report received nonstandard neg. frames
+FDT	Begin phase C data transmission	+FNSS	Report received nonstandard neg. frames
+FECM	Error correction mode control	+FPOLL	Remote polling indication
+FK	Session termination	+FPTS	Receive/transmit page transfer status
+FLID	Local ID string	+FTSI	Report the remote ID
+FLNFC	Page length format conversion		

User Information (continued)

Table 4. VOICE Commands Table (Data/FAX/Voice Products Only)

Command	Description	Command	Description
#BDR	Select baud rate (turn off auto baud).	#VLS	Voice line select (GSM)
#CID	Enable Caller ID detection and select reporting format	#VRA	Ring back goes away timer (originate)
#CLS	Select data, FAX, or voice	#VRN	Ring back never came timer (originate)
#MDL?	Identify model	#VRX	Voice Receive Mode (GSM)
#MFR?	Identify manufacturer	#VSD	Silence deletion tuner (voice receive, GSM)
#REV?	Identify revision level	#VSK	Buffer skid setting
#VBQ?	Query buffer size	#VSP	Silence detect period (voice receive, GSM)
#VBS	Bits per sample (GSM) and compression type	#VSR	Sampling rate selection (GSM)
#VBT	Beep tone timer	#VSS	Silence sensitivity tuner
#VCI?	Identify compression method (GSM)	#VTD	DTMF/tone reporting capability
#VGR	Receiver gain selection	#VTS	Play tone string
#VGT	Transmit volume selection	#VTX	Voice transmit mode (GSM)

* These commands will be changed to conform IS-101 standard.

Table 5. V.25bis Command Set Summary (Data/FAX/Voice and Data/FAX/Cell Products Only)

Command	Description	Command	Description
CIC	Enable autoanswer	PRN	Store telephone number
CRN	Dial command	RLD	Display delayed numbers
CRS	Dial stored number	RLN	Display stored number
DIC	Disable autoanswer		

User Information (continued)

Table 6. S Register Command Summary

Reg.	Default	Description
0	000	Ring to autoanswer on
1	000	Ring count
2	043	Escape character
3	013	Carriage return <CR> character
4	010	Line feed <LF> character
5	008	Back space <BS> character
6	002	Wait before dialing
7	030*	Wait for carrier
8	002	Pause time for command or dial modifier
9	006	Carrier recovery time
10	014	Lost carrier hang up delay
11	095	DTMF dialing speed
12	050	Guard time
14	176	Bit mapped options
16	00H	Modem test options
18	000	Modem test timer
19	000	Hayes *AutoSync* bit mapped options
20	000	HDLC address or BSC sync character
21	048	Bit mapped options
22	118	Bit mapped options
23	015	Bit mapped options
25	005	Detect DTR change
26	001	RTS to CTS delay interval
27	064	Bit mapped options
30	000	Inactivity timer value
32	020	Wait for <CR> time
37	000	Desired DCE speed
95	000	Extended result code bit map
108	001	Signal quality selector
109	062‡	V.32/V.32bis/V.32terbo bis carrier speed selector
110	002†	V.32/V.32bis/V.32terbo selector
112	000	DTE speed select during data transfer

* 090 for 14.4 Data/Fax/Voice
† 003 for 19.2 Data/Fax
‡ 254 for 19.2 Data/Fax

User Information (continued)

Table 7. Result Code Summary

Numeric	Verbose	Description
0	OK	Command executed.
1	CONNECT	Connection at any speed if X0 selected; otherwise, connection at 0—300 bits/s.
2	RING	Ring signal detected.
3	NO CARRIER	Carrier signal not detected or lost.
4	ERROR	Invalid command, checksum, error in command line, or command line too long.
5	CONNECT 1200	Connection at 1200 bits/s. Disabled by X0.
6	NO DIALTONE	No dial tone detected. Enabled by X2, X4, or W dial modifier.
7	BUSY	Busy detected. Enabled by X3 or X4.
8	NO ANSWER	No silence detected when dialing a system not providing a dial tone. Enabled by @ dial modifier.
10	CONNECT 2400	Connection at 2400 bits/s.
11	CONNECT 4800	Connection at 4800 bits/s.
12	CONNECT 9600	Connection at 9600 bits/s.
13	CONNECT 14400	Connection at 14400 bits/s.
14	CONNECT 19200	Connection at 19200 bits/s. Enabled by W0.
15	CONNECT 16800	Connection at 16800 bits/s
18	CONNECT 57600	Connection at 57600 bits/s. Enabled by W0.
24	CONNECT 7200	Connection at 7200 bits/s.
25	CONNECT 12000	Connection at 12000 bits/s.
26	CONNECT 1200/75	Connection at 1200 bits/s/75 bits/s.
27	CONNECT 75/1200	Connection at 75 bits/s/ 200 bits/s.
28	CONNECT 38400	Connection at 38400 bits/s.
31	CONNECT 115200	Connection at 115.2 Kbits/s

User Information (continued)

Table 8. **Negotiation Progress Messages** (Displayed when W1 is set.)

Numeric	Verbose	Description
40	CARRIER 300	Carrier detected at 300 bits/s.
42	CARRIER 75/1200	Carrier detected at 75 bits/s/1200 bits/s.
43	CARRIER 1200/75	Carrier detected at 1200 bits/s/75 bits/s.
46	CARRIER 1200	Carrier detected at 1200 bits/s.
47	CARRIER 2400	Carrier detected at 2400 bits/s.
48	CARRIER 4800	Carrier detected at 4800 bits/s.
49	CARRIER 7200	Carrier detected at 7200 bits/s.
50	CARRIER 9600	Carrier detected at 9600 bits/s.
51	CARRIER 12000	Carrier detected at 12000 bits/s.
52	CARRIER 14400	Carrier detected at 14400 bits/s.
53	CARRIER 16800	Carrier detected at 16800 bits/s.
54	CARRIER 19200	Carrier detected at 19200 bits/s.
66	COMPRESSION: *MNP* 5	*MNP* compression negotiated. †
67	COMPRESSION: V.42BIS	V.42bis compression negotiated. †
69	COMPRESSION: NONE	No compression negotiated. †
70	PROTOCOL: NONE	Asynchronous mode. *
77	PROTOCOL: LAP-M	V.42 LAPM. *
80	PROTOCOL: *MNP*	*MNP* negotiated. *
81	PROTOCOL: *MNP* 2	*MNP* Class 2 negotiated. *
82	PROTOCOL: *MNP* 3	*MNP* Class 3 negotiated. *
83	PROTOCOL: *MNP* 2, 4	*MNP* Class 2 and 4 negotiated. *
84	PROTOCOL: *MNP* 3, 4	*MNP* Class 3 and 4 negotiated. *
85	PROTOCOL: *MNP* 2, 10	*MNP* Class 2 and 10 negotiated. *
86	PROTOCOL: *MNP* 3, 10	*MNP* Class 3 and 10 negotiated. *
87	PROTOCOL: *MNP* 2, 4, 10	*MNP* Class 2, 4, and 10 negotiated. *
88	PROTOCOL: *MNP* 3, 4, 10	*MNP* Class 3, 4, and 10 negotiated. *

* These codes are enabled by setting bit 6 of S register 95.
† These codes are enabled by setting bit 5 of S register 95.

User Information (continued)

Autobaud Operation

When the modem enters COMMAND mode, the autobaud operation is enabled. While autobaud is operating, the modem searches for the A or a which begins an AT command sequence. It determines the data rate from this character and tests the next character received to see if it is a T or t. If the AT or at sequence is detected, parity and bit lengths are determined from the two, and the remainder of the command line is parsed after a carriage return is detected. If the command buffer overflows, or if a parity or framing error is detected, autobaud operation will resume.

The modem will autobaud to speeds of 300, 600, 1200, 2400, 4800, 7200, 9600, 14400, 19200, 38400, and 57600 bits/s. The following character formats are valid:

Data Bits	Parity	Stop Bits
7	N	2
7	O	1
7	E	1
8	N	1

Establishing Modem Connections

Connection Speeds

The supported data modem to modem connection modes/speeds and FAX modem to modem connection modes/speeds are listed in Table 9.

Table 9. Supported Data and FAX Modes

Data Modes	Data Rate (bits/s)
V.32terbo	19200
	16800
V.32bis	14400
	12000
	7200
V.32	9600
	4800
V.22bis	2400
V.22	1200
V21	300
V.23	1200/75
Bell 212A	1200
Bell 103	300

FAX Modes	Data Rate (bits/s)
V.17	14400
	12000
	9600
	7200
V.29	9600
	7200
V.27ter	4800
	2400
V.21 ch 2	300

Dial Tone Detection

The detection frequency range is from 340 Hz to 640 Hz, and the detection level is greater than or equal to –43 dBm.

User Information (continued)

Blind Dialing

Blind dialing allows the modem to not detect dial tone prior to dialing. The modem can be configured to dial from 2 seconds to 255 seconds after going off-hook by changing the value in S-register 6. The default time, as well as minimum time, is 2 seconds. The mode is enabled by ATX1, X0, or X3.

Pulse Dialing

The ATDP command designates that subsequent dialing operations will use pulse dialing. The modem pulse dials at 8—11 pulses/s. AT&P0 selects the default make/break ratio of 39% make to 61% break. AT&P1 selects an alternate ratio of 33% make to 67% break required in some countries.

DTMF Dialing

Table 10 lists the DTMF tone pairs used for tone dialing. All tones are generated within ±1.5%, conforming to Bell System Communications Technical Reference Publication 47001 dated August 1976.

Table 10. DTMF Tones

		High Frequency (Hz)			
		1209	1336	1477	1633
Low Frequency (Hz)	697	1	2	3	A
	770	4	5	6	B
	852	7	8	9	C
	941	*	0	#	D

Ring Detection

A ring signal between 15 Hz and 68 Hz will be detected.

Call Progress

Frequency: 340 Hz—640 Hz
Level: On > –43 dBm
Busy Timing: 500 ms ± 10% (2 cycles) = Normal busy

Reference: Bell System Technical Reference PUB 61100.

Answer Tone Detection

The answer tone detection range for V.32terbo, V.32bis, V.32, V.22bis, V.22, V.21, and V.23 is 2100 Hz ± 40 Hz. The detection range for Bell 212A and 103 is 2225 Hz ± 40 Hz. The detection level for both CCITT and Bell answer tones is greater than or equal to –43 dBm.

Billing Protection

The answering modem must remain silent for a period of time to allow the network administration to send billing information between central offices. After going off-hook, the modem must wait at least 2 seconds before sending answer tone.

User Information (continued)

Automode

Automode from V.32terbo to V.22bis is implemented according to V.32 annex A (11/22/90), and automode to V.21, Bell 103, and Bell 212A is implemented according to the EIA/TIA draft standard from subcommittee TR-30.1.

Modem Handshaking Protocol

The calling modem aborts the call if it does not detect carrier after the time period defined in S register 7. The default time is 30 seconds for the data/FAX chip set and 90 seconds for the 14.4 Data/Fax/Voice Chip Set.

Phone Number Dialing

The modem can dial numbers entered in the command buffer or dial stored numbers. When the **ATD** is detected in the command, the following characters in the command buffer are treated as digits or dial modifiers. The dial digits are 0—9, A, B, C, D, #, and *.

Dial Modifiers

P	Pulse dial (default).
T	Tone dial.
,	Pause for number of seconds in S register 8.
!	Hook-flash (on-hook for 1/2 second).
@	Wait for at least 1 ring followed by 5 seconds of silence.
W	Wait for dial tone for number of seconds in S register 7.
;	Return to COMMAND mode after dialing.
S=n	Dial stored number in Directory entry n.
R	Originate in answer mode (Go to answer mode after dialing).

Stored Numbers

The **AT&Z*n*=*x*** command sets the contents of directory entry ***n***, which can be 0 through 3, to be the dial string ***x***. Up to 36 characters can be stored in a directory entry. The only dial modifier which cannot be stored is **S**.

Answering

The modem will answer an incoming call when the ring counter (S register 1) equals the ring to answer on (S register 0), unless S register 0 = 0 or unless DTR is required and is not true. The **AT&Dn** commands govern the use of DTR. **AT&D2** causes the modem to disable autoanswer on an on-to-off transition of DTR—and to re-enable autoanswer on an off-to-on transition of DTR. The other **AT&Dn** commands cause DTR to not affect the autoanswer function. The modem may also be caused to answer manually with the **ATA** command.

Stored Profiles

After the user has set up the modem for a particular configuration, that configuration may be stored as one of two user profiles which can be recalled at any time. The **AT&W*n*** command will store the current modem configuration as user profile ***n***, where n can be 0 or 1. Either profile can be recalled at any time with the **ATZ*n*** command. Likewise, either profile can be designated to be the default configuration at powerup with the **AT&Y*n*** command. The **AT&V** command displays the active configuration and both stored profiles. The factory configuration can be made the active configuration with the **AT&F** command.

User Information (continued)

Data Mode

Flow Control

The modem provides the ability for the data terminal or computer port to pause the flow of data from the modem and for the modem to pause the flow of data from the data terminal or computer port. Flow control is required when a DTE or the modem cannot handle data as fast as it is received. Two types of flow control are provided: EIA flow control (RTS-CTS) and XON/XOFF flow control.

Escape Sequence Detection

S register 2 contains the decimal representation of the ASCII character used to enter COMMAND mode. The factory default is a decimal 043, the plus (+) character. A value of 128 or greater disables the escape function.

Break Detection

The modem detects a BREAK signal from either the DTE or the remote modem. The following table summarizes the modem's response to a received BREAK signal depending on the **AT\K** command. The default value is \K5.

(In connect state, if reliable mode or normal mode, then transmit break to remote)

0, 2, 4: Enter command state but do not send a break
1: Destructive/Expedited.
3: Nondestructive/Expedited.
5: Nondestructive/Nonexpedited.

(In command state and transmit break command issued, if reliable mode or normal mode, then transmit break to remote)

0, 1: Destructive/Expedited.
2, 3: Nondestructive/Expedited.
4, 5: Nondestructive/Nonexpedited.

(In connect state, if direct mode, then receive break at serial port)

0, 2, 4: Immediately send break and enter command state.
1, 3, 5: Immediately send break through.

(In connect state, if normal mode, receive break at modem port, send to serial port)

0, 1: Destructive/Expedited.
2, 3: Nondestructive/Expedited.
4, 5: Nondestructive/Nonexpedited.

Telephone Line Monitoring

Loss of Carrier

S register 10 specifies the amount of time (0 to 255 in 1 tenth of a second increments) needed to recognize the loss of carrier. The default value of S10 is 14, or 1.4 seconds.

Long-Space Disconnect

The **ATYn** command allows the user to control the operation of long-space disconnect. When enabled, the modem will terminate the connection if it receives a break 1.6 seconds in length, and will send a break four seconds in length prior to any controlled disconnect.

User Information (continued)

Error Control

At 1200 bits/s—14400 bits/s (1200—19,200 bits/s for the 19.2 Data/FAX and 1200—9600 for the 9.6 Data/Fax), the modem operates in full compliance with CCITT V.42, the international standard for point-to-point modem error control. Link access procedure for modems, more commonly referred to as LAPM, is the primary protocol, and annex A, the alternate protocol, provides backward compatibility with *MNP* (Microcom Network Protocol) Classes 2 through 4. *MNP* and V.42 selections are performed via the \N commands. *MNP* or V.42 negotiation, if enabled, is automatic when a call is placed or received. The communicating modems will arrive at the highest class of *MNP* supported by both before data transmission begins.

V.42 Appendix III

All AT&T HSM Complete Chip Sets support Appendix III to recommendation V.42 (III.1 through III.5) for additional information for implementers of V.42 regarding robustness of operation. Appendix III permits modifications of the detection phase and LAPM protocol which may improve performance under some channel conditions. The following implementations are supported:

Appendix III.1 — Transmission of the answerer detection pattern
Appendix III.2 — Value of parameter N400 (maximum number of retransmissions)
Appendix III.3 — Incomplete XID Exchange
Appendix III.4 — Selective Retransmission
Appendix III.5 — Rejection on detection of errored frames

A more detailed description can be found in the CCITT recommendation V.42 Appendix III.

MNP 10

The HSM 14.4 data/FAX/cell chip set supports Microcom Networking Protocol 10 or *MNP* 10. *MNP* 10 utilizes various techniques to improve the performance for impaired cellular connections. The following features are supported by this chip set:

Robust Auto Reliable. Allows multiple attempts and to connect with error protection over adverse lines. Remains compatible with non-*MNP* 10 connections.

Negotiated Speed Upshift. Begins reliable negotiations at the lowest possible speed and immediately shifts to a higher speed if line conditions permit.

Aggressive Adaptive Packet Assembly. Improves under severely impaired line conditions such as cellular connections. Begins transmitting small data packets and increases packet size to the most efficient size.

Dynamic Speed Shift. Automatically adjusts the speed to the highest effective rate for a reliable connection. Continuously monitors line conditions and upshifts or downshifts speeds to maintain error-free transmission at the most effective level.

Dynamic Transmit Level Adjustment. Begins at –10 dBm and determines the most suitable transmit level by sampling management packets at various levels. Dynamically adjusts to the optimal transmit level.

Data Compression

The AT&T HSM Complete Chip Set supports CCITT V.42bis, the international standard for data compression which provides compression capabilities up to 4:1, for use by modems incorporating the V.42 LAPM error control standard. *MNP* Class 5 provides capabilities up to 2:1 compression. The "H3 command enables V.42bis data compression. The %C1 command enables *MNP* 5 data compression.

Programmable Inactivity Timer

The inactivity timer is the length of time the modem will wait before disconnecting when no data is sent or received. This timer is set using the \Tn command. It is programmable between 0 and 90 minutes. The default value is 0 (disabled).

User Information (continued)

V.25bis

The AT&T HSM 14.4 Data/FAX/Voice and 14.4 Data/FAX/Cell Complete Chip Set supports V.25bis. This recommendation specifies setting up a data connection over the GSTN where automatic calling and/or answering equipment interfaces to the DTE via the 100-series interchange circuits. This procedure is also known as serial automatic calling. For more detailed information, refer to the V.25bis recommendation. The V.25bis commands are shown on page 16.

GSM Speech Coder

GSM is a standardized method of voice compression which compresses a digitally sampled voice stream (8K samples/second at 8 bits/sample) at a 4.9 to 1 ratio while maintaining toll quality voice. The GSM data rate is 13 Kbits/s. This method is implemented by the AT&T DSP16A (ME-ROM code).

AT Voice Command Set

The HSM 14.4 Data/FAX/voice supports TIA-2986, now approved and known as TIA Interim Standards IS-101. Please refer to pages 92—97 for detailed information an the AT voice command set.

Modem Testing

The following tests are available for testing the local modem and for testing of a remote modem:

Analog Loopback Tests

These tests verify the operation of a local modem without use of a telephone line or a remote modem.

Local Analog Loopback. These tests take characters from the local terminal and send them from the modem transmitter to the modem receiver, where they are echoed back to the terminal. The two tests are identical, except that AT&T1O tests the low-frequency channel of the modem and AT&T1A tests the high-frequency channel. Start the test with AT&T1O or AT&T1A. Type a few lines to test if the data echoes back correctly. Return to COMMAND mode via the escape sequence. Issue the AT&T0 command to stop the test.

Local Analog Loopback with Self-Test. Set the test timer to a number of seconds (1—255) to run the test. Start the test with AT&T8. The modem will generate a test pattern to its own receiver and verify its reception. At the end of the test, a number between 0 and 255 will be displayed, indicating the numbers of errors during the test.

Digital Loopback Tests

These tests verify a local or remote modem's operation. By default, the modem will allow loopback tests ordered by a remote modem. This feature can be enabled and disabled by the user. The AT&T5 command will cause the modem to deny remote digital loopback (RDL) requests from the remote modem. The AT&T4 command will cause the modem to grant RDL requests from the remote modem.

Remote Digital Loopback (RDL). This test commands the remote modem to send back all of the data it receives. Initiate a connection with the remote modem, then enter COMMAND mode and issue the AT&T6 command. The data typed should echo back without error. Enter COMMAND mode and issue the AT&T0 command to end the test.

User Information (continued)

Remote Digital Loopback with Self-Test. Set the test timer to a number of seconds (1—255) to run the test. Establish a connection with the remote modem, and start the test with AT&T7. The local modem will generate a test message and send it to the remote modem. The remote modem will send back the data it receives. The local modem will verify its reception. At the end of the test, a number between 0 and 255 will be displayed indicating the numbers of errors during the test.

Local Digital Loopback

This test causes the local modem to send back everything it receives from the remote modem. Establish a connection with the remote modem, then enter COMMAND mode and issue the AT&T3 command. The operator at the remote modem should type some data and verify that it echoes back properly. Enter COMMAND mode and issue AT&T0 to end the test.

Power Switching (Laptop and PCMCIA)

When the modem is on-hook and not processing a command, it will enter the SLEEP mode after 3 seconds. In this mode, the power consumption is approximately 50 µW. From SLEEP mode, ring indicator or any data from the computer will cause the modem to enter the IDLE state. This transition is transparent to the user. In the IDLE state, power consumption is approximately 25 mW. When the modem is off-hook or in TEST mode, the power consumption of the chip set is approximately 700 mW. During sleep mode, the address, data bus, $\overline{\text{ROMCS}}$, $\overline{\text{RAMCS}}$, $\overline{\text{IOCS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ are 3-Stated.

Autosync Operation

AT&Q4 selects *Autosync* mode. In this mode, the modem translates the asynchronous data from the computer port to BISYNC or SDLC (HDLC) NRZ on the communications link. NRZI is supported. Application software on the host computer must be able to support the modem in this mode. Three S registers are used in *Autosync* mode:

- S register 19 — bit mapped protocol S register:

Bit	Use
0	0 = BISYNC, 1 = SDLC
1	1 = SDLC Address Detect on
2	0 = NRZI, 1 = NRZ
3	0 = SDLC idle MARK, 1 = SDLC idle FLAG

- S register 20 in BISYNC mode contains the SYNC character. In SDLC mode, it contains the ADDRESS character if address detect is on.
- S register 25 contains the time in seconds that the modem will wait for DTR to come true after a connection has been made. This allows time for the computer to switch from async to *Autosync* mode.

Rate Negotiation (V.32terbo, V.32bis, and V.32 Modes Only)

Initial Rate Negotiation. The modems will negotiate the highest possible transmission rate based on line quality during the initial connection.

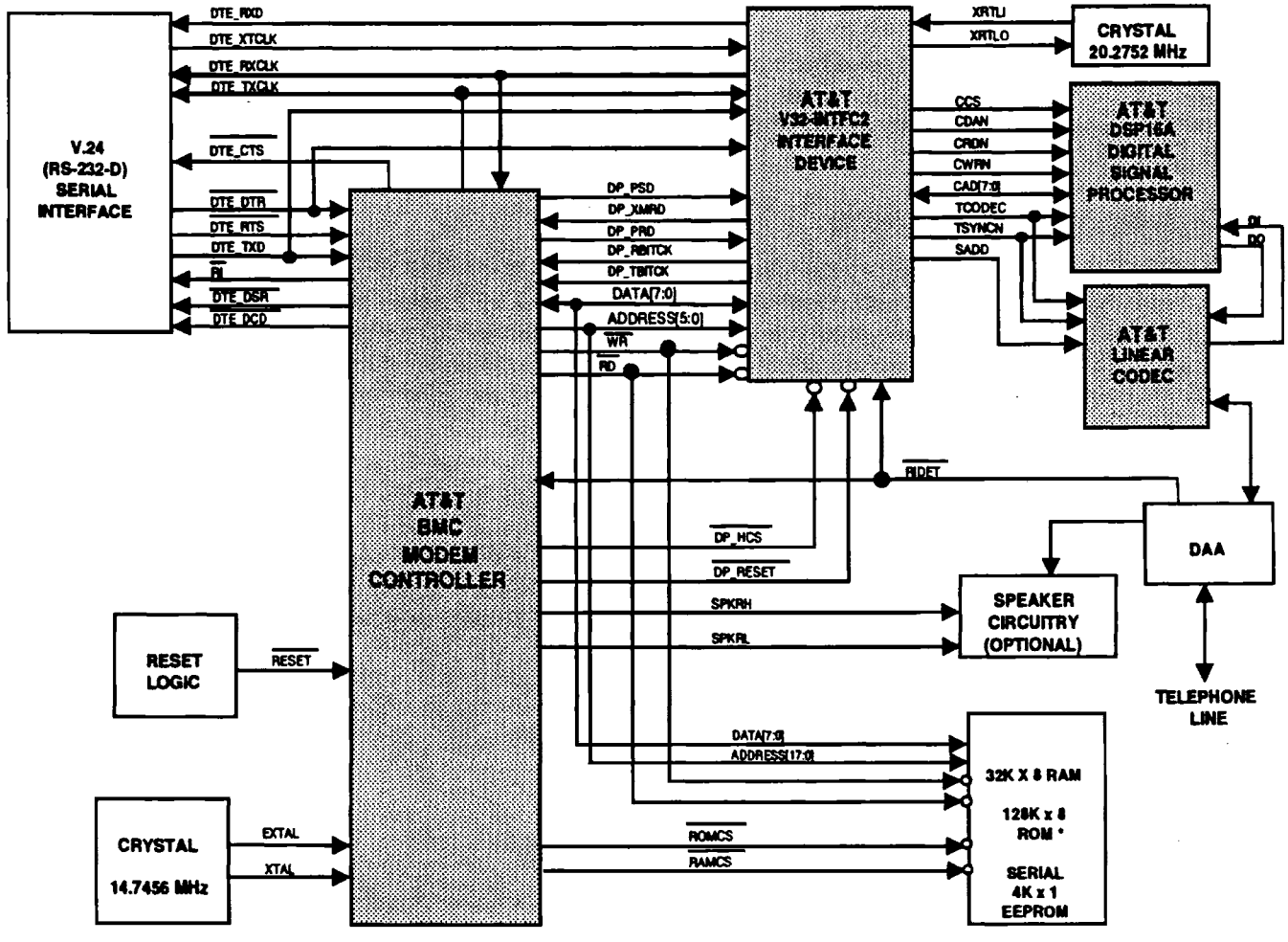
Automatic Fall-Back and Fall-Forward. The modem will fall back to a lower speed if line conditions deteriorate and fall forward to a higher speed if line conditions improve. The speed change is done with a fast rate change in V.32bis and V.32terbo mode and with a retrain in V.32 mode. The command AT%Gn is used to disable or enable this feature (see %Gn command description on page 77).

Manual Rate Change. The connection speed can be changed while on-line in V.32bis, and V.32terbo modes by using the command ATOn (see On command description on page 69).

Hardware Interface

Connection Diagrams

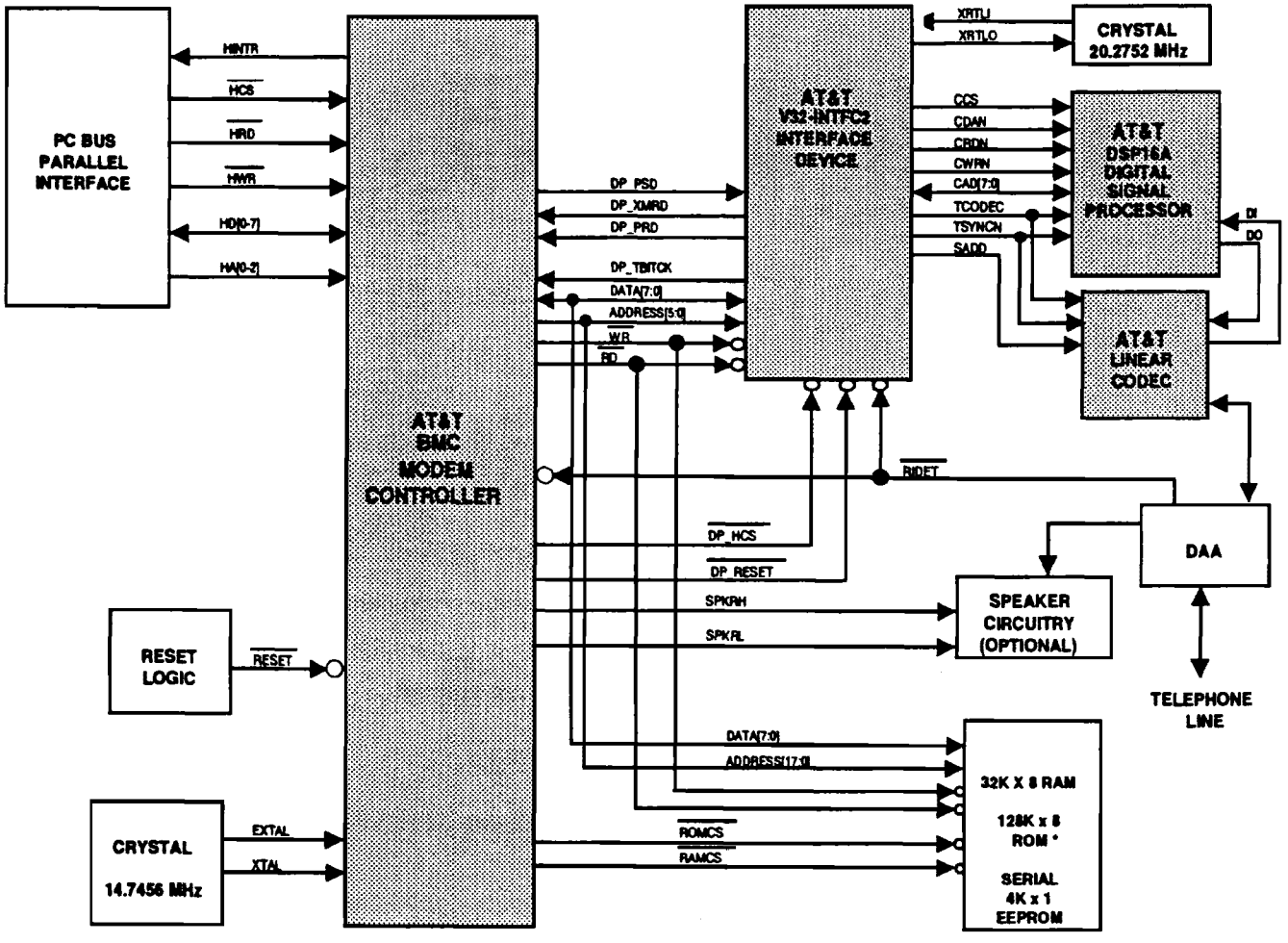
The AT&T HSM Complete Hardware Interface Signals for the serial and parallel interfaces are shown in Figures 2 and 3.



Note: * Data/Fax/Voice feature requires 256K X 8 ROM.

Figure 2. Serial Interface Connection Diagram

Hardware Interface (continued)



Note: * Data/FAX/Voice feature requires 256K X 8 ROM.

Figure 3. Parallel Interface Connection Diagram

Hardware Interface (continued)

DeskTop Packages

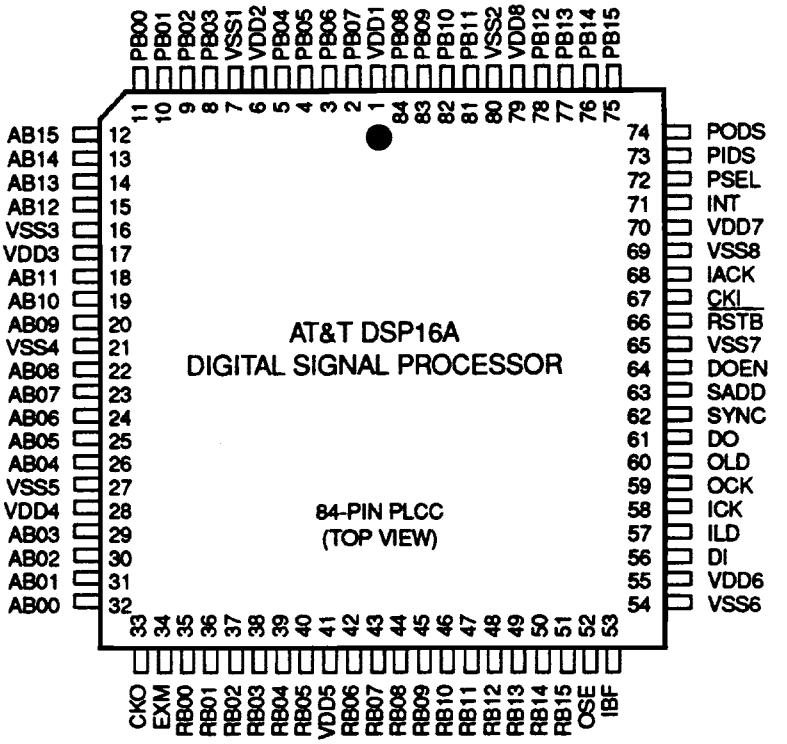


Figure 4. AT&T DSP16A Device Pin Locations, 84 Pin PLCC

Hardware Interface (continued)

Table 11. AT&T DSP16A Pin Signals, 84 pin PLCC

In the following table, I = input, O = output, and P = power.

Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O
1	VDD1	P	29	AB03	O	57	ILD	I/O
2	PB07	I/O	30	AB02	O	58	ICK	I/O
3	PB06	I/O	31	AB01	O	59	OCK	I/O
4	PB05	I/O	32	AB00	O	60	OLD	I/O
5	PB04	I/O	33	CK0	O	61	DO	O
6	VDD2	P	34	EXM	I	62	SYNC	I/O
7	VSS1	P	35	RB00	I	63	SADD	I/O
8	PB03	I/O	36	RB01	I	64	DOEN	I/O
9	PB02	I/O	37	RB02	I	65	VSS7	P
10	PB01	I/O	38	RB03	I	66	$\overline{\text{RTSB}}$	I
11	PB00	I/O	39	RB04	I	67	CKI	I
12	AB15	O	40	RB05	I	68	IACK	O
13	AB14	O	41	VDD5	P	69	VSS8	P
14	AB13	O	42	RB06	I	70	VDD7	P
15	AB12	O	43	RB07	I	71	INT	I
16	VSS3	P	44	RB08	I	72	PSEL	O
17	VDD3	P	45	RB09	I	73	PIDS	I/O
18	AB11	O	46	RB10	I	74	PODS	I/O
19	AB10	O	47	RB11	I	75	PB15	I/O
20	AB09	O	48	RB12	I	76	PB14	I/O
21	VSS4	P	49	RB13	I	77	PB13	I/O
22	AB08	O	50	RB14	I	78	PB12	I/O
23	AB07	O	51	RB15	I	79	VDD8	P
24	AB06	O	52	OSE	O	80	VSS2	P
25	AB05	O	53	IBF	O	81	PB11	I/O
26	AB04	O	54	VSS6	P	82	PB10	I/O
27	VSS5	P	55	VDD6	P	83	PB09	I/O
28	VDD4	P	56	DI	I	84	PB08	I/O

Hardware Interface (continued)

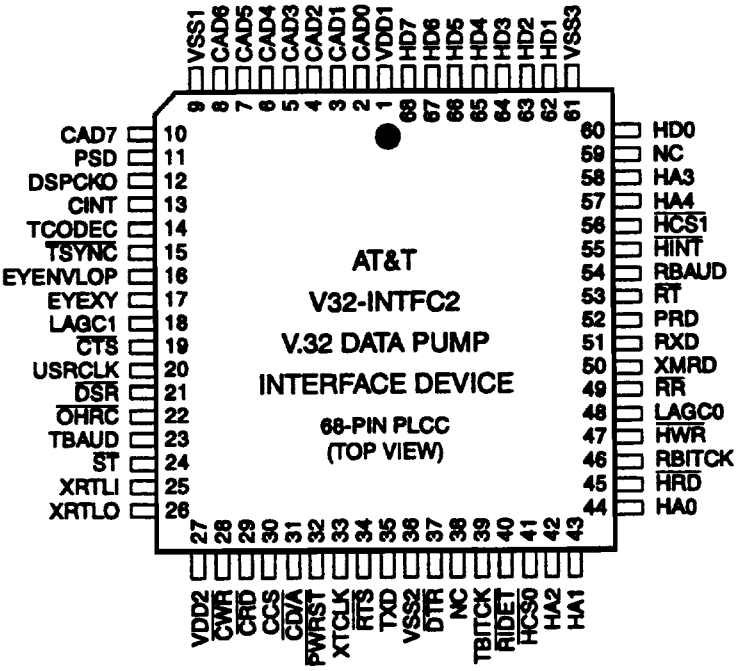


Figure 5. AT&T V32-INTFC2 Device Pin Locations, 68 Pin PLCC

Hardware Interface (continued)

Table 12. AT&T V.32 INTFC2 Pin Signals, 68 pin PLCC

In the following table, I = input, O = output, and P = power.

Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O
1	VDD1	P	24	$\overline{ST}$	O	47	$\overline{HWR}$	I
2	CAD0	I/0	25	XRTLI	I	48	LAGCO	O
3	CAD1	I/0	26	XRTLO	O	49	$\overline{RR}$	O
4	CAD2	I/0	27	VDD2	P	50	XMRD	O
5	CAD3	I/O	28	$\overline{CWR}$	I	51	RXD	O
6	CAD4	I/O	29	$\overline{CRD}$	I	52	PRD	O
7	CAD5	I/O	30	CCS	I	53	$\overline{RT}$	O
8	CAD6	I/O	31	$\overline{CD/A}$	I	54	RBAUD	O
9	VSS1	P	32	$\overline{PWRST}$	I	55	$\overline{HINT}$	O
10	CAD7	I/O	33	XTCLK	I	56	$\overline{HCS1}$	—
11	PSD	I	34	$\overline{RTS}$	I	57	HA4	I
12	DSPCK0	O	35	TXD	I	58	HA3	I
13	CINT	O	36	VSS2	P	59	NC	—
14	TCODEC	O	37	$\overline{DTR}$	I	60	HD0	I/O
15	$\overline{TSYNC}$	I/O	38	NC	—	61	VSS3	P
16	EYENVLOP	O	39	TBITCLK	O	62	HD1	I/O
17	EYEXY	O	40	$\overline{RIDET}$	I	63	HD2	I/O
18	LAGC1	O	41	$\overline{HCS0}$	I	64	HD3	I/O
19	$\overline{CTS}$	O	42	HA2	I	65	HD4	I/O
20	USRCLK	O	43	HA1	I	66	HD5	I/O
21	$\overline{DSR}$	O	44	HA0	I	67	HD6	I/O
22	$\overline{OHRC}$	O	45	$\overline{HRD}$	I	68	HD7	I/O
23	TBAUD	O	46	RBITCLK	O	—	—	—

Hardware Interface (continued)

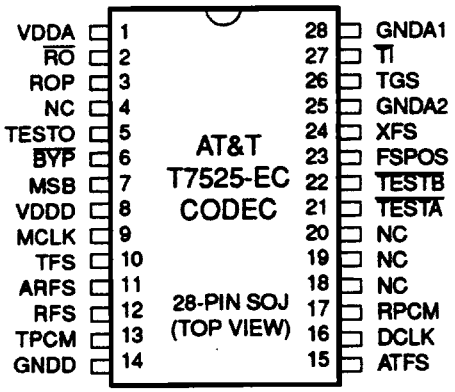


Figure 6. AT&T T7525 Device Pin Location, 28 Pin SOJ

Table 13. AT&T T7525 Codec Pin Signals, 28 pin SOJ

In the following table, I = input, O = output, and P = power.

Pin	Name	I/O	Pin	Name	I/O
1	VDDA	P	15	ATFS	I
2	$\overline{RO}$	O	16	DCLK	I
3	ROP	O	17	RPCM	I
4	NC	—	18	NC	—
5	TESTO	O	19	NC	—
6	$\overline{BYP}$	I	20	NC	—
7	MSB	I	21	$\overline{TSTA}$	I
8	VDDD	P	22	$\overline{TSTB}$	I
9	MCLK	I	23	FSPOS	I
10	TFS	I	24	XFS	O
11	ARFS	I	25	GNDA2	P
12	RFS	I	26	TGS	O
13	TPCM	O	27	$\overline{TI}$	I
14	GNDD	P	28	GNDA1	P

Note: NC = no connection; leave pin disconnected (open).

Hardware Interface (continued)

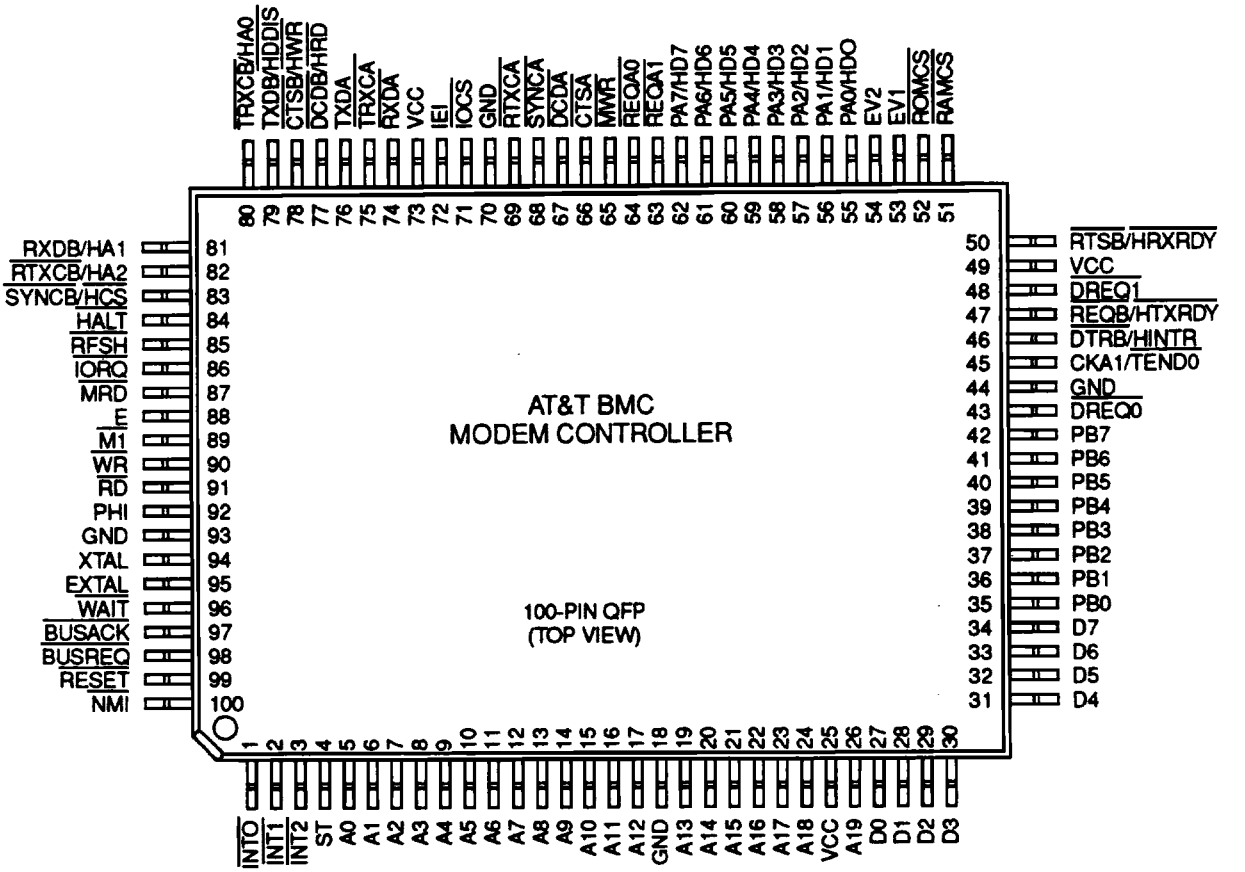


Figure 7. AT&T BMC QFP Device Pin Locations, 100 Pin QFP

Hardware Interface (continued)

Table 14. AT&T BMC Pin Signals, 100 pin QFP

In the following table, I = input, O = output, P = power, and 3 = 3-state.

Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O
1	$\overline{\text{INT0}}$	I	35	PB0	I/O 3	68	$\overline{\text{SYNCA}}$	I
2	$\overline{\text{INT1}}$	I	36	PB1	I/O 3	69	$\overline{\text{RTXCA}}$	I
3	$\overline{\text{INT2}}$	I	37	PB2	I/O 3	70	GND	P
4	ST	O	38	PB3	I/O 3	71	$\overline{\text{IOCS}}$	O 3
5	A0	I/O 3	39	PB4	I/O 3	72	IEI	I
6	A1	I/O 3	40	PB5	I/O 3	73	VCC	P
7	A2	I/O 3	41	PB6	I/O 3	74	RXDA	I
8	A3	I/O 3	42	PB7	I/O 3	75	$\overline{\text{TRXCA}}$	I
9	A4	I/O 3	43	$\overline{\text{DREQ0}}$	I	76	TXDA	O
10	A5	I/O 3	44	GND	P	77	$\overline{\text{DCDB}}$ / $\overline{\text{HRD}}$	I
11	A6	I/O 3	45	CKA1/ $\overline{\text{TENDO}}$	NC	78	$\overline{\text{CTSB}}$ / $\overline{\text{HWR}}$	I
12	A7	I/O 3	46	$\overline{\text{DTRB}}$ / HINTR	O	79	TXDB/ $\overline{\text{HDDIS}}$	O
13	A8	I/O 3	47	$\overline{\text{REQB}}$ / $\overline{\text{HTXRDY}}$	O	80	$\overline{\text{TRXCB}}$ /HA0	I
14	A9	I/O 3	48	$\overline{\text{DREQ1}}$	I	81	RXDB/HA1	I
15	A10	I/O 3	49	VCC	P	82	$\overline{\text{RTXCB}}$ /HA2	I
16	A11	I/O 3	50	$\overline{\text{RTSB}}$ / $\overline{\text{HRXRDY}}$	O	83	$\overline{\text{SYNCB}}$ / $\overline{\text{HCS}}$	I
17	A12	I/O 3	51	$\overline{\text{RAMCS}}$	O 3	84	$\overline{\text{HALT}}$	O
18	GND	P	52	$\overline{\text{ROMCS}}$	O 3	85	$\overline{\text{RFSH}}$	NC
19	A13	I/O 3	53	EV1	I	86	$\overline{\text{IORQ}}$	NC
20	A14	I/O 3	54	EV2	I	87	$\overline{\text{MRD}}$	NC
21	A15	I/O 3	55	PA0/HD0	I/O 3	88	E	NC
22	A16	I/O 3	56	PA1/HD1	I/O3	89	$\overline{\text{M1}}$	NC
23	A17	I/O 3	57	PA2/HD2	I/O 3	90	$\overline{\text{WR}}$	O 3
24	A18	I/O 3	58	PA3/HD3	I/O 3	91	$\overline{\text{RD}}$	O 3
25	VCC	P	59	PA4/HD4	I/O 3	92	PHI	O
26	A19	I/O 3	60	PA5/HD5	I/O 3	93	GND	P
27	D0	I/O 3	61	PA6/HD6	I/O 3	94	XTAL	I
28	D1	I/O 3	62	PA7/HD7	I/O 3	95	EXTAL	I
29	D2	I/O 3	63	$\overline{\text{REQA1}}$	O	96	$\overline{\text{WAIT}}$	I
30	D3	I/O 3	64	$\overline{\text{REQA0}}$	O	97	$\overline{\text{BUSACK}}$	NC
31	D4	I/O 3	65	$\overline{\text{MWR}}$	NC	98	$\overline{\text{BUSREQ}}$	I
32	D5	I/O 3	66	$\overline{\text{CTSA}}$	I	99	$\overline{\text{RESET}}$	I
33	D6	I/O 3	67	$\overline{\text{DCDA}}$	I	100	$\overline{\text{NMI}}$	I
34	D7	I/O 3	—	—	—	—	—	—

Hardware Interface (continued)

LapTop Packages

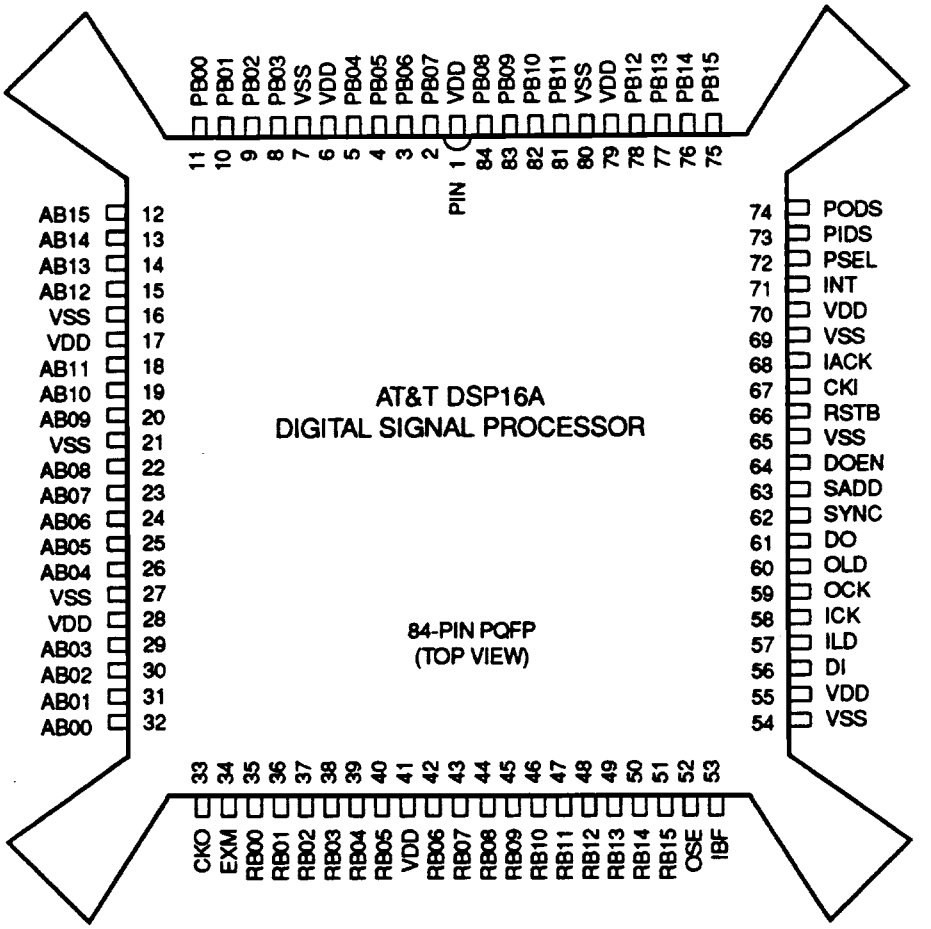


Figure 8. AT&T DSP16A Pin Locations, 84 Pin PQFP

Hardware Interface (continued)

Table 15. AT&T DSP16A Signals, 84 pin PQFP

In the following table, I = input, O = output, and P = power.

Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O
1	VDD	P	29	AB03	O	57	ILD	I/O
2	PB07	I/O	30	AB02	O	58	ICK	I/O
3	PB06	I/O	31	AB01	O	59	OCK	I/O
4	PB05	I/O	32	AB00	O	60	OLD	I/O
5	PB04	I/O	33	CK0	O	61	DO	O
6	VDD	P	34	EXM	I	62	SYNC	I/O
7	VSS	P	35	RB00	I	63	SADD	I/O
8	PB03	I/O	36	RB01	I	64	DOEN	I/O
9	PB02	I/O	37	RB02	I	65	VSS	P
10	PB01	I/O	38	RB03	I	66	RSTB	I
11	PB00	I/O	39	RB04	I	67	CKI	I
12	AB15	O	40	RB05	I	68	IACK	O
13	AB14	O	41	VDD	P	69	VSS	P
14	AB13	O	42	RB06	I	70	VDD	P
15	AB12	O	43	RB07	I	71	INT	I
16	VSS	P	44	RB08	I	72	PSEL	O
17	VDD	P	45	RB09	I	73	PIDS	I/O
18	AB11	O	46	RB10	I	74	PODS	I/O
19	AB10	O	47	RB11	I	75	PB15	I/O
20	AB09	O	48	RB12	I	76	PB14	I/O
21	VSS	P	49	RB13	I	77	PB13	I/O
22	AB08	O	50	RB14	I	78	PB12	I/O
23	AB07	O	51	RB15	I	79	VDD	P
24	AB06	O	52	OSE	O	80	VSS	P
25	AB05	O	53	IBF	O	81	PB11	I/O
26	AB04	O	54	VSS	P	82	PB10	I/O
27	VSS	P	55	VDD	P	83	PB09	I/O
28	VDD	P	56	DI	I	84	PB08	I/O

Note: AT&T PQFP package conforms to JEDEC standard for 84-pin device.

Hardware Interface (continued)

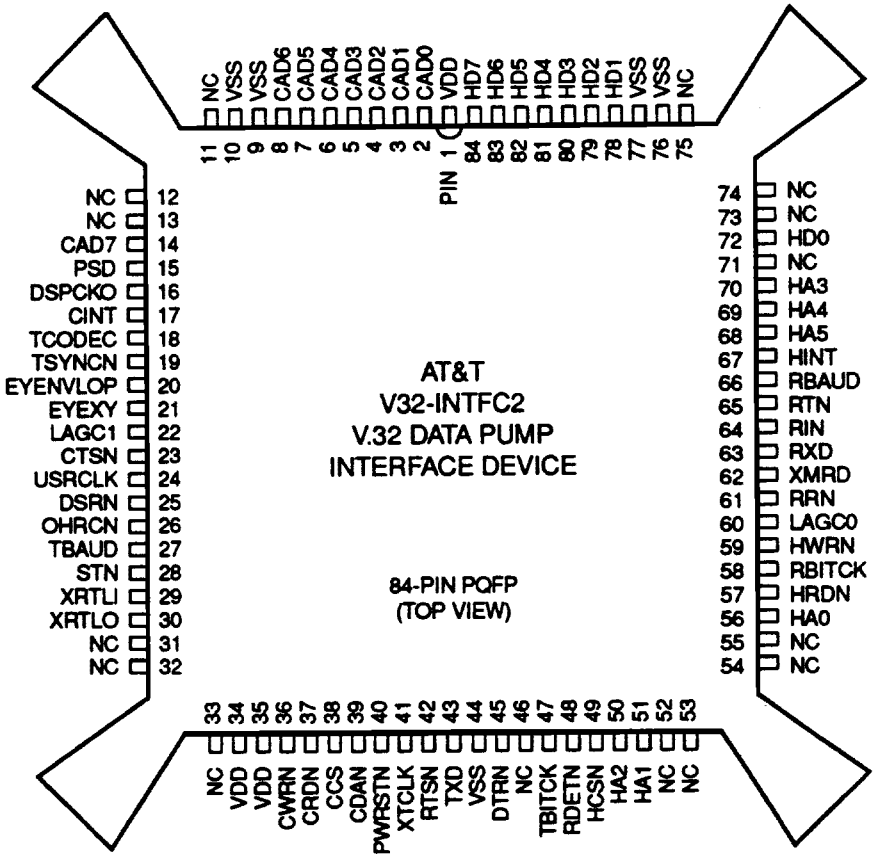


Figure 9. AT&T V32-INTFC2 Pin Locations, 84 Pin PQFP

Hardware Interface (continued)

Table 16. AT&T V32-INTFC2 Signals, 84 pin PQFP

In the following table, I = input, O = output, and P = power.

Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O
1	VDD	P	29	XRTLI	I	57	HRDN	I
2	CAD0	I/O	30	XRTLO	O	58	RBITCK	O
3	CAD1	I/O	31	NC	—	59	HWRN	I
4	CAD2	I/O	32	NC	—	60	LAGC0	O
5	CAD3	I/O	33	NC	—	61	RRN	O
6	CAD4	I/O	34	VDD	P	62	XMRD	O
7	CAD5	I/O	35	VDD	P	63	RXD	O
8	CAD6	I/O	36	CWRN	I	64	RIN	O
9	VSS	P	37	CRDN	I	65	RTN	O
10	VSS	P	38	CCS	I	66	RBAUD	O
11	NC	—	39	CDAN	I	67	HINT	O
12	NC	—	40	PWRSTN	I	68	HA5	I
13	NC	—	41	XTCLK	I	69	HA4	I
14	CAD7	I/O	42	RTSN	I	70	HA3	I
15	PSD	I	43	TXD	I	71	NC	—
16	DSPCK0	O	44	VSS	P	72	HD0	I/O
17	CINT	O	45	DTRN	I	73	NC	—
18	TCODEC	O	46	NC	—	74	NC	—
19	TSYNCN	I/O	47	TBITCK	O	75	NC	—
20	EYENVLOP	O	48	RDETN	I	76	VSS	P
21	EYEXY	O	49	HCSN	I	77	VSS	P
22	LAGC1	O	50	HA2	I	78	HD1	I/O
23	CTSN	O	51	HA1	I	79	HD2	I/O
24	USRCLK	O	52	NC	—	80	HD3	I/O
25	DSRN	O	53	NC	—	81	HD4	I/O
26	OHRCN	O	54	NC	—	82	HD5	I/O
27	TBAUD	O	55	NC	—	83	HD6	I/O
28	STN	O	56	HA0	I	84	HD7	I/O

Note: AT&T PQFP package conforms to JEDEC standard for 84-pin device.

Hardware Interface (continued)

AT&T T7525 28-Pin SOJ pinout — refer to Figure 6 on page 32.

AT&T T7525 28-Pin SOJ listing — refer to Table 13 on page 32.

AT&T BMC 100-Pin QFP pinout — refer to Figure 7 on page 33.

AT&T BMC 100-Pin QFP listing — refer to Table 14 on page 34.

PCMCIA Packages

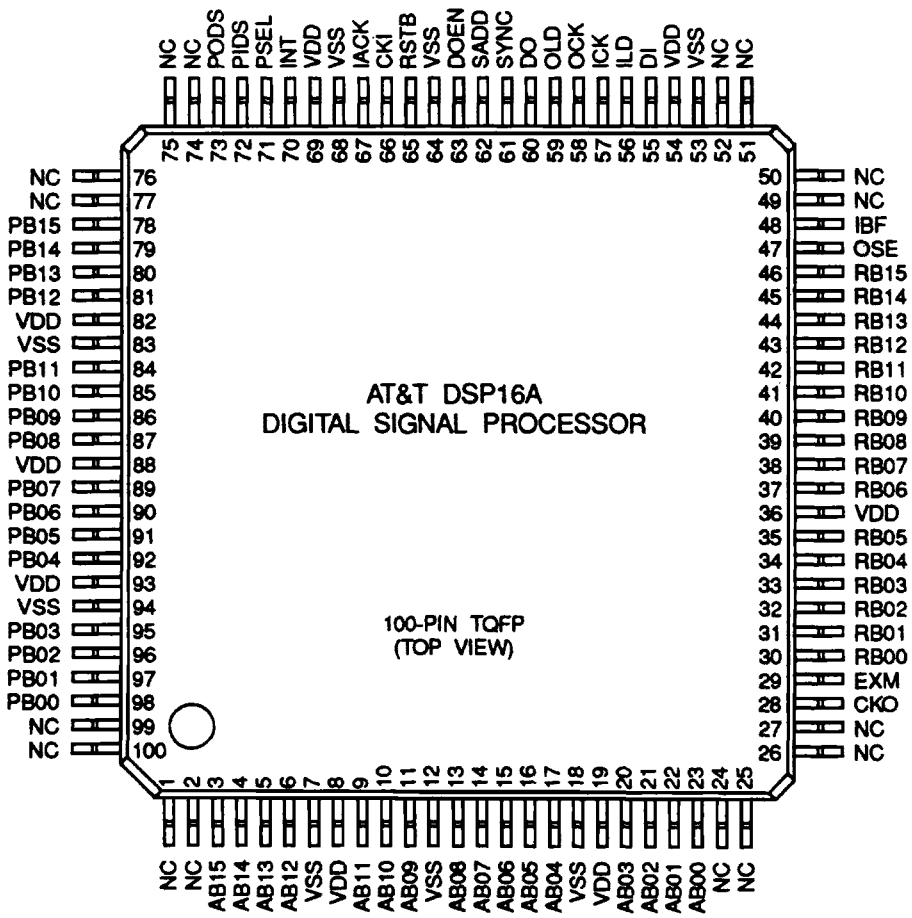


Figure 10. AT&T DSP16A TQFP Device Pin Locations, 100 Pin TQFP

Hardware Interface (continued)

Table 17. AT&T DSP16A Signals, 100 pin TQFP

In the following table, I = input, O = output, and P = power.

Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O
1	NC	—	26	NC	—	51	NC	—	76	NC	—
2	NC	—	27	NC	—	52	NC	—	77	NC	—
3	AB15	O	28	CKO	O	53	VSS	P	78	PB15	I/O
4	AB14	O	29	EXM	I	54	VDD	P	79	PB14	I/O
5	AB13	O	30	RB00	I	55	DI	I	80	PB13	I/O
6	AB12	O	31	RB01	II	56	ILD	I/O	81	PB12	I/O
7	VSS	P	32	RB02	I	57	ICK	I/O	82	VDD	P
8	VDD	P	33	RB03	I	58	OCK	I/O	83	VSS	P
9	AB11	O	34	RB04	I	59	OLD	I/O	84	PB11	I/O
10	AB10	O	35	RB05	I	60	DO	O	85	PB10	I/O
11	AB09	O	36	VDD	P	61	SYNC	I/O	86	PB09	I/O
12	VSS	P	37	RB06	I	62	SADD	I/O	87	PB08	I/O
13	AB08	O	38	RB07	I	63	DOEN	I/O	88	VDD	P
14	AB07	O	39	RB08	I	64	VSS	P	89	PB07	I/O
15	AB06	O	40	RB09	I	65	RSTB	I	90	PB06	I/O
16	AB05	O	41	RB10	I	66	CKI	I	91	PB05	I/O
17	AB04	O	42	RB11	I	67	IACK	O	92	PB04	I/O
18	VSS	P	43	RB12	I	68	VSS	P	93	VDD	P
19	VDD	P	44	RB13	I	69	VDD	P	94	VSS	P
20	AB03	O	45	RB14	I	70	INT	I	95	PB03	I/O
21	AB02	O	46	RB15	I	71	PSEL	O	96	PB02	I/O
22	AB01	O	47	OSE	O	72	PIDS	I/O	97	PB01	I/O
23	AB00	O	48	IBF	O	73	PODS	I/O	98	PB00	I/O
24	NC	—	49	NC	—	74	NC	—	99	NC	—
25	NC	—	50	NC	—	75	NC	—	100	NC	—

Hardware Interface (continued)

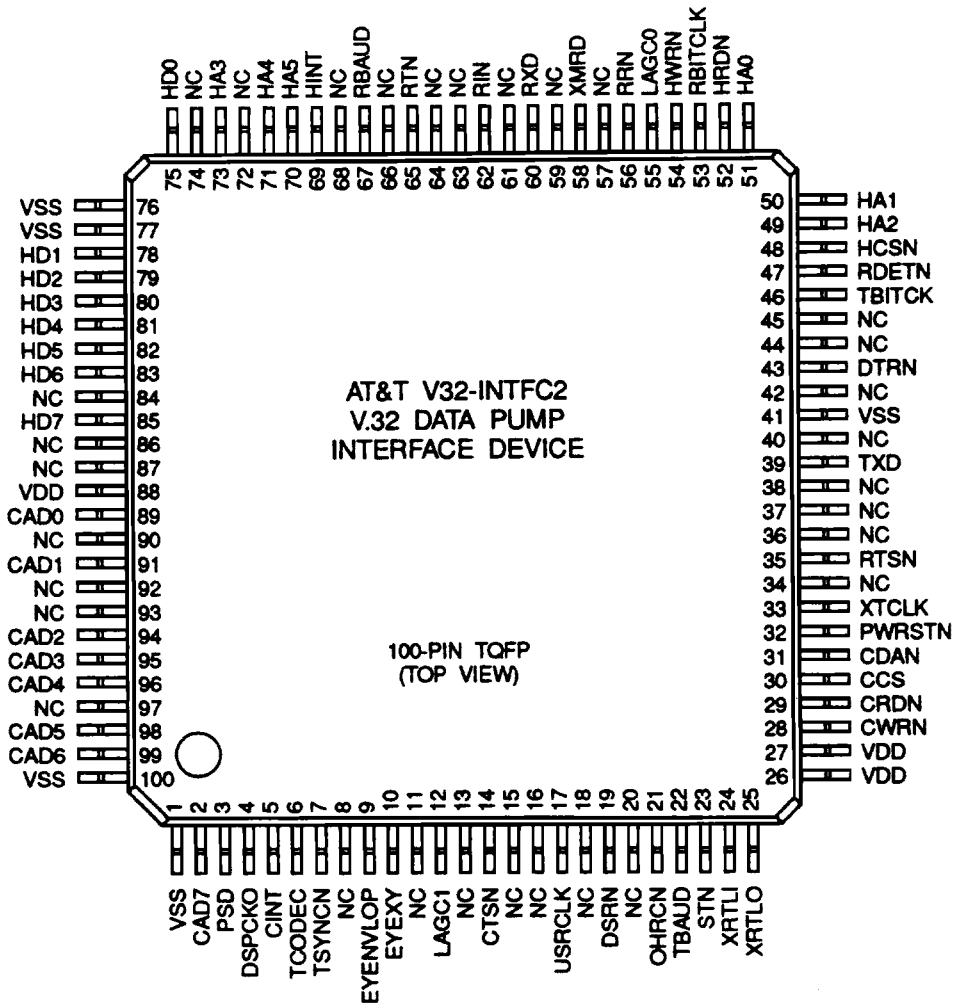


Figure 11. AT&T V32-INTFC2 TQFP Device Pin Locations, 100 Pin TQFP

Hardware Interface (continued)

Table 18. AT&T V32-INTFC2 Pin Signals, 100 pin TQFP

In the following table, I = input, O = output, NC = co connect, and P = power.

Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O
1	VSS	P	26	VDD	P	51	HA0	I	76	VSS	P
2	CAD7	I/O	27	VDD	P	52	HRDN	O	77	VSS	P
3	PSD	I	28	CWRN	I	53	RBITCLK		78	HD1	I/O
4	DSPCK0	O	29	CRDN	I	54	HWRN	I	79	HD2	I/O
5	CINT	O	30	CCS	I	55	LAGCO	O	80	HD3	I/O
6	TCODEC	O	31	CDAN	I	56	RRN	O	81	HD4	I/O
7	TSYNCN	I/O	32	PWRSTN	I	57	NC	—	82	HD5	I/O
8	NC	—	33	XTCLK	I	58	XMRD	O	83	HD6	I/O
9	EYENVLOP	O	34	NC	—	59	NC	—	84	NC	—
10	EYEXY	O	35	RTSN	I	60	RXD	O	85	HD7	I/O
11	NC	—	36	NC	—	61	NC	—	86	NC	—
12	LAGC1	O	37	NC	—	62	RIN	I	87	NC	—
13	NC	—	38	NC	—	63	NC	—	88	VDD	P
14	CTSN	O	39	TXD	I	64	NC	—	89	CAD0	I/O
15	NC	—	40	NC	—	65	RTN	O	90	NC	—
16	NC	—	41	VSS	P	66	NC	—	91	CAD1	I/O
17	USRCLK	O	42	NC	—	67	RBAUD	I	92	NC	—
18	NC	—	43	DTRN	I	68	NC	—	93	NC	—
19	DSRN	O	44	NC	—	69	HINT	O	94	CAD2	I/O
20	NC	—	45	NC	—	70	HA5	I	95	CAD3	I/O
21	OHRCN	O	46	TBITCK	O	71	HA4	I	96	CAD4	I/O
22	TBAUD	O	47	RDETN	I	72	NC	—	97	NC	—
23	STN	O	48	HCSN	I	73	HA3	I	98	CAD5	I/O
24	XRTLI	I	49	HA2	I	74	NC	—	99	CAD6	I/O
25	XRTLO	O	50	HA1	I	75	HDO	I/O	100	VSS	P

Hardware Interface (continued)

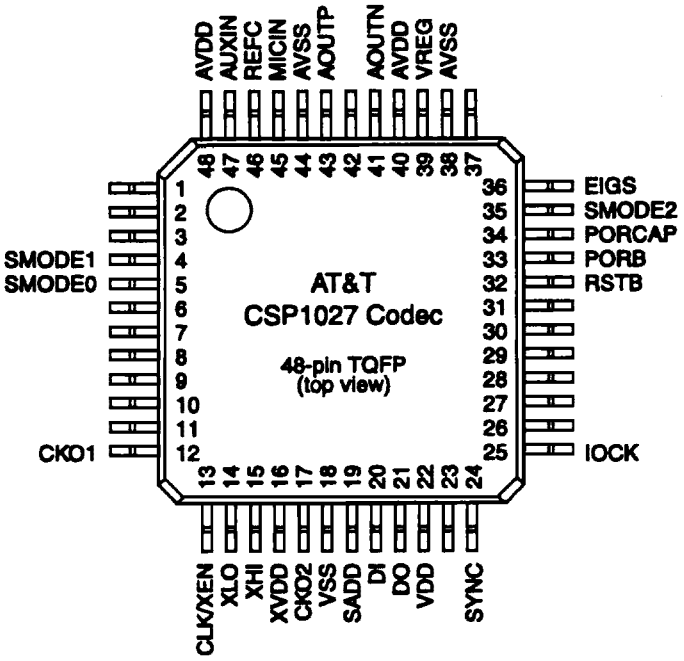


Figure 12. AT&T CSP1027 TQFP Device Pin Locations, 48 Pin TQFP

Table 19. AT&T CSP1027 Pin Signals, 48 pin TQFP

In the following table, I = input, O = output, NC = no connect, and P = power.

Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O
1	NC	—	17	CKO2	O	33	PORB	O
2	NC	—	18	VSS	P	34	PORCAP	I
3	NC	—	19	SADD	I/O	35	SMODE2	I
4	SMODE1	I	20	DI	I	36	EIGS	I
5	SMODE0	I	21	DO	O	37	NC	—
6	NC	—	22	VDD	P	38	AVSS	P
7	NC	—	23	NC	—	39	VREG	O
8	NC	—	24	SYNC	I/O	40	AVDD	P
9	NC	—	25	IOCK	I	41	AOUTN	O
10	NC	—	26	NC	—	42	NC	—
11	NC	—	27	NC	—	43	AOUTP	O
12	CKO1	O	28	NC	—	44	AVSS	P
13	CLK/XEN	I	29	NC	—	45	MICIN	I
14	XLO	I	30	NCN	—	46	REFC	I
15	XHI	I	31	NC	—	47	AUXIN	I
16	XVDD	P	32	RSTB	I	48	AVDD	P

Hardware Interface (continued)

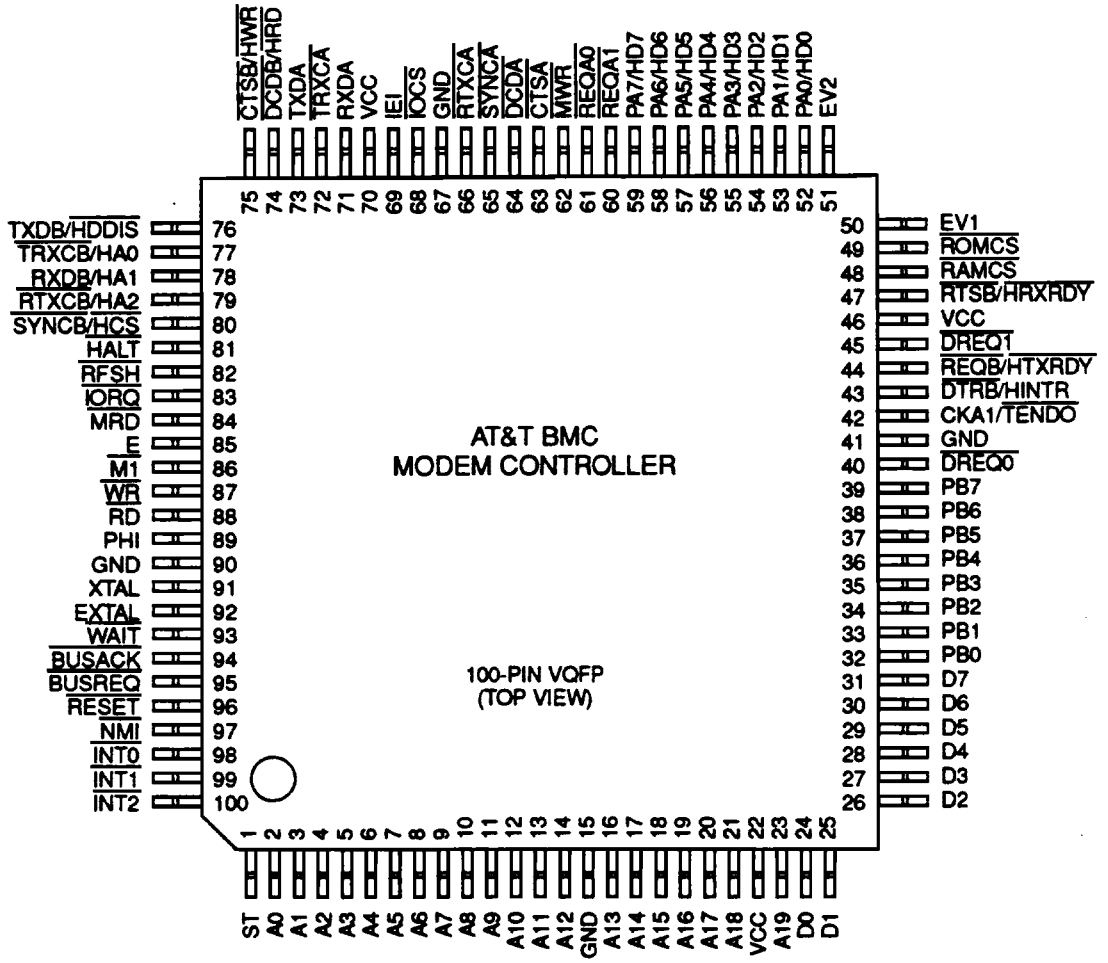


Figure 13. AT&T BMC VQFP Device Pin Locations, 100 Pin VQFP

Hardware Interface (continued)

Table 20. AT&T BMC Pin Signals,- 100 pin VQFP

In the following table, I = input, O = output, P = power, and 3 = 3-state.

Pin	Name	I/O	Pin	Name	I/O	Pin	Name	I/O
1	ST	NC	35	PB3	I/O 3	68	$\overline{\text{IPCS}}$	O 3
2	A0	I/O 3	36	PB4	I/O 3	69	IEI	I
3	A1	I/O 3	37	PB5	I/O 3	70	VCC	P
4	A2	I/O 3	38	PB6	I/O 3	71	RXDA	I
5	A3	I/O 3	39	PB7	I/O 3	72	$\overline{\text{TRCA}}$	I
6	A4	I/O 3	40	$\overline{\text{DREQ0}}$	I	73	TXDA	O
7	A5	I/O 3	41	GND	P	74	$\overline{\text{DCDB}}$ / $\overline{\text{HRD}}$	I
8	A6	I/O 3	42	CKA1/ $\overline{\text{TEND0}}$	NC	75	$\overline{\text{CTSB}}$ / $\overline{\text{HWR}}$	I
9	A7	I/O 3	43	$\overline{\text{DTRB}}$ / HINTR	O	76	TXDB/ $\overline{\text{HDDIS}}$	NC
10	A8	I/O 3	44	$\overline{\text{REQB}}$ / $\overline{\text{HTXRDY}}$	NC	77	$\overline{\text{TRXCB}}$ /HA0	I
11	A9	I/O 3	45	$\overline{\text{DREQ1}}$	I	78	RXDB/HA1	I
12	A10	I/O 3	46	VCC	P	79	$\overline{\text{RTXCB}}$ /HA2	I
13	A11	I/O 3	47	$\overline{\text{RTSB}}$ / $\overline{\text{HTXRDY}}$	NC	80	$\overline{\text{SYNCB}}$ / $\overline{\text{HCS}}$	I
14	A12	I/O 3	48	$\overline{\text{RAMCS}}$	O 3	81	$\overline{\text{HALT}}$	O
15	GND	P	49	$\overline{\text{ROMCS}}$	O 3	82	$\overline{\text{RFSH}}$	NC
16	A13	I/O 3	50	EV1	I	83	$\overline{\text{IORQ}}$	NC
17	A14	I/O 3	51	EV2	I	84	$\overline{\text{MRD}}$	NC
18	A15	I/O 3	52	PA0/HD0	I/O 3	85	E	NC
19	A16	I/O 3	53	PA1/HD1	I/O 3	86	$\overline{\text{M1}}$	NC
20	A17	I/O 3	54	PA2/HD2	I/O 3	87	$\overline{\text{WR}}$	O 3
21	A18	I/O 3	55	PA3/HD3	I/O 3	88	$\overline{\text{RD}}$	O 3
22	VCC	P	56	PA4/HD4	I/O 3	89	PHI	NC
23	A19	I/O 3	57	PA5/HD5	I/O 3	90	GND	P
24	D0	I/O 3	58	PA6/HD6	I/O 3	91	XTAL	I
25	D1	I/O 3	59	PA7/HD7	I/O 3	92	EXTAL	I
26	D2	I/O 3	60	$\overline{\text{REQA1}}$	O	93	$\overline{\text{WAIT}}$	I
27	D3	I/O 3	61	$\overline{\text{REQA0}}$	O	94	$\overline{\text{BUSACK}}$	NC
28	D4	I/O 3	62	$\overline{\text{MWR}}$	NC	95	$\overline{\text{BUSREQ}}$	I
29	D5	I/O 3	63	$\overline{\text{CSTA}}$	I	96	$\overline{\text{RESET}}$	I
30	D6	I/O 3	64	$\overline{\text{DCDA}}$	I	97	$\overline{\text{NMI}}$	I
31	D7	I/O 3	65	$\overline{\text{SYNCA}}$	I	98	$\overline{\text{INT0}}$	I
32	PB0	I/O 3	66	$\overline{\text{RTXCA}}$	I	99	$\overline{\text{INT1}}$	I
33	PB1	I/O 3	67	GND	P	100	$\overline{\text{INT2}}$	I
34	PB2	I/O 3	—	—	—	—	—	—

Hardware Interface (continued)

Hardware Interface Signals

Table 21. V.24/RS232D Interface Pins (Serial Mode Only)

Signal	Type	Name/Description
$\overline{\text{DTE\_RXD}}$	O	**Receive Data (Active-Low EIA).** This output is for digital data to the DTE that was received from the analog telephone line.
$\overline{\text{DTE\_TXD}}$	I	**Transmitted Data (Active-Low EIA).** This input is for digital data from the DTE to be transmitted over the analog telephone line.
$\overline{\text{DTE\_RTS}}$	I	**Request to Send (Active-Low EIA).** This input is generated by the DTE and represents request to send to the modem.
$\overline{\text{DTE\_CTS}}$	O	**Clear to Send (Active-Low EIA).** This output to the DTE indicates the modem is clear to send data.
$\overline{\text{DTE\_DTR}}$	I	**Data Terminal Ready (Active-Low EIA).** This input indicates to the modem that the DTE is ready.
DTE_XTCLK	I	**External Clock.** This input is for the DTE supplying the external transmit data clock in synchronous mode.
DTE_RXCLK	O	**Receive Clock.** This output is the clock for RXD in synchronous mode.
DTE_TXCLK	O	**Transmit Clock.** This output is the clock for TXD in synchronous mode.
$\overline{\text{DTE\_DSR}}$	O	**Data Set Ready (Active-Low EIA).** This output indicates to the DTE that the modem is ready.
$\overline{\text{DTE\_DCD}}$	O	**Carrier Detect (Active-Low EIA).** This output indicates if the modem has detected carrier.
$\overline{\text{RI}}$	O	**Ring Detect (Active-Low EIA).** This output indicates the modem has detected a ring signal.

Table 22. Line Interface Pins

Signal	Type	Name/Description
$\overline{\text{RO}}$	O	**Receive Output (Negative).** Inverting output of the power amplifier.
ROP	O	**Receive Output (Positive).** Noninverting output of the power amplifier.
TIN	I	**Transmit Input (Negative).** Inverting analog input to the input operational amplifier.
TGS	O	**Transmit Gain Setting.** Output terminal of the input operational amplifier; should be connected to external gain control network of resistors.

Table 23. Speaker Interface

Signal	Type	Name/Description
SPKRH SPKRL	O O	**Speaker Volume Control.** SPKRH and SPKRL are outputs that control the speaker volume.

Level	SPKRH	SPKRL
Off	0	0
Low	0	1
Medium	1	0
High	1	1

Hardware Interface Signals (continued)

Table 24. Memory Bus Interface Pins

Symbol	Type	Name/Description
A0—A17	O 3	**Address Bus Lines 0—17.** Address bus between BMC, AT&T V.32 Interface2 device, and memory.
D0—D7	I/O 3	**Data Bus Lines 0—7.** Data bus between BMC, memory, and AT&T V.32 Interface2 Device.
$\overline{\text{ROMCS}}$	O 3	**ROM Chip Select (Active-Low).** A low on this output selects the ROM.
$\overline{\text{RAMCS}}$	O 3	**RAM Chip Select (Active-Low).** A low on this output selects the RAM.
$\overline{\text{RD}}$	O 3	**Memory Read (Active-Low).** A low on this output enables data to be transferred from the data lines to the BMC.
$\overline{\text{WR}}$	O 3	**Memory Write (Active-Low).** A low on this output enables data to be transferred from the BMC to the data lines.

Table 25. PC Bus Parallel Interface Pins

Symbol	Type	Name/Description
HINTR	O	**Host Interrupt.** A high on this output indicates an interrupt request for the PC.
$\overline{\text{HCS}}$	I	**Host chip select (Active-Low).** A low on ths input enables the parallel interface bus.
$\overline{\text{HRD}}$	I	**Host Read (Active-Low).** A low on this input enables data to be transfered from the BMC to the host.
$\overline{\text{HWR}}$	I	**Host Write (Active-Low).** A low on this input enables data to be transfered from the host to the BMC.
HD0—HD7	I/O	**Host Data Bus 0—7.** Data bus between BMC and PC parallel interface.
HA0—HA2	I	**Host Address Bus 0—2.** Address bus between BMC and PC parallel Interface.

Table 26. Miscellaneous Pins

Signal	Type	Name/Description
$\overline{\text{RIDET}}$	I	**Ring Detect (Active-Low).** Ring signal input to V32-INTFC2 device and BMC.
EXTAL XTAL	I I	**BMC Crystal Input.** The EXTAL pin must be connected to an external 14.7456 MHz crystal.
$\overline{\text{RESET}}$	I	**Reset (Active-Low).** A low on this input resets the AT&T HSM chip set.
XRTLI XRTLO	I O	**V32-INTFC2 Crystal Input.** The EXTAL pin must be connected to an external 20.2752 MHz crystal.

Electrical Characteristics

The electrical characteristics in this data sheet are preliminary and are subject to change.
Electrical characteristics are presented here for the data pump (DSP16A, INTFC2, and T7525), and the AT&T BMC modem controller (BMC). Additional information regarding the AT&T DSP16A device, the AT&T T7525 Codec, and the AT&T CSP1027 are available in their respective data sheets.

Electrical Characteristics (continued)

Data Pump Electrical Characteristics

These parameters are valid for the following conditions: T_A = 0 °C to 70 °C, V_{CC} = 5 V ± 5%, V_{SS} = GND = GND_A = 0 V.

Parameter	Symbol	Min.	Max.	Unit
Input Voltage (all external data pump inputs, except those listed in the next category):*				
Low	V_{IL}	—	0.8	V
High	V_{IH}	2.0	—	V
Input Voltage (V32-INTFC2 pins: MBUS, XRTLI):				
Low	V_{IL}	—	0.8	V
High	V_{IH}	V_{CC} – 1.5	—	V
Output Voltage:				
Low	V_{OL}	—	0.4	V
(I_{OL} = 2 mA) All Pins Except Those Below				
(I_{OL} = 4 mA) USRCLK				
(I_{OL} = 10 mA) HAD[7:0]				
(I_{OL} = 20 mA) OHRCN				
High	V_{OH}	2.4	—	V
(I_{OL} = 2 mA) All Pins Except Those Below				
(I_{OL} = 4 mA) USRCLK				
(I_{OL} = 10 mA) HAD[7:0]				
(I_{OL} = 20 mA) OHRCN				
Input Current (all external data pump inputs, except those listed in the next category):				
High (V_{IH} = V_{CC} + 5 V)	I_{IH}	—	10	µA
Low (V_{IL} = 0.0 V)	I_{IL}	—	10	µA
Input Current (V32-INTFC2 pins: PWRSTN, RDETN, HCSN, PSD, PRD, MBUS):				
High (V_{IH} = V_{CC} + 5 V)	I_{IH}	—	10	µA
Low (V_{IL} = 0.0 V)	I_{IL}	60	250	µA
Output 3-state Current:				
High (V_{OH} = 5.5 V)	I_{OZH}	—	10	µA
Low (V_{OL} = 0.0 V)	I_{OZL}	—	10	µA
Capacitance:				
Input Pins (fc = 1 MHz)	C_I	—	6	pF
Output, I/O Pins (fc = 1 MHz)	C_O	—	10	pF

* Signals RDETN, RTSN, and PWRSTN have a 0.3 V hysteresis window.

Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Voltage Range on Any Pin with Respect to Ground ..... –0.3 V to V_{CC} + 0.3 V
Ambient Temperature Range ..... 0 °C to 70 °C
Storage Temperature Range ..... –65 °C to +150 °C

Electrical Characteristics (continued)

BMC Device Electrical Characteristics

These parameters are valid for the following conditions: T_A = 0 to 70 °C, V_{CC} = 5 V ± 5%, G_{NDA} = G_{NDD} = 0 V.

Parameter	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input Voltage:						
Low ($\overline{\text{RESET}}$, EXTAL)	V_{IL1}		–0.3	—	0.6	V
Low (all other pins)	V_{IL2}		–0.3	—	0.8	V
High ($\overline{\text{RESET}}$, EXTAL)	V_{IH1}		Vcc – 1.0	—	Vcc + 0.3	V
High (all other pins)	V_{IH2}		2.0	—	Vcc + 0.3	V
Output Voltage:						
Low (all outputs)	V_{OL1}	I_{OL} = 2.0 mA	—	—	0.40	V
High (all outputs)	V_{OH1}	I_{OH} = –250 µA	2.4	—	—	V
		I_{OH} = –25 µA	Vcc – 1.2	—	—	V
Input Leakage Current (all inputs except XTAL, EXTAL)	I_{IL}	VIN = 0.5 Vcc – 0.5	—	—	10	µA
3-state Leakage Current	ITL	V_{IN} = 0.5 Vcc – 0.5	—	—	10	µA
Power Dissipation Normal*	Icc	f = 16 MHz	—	50	100	mA
Power Dissipation IDLE			—	5	10	mA
Power Dissipation STANDBY			—	10	10	µA
Pin Capacitance	CP	V_{IN} = 0 V, f = 1 MHz T_A = 25 °C	—	—	12	pF

*V_{IH} Min = Vcc – 1.0 V, VILmax = 0.8 V (all output terminals are at no load).

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Vcc Supply Voltage Range ..... –0.3 V to 7 V
Input Voltage Range ..... –0.3 V to Vcc + 0.3 V
Operating Temperature Range ..... 0 °C to 70 °C
Storage Temperature Range ..... –55 °C to 150 °C

Timing Characteristics and Requirements

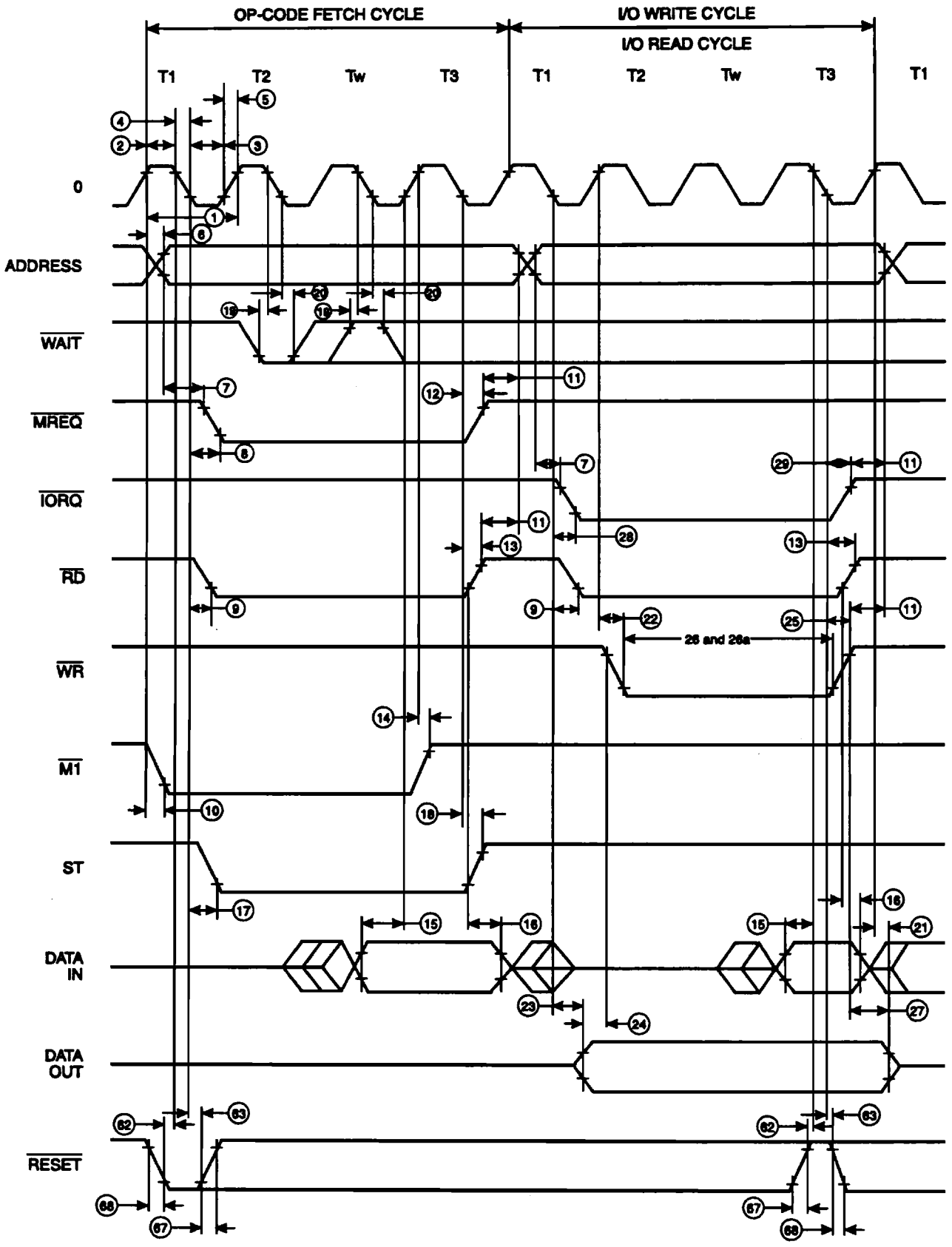
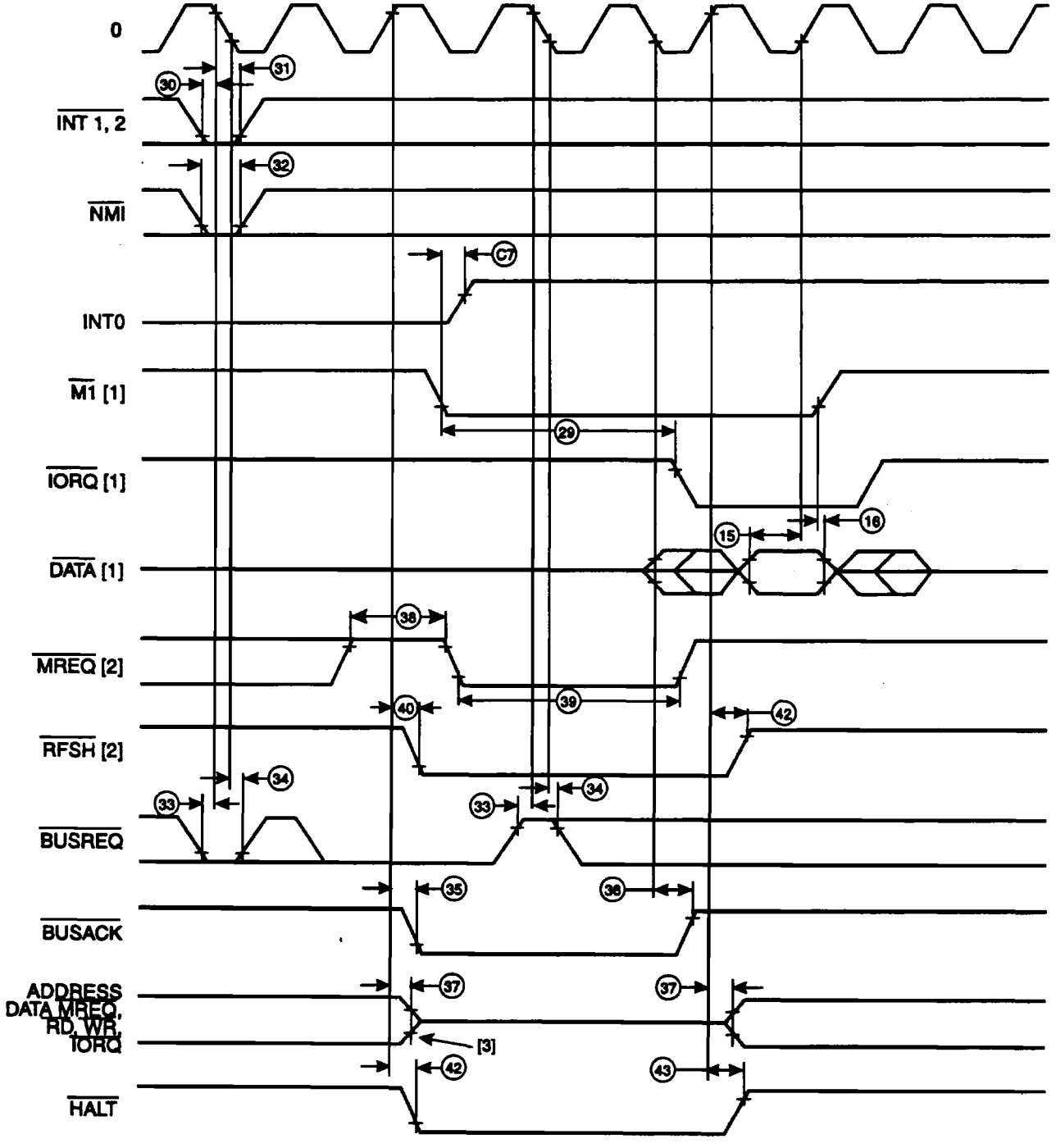


Figure 14. BMC Active Mode Timing

Timing Characteristics and Requirements (continued)



[1] During INTO acknowledge-cycle
[2] During refresh cycle
[3] Outpu buffer is off at this point

Figure 15. BMC Sleep Mode Timing

Timing Characteristics and Requirements (continued)

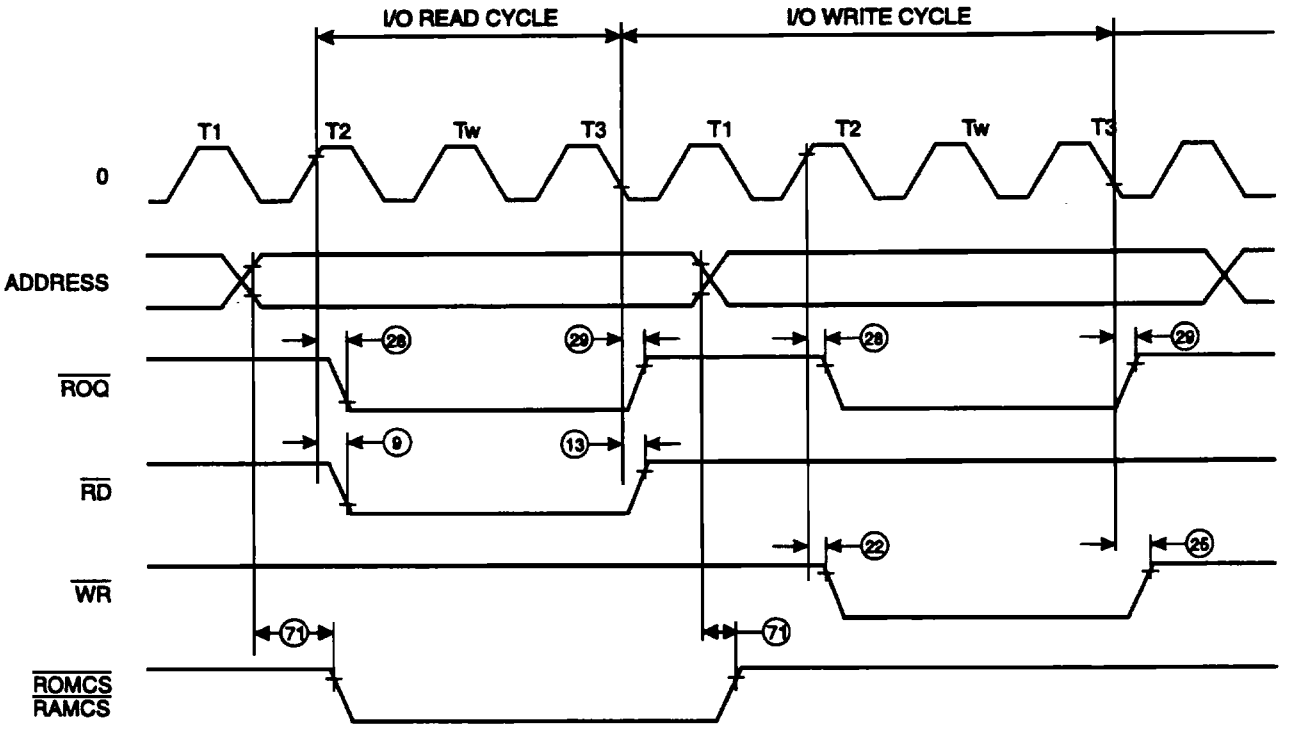


Figure 16. BMC Timing

Table 27. BMC Timing

NO	Sym	Parameter	BMC		Unit	Note
			Min	Max		
1	tcyc	Clock Cycle Time	62	dc	ns	[1]
2	tCHW	Clock Pulse Width (High)	26	dc	ns	[1]
3	tCLW	Clock Pulse Width (Low)	26	dc	ns	[1]
4	tcf	Clock Fall Time		5	ns	[1]
5	tcr	Clock Rise Time		5	ns	[1]
6	tAD	Address Valid from Clock Rise		14	ns	
7	tAS	Address Valid to $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{MRD}}$ Fall	5		ns	
8	tMED1	Clock Fall to $\overline{\text{MREQ}}$ Fall Delay		25	ns	
9	tRDD1	Clock Fall to $\overline{\text{RD}}$, $\overline{\text{MRD}}$ (/IOC = 1) Clock Rise to $\overline{\text{RD}}$, $\overline{\text{MRD}}$ Fall (/IOC = 0)		25 25	ns ns	
10	tM1D1	Clock Rise to $\overline{\text{M1}}$ Fall Delay		45	ns	
11	tAH	Address Hold Time ($\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MRD}}$)	18		ns	
12	tMED2	Clock Fall to $\overline{\text{MREQ}}$ Rise Delay		12	ns	
13	tRDD2	Clock Fall to $\overline{\text{RD}}$, $\overline{\text{MRD}}$ Rise Delay		12	ns	
14	tM1D2	Clock Rise to $\overline{\text{M1}}$ Rise Time		45	ns	

Timing Characteristics and Requirements (continued)

Table 28. BMC Timing (continued)

NO	Sym	Parameter	BMC Min	BMC Max	Unit	Note
15	tDRS	Data Read Setup Time	19		ns	
16	tDRH	Data Read Hold Time	0		ns	
17	tSTD1	Clock Edge to ST Fall		35	ns	
18	tSTD2	Clock Edge to ST Rise		35	ns	
19	tWS	$\overline{WAIT}$ Setup Time to Clock Fall	15		ns	[2]
20	tWH	$\overline{WAIT}$ Hold Time from Clock Fall	10		ns	
21	tWDZ	Clock Rise to Data Float Delay		40	ns	
22	tWRD1	Clock Rise to $\overline{WR}$, $\overline{MWR}$ Fall Delay		25	ns	
23	tWDD	Clock Fall to Write Data Delay		30	ns	
24	tWDS	Write Data Setup Time to $\overline{WR}$, $\overline{MWR}$ Fall	10		ns	
25	tWRD2	Clock Fall to $\overline{WR}$ Rise		12	ns	
26	tWRP	$\overline{WR}$ Pulse Width (memory write cycles)	80		ns	
26a		$\overline{WR}$ Pulse Width (I/O write cycles)	150		ns	
27	tWDH	Write Data Hold Time from $\overline{WR}$ Rise	10		ns	
28	tIOD1	Clock Fall to $\overline{IORQ}$ Fall Delay (/IOC = 1) Clock Rise to $\overline{IORQ}$ Fall Delay (/IOC = 0)		30 30	ns ns	
29	tIOD2	Clock Fall $\overline{IORQ}$ Rise Delay		12	ns	
30	tIOD3	$\overline{M1}$ Fall to $\overline{IORQ}$ Fall Delay	120		ns	
31	tINTS	$\overline{INT}$ Setup Time to Clock Fall	20		ns	
32	tINTH	$\overline{INT}$ Hold Time from Clock Fall	10		ns	
33	tNMIW	$\overline{NMI}$ Pulse Width	40		ns	
34	tBRS	$\overline{BUSREQ}$ Setup Time to Clock Fall	10		ns	
35	tBRH	$\overline{BUSREQ}$ Hold Time from Clock Fall	10		ns	
36	tBAD1	Clock Rise to $\overline{BUSACK}$ Fall Delay		30	ns	
37	tBAD2	Clock Fall to $\overline{BUSACK}$ Rise Delay		30	ns	
38	tBZD	Clock Rise to Bus Floating Delay Time		45	ns	
39	tMEWH	$\overline{MREQ}$ Pulse Width (High)	45		ns	
40	tMEWL	$\overline{MREQ}$ Pulse Width (Low)	45		ns	
42	tRFD2	Clock Rise to $\overline{RFSH}$ Rise Delay		25	ns	
43	tHAD1	Clock Rise to $\overline{HALT}$ Fall Delay		20	ns	
62	tRES	$\overline{RESET}$ Setup Time to Clock Fall	45		ns	
63	tREH	$\overline{RESET}$ Hold Time from Clock Fall	30		ns	

Timiing Characteristics and Requirements (continued)

Table 29. BMC Timing (continued)

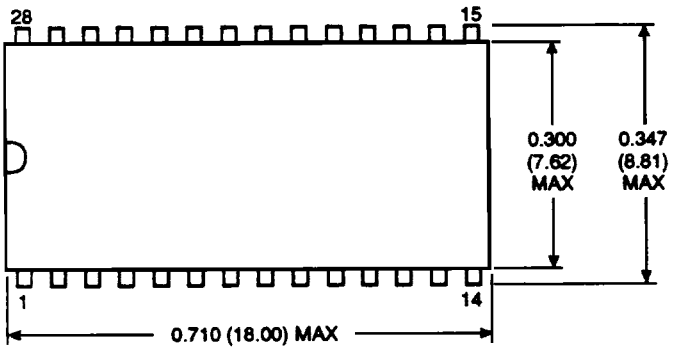
NO	Sym	Parameter	BMC		Unit	Note
			Min	Max		
67	tRr	$\overline{\text{RESET}}$ Rise Time		50	ns	[2]
68	tRf	$\overline{\text{RESET}}$ Fall Time		550	ns	[2]
C7	ThRxD(RxCf)	RxD to $\overline{\text{RXC}}$ Hold Time	50		ns	[3]
71	Tdcs	Address valid to $\overline{\text{ROMCS}}$, $\overline{\text{RAMCS}}$ Valid Delay		24	ns	—

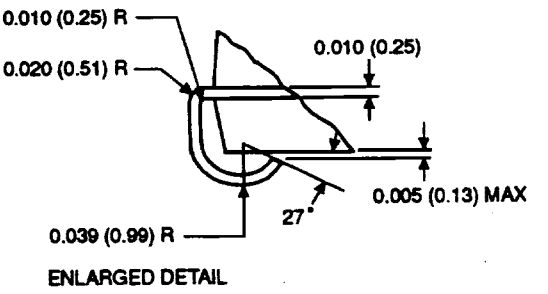
[1] tcyc = tCHW + tCLW + tcf + tcr
[2] This parameter has to be modified if other specification(s) cannot be met.

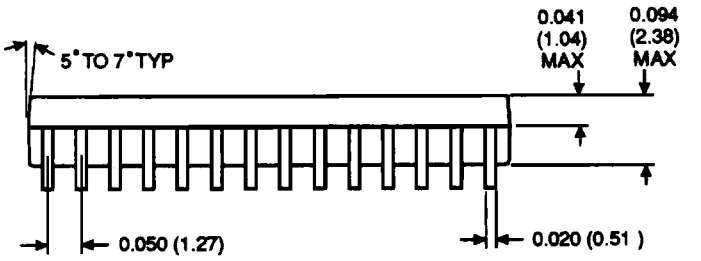
Pin Outline Diagrams

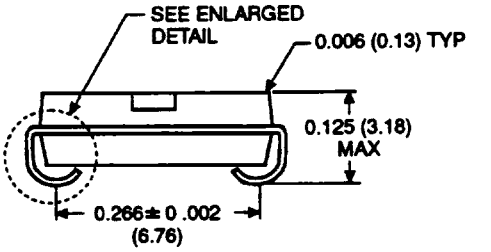
28-Pin SOJ For AT&T T7525 Codec

Dimensions are in inches and (millimeters).







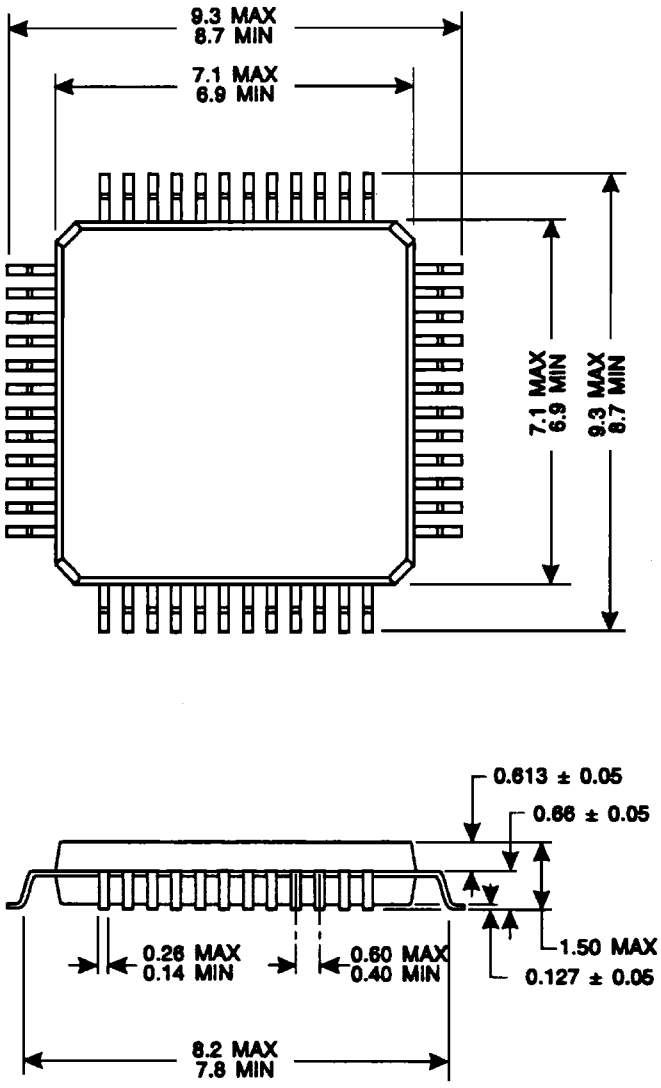


Note: Chip die to ambient thermal resistance is 75° C/W.

Pin Outline Diagrams (continued)

48-Pin TQFP for CSP1027 Codec

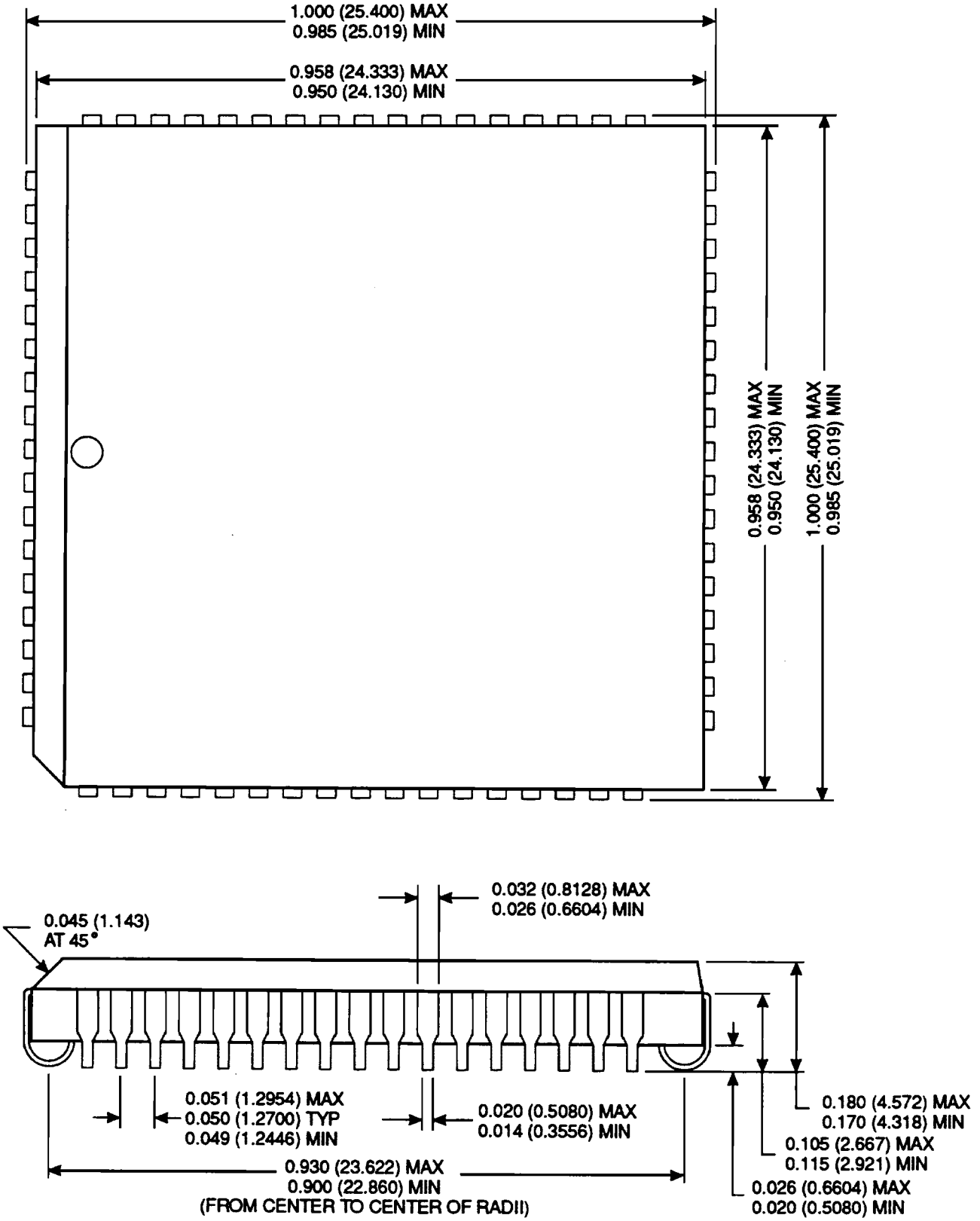
Dimensions are in millimeters.



Pin Outline Diagrams (continued)

68-Pin PLCC for AT&T V32-INTFC2

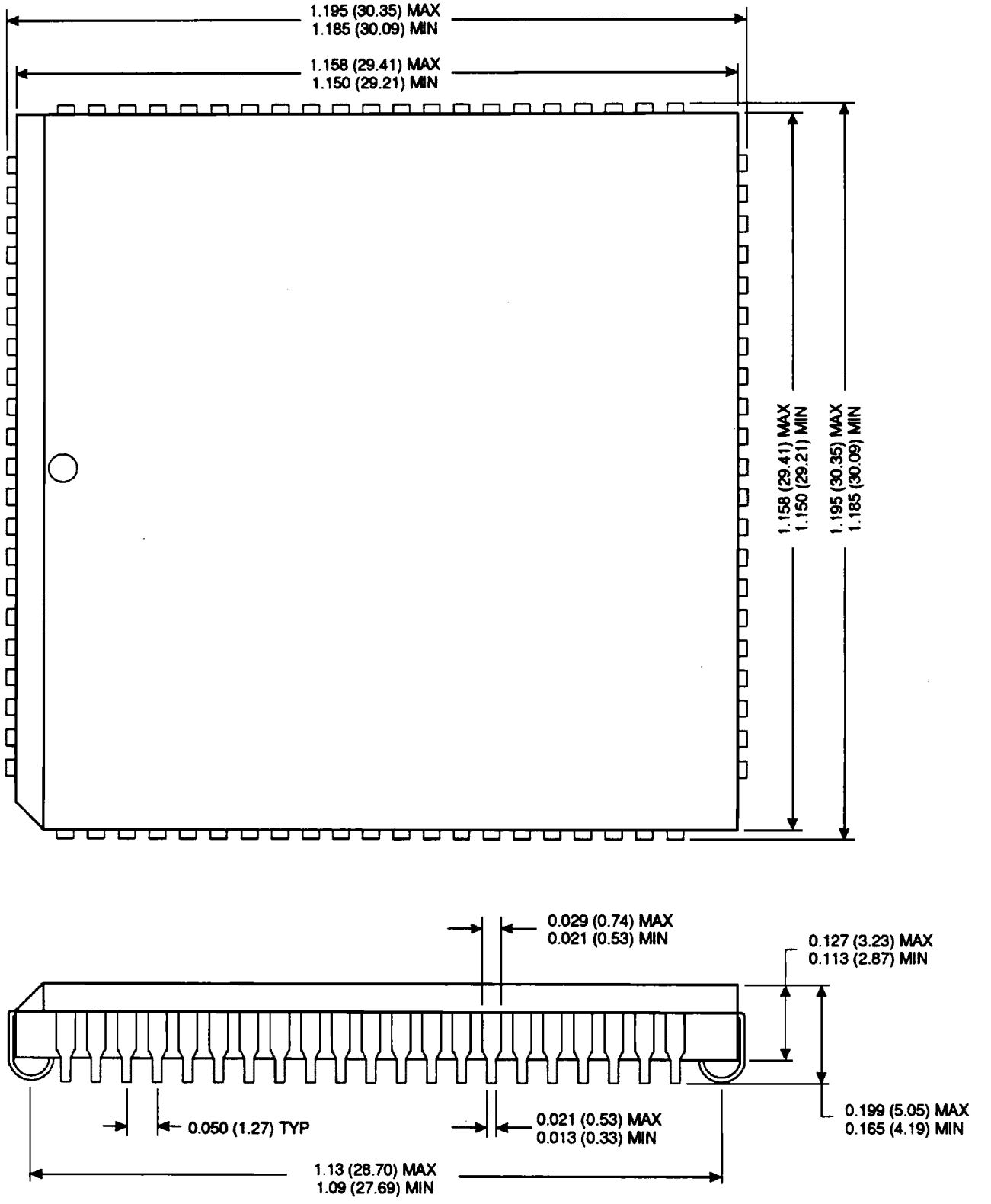
Dimensions are in inches and (millimeters).



Pin Outline Diagrams (continued)

84-Pin PLCC for AT&T DSP16A

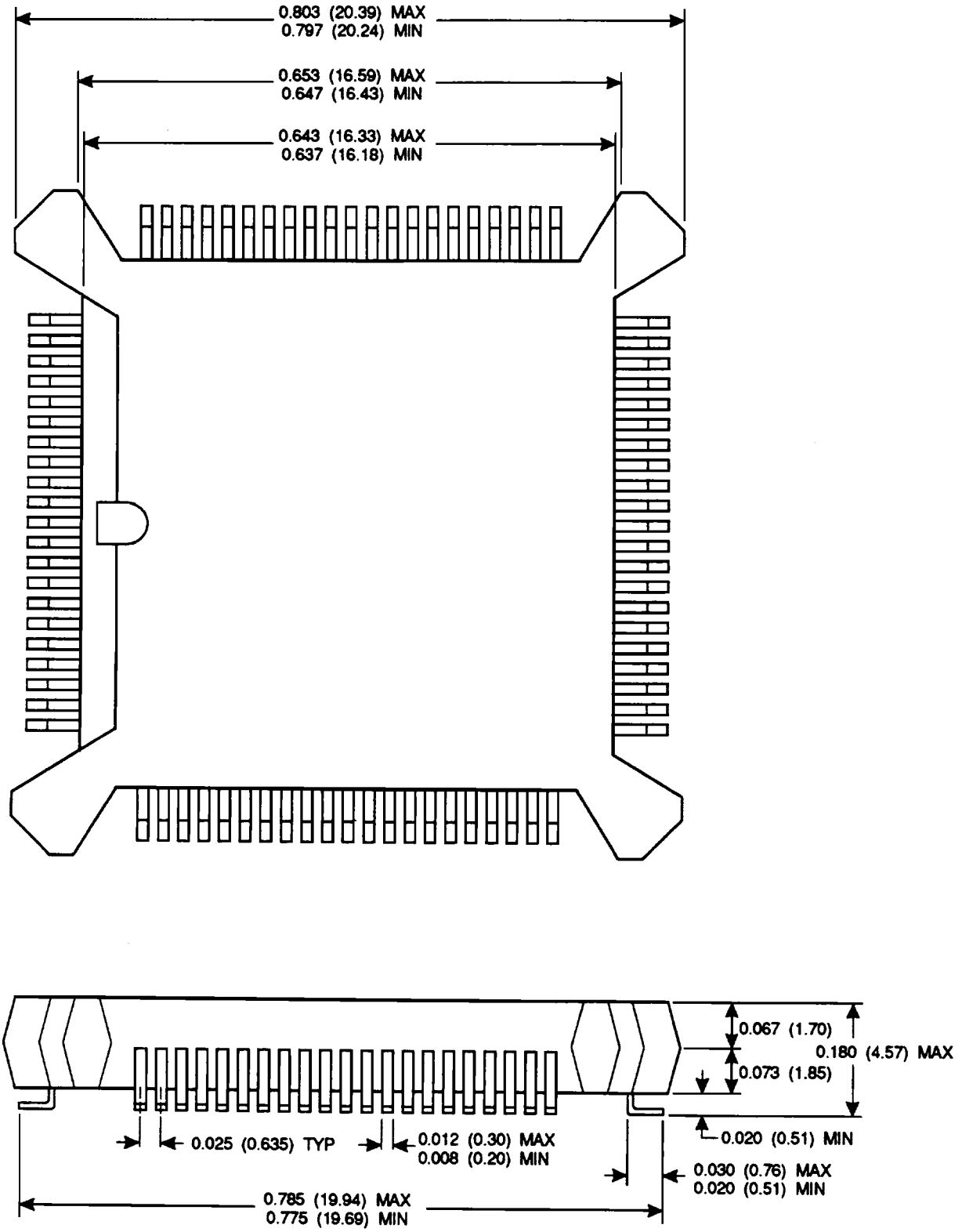
Dimensions are in inches and (millimeters).



Pin Outline Diagrams (continued)

84-Pin PQFP for AT&T DSP16A and AT&T V32-INTFC2

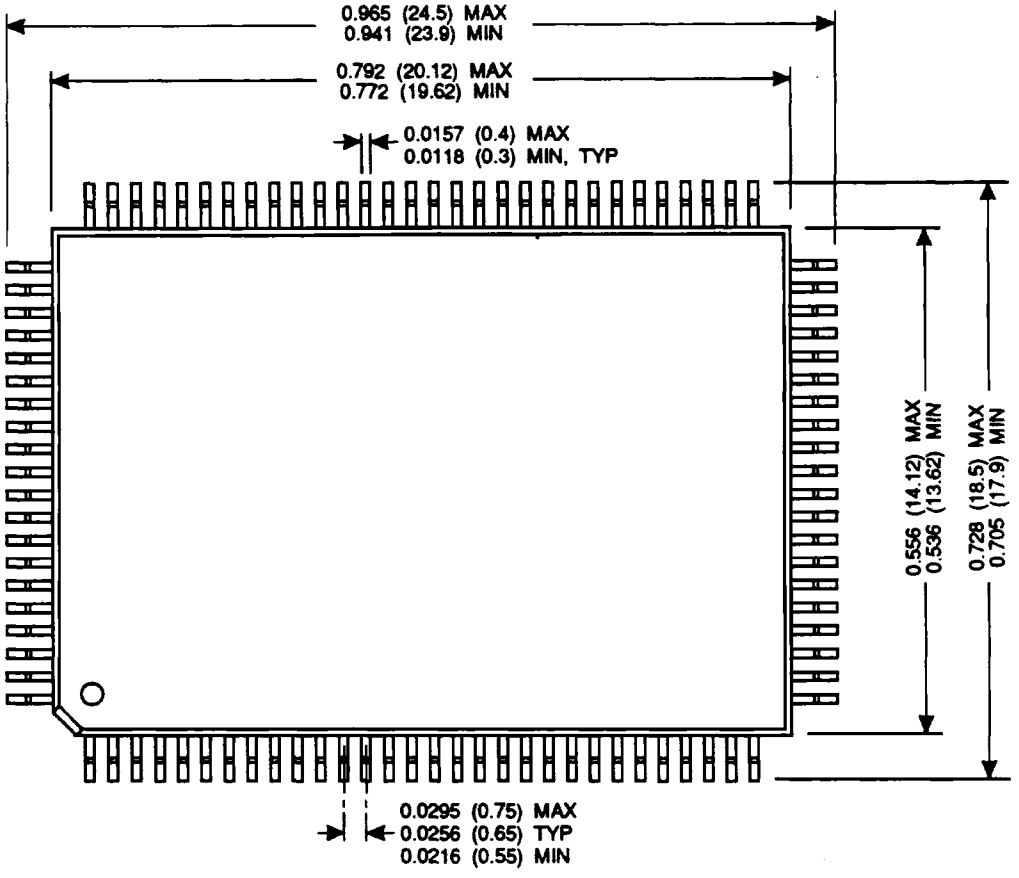
Dimensions are in inches and (millimeters).

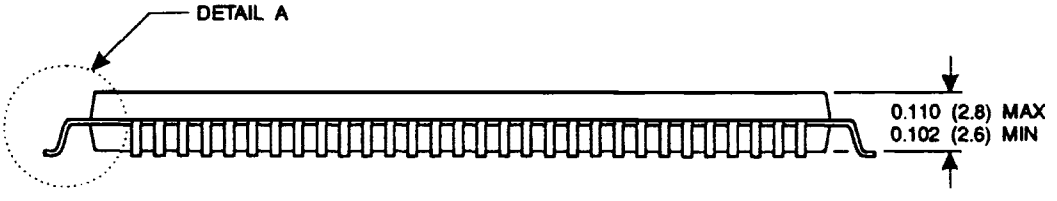


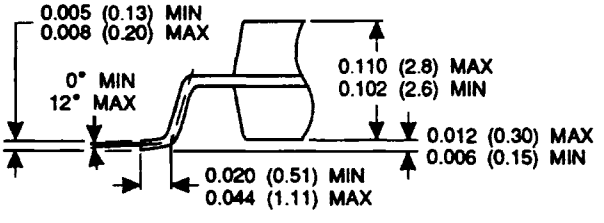
Pin Outline Diagrams (continued)

100-Pin QFP for AT&T BMC

Dimensions are in inches and (millimeters).





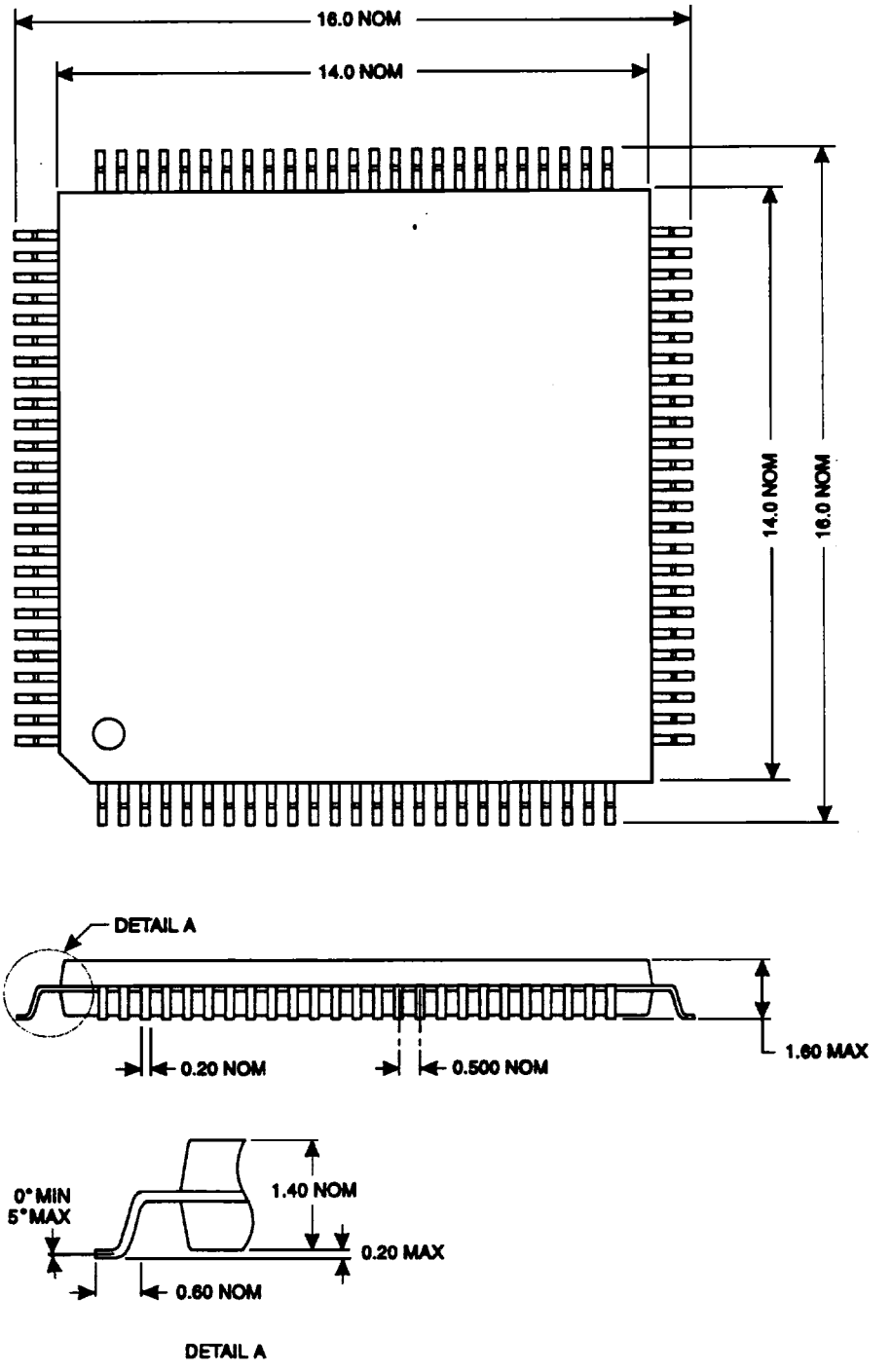


DETAIL A

Pin Outline Diagrams (continued)

100-Pin VQFP for AT&T BMC

Dimensions are in millimeters.



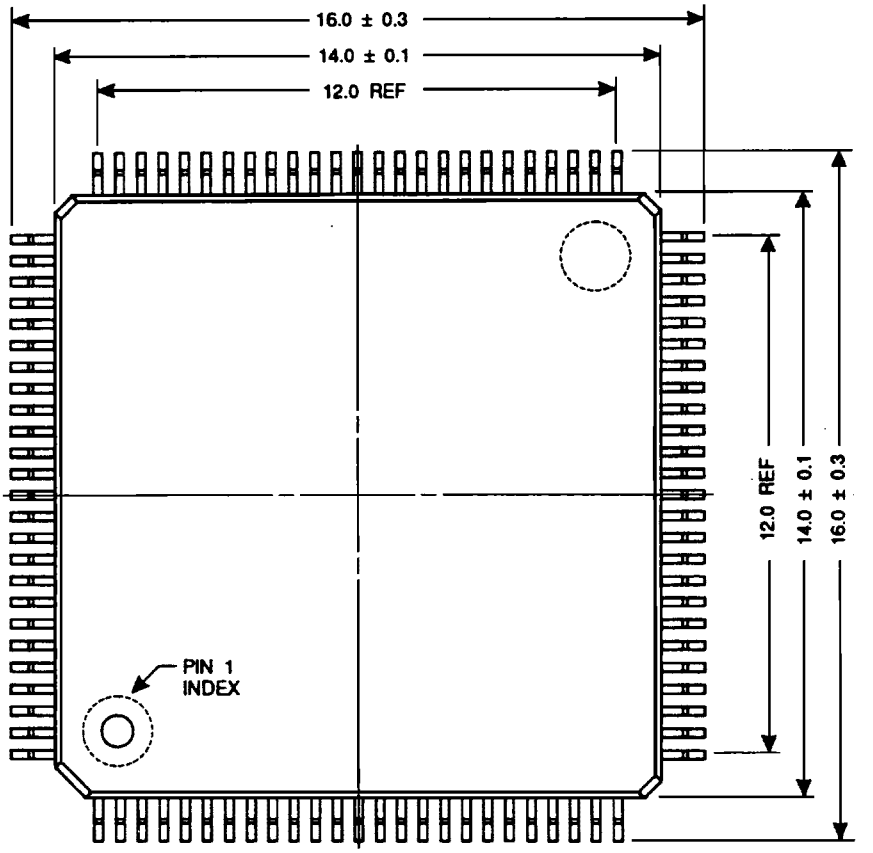
Notes:

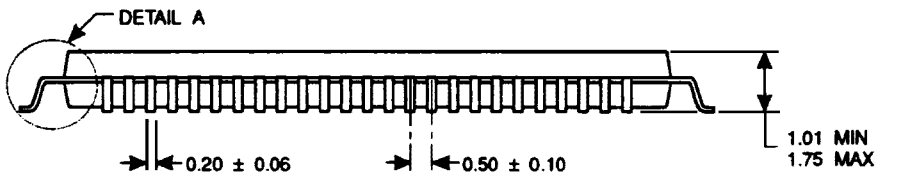
Solderability	MIL-STD-883C Method 2003.5 8 Hours Steam Age
Mark Permanency	3X Soak into trichlorethane 1.1.1 1 Min. duration each soak Mech. brush after each soak
Coplanarity	Maximum 4 mils deviation

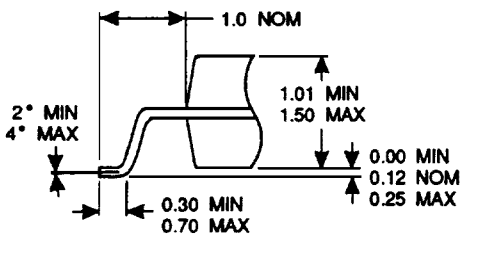
Pin Outline Diagrams (continued)

100-Pin TQFP for AT&T DSP16A and AT&T V32-INTFC2

Dimensions are in millimeters.

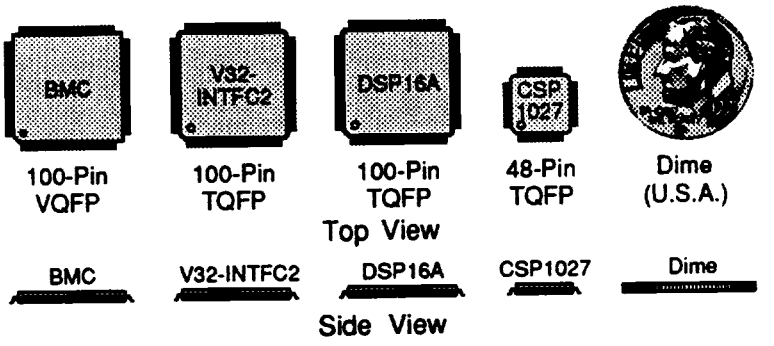




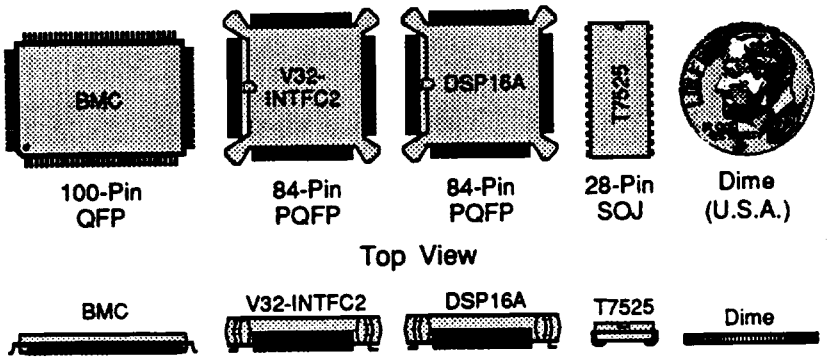


DETAIL A

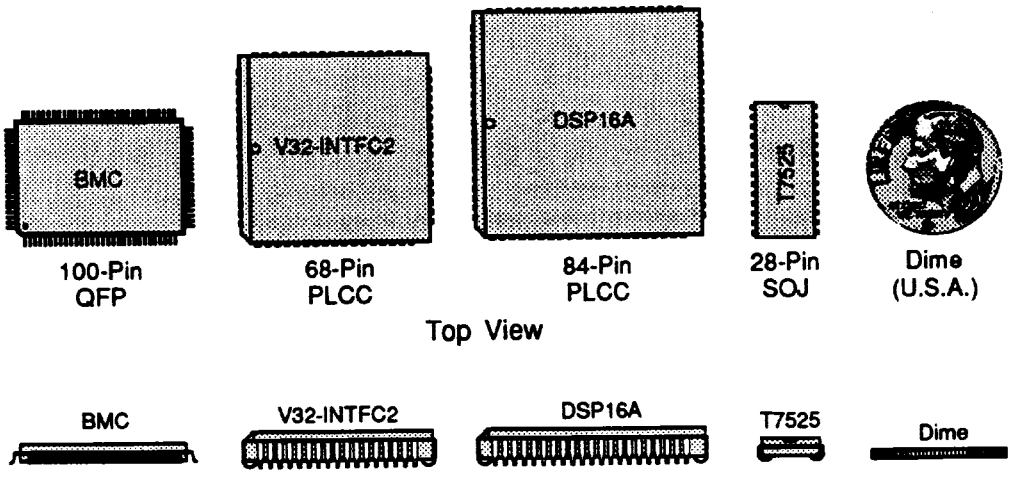
Package Options



A. PCMCIA Option



B. LapTop Option



C. DeskTop Option

Figure 17. AT&T HSM Complete Modem Chip Sets Package Size Comparison