Integrated Device Technology, Inc.

16 x 16-BIT PARALLEL CMOS MULTIPLIER WITH 32-BIT OUTPUT

PRELIMINARY
IDT 7317

FEATURES

- 16 x 16-bit parallel multiplier with 32-bit output available immediately
- 20ns clocked multiply time
- Low power consumption: 400mW Max.
- One clock and three register enables
- Unsigned, Two's Complement or Mixed-Mode operations
- Flexible output scaling shifter
- Pipeline or Flow-through modes
- TTL-compatible input/output
- Three-state outputs
- Produced with advanced submicron CEMOS™ technology
- Available in 84-pin PLCC and 84-lead Pin Grid Array (PGA)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

The IDT7317 is high-speed, low-power 16 x 16-bit multiplier that has double the throughput of comparable devices by virtue of a full 32-bit output product bus. The Most Significant Product (MSP) and Least Significant Product (LSP) can be independently enabled on an external 16-bit bus or simultaneously enabled on an external 32-bit bus. IDT's high-performance CEMOS™ technology produces very fast (20ns) clocked multiply times.

The output structure includes a programmable one-bit shifter for improved dynamic range algorithms using block floating point. This multiplier offers flexible configurations for clocked and flowed-through multiplications.

The IDT7317 is ideal for digital signal processing (DSP) applications requiring single-cycle 32-bit integer products. Some typical applications for this multiplier are 1-D and 2-D fast Fourier transforms (FFT), matrix multiplications, FIR and IIR filtering.

Military versions of the IDT7317 are manufactured in compliance with the latest revision of MIL-STD-883, Class B for high-reliability systems.

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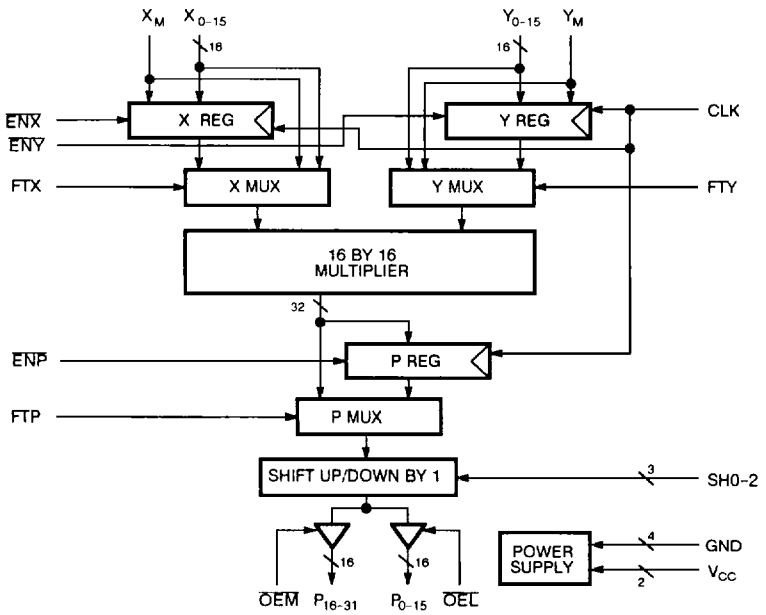
FUNCTIONAL BLOCK DIAGRAMS



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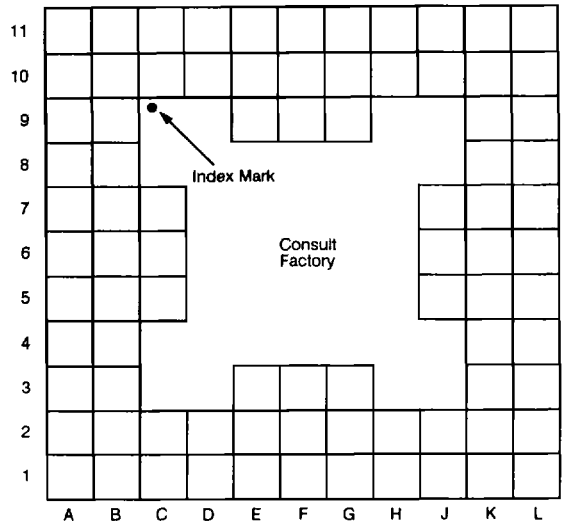
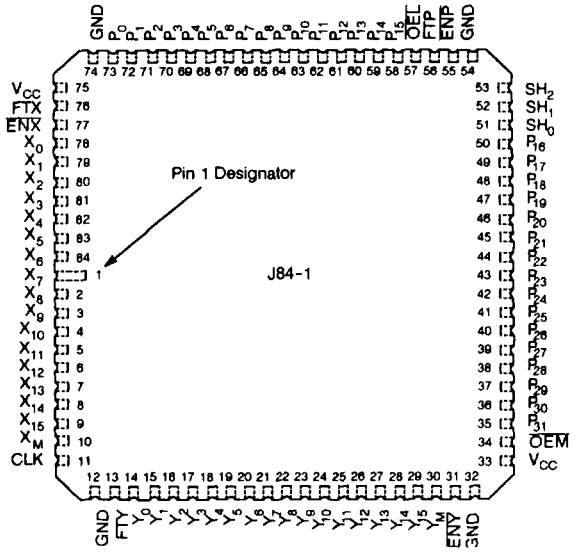


PGA TOP VIEW



PLCC TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
X_0 - X_{15}	I	Sixteen multiplicand data inputs.
XM	I	Mode control for X data input port. A LOW designates unsigned data input and a HIGH designates two's complement data input.
Y_0 - Y_{15}	I	Sixteen multiplier data inputs.
YM	I	Mode control for Y data input port. A LOW designates unsigned data input and a HIGH designates two's complement data input.
CLK	I	The rising edge of the clock loads all registers.
$\overline{ENX}$	I	Register enable for the X data input port along with the XM pin.
$\overline{ENY}$	I	Register enable for the Y data input port along with the YM pin.
$\overline{ENP}$	I	Register enable for the P output product.
FTX	I	When this control is HIGH, the X register is transparent; X input data and XM are not clocked.
FTY	I	When this control is HIGH, the Y register is transparent; Y input data and YM are not clocked.
FTP	I	When this control is HIGH, the P register is transparent; P output data is not clocked.
SH_0 - SH_2	I	Controls output product shifting. Shifting is controlled as follows:

SH_2	SH_1	SH_0	ACTION
0	X	X	no shift.
1	0	0	arithmetic shift left (up) by 1 position with 0 fill.
1	0	1	logical shift left (up) by 1 position with 0 fill.
1	1	0	arithmetic shift right (down) by 1 position with sign extension.
1	1	1	logical shift right (down) by 1 position with 0 fill.

$\overline{OEM}$	I	Three-state enable for most significant product (P_{16} - P_{31}).
$\overline{OEL}$	I	Three-state enable for least significant product (P_0 - P_{15}).
P_0 - P_{15}	O	Sixteen least significant product outputs.
P_{16} - P_{31}	O	Sixteen most significant product outputs.
V_{CC}		Two power pins at +5V potential nominal.
GND		Four ground pins.

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled at initial characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open; f = 20MHz	–	30	60	–	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	15	35	–	15	45	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq$ 0.2V	–	2	10	–	2	15	mA
I_{CC}/f (2,3)	Increase in Power Supply Current MHz	V_{CC} = Max., f > 20MHz	–	–	4	–	–	6	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4mA	–	–	0.4	–	–	0.4	V

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 20MHz and V_{IN} = 0 to 3V. For frequencies greater than 20MHz, the following equation are used; for the commercial range, I_{CC} = 60 +4(f-20)mA; for the military range, I_{CC} = 80 + 6(f-20)mA; f is the operating frequency in MHz.
3. These limits are guaranteed but not tested..

AC ELECTRICAL CHARACTERISTICS – COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	7317L20		7317L35		7317L55		7317L75		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{MUC}	Unlocked Multiply Time[2]	–	35	–	55	–	75	–	100	ns
t_{MC}	Clocked Multiply Time[2]	–	20	–	35	–	55	–	75	ns
t_{SD}	X,Y Input Data Set-up Time[2]	8	–	10	–	13	–	18	–	ns
t_{HD}	X,Y Input Data Hold Time[2]	2	–	2	–	2	–	2	–	ns
t_{SE}	Clock Enable Set-up Time[2]	8	–	8	–	8	–	8	–	ns
t_{HE}	Clock Enable Hold Time[2]	2	–	2	–	2	–	2	–	ns
t_{PWH}	Clock Pulse Width High[2]	9	–	10	–	15	–	20	–	ns
t_{PWL}	Clock Pulse Width Low[2]	9	–	10	–	15	–	20	–	ns
t_{PDP}	Clock Output to P[2]	–	18	–	25	–	30	–	35	ns
t_{ENA}	3-State Enable Time[1]	–	18	–	25	–	30	–	35	ns
t_{DIS}	3-State Disable Time[1]	–	15	–	22	–	25	–	30	ns

NOTE:
1. Transition is measured +500mV from steady-state voltage with loading specified in Figure 1. V_X = 0 V and 2.6 V.
2. I_{OL} = 3.2 mA and I_{OH} = -0.8 mA during AC tests.

AC ELECTRICAL CHARACTERISTICS – MILITARY (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	7317L25		7317L40		7317L65		7317L90		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{MUC}	Unlocked Multiply Time[2]	–	38	–	60	–	85	–	125	ns
t_{MC}	Clocked Multiply Time[2]	–	25	–	40	–	65	–	90	ns
t_{SD}	X,Y Input Data Set-up Time[2]	12	–	15	–	20	–	25	–	ns
t_{HD}	X,Y Input Data Hold Time[2]	2	–	3	–	3	–	3	–	ns
t_{SE}	Clock Enable Set-up Time[2]	12	–	15	–	15	–	15	–	ns
t_{HE}	Clock Enable Hold Time[2]	2	–	3	–	3	–	3	–	ns
t_{PWH}	Clock Pulse Width High[2]	10	–	12	–	15	–	25	–	ns
t_{PWL}	Clock Pulse Width Low[2]	10	–	12	–	15	–	25	–	ns
t_{PDP}	Clock Output to P[2]	–	20	–	25	–	30	–	40	ns
t_{ENA}	3-State Enable Time[1]	–	20	–	25	–	30	–	40	ns
t_{DIS}	3-State Disable Time[1]	–	18	–	22	–	30	–	35	ns

NOTE:
1. Transition is measured +500mV from steady-state voltage with loading specified in Figure 1. V_X = 0 V and 2.6 V.
2. I_{OL} = 3.2 mA and I_{OH} = -0.8 mA during AC tests.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

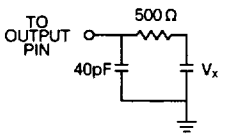

Figure 1. AC Output Test Load (V_X = 2.0V except for t_{DIS} and t_{ENA})

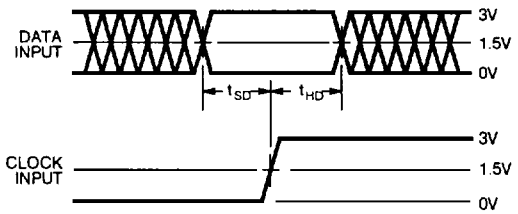

Figure 2. Set-Up And Hold Time

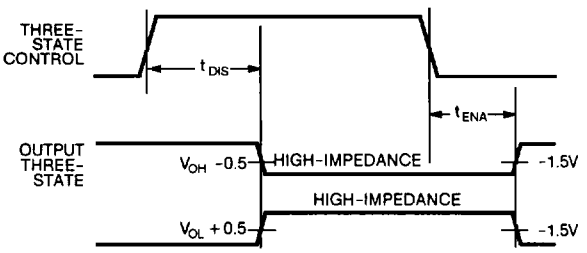

Figure 3. Three-State Control Timing Diagram

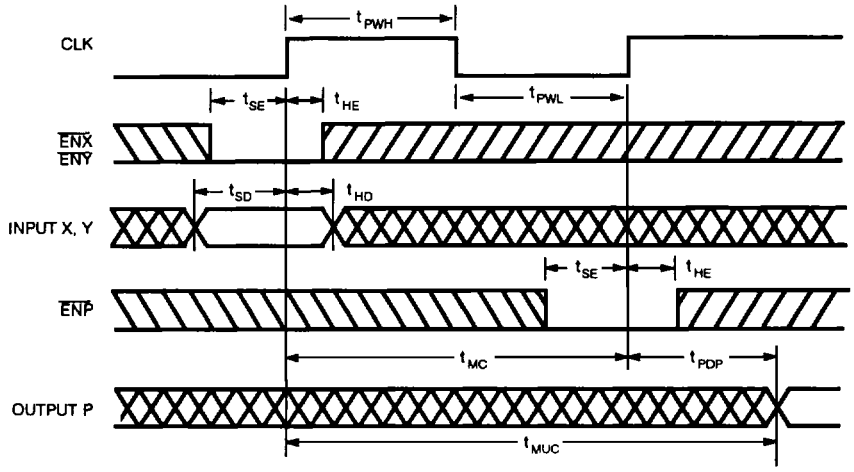

Figure 4. IDT7317 Timing Diagram

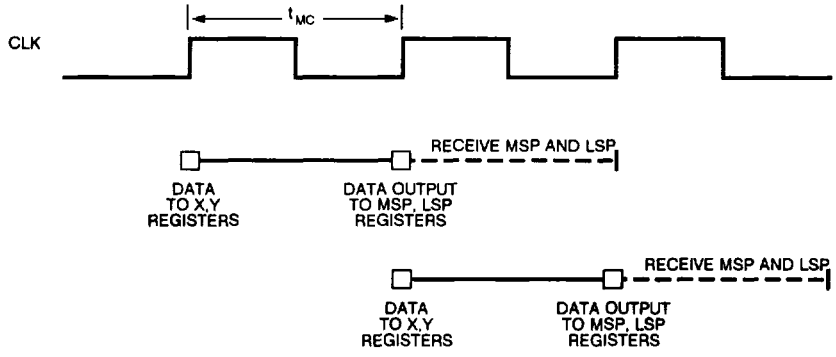

Figure 5. Simplified Timing Diagram-Typical Application

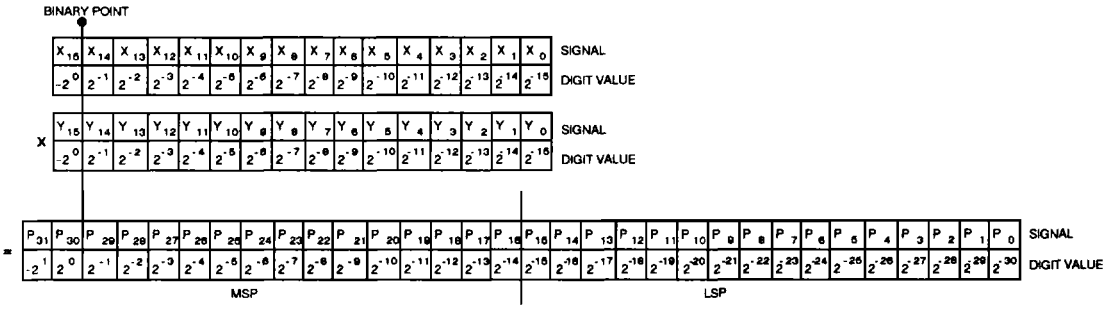

Figure 6. Fractional Two's Complement Notation

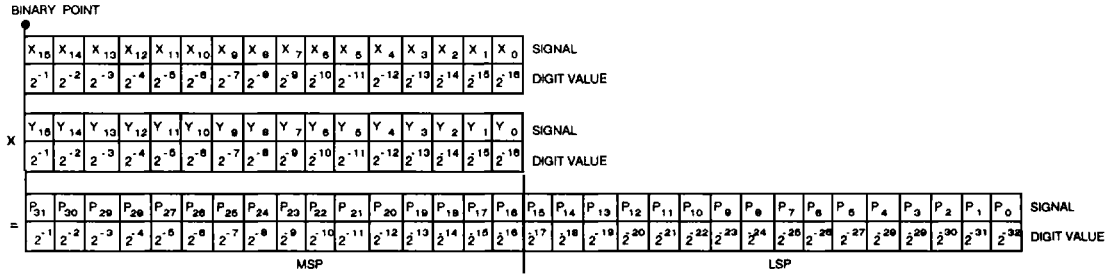

Figure 7. Fractional Unsigned Magnitude Notation

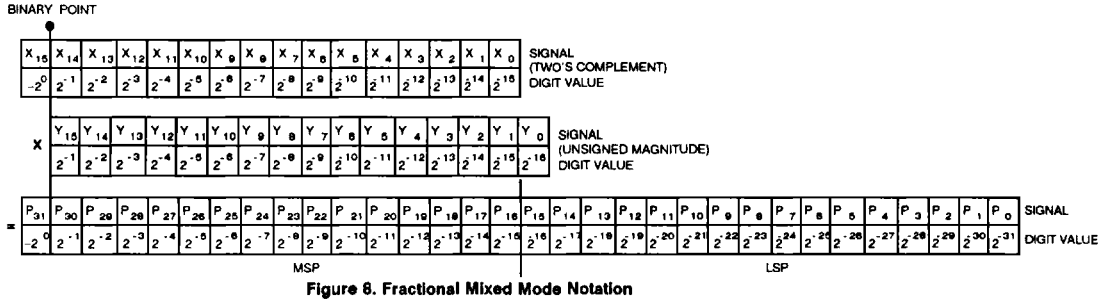

Figure 8. Fractional Mixed Mode Notation

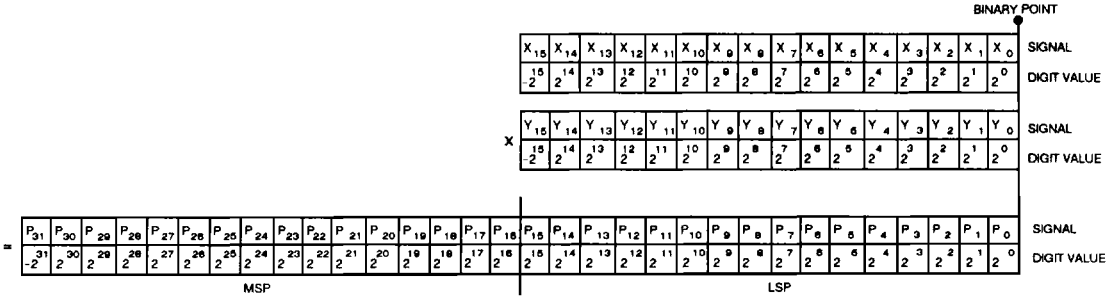

Figure 9. Integer Two's Complement Notation

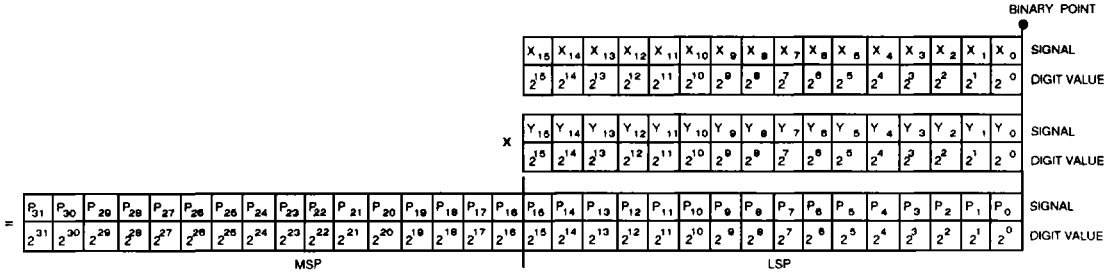

Figure 10. Integer Unsigned Magnitude Notation

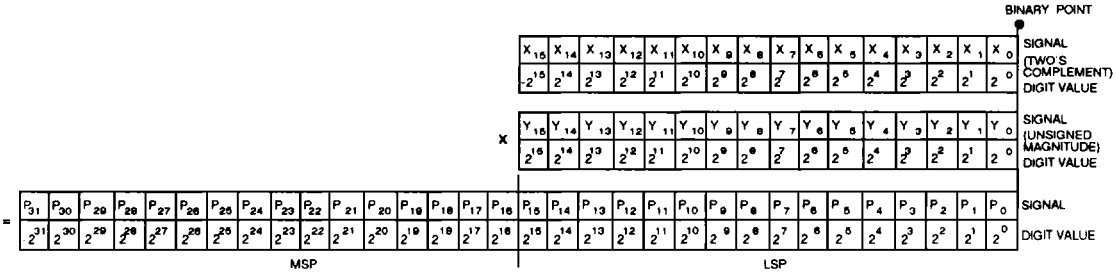

Figure 11. Integer Mixed Mode Notation

ORDERING INFORMATION