



L8115

LINEAR INTEGRATED CIRCUIT

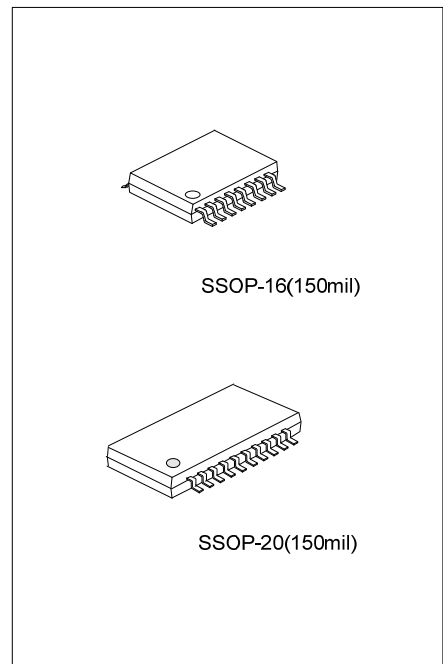
FET BIAS CONTROLLER WITH POLARIZATION SWITCH AND TONE DETECTION

DESCRIPTION

The UTC **L8115** is designed to bias the MOSFETs that are commonly used in LNBS that can implies minimum external components requires.

FEATURES

- * Can bias up to 3 FETs
- * HB and LB switch for LNBS.
- * Drain current adjustable by external resistors.
- * Band switching by 22KHz tone detection.



Lead-free: L8115L

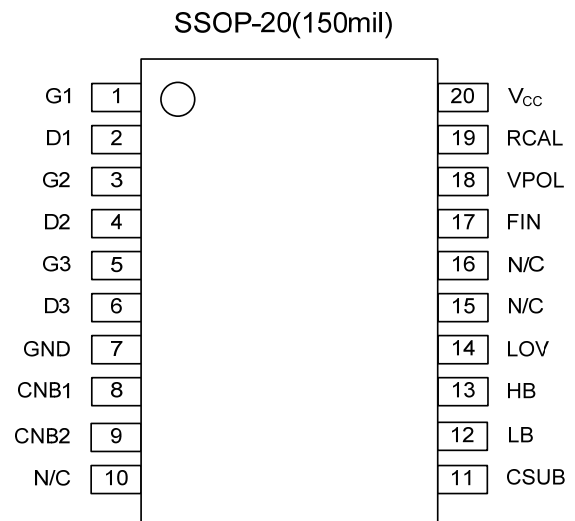
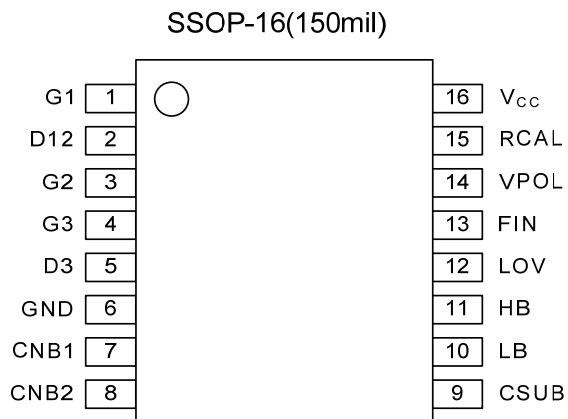
Halogen-free: L8115G

ORDERING INFORMATION

Normal	Ordering Number		Package	Packing
	Lead Free Plating	Halogen Free		
L8115-R16-R	L8115L-R16-R	L8115G-R16-R	SSOP-16	Tape Reel
L8115-R20-R	L8115L-R20-R	L8115G-R20-R	SSOP-20	Tape Reel

<p>L8115L-R16-R</p> <p>(1)Packing Type (2)Package Type (3)Lead Plating</p>	<p>(1) R: Tape Reel (2) R16: SSOP-16, R20: SSOP-20 (3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn</p>
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■ PIN CONFIGURATION



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.6 ~ +12	V
Input Voltage	V_{IN}	25 Continuous	V
Supply Current	I_{CC}	100	mA
Drain Current (per FET)(set by RCAL)	I_D	0 ~ 15	mA
Power Dissipation($T_a=25^\circ\text{C}$)	P_D	500	mW
Operating Temperature	T_{OPR}	-40~+80	$^\circ\text{C}$
Storage Temperature	T_{STG}	-50~+85	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

($T_a=25^\circ\text{C}$, $V_{CC}=5\text{V}$, $I_D=10\text{mA}$, $R_{CAL}=33\text{K}\Omega$, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Supply Voltage	V_{CC}		5		10	V	
Supply Current	I_{CC}	$I_{D1}=I_{D2}$ (or $I_{D12})=I_{D3}=0$		8.5	15	mA	
		$I_{D1}=0, I_{D2}$ (or $I_{D12})=I_{D3}=10\text{mA}$, $V_{POL}=14\text{V}$		28	35	mA	
		$I_{D2}=0, I_{D1}$ (or $I_{D12})=I_{D3}=10\text{mA}$, $V_{POL}=15.5\text{V}$		28	35	mA	
		I_{D1} and $I_{D3}=0$, $I_{LB}=10\text{mA}$		18	25	mA	
		I_{D1} and $I_{D3}=0$, $I_{HB}=10\text{mA}$		18	25	mA	
Substrate Voltage	V_{SUB}	(Internally generated)	$I_{SUB}=0$	-3.05	-2.8	-2.55	V
			$I_{SUB}=-200\mu\text{A}$			-2.4	V
Output Noise	Gate Voltage	E_{NG}	$C_G=4.7\text{nF}, C_D=10\text{nF}$		0.005	Vpkpk	
	Drain Voltage	E_{ND}			0.02	Vpkpk	
Oscillator Frequency	f_{OSC}		180	330	800	kHz	

■ GATE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT		
Output Current Range	I_{GO}		-30		2000	μA		
Output Voltage Gate 1	Off	V_{G1O}	$I_{D1}=0\text{mA}$, $V_{POL}=14\text{V}$, $I_{GO1}=-10\mu\text{A}$		-2.5	-2.25	-2	V
	Low	V_{G1L}	$I_{D1}=12\text{mA}$, $V_{POL}=15.5\text{V}$, $I_{GO1}=-10\mu\text{A}$		-2.5	-2.25	-2	V
	High	V_{G1H}	$I_{D1}=8\text{mA}$, $V_{POL}=15.5\text{V}$, $I_{GO1}=0\mu\text{A}$		0.4	0.75	1	V
Output Voltage Gate 2	Off	V_{G2O}	$I_{D2}=0\text{mA}$, $V_{POL}=15.5\text{V}$, $I_{GO2}=-10\mu\text{A}$		-2.5	-2.25	-2	V
	Low	V_{G2L}	$I_{D2}=12\text{mA}$, $V_{POL}=14\text{V}$, $I_{GO2}=-10\mu\text{A}$		-2.5	-2.25	-2	V
	High	V_{G2H}	$I_{D2}=8\text{mA}$, $V_{POL}=14\text{V}$, $I_{GO2}=0\mu\text{A}$		0.4	0.75	1	V
Output Voltage Gate 3	Low	V_{G3L}	$I_{D3}=12\text{mA}$, $I_{GO3}=-10\mu\text{A}$		-3	-2.75	-2	V
	High	V_{G3H}	$I_{D3}=8\text{mA}$, $I_{GO3}=0\mu\text{A}$		0.4	0.75	1	V

■ DRAIN CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current	I_D		8	10	12	mA
Current range	I_{DRNG}	Set by R_{CAL}	0		15	mA
Current Change	With V_{CC}	ΔI_{DV}	$V_{CC}=5 \sim 10\text{V}$		0.5	%/V
	With T_J	ΔI_{DT}	$T_J=-40 \sim +70^\circ\text{C}$		0.05	%/ $^\circ\text{C}$
Drain 1 Voltage: High	V_{D1}	$I_{D1}=10\text{mA}, V_{POL}=15.5\text{V}$	2	2.2	2.4	V
Drain 2 Voltage: High	V_{D2}	$I_{D2}=10\text{mA}, V_{POL}=14\text{V}$	2	2.2	2.4	V
Drain 3 Voltage: High	V_{D3}	$I_{D3}=10\text{mA}, V_{POL}=15.5\text{V}$	2	2.2	2.4	V
Voltage Change	With V_{CC}	ΔV_{DV}	$V_{CC}=5 \sim 10\text{V}$		0.5	%/V
	With T_J	ΔV_{DT}	$T_J=-40 \sim +70^\circ\text{C}$		50	ppm
Leakage Current (SSOP-20 only)	Drain 1	I_{LEAK1}	$V_{D1}=0.5\text{V}, V_{POL}=14\text{V}$		10	μA
	Drain 2	I_{LEAK2}	$V_{D2}=0.5\text{V}, V_{POL}=15.5\text{V}$		10	μA

■ TONE DETECTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Filter Amplifier							
Bias Voltage	V_{OUT}	$I_{FIN}=0$	1.75	1.95	2.15	V	
Input Impedance	F_{INZ}	$V_{FIN}=100\text{mV p/p}$		150		Ω	
Amplifier Gain	A_G	$V_{FIN}=100\text{mV p/p}$		30		V/mA	
V Threshold	F_{VT}		100	170	350	mVp/p	
Output Stage							
Lov Bias Current	I_{LOV}	$V_{LOV}=0\text{V}$	0.02	0.15	1	μA	
Lov Volt Range	V_{LOV}	$I_L=50\text{mA(LB or HB)}$	-0.5		$V_{CC}-1.8$	V	
LB Output Low	V_{LBL}	$V_{LOV}=0\text{V}, I_L=0\text{mA}, R_{lb-Csub}=1\text{M}\Omega$	Enabled	-3.05	-2.8	-2.55	V
		$V_{LOV}=3\text{V}, I_L=0\text{mA}, R_{lb-Gnd}=1\text{M}\Omega$	Enabled	-0.01	0	0.1	V
LB Output High	V_{LBH}	$V_{LOV}=0\text{V}, I_L=10\text{mA}$	Disabled	-0.025	0	0.025	V
		$V_{LOV}=3\text{V}, I_L=50\text{mA}$	Disabled	2.9	3	3.1	
HB Output Low	V_{HBL}	$V_{LOV}=0\text{V}, I_L=0\text{mA}, R_{hb-Csub}=1\text{M}\Omega$	Disabled	-3.05	-2.80	-2.55	V
		$V_{LOV}=3\text{V}, I_L=0\text{mA}, R_{hb-Gnd}=1\text{M}\Omega$	Disabled	-0.01	0	0.1	V
HB Output High	V_{HBH}	$V_{LOV}=0\text{V}, I_L=10\text{mA}$	Enabled	-0.025	0	0.025	V
		$V_{LOV}=3\text{V}, I_L=50\text{mA}$	Enabled	2.9	3	3.1	

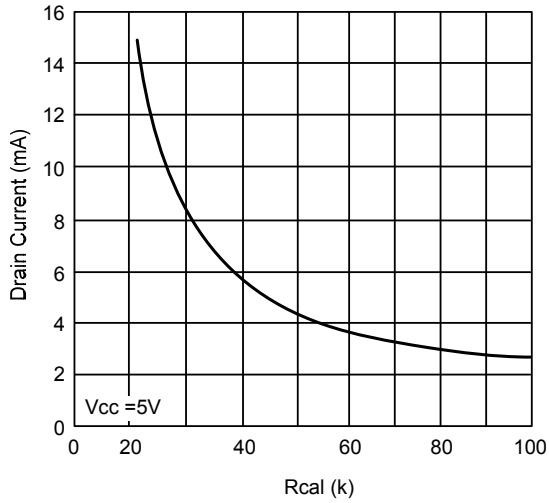
Note: Noise voltage measurement would be ignored in production.

■ POLARITY SWITCH CHARACTERISTICS

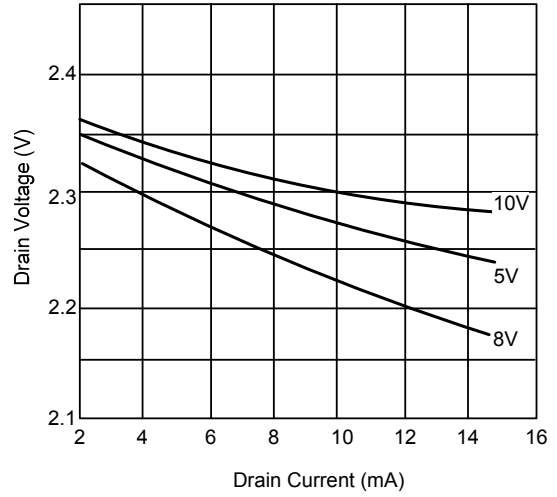
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Current	I_{POL}	$V_{POL}=25\text{V}$ (Applied via $R_{POL}=2\text{k}\Omega$)	10	25	40	μA
Threshold Voltage	V_{TPOL}	$V_{POL}=25\text{V}$ (Applied via $R_{POL}=2\text{k}\Omega$)	14	14.75	15.5	V
Switching Speed	T_{SPOL}	$V_{POL}=25\text{V}$ (Applied via $R_{POL}=2\text{k}\Omega$)			100	ms

TYPICAL CHARACTERISTICS

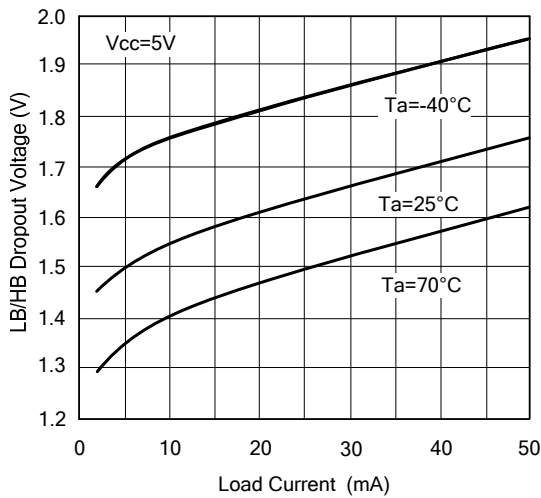
JFET Drain Current vs. Rcal



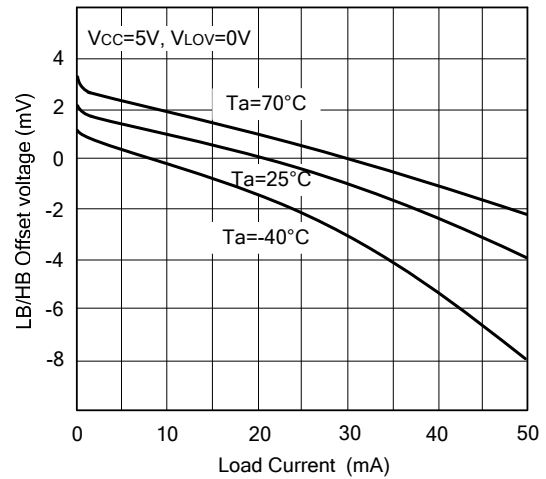
JFET Drain Voltage vs. Drain Current



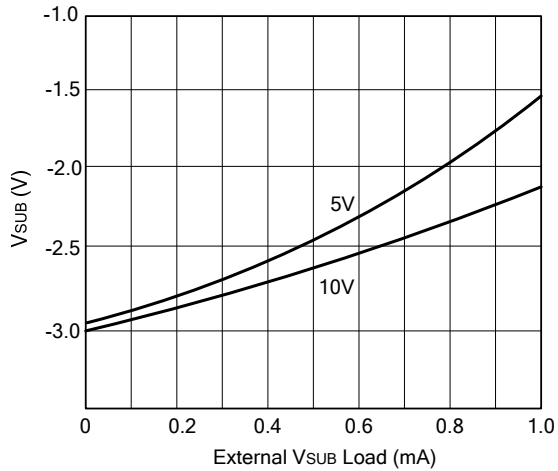
LB/HB Dropout Voltage vs. Load Current



LB/HB Offset Voltage vs. Load Current



Vsub vs. External Load



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