MOTOROLA

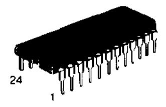
MC14580B

4 x 4 MULTIPORT REGISTER

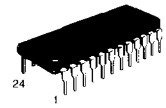
The MC14580B is a 4 by 4 multiport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

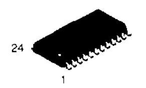
- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or one Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin Compatible with CD40108



L SUFFIX
CERAMIC
CASE 623



P SUFFIX
PLASTIC
CASE 709



DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A 55 to 125 C for all packages

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

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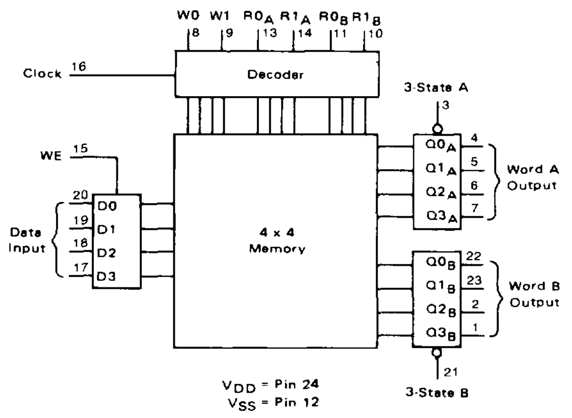
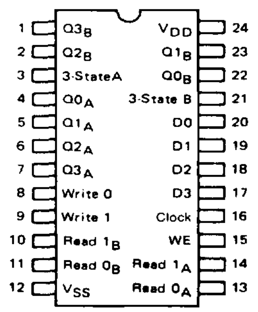
BLOCK DIAGRAM



PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.010	5.0	—	150	μAdc
		10	—	10	—	0.020	10	—	300	
		15	—	20	—	0.030	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.18 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.91 μA/kHz) f + I_{DD}							
		15	I_T = (2.67 μA/kHz) f + I_{DD}							
Three-State Leakage Current	I_{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

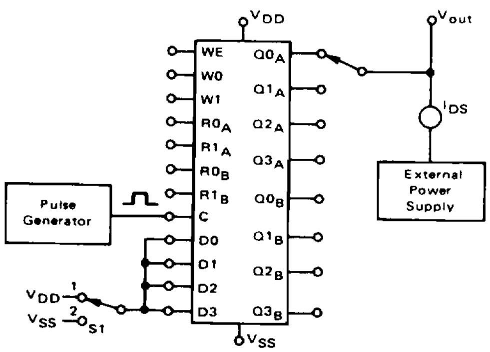
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH}, $t_{THL} = (1.5$ ns/pF$)$ $C_L + 25$ ns t_{TLH}, $t_{THL} = (0.75$ ns/pF$)$ $C_L + 12.5$ ns t_{TLH}, $t_{THL} = (0.55$ ns/pF$)$ $C_L + 9.5$ ns	t_{TLH}, t_{THL} (Figures 3 and 6)	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay Time Clock to Output	t_{PLH}, t_{PHL} (Figures 3 and 6)	5.0 10 15	— — —	650 250 170	1300 500 340	ns
Write Enable Setup Time (Enabling a Write or Read)	t_{su} (Figure 5)	5.0 10 15	800 300 200	400 150 100	— — —	ns
Write Enable Removal Time (Disabling a Write or Read)	t_{rem} (Figure 5)	5.0 10 15	0 0 0	−100 −50 −35	— — —	ns
Setup Time** Address, Data to Clock	t_{su} (Figure 3)	5.0 10 15	50 30 25	20 0 0	— — —	ns
Hold Time** Clock to Address, Data	t_h (Figure 3)	5.0 10 15	480 195 150	160 65 50	— — —	ns
3-State Enable/Disable Delay Time	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL} (Figures 4 and 7)	5.0 10 15	— — —	130 60 45	260 120 90	ns
Clock Pulse Width	t_w (Figure 3)	5.0 10 15	820 330 220	410 165 110	— — —	ns

**When loading repetitive highs, the output may glitch low momentarily after the rising edge of Clock. However, data integrity remains unaffected and data is valid after the propagation delays listed in the Switching Characteristics Table.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



	Sink Current	Source Current
Position of S1	2	1
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS (3-State Inputs are High)

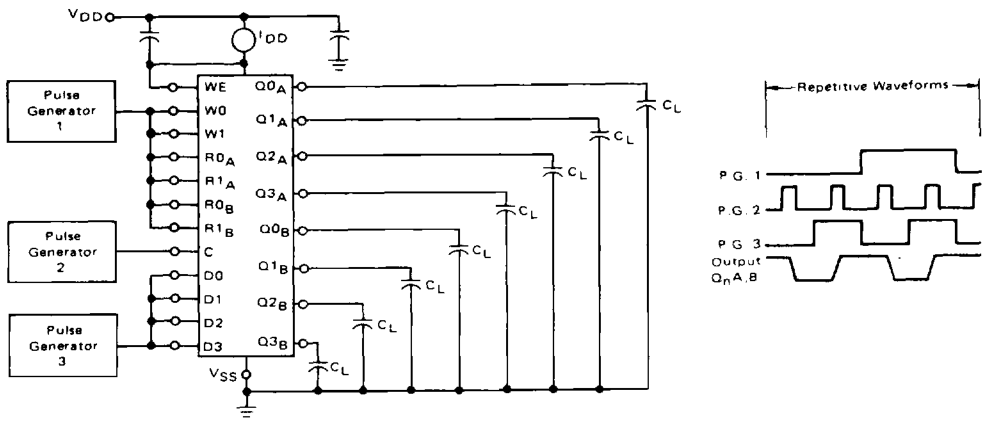


FIGURE 3

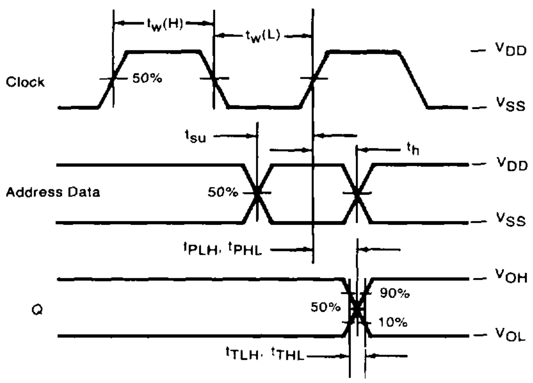


FIGURE 4

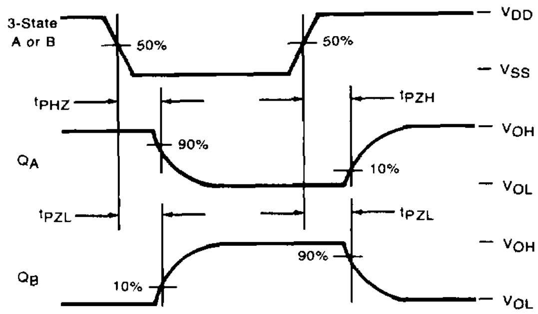


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FIGURE 5

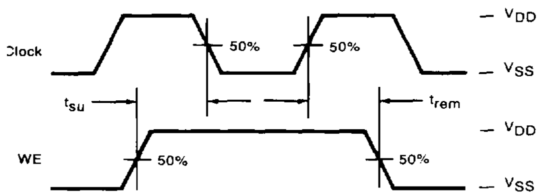


FIGURE 6 — TEST CIRCUIT

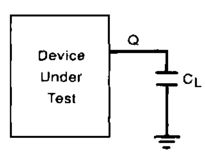
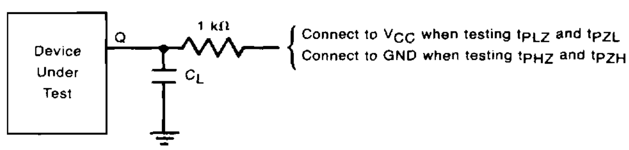
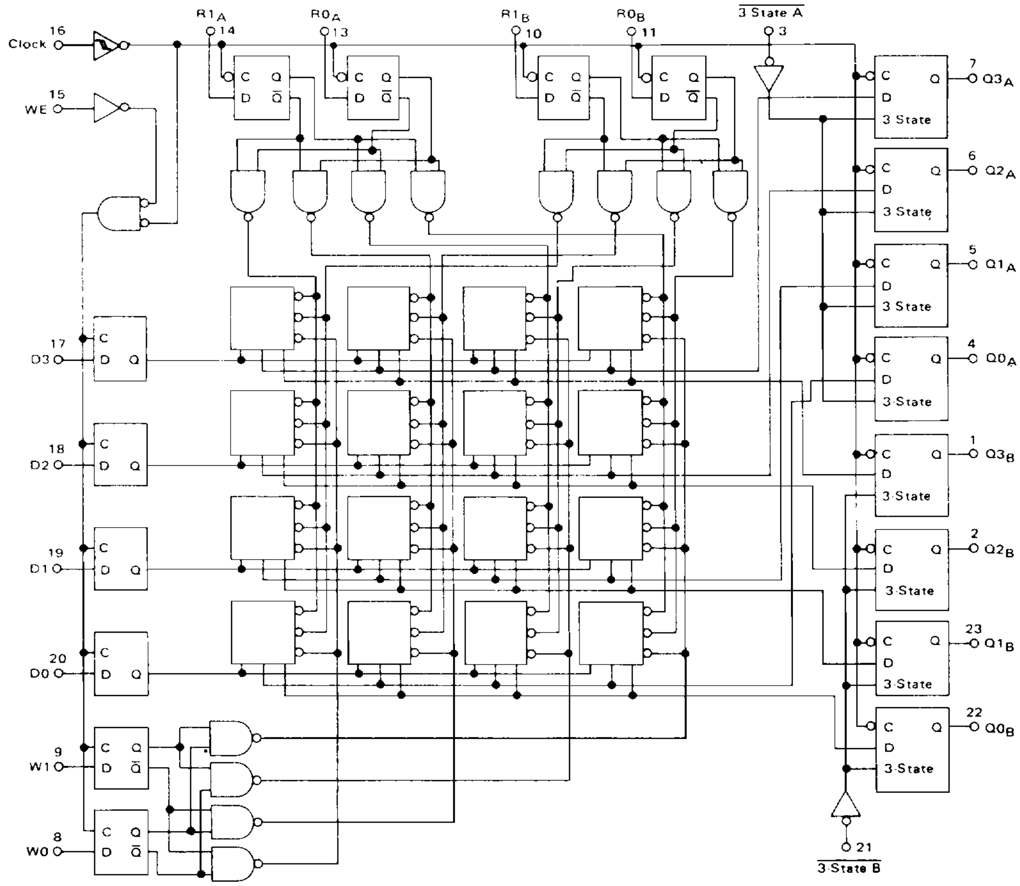


FIGURE 7 — TEST CIRCUIT



LOGIC DIAGRAM



TRUTH TABLE

Clock	WE	Write 1	Write 0	Read 1_A	Read 0_A	Read 1_B	Read 0_B	3-State A	3-State B	D_n	Q_nA	Q_nB
↑	1	0	1	0	1	0	1	1	1	1	1	1
↑	1	0	1	0	1	0	1	1	1	0	0	0
↓	X	X	X	X	X	X	X	1	1	X	No Change	No Change
X	X	X	X	X	X	X	X	0	0	X	Z	Z
0	X	X	X	X	X	X	X	1	1	X	No Change	No Change
1	X	X	X	X	X	X	X	1	1	X	No Change	No Change
↑	1	0	0	0	1	1	0	1	1	D_n to word 0	Contents of word 1 displayed	Contents of word 2 displayed
↑	0	0	0	0	1	1	0	1	1	Word 0 not altered	Contents of word 1 displayed	Contents of word 2 displayed

Z = High Impedance
X = Don't care

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