Dense-Pac Microsystems, Inc.

64KX1 BASED

CMOS SRAM FAMILY - DIPS

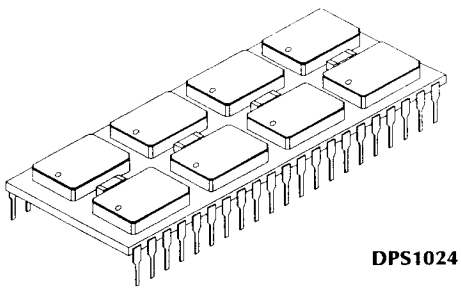
DESCRIPTION:

The Dense-Pac 64K X 1 module family consists of very high speed 64K X 1 based static RAMs which have been configured in the organizations described below. These modules are best suited for high speed military computers and signal processing applications.

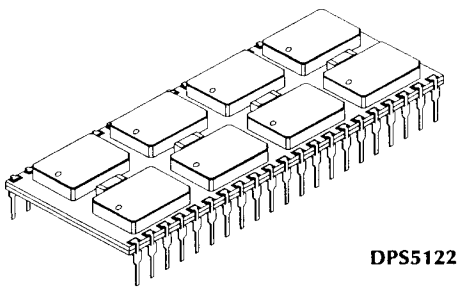
FEATURES:

- Organizations Aavailable:
  - DPS1024 - 64K X 16, 128K X 8, 256K X 4
  - DPS1025 - 64K X 16, 128K X 8
  - DPS1026 - 64K X 16, 128K X 8, 256K X 4
  - DPS1027 - 64K X 16, 128K X 8, 256K X 4
  - DPS1152 - 64K X 18, 128K X 9
  - DPS5122 - 512K X 2, 1MB X 1
- Fast Access Times:
  - DPS64K X 1-25 - 25ns (max)
  - DPS64K X 1-35 - 35ns (max)
  - DPS64K X 1-45 - 45ns (max)
  - DPS64K X 1-55 - 55ns (max)
- Low Power Dissipation
- Completely Static Operation: No Clock Or Refresh Needed
- Single +5V Power Supply ± 10% Tolerance
- Specifications Guaranteed Over Full Military Temperatures (-55°C to +125°C)
- TTL Compatible
- Three State Output
- Standard Packages:
  - 40-Pin DIP - DPS1025, DPS1026, DPS1027
  - 42-Pin DIP - DPS1024, DPS5122
  - 50-Pin DIP - DPS1152

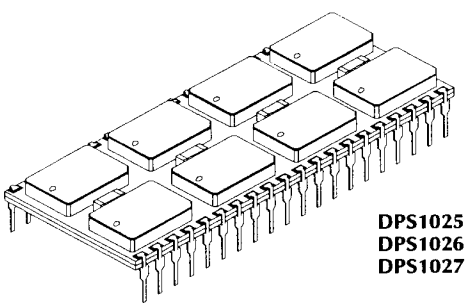
PIN NAMES	
A0-A15	Address Inputs
DI0 - DI8, D_{IN}	Data Inputs
DO0 - DO18, D_{OUT}	Data Outputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$, $\overline{CE0}$-$\overline{CE17}$,	Chip Enables
$\overline{CET}$, $\overline{CET0}$-$\overline{CET1}$	Chip Enable Top
$\overline{CEB}$, $\overline{CEB0}$-$\overline{CEB1}$	Chip Enable Bottom
$\overline{WE}$	Write Enables
$\overline{WET}$, $\overline{WEB}$	Write Enable Top/Bottom
V_{DD}	Power (+5V)
V_{SS}	Ground
NC	No Connect



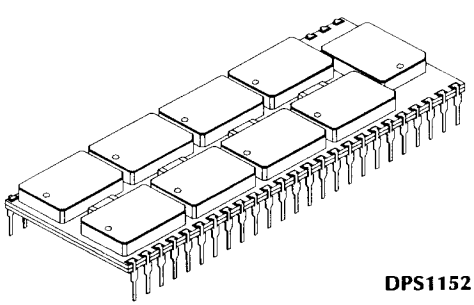
DPS1024



DPS5122



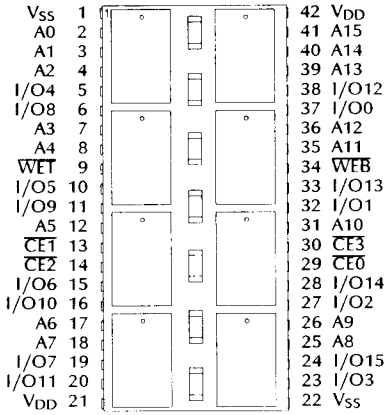
DPS1025
DPS1026
DPS1027



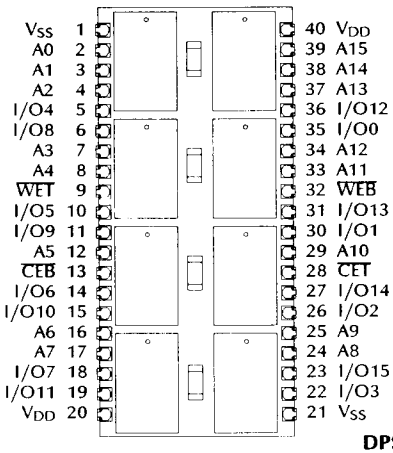
DPS1152

2

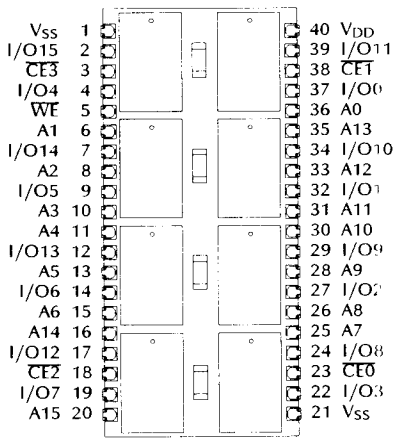
MODULE PIN-OUT DIAGRAMS



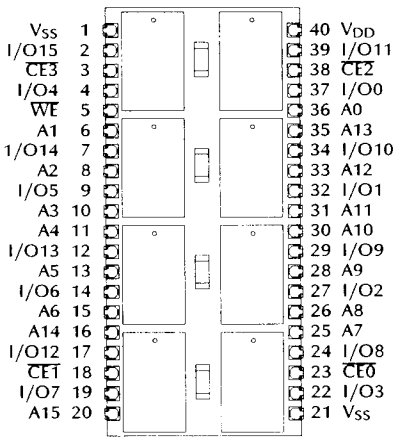
DPS1024



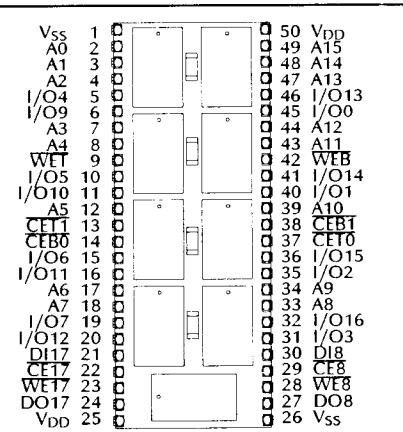
DPS1025



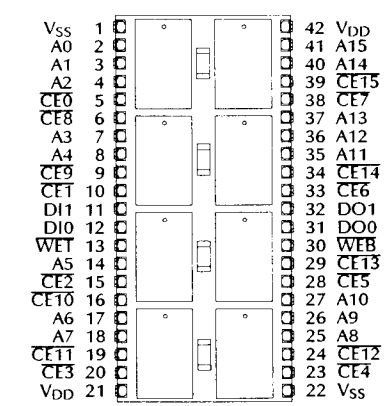
DPS1026



DPS1027

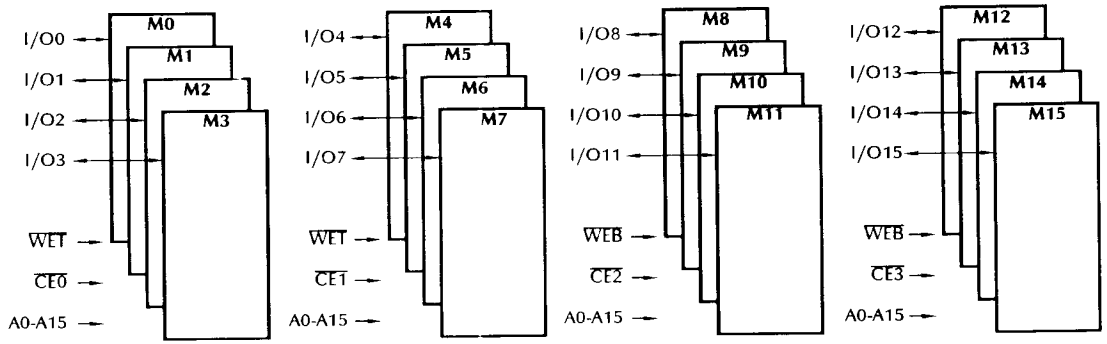


DPS1152

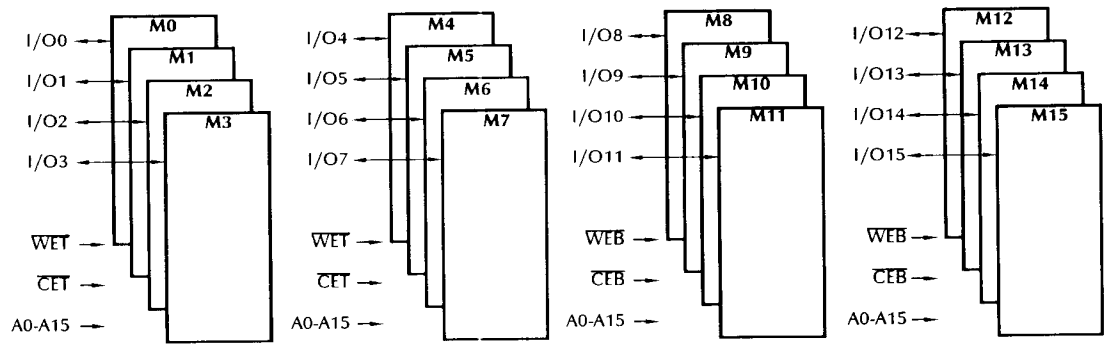


DPS5122

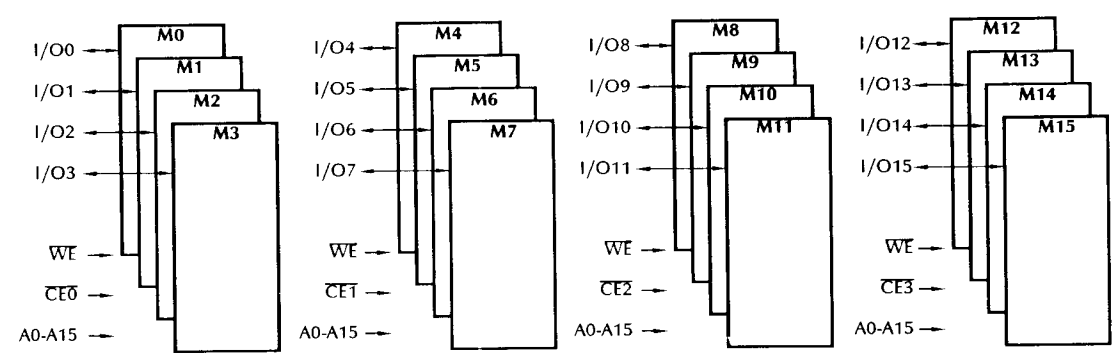
FUNCTIONAL BLOCK DIAGRAMS



DPS1024

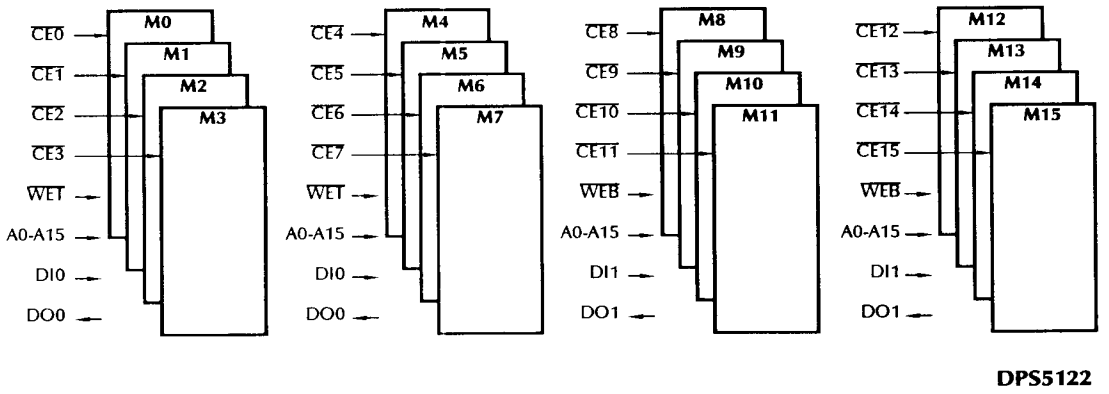


DPS1025

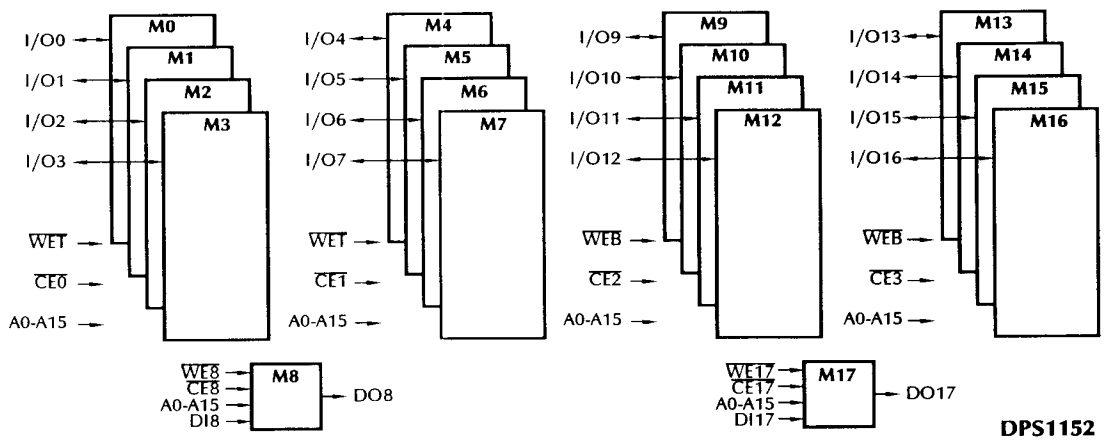


DPS1026, DPS1027

FUNCTIONAL BLOCK DIAGRAMS



DPS5122



DPS1152

CAPACITANCE: $T_A = 25°C$, $F = 1.0MHz$[1]									
Symbol	Parameter	DPS1024 Max.	DPS1025 Max.	DPS10626 Max.	DPS1027 Max.	DPS1152 Max.	DPS5122 Max.	Unit	Condition
C_{CE}	Chip Enable	40	60	60	60	60	25		
C_{ADR}	Address Input	160	160	160	160	160	160		
C_{WE}	Write Enable	75	75	150	150	75	40	pF	$V_{IN} = 0V$
$C_{I/O}$	Data In/Out	20	20	20	20	20	-		
C_{IN}	Data Input	-	-	-	-	20	140		
C_{OUT}	Data Output	-	-	-	-	20	140		

TRUTH TABLE					
Mode	Chip Enable	Write Enable	Data In	Data Out	Power Level
Not Selected	HIGH	Don't Care	Don't Care	HIGH-Z	Standby
Read	LOW	HIGH	Don't Care	D_{OUT}	Active
Write	LOW	LOW	D_{IN}	HIGH-Z	Active

DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions		DPS102X Min.	DPS102X Max.	DPS1152 Min.	DPS1152 Max.	DPS5122 Min.	DPS5122 Max.	Unit
I_{IN}	Input Leakage Current	$\overline{CE} = V_{IH}$, $V_{IN} = 0.5V$ and 5.5V	M	-20	+20	-20	+20	-20	+20	µA
			I	-20	+20	-20	+20	-20	+20	
			C	-20	+20	-20	+20	-20	+20	
I_{OUT}	Output Leakage Current (On Data Outputs)	$\overline{CE} = V_{IH}$, $V_{OUT} = 0.V$ and 5.5V	M	-20	+20	-20	+20	-20	+20	µA
			I	-20	+20	-20	+20	-20	+20	
			C	-20	+20	-20	+20	-20	+20	
I_{CC100}	Operating Power Supply Current (100% Duty Cycle)	$\overline{CE} = V_{IL}$, Output Open	M		880		990		300(165)	mA
			I		875		980		295(125)	
			C		830		930		275(115)	
I_{CC50}	Operating Power Supply Current (8 Bit Mode)	$\overline{CE} = V_{IL}$, Output Open	M		550(470)		575(480)		-	mA
			I		540(445)		570(450)		-	
			C		510(420)		535(420)		-	
I_{CC25}	Operating Power Supply Current (4 Bit Mode)	$\overline{CE} = V_{IL}$, Output Open	M		380(265)		420(275)		-	mA
			I		375(235)		415(235)		-	
			C		355(245)		390(220)		-	
I_{CC2}	Dynamic Operating Supply Current	Min. Read Cycle Duty = 100%	M		1010		1135		-	mA
			I		990		1110		-	
			C		915		1030		-	
I_{SB1}	Standby Supply Current	$\overline{CE} \leq V_{IH}$ See Note 2	M		215		240		215	mA
			I		210		235		210	
			C		195		220		195	
I_{SB2}	Full Standby Supply Current	See Note 3	M		60		70		60	mA
			I		20		20		20	
			C		15		15		15	
I_{CCDR2}	Data Retention Current	$V_{DR} = 2.0V$	M		12.5		13.4		12.5	mA
			I		2.75		2.8		2.75	
			C		1.5		1.65		1.5	
I_{CCDR3}	Data Retention Current	$V_{DR} = 3.0V$	M		20		22.5		20	mA
			I		5.3		6		5.3	
			C		3.5		4		3.5	
V_{OL}	Output Low Voltage	$I_{OL} = 8.0mA$			0.4		0.4		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$		2.4		2.4		2.4		V

NOTE: Dense-Pac has other specialized suppliers that may provide better A.C. or D.C. Characteristics. Values in parentheses are valid when all inputs are at CMOS levels.

RECOMMENDED OPERATING RANGE[4]

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		$V_{DD}+.5$	V
V_{IL}	Input LOW Voltage	-0.5		0.8	V

ABSOLUTE MAXIMUM RATINGS[5]

Voltage on Any Pin with Respect to V_{SS}	-2.0V to +7.0V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C

PART NUMBERING SYSTEM

DP S 1024 - 25 M

PREFIX — **DEVICE TYPE**

S - SRAM
D - DRAM
E - EEPROM
V - EPROM
N - NOVRAM
O - VIDEORAM

FAMILY

SPEED

TEMPERATURE/SCREENING

C - 0°C to 70°C
I - -40°C to +85°C, plus Burn-In
M - -55°C to +125°C, MIL Processed
B - -55°C to +125°C, Fully Processed to Methods 5004 and 5005

AC TEST CONDITIONS	
Input Pulse Levels	0.5V to 2.5V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	0.8V and 2.2V
Output Load	See Figures 1 and 2

* Transient between 0.8V and 2.2V

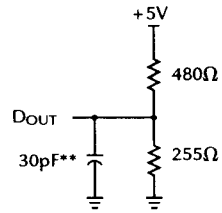


Figure 1. Output Load I

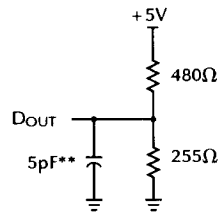


Figure 2. Output Load II

** Including scope and jig.

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

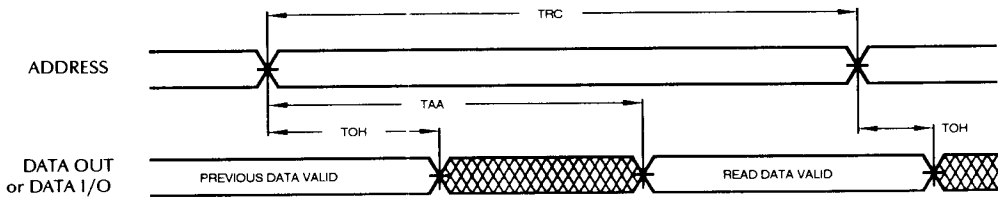
No.	Symbol	Parameter	-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	25		35		45		55		ns
2	t_{AA}	Address Access Time		25		35		45		55	ns
3	t_{CO}	Chip Enable to Output Valid		25		35		45		55	ns
4	t_{OH}	Output Hold for Address Change	5		5		5		5		ns
5	t_{CLZ}	Chip Enable to Output in Low-Z [6, 7]	5		5		5		5		ns
6	t_{CHZ}	Chip Enable to Output in High-Z [6, 7]		25		30		30		30	ns
7	t_{OC}	Output Hold from Chip Enable	5		5		5		5		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [8, 9]

No.	Symbol	Parameter	-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
8	t_{WC}	Write Cycle Time	25		35		45		55		ns
9	t_{CW}	Chip Selection to End of Write	20		30		40		50		ns
10	t_{AW}	Address Valid to End of Write	20		30		40		50		ns
11	t_{AS}	Address Setup Time†	0		0		0		0		ns
12	t_{WP}	Write Pulse Width	25		25		25		35		ns
13	t_{AH}	Address Hold Time[10]	0		0		0		0		ns
14	t_{DW}	Data Valid to End of Write	25		25		25		25		ns
15	t_{DH}	Data Hold Time					0		0		ns
16	t_{WHZ}	Write Enabled to Output in HIGH-Z		25		25		25		25	ns
17	t_{WLZ}	Write Enabled to Output in LOW-Z	0		0		0		0		ns

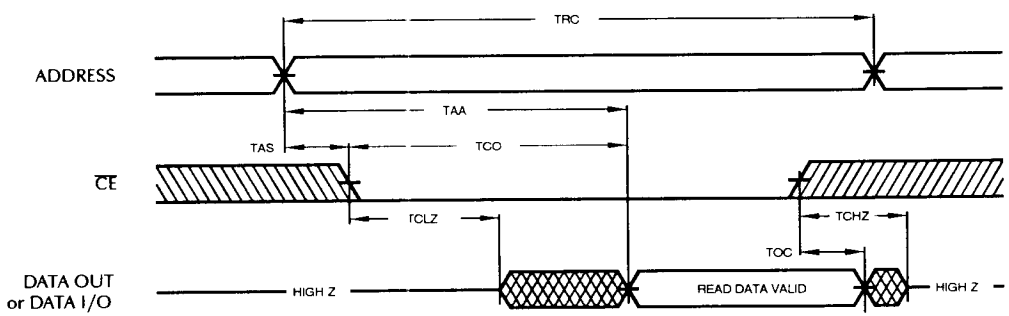
† Valid for both Read and Write Cycles.

READ CYCLE 1: Address Controlled. $\overline{CE}$ is LOW. $\overline{WE}$ is HIGH.



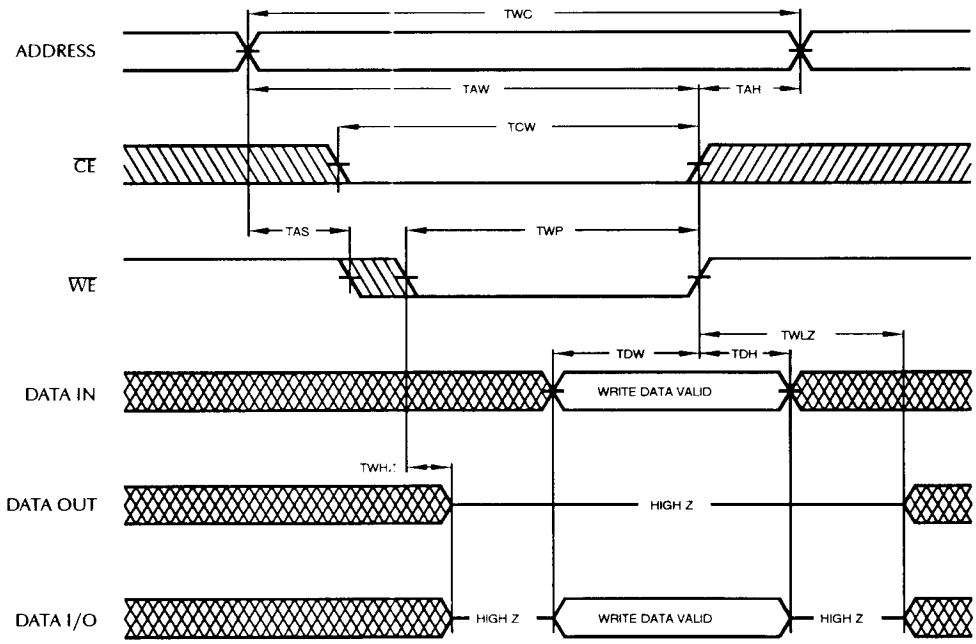
2

READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.

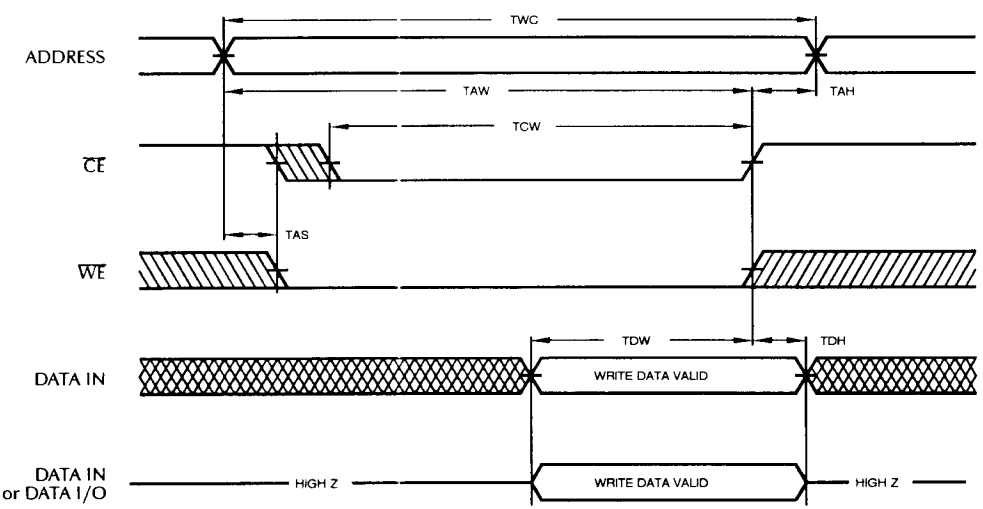


WAVEFORM KEY

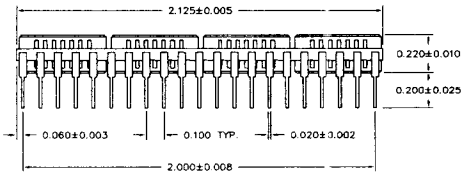
WRITE CYCLE 1: $\overline{WE}$ Controlled.



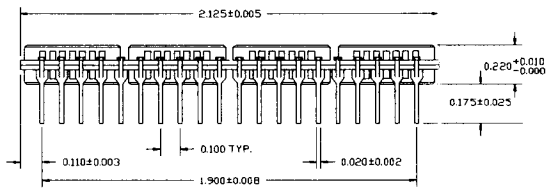
WRITE CYCLE 2: $\overline{CE}$ Controlled.



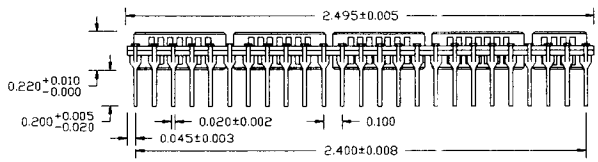
MECHANICAL DIAGRAMS



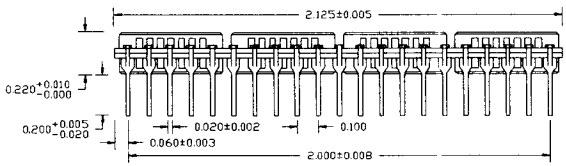
DPS1024



DPS1025, DPS1026, DPS1027



DPS1152



DPS5122

2

NOTES:

1. This parameter is sampled but not 100% tested.
2. This parameter is measured with Chip Enable ($\overline{CE}$) HIGH and inputs at valid TTL levels (0.8 and 2.2V).
3. This parameter is measured with input levels either V_{DD}-0.2V or 0.2V, including $\overline{CE}$ which must be V_{DD}-0.2V. This condition results in significant reduction in current in the input buffer circuitry and consequently a lower overall current level.
4. All voltages are referenced to V_{SS} pin = 0V.
5. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
6. Transition is measured at the point of ± 100mV from steady state voltage.
7. This parameter is measured with specified loading in Figure 2, Output load II.
8. If $\overline{OE}$ and $\overline{CE}$ are in the Read mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
9. The outputs are in a HIGH impedance state when $\overline{WE}$ is LOW.
10. t_{AH} is defined from the end point of write mode. The last time when $\overline{WE}$ and $\overline{CE}$ are both LOW.

TYPICAL SCREENING FLOW					
Seq. #	Test or Examination	MIL-STD 883, Condition	C	I	M
1	Internal Visual	2010B or DP Spec.	**	**	**
2	Stabilization Bake	1008C, 24 hrs. @+150°C	**	100%	100%
3	Temp. Cycling	1010C, 10 cycles required; 1 cycle -65°C / 10 min. | +25°C / 5 min. | +125°C / 10 min. | +25°C / 5 min.	**	100%	100%
4	Constant Acceleration	2001E (Y_1), 30,000 G's for 1 min.	**	100%	100%
5	Fine Leak	1014A, $\leq 5.0 \times 10^{-8}$	**	100%	100%
6	Gross Leak	1014C, 2 hrs. @60 psig	**	100%	100%
7	Burn-In	1015, # of hours, +8 -0@+125°C	**	48	160
8	Serialize	DP Drawing #	**	N/A	N/A
9	Final Electrical Test	S.C.D./Detailed Specification	100%	100%	100%
10	External Visual	2009, Ref. DP Drawing #	100%	100%	100%

**Screening depends upon supply source.

ORDERING INFORMATION					
Part Number	Speed	Temperature	Part Number	Speed	Temperature
DPS1024-25C	25ns	0 to 70°C	DPS1024-35C	35ns	0 to 70°C
DPS1024-45C	45ns	0 to 70°C	DPS1024-55C	55ns	0 to 70°C
DPS1024-25I	25ns	-40 to 85°C	DPS1024-35I	35ns	-40 to 85°C
DPS1024-45I	45ns	-40 to 85°C	DPS1024-55I	55ns	-40 to 85°C
DPS1024-25M	25ns	-55 to 125°C	DPS1024-35M	35ns	-55 to 125°C
DPS1024-45M	45ns	-55 to 125°C	DPS1024-55M	55ns	-55 to 125°C
DPS1025-25C	25ns	0 to 70°C	DPS1025-35C	35ns	0 to 70°C
DPS1025-45C	45ns	0 to 70°C	DPS1025-55C	55ns	0 to 70°C
DPS1025-25I	25ns	-40 to 85°C	DPS1025-35I	35ns	-40 to 85°C
DPS1025-45I	45ns	-40 to 85°C	DPS1025-55I	55ns	-40 to 85°C
DPS1025-25M	25ns	-55 to 125°C	DPS1025-35M	35ns	-55 to 125°C
DPS1025-45M	45ns	-55 to 125°C	DPS1025-55M	5ns	-55 to 125°C
DPS1026-25C	25ns	0 to 70°C	DPS1026-35C	35ns	0 to 70°C
DPS1026-45C	45ns	0 to 70°C	DPS1026-55C	55ns	0 to 70°C
DPS1026-25I	25ns	-40 to 85°C	DPS1026-35I	35ns	-40 to 85°C
DPS1026-45I	45ns	-40 to 85°C	DPS1026-55I	55ns	-40 to 85°C
DPS1026-25M	25ns	-55 to 125°C	DPS1026-35M	35ns	-55 to 125°C
DPS1026-45M	45ns	-55 to 125°C	DPS1026-55M	55ns	-55 to 125°C
DPS1027-25C	25ns	0 to 70°C	DPS1027-35C	35ns	0 to 70°C
DPS1027-45C	45ns	0 to 70°C	DPS1027-55C	55ns	0 to 70°C
DPS1027-25I	25ns	-40 to 85°C	DPS1027-35I	35ns	-40 to 85°C
DPS1027-45I	45ns	-40 to 85°C	DPS1027-55I	55ns	-40 to 85 c
DPS1027-25M	25ns	-55 to 125°C	DPS1027-35M	35ns	-55 to 125°C
DPS1027-45M	45ns	-55 to 125°C	DPS1027-55M	55ns	-55 to 125°C
DPS1152-25C	25ns	0 to 70°C	DPS1152-35C	35ns	0 to 70°C
DPS1152-45C	45ns	0 to 70°C	DPS1152-55C	55ns	0 to 70°C
DPS1152-25I	25ns	-40 to 85°C	DPS1152-35I	35ns	-40 to 85°C
DPS1152-45I	45ns	-40 to 85°C	DPS1152-55I	55ns	-40 to 85°C
DPS1152-25M	25ns	-55 to 125°C	DPS1152-35M	35ns	-55 to 125°C
DPS1152-45M	45ns	-55 to 125°C	DPS1152-22M	55ns	-55 to 125°C
DPS5122-25C	25ns	0 to 70°C	DPS5122-35C	35ns	0 to 70°C
DPS5122-45C	45ns	0 to 70°C	DPS5122-55C	55ns	0 to 70°C
DPS5122-25I	25ns	-40 to 85°C	DPS5122-35I	35ns	-40 to 85°C
DPS5122-45I	45ns	-40 to 85°C	DPS5122-55I	55ns	-40 to 85°C
DPS5122-25M	25ns	-55 to 125°C	DPS5122-35M	35ns	-55 to 125°C
DPS5122-45M	45ns	-55 to 125°C	DPS5122-55M	55ns	-55 to 125°C

Dense-Pac Microsystems, Inc.
7321 Lincoln Way • Garden Grove, California 92641-1428
(714) 898-0007 • (800) 642-4477 (Outside CA) • FAX: (714) 897-1772
30A006-00
REV B