QUADRUPLE 2-INPUT AND GATE

The HEF4081B provides the positive quadruple 2-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.
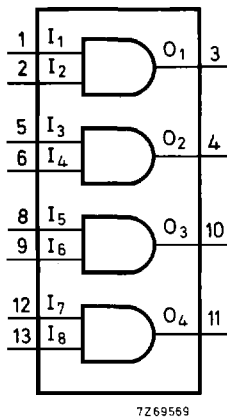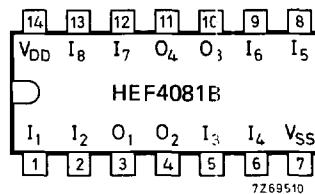

Fig.1 Functional diagram.

Fig.2 Pinning diagram.

HEF4081BP(N): 14-lead DIL; plastic
(SOT27-1)
HEF4081BD(F): 14-lead DIL; ceramic (cerdip)
(SOT73)
HEF4081BT(D): 14-lead SO; plastic
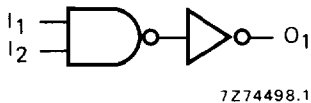(SOT108-1)
( ): Package Designator North America

Fig.3 Logic diagram (one gate).

FAMILY DATA } see Family Specifications

I_{DD} **LIMITS category GATES**

HEF4081B

gates

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25\ °C$; $C_L = 50$ pF; input transition times $\leqslant 20$ ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \longrightarrow O_n$	5		55	110	ns	28 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		45	90	ns	18 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times						
HIGH to LOW	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$450\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF)
	10	$2\,900\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	$\Sigma(f_oC_L)$ = sum of outputs
	15	$11\,700\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	V_{DD} = supply voltage (V)