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NEC Electronics Inc.

μPC398 MONOLITHIC SAMPLE-AND-HOLD CIRCUIT

Description

The μPC398 is a monolithic sample and hold circuit which combines J-FET and bipolar circuitry on the same substrate to provide a high input impedance input buffer and a high speed output buffer. Operating as a unity gain input buffer circuit, DC accuracy is typically 0.004% and acquisition time is as low as 6 μs with a maximum gain error of 0.01 %. This device is ideal for data acquisition circuits requiring high speed and high input impedance.

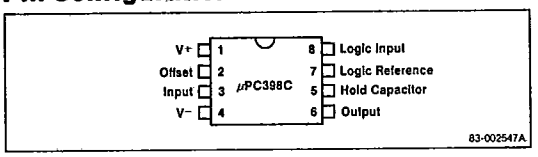
Features

- ☐ Fast acquisition time
- ☐ Gain accuracy: 0.004%
- ☐ Input offset voltage: 2 mV
- ☐ Direct interface to TTL/CMOS
- ☐ LF398 direct replacement

Ordering Information

Part Number	Package	Temperature Range
μPC398C	Plastic DIP	−20°C to +70°C

Pin Configuration



Absolute Maximum Ratings

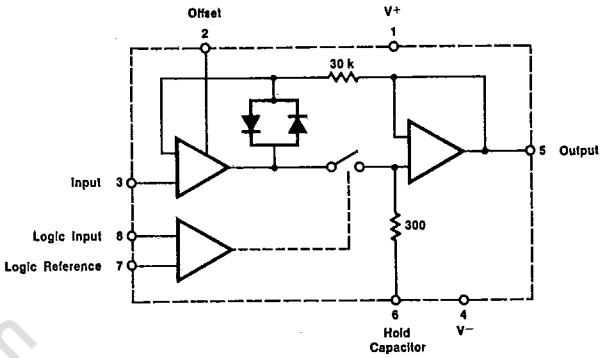
$T_A = 25°C$

Voltage Between V+ and V−	36 V
Input Voltage Range (Note 1)	±15 V
Logic to Logic Reference Differential Voltage	−0.3 to +7.0 V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 s
Power Dissipation	350 mW
Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−55 to +150°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Equivalent Circuit



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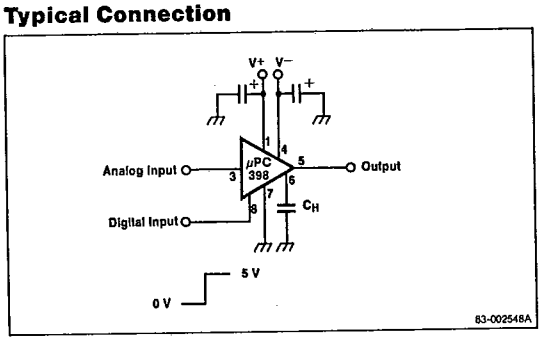
Recommended Operating Conditions

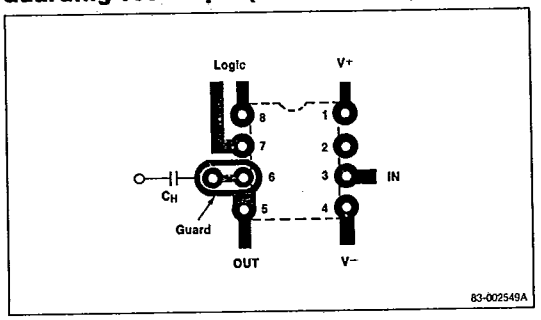
$T_A = 25°C$, $V\pm = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Power Supply Voltage	$V\pm$	±5	±15	±16.5	V	
Analog Input Voltage	V_{IN}	−11.5		+11.5	V	
Sample Mode Logic Input Voltage	V_{SH}	2.7		5.25	V	$V_{REF} = 0$
Hold Mode Logic Input Voltage	V_{SH}	−15		0.5	V	$V_{REF} = 0$
Logic Input Voltage Slew Rate	SR	0.2			V/μs	
Hold Capacitor	C_H	0.001		0.1	μF	

Typical Connection



Guarding Technique (Bottom View)



Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 15$ V, $-11.5\ V \le V_{IN} \le +11.5$ V, $C_H = 0.01\ \mu F$, $R_L = 10\ k\Omega$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{IO}			7.0	mV	
Input Bias Current	I_b			50	nA	
Input Impedance	R_{IN}		10^{10}		Ω	
Gain Error				0.01	%	
Feedthrough Attenuation Ratio		80			dB	f = 1 kHz
Output Impedance	Z_o			4.0	Ω	
Hold Step Voltage	V_{HS}			2.5	mV	$V_O = 0$
Leakage Current into Hold Capacitor	I_{OLK}			200	pA	$V\pm = \pm 5$ V to ±18 V
Acquisition Time	t_{aq}		4		μs	$\Delta V_O = 10$ V, 0.1% Error, $C_H = 1000$ pF
	t_{aq}		20		μs	$\Delta V_O = 10$ V, 0.1% Error, $C_H = 0.01$ pF
Hold Capacitor Charging Current	I_{CH}		5		mA	$V_{IN} - V_O = 2$ V
Logic Input Current	I_{IN}			10	μA	
Logic Threshold	V_{TH}	0.8		2.4	V	
Supply Voltage Rejection Ratio	SVRR	80			dB	
Supply Current	I_{CC}			±6.5	mA	$V\pm = \pm 15$ V to ±18 V