HEWLETT PACKARD

Low Input Current, High Gain Optocouplers

Technical Data

CNW138
CNW139

Features

- **5000 Vrms/1 Minute Insulation Withstand Capability**
- **Worldwide Safety Approval**
  UL1577 (File No. E55361)
  VDE 0884 Certification (V_{IORM} = 1 kV_{RMS})
  VDE 860/805/806/804/750-1/ IEC 950
  BSI According to BS 415/ 7002/6301
  SETI-SEMKO-NEMKO-DEMKO-According to IEC 65/380/950/335
- **High Current Transfer Ratio – 3000% Typical**
- **Low Input Current Requirement – 0.5 mA**
- **TTL Compatible Output – 0.1 V V_{OL} Typical**
- **Performance Guaranteed Over Temperature 0°C to 70°C**
- **Base Access Allows Gain Bandwidth Adjustment**
- **High Output Current – 60 mA**
- **Pin Compatible with 6N138/9**

Applications

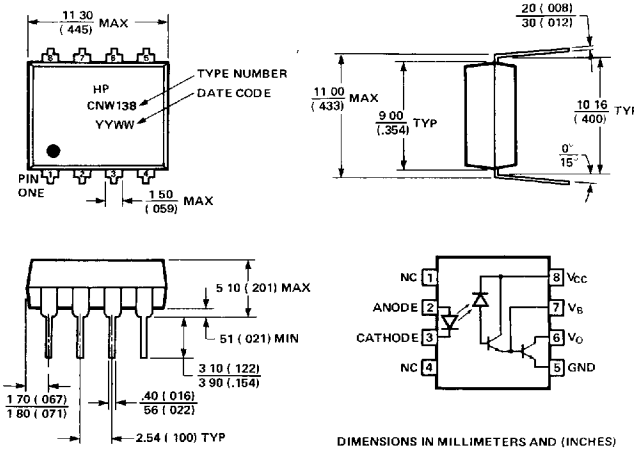
- **High Voltage Insulation**
- **Low Input Current Line Receiver**
- **Ground Isolation - TTL/ TTL, CMOS/TTL, CMOS/ CMOS, LSTTL/TTL, CMOS/ LSTTL**
- **EIA RS-232C Line Receiver**
- **Telephone Ring Detector**
- **AC Line Voltage Sensing**
- **Low Power Systems**

Description

These high-voltage, high-gain optocouplers use an AlGaAs LED and an integrated high gain photodetector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

OPTO COUPLERS

Package Outline



DIMENSIONS IN MILLIMETERS AND (INCHES)

A widebody encapsulation is used to provide creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

The CNW139 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5 mA of LED current.

The CNW138 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6 mA (1 TTL load). A 300% minimum CTR enables operation with a fanout of 1 TTL Load using a 2.2 kΩ pull-up resistor.

Regulatory Information

The CNW138/9 features a wide body DIL 8 encapsulation. This package was specifically designed to meet regulatory insulation requirements worldwide. The CNW138/9 has been approved by the following organizations:

UL – Covered under UL component recognition FILE E55361

VDE – Approved according to VDE 0884/08.87 (marks License No. 70975)
Complied for reinforced insulation at 250 V AC with:
DIN IEC 380/VDE 0806
DIN IEC 435/VDE 0805 "ENTWURF"
DIN 57804/VDE 0804 (insulation group C)
DIN VDE 0860 (HD 195 SC)
DIN IEC 601 Teil 1/VDE 0750-1
DIN VDE 0160
EN 60950/IEC 950

NORDIC – Tested for applications (reinforced insulation) – Class II applications for plugable apparatus in normal tight execution.
-SETI-SEMKO-NEMKO-DEMKO-According to IEC 65-IEC380-IEC950-IEC335

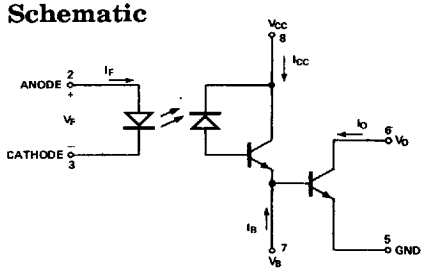
BSI – Certification according to BS415:1990, BS7002:1989 and BS6301:1982 pending

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -55°C to 85°C
Lead Solder Temperature ..... 260°C for 10 s (up to seating plane)
Average Input Current – I_F ..... 100 mA
Peak Transient Input Current – I_F ..... 1.0 A (≤1 µs pulse width, 300 pps)
Reverse Input Voltage – V_R ..... 5 V
Input Power Dissipation (up to 70°C) ..... 250 mW*
Output Current – I_O (Pin 6) ..... 60 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 0.5 V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5)
CNW138 ..... -0.5 to 7 V
CNW139 ..... -0.5 to 18 V
Output Power Dissipation ..... 100 mW

*Derate at 5.0 mW/°C for operating temperatures above 70°C.

Schematic



CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

VDE 0884 Insulation Characteristics – Pending Approval

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 for rated mains voltage ≤ 600 V_{RMS} for rated mains voltage ≤ 1000 V_{RMS}		 I-IV I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0109/12.83)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{PEAK}
		1000	V_{RMS}
Input to Output Test Voltage, Method b* V_{PR} = 1.6 x V_{IORM}, 100% Production Test with tp = 1 sec, Partial Discharge < 5 pC	V_{PR}	2263	V_{PEAK}
		1600	V_{RMS}
Input to Output Test Voltage, Method a* V_{PR} = 1.2 x V_{IORM}, Type and sample test, tp = 60 sec, Partial Discharge < 5 pC	V_{PR}	1697	V_{PEAK}
	V_{PR}	1200	V_{RMS}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	8000	V_{PK}
Safety-Limiting Values (Maximum values allowed in the event of a failure, also see Figure 10)			
Case Temperature	T_{SI}	150	°C
Current (Input Current I_F, P_{SI} = 0)	I_{SI}	400	mA
Output Power (obtained by setting pin 8 = 5.5 V, pins 7, 6, 5 = ground)	$P_{SI, OUTPUT}$	700	mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_{IS}	≥ 10^9	ohm

*Refer to the front of the optocoupler section of the optoelectronics Designer's Catalog, under Product Safety Regulations section, (VDE 0884) for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Clearance (External Air Gap)	L(IO1)	9.6	mm	Measured from input terminals to output terminals
Min. External Creepage (External Tracking Path)	L(IO2)	10.0	mm	Measured from input terminals to output terminals
Min. Internal Clearance (Internal Plastic Gap)		1.0	mm	Through insulation distance conductor to conductor
Min. Internal Creepage (Internal Tracking Path)		4.0	mm	Measured from input terminals to output terminals
Comparative Tracking Index	CTI	200	volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group (DIN VDE 0109)

Electrical Specifications

Over Recommended Temperature (T_A = 0°C to 70°C) unless otherwise specified. (See note 7.)

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	CNW139	400	4500		%	I_F = 0.5 mA; V_{CC} = 4.5 V, V_O = 0.4 V	1, 2, 3	1, 2
			500	3000			I_F = 1.6 mA		
			300	1600			I_F = 5.0 mA		
			200	850			I_F = 12 mA		
		CNW138	300	1500		%	I_F = 1.6 mA		
Logic Low Output Voltage	V_{OL}	CNW139		0.1	0.4	V	I_F = 0.5 mA, I_O = 2 mA; V_{CC} = 4.5 V	1	2
							I_F = 1.6 mA, I_O = 8 mA		
							I_F = 5.0 mA, I_O = 15 mA		
							I_F = 12 mA, I_O = 24 mA		
		CNW138		0.1	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA		
Logic High Output Current	I_{OH}	CNW139		0.10	100	µA	V_O = V_{CC} = 18 V; I_F = 0 mA		2
		CNW138		0.05	250		V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}			0.5	2	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V	9	2
Logic High Supply Current	I_{CCH}			0.010	1	µA	I_F = 0 mA, V_O = Open V_{CC} = 18 V		2
Input Forward Voltage	V_F		1.25	1.45	1.70	V	T_A = 25°C; I_F = 1.6 mA	4, 8	
			1.10		1.80				
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA, T_A = 25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			1.9		mV/°C	I_F = 1.6 mA		
Input Capacitance	C_{IN}			90		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Voltage	V_{ISO}		5000			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		3, 8
Resistance (Input-Output)	R_{I-O}		10^{12}	10^{13}		Ω	V_{I-O} = 500 V_{DC}		3
			10^{11}				T_A = 100°C		
Capacitance (Input-Output)	C_{I-O}			0.5	0.6	pF	f = 1 MHz		3

*All typicals at T_A = 25°C.

Switching Specifications

Over Recommended Temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	CNW139		7	25	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 11	2, 4
					30				
				0.3	1		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω	7, 11	
					1.1				
		CNW138		2	10		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ	6, 11	
					11				
Propagation Delay Time to Logic High at Output	t_{PLH}	CNW139		40	60	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 11	2, 4
					115				
				3.5	7		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω	7, 11	
					11				
		CNW138		20	35		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ	6, 11	
					70				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		500			V/µs	I_F = 0 mA, R_L = 2.2 kΩ, R_{CC} = 0 Ω, V_{CM} = 10 V	12	5, 6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		500			V/µs	I_F = 1.6 mA, R_L = 2.2 kΩ, R_{CC} = 0 Ω, V_{CM} = 10 V	12	5, 6

*All typicals are at T_A = 25°C.

Notes:

1. DC CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Pin 7 Open.
3. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e. $V_O > 2.0$ V) Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e. $V_O < 0.8$ V).
6. In applications where dV/dt may exceed 50,000 V/µs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is
$$R_{CC} \approx \frac{1V}{0.15\ I_F\ (mA)}\ k\Omega.$$
7. Use of a 0.1 µF bypass capacitor connected betweens pin 5 and 8 is recommended for operation.
8. In accordance with UL 1577, each product is tested by applying an insulation test voltage of ≥ 6000 V_{rms} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA). This test is performed in addition to the tests shown in the VDE 0884 Insulation Characteristics table.

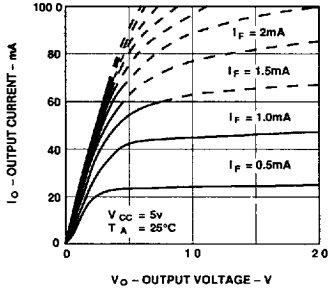


Figure 1. CNW138/9 DC Transfer Characteristics.

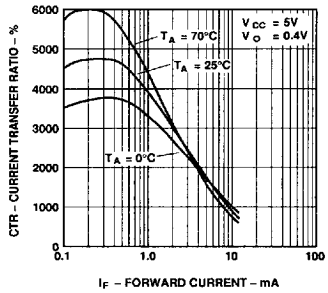


Figure 2. Current Transfer Ratio vs. Forward Current CNW138/9.

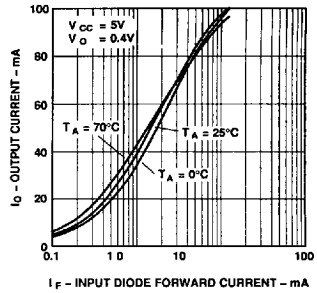


Figure 3. CNW 138/9 Output vs. Input Diode Forward Current.

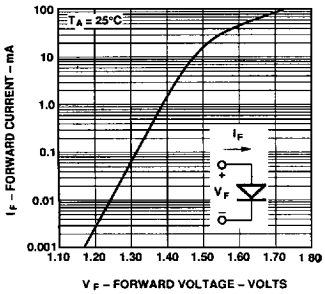


Figure 4. Input Diode Forward Current vs. Forward Voltage.

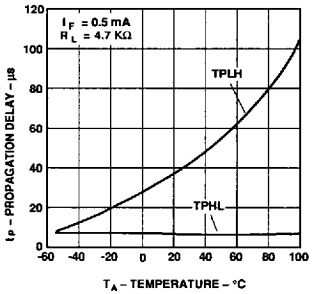


Figure 5. Propagation Delay vs. Temperature.

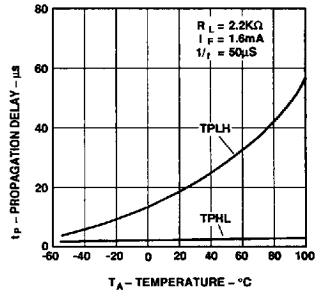


Figure 6. Propagation Delay vs. Temperature.

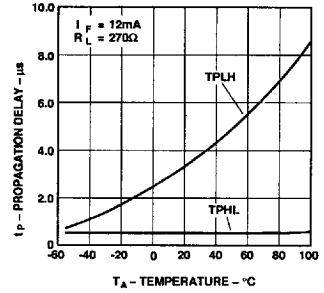


Figure 7. Propagation Delay vs. Temperature.

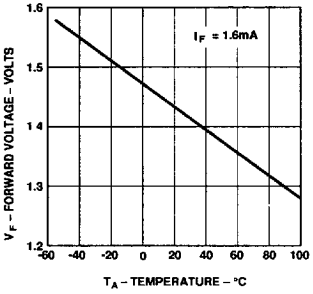


Figure 8. Forward Voltage vs. Temperature.

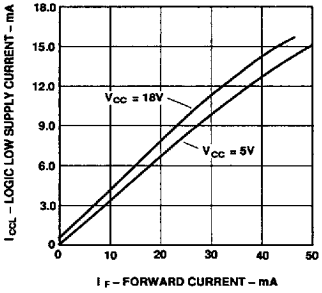


Figure 9. Logic Low Supply Current vs. Forward Current, CNW139.

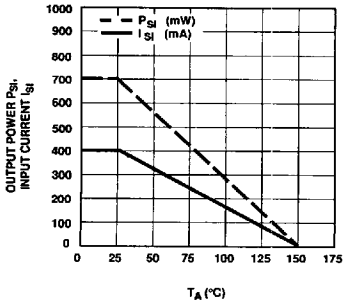


Figure 10. Dependence of Safety Maximum Ratings with Ambient Temperature.

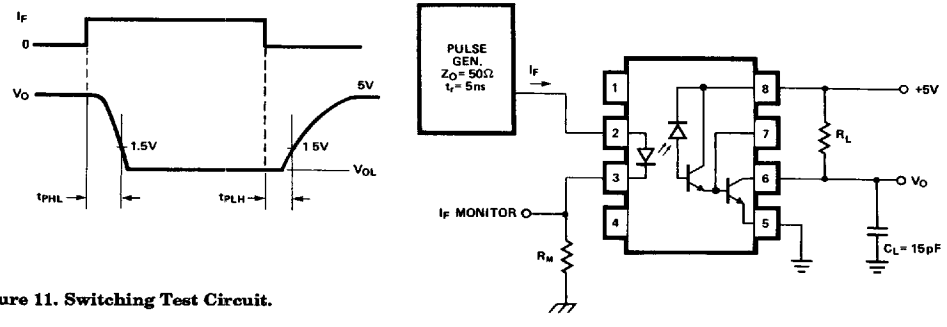


Figure 11. Switching Test Circuit.

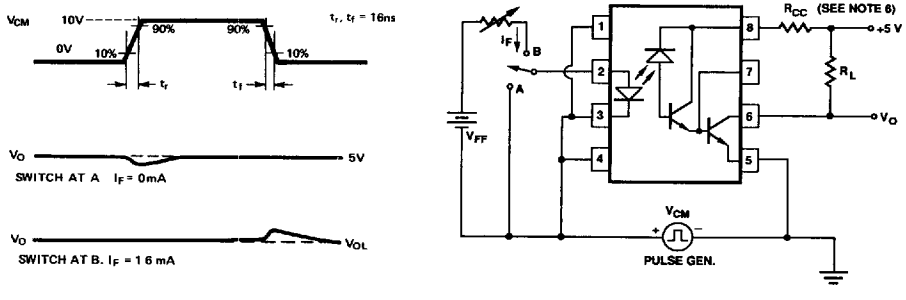


Figure 12. Test Circuit for Transient Immunity and Typical Waveforms.