FAIRCHILD SEMICONDUCTOR®

March 2013

FDD4N60NZ

N-Channel UniFET^{TM} II MOSFET

600 V, 3.4 A, 2.5 Ω

Features

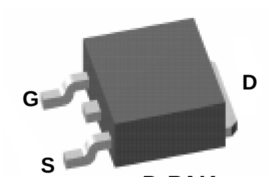
- $R_{DS(on)}$ = 1.9 Ω (Typ.) @ V_{GS} = 10 V, I_D = 1.7 A
- Low Gate Charge (Typ. 8.3 nC)
- Low C_{rss} (Typ. 3.7 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Applications

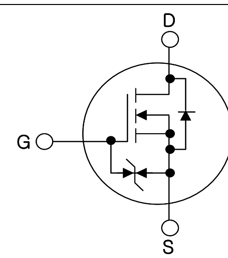
- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

Description

UniFET^{TM} II MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET^{TM} II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



D-PAK



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter			FDD4N60NZ	Unit
V_{DSS}	Drain to Source Voltage			600	V
V_{GSS}	Gate to Source Voltage			±25	V
I_D	Drain Current	- Continuous (T_C = 25°C)		3.4	A
		- Continuous (T_C = 100°C)		2	
I_{DM}	Drain Current	- Pulsed	(Note 1)	13.6	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	179.2	mJ
I_{AR}	Avalanche Current		(Note 1)	3.4	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	11.4	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	5	V/ns
P_D	Power Dissipation	(T_C = 25°C)		114	W
		- Derate above 25°C		0.9	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	FDD4N60NZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD4N60NZ	FDD4N60NZ	D-PAK	380mm	16mm	2500

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_J = 25^oC$	600	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.6	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600V$, $V_{GS} = 0V$	-	-	50	μA
		$V_{DS} = 480V$, $T_C = 125^oC$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25V$, $V_{DS} = 0V$	-	-	±10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 1.7A$	-	1.9	2.5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20V$, $I_D = 1.7A$	-	3.4	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz	-	385	510	pF
C_{oss}	Output Capacitance		-	40	60	pF
C_{rss}	Reverse Transfer Capacitance		-	3.7	5	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 480V$ $I_D = 3.4A$ $V_{GS} = 10V$ (Note 4)	-	8.3	10.8	nC
Q_{gs}	Gate to Source Gate Charge		-	2.1	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	3.3	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300V$, $I_D = 3.4A$ $V_{GS} = 10V$, $R_G = 25\Omega$ (Note 4)	-	12.7	35.4	ns
t_r	Turn-On Rise Time		-	15.1	40.2	ns
$t_{d(off)}$	Turn-Off Delay Time		-	30.2	70.4	ns
t_f	Turn-Off Fall Time		-	12.8	35.6	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	3.4	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	13.6	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 3.4A$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 3.4A$ $dI_F/dt = 100A/\mu s$	-	168	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.7	-	μC

Notes:
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 31mH, $I_{AS} = 3.4A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25°C$
3. $I_{SD} \leq 3.4A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

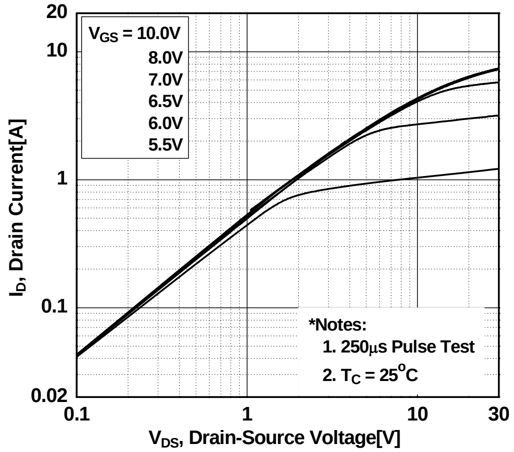


Figure 2. Transfer Characteristics

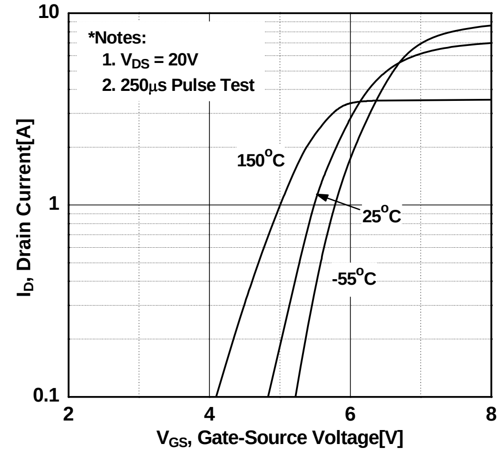


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

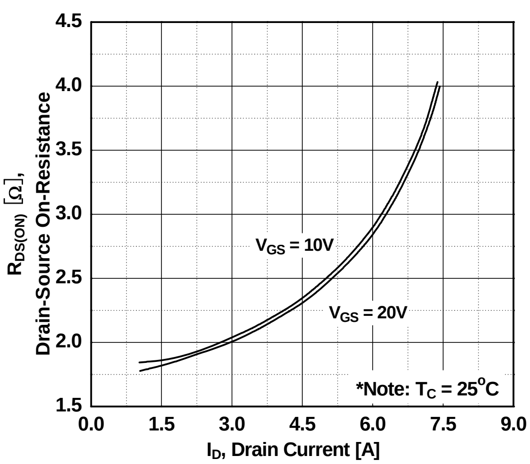


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

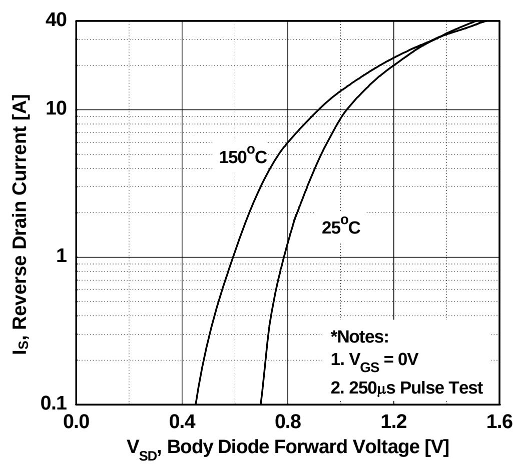


Figure 5. Capacitance Characteristics

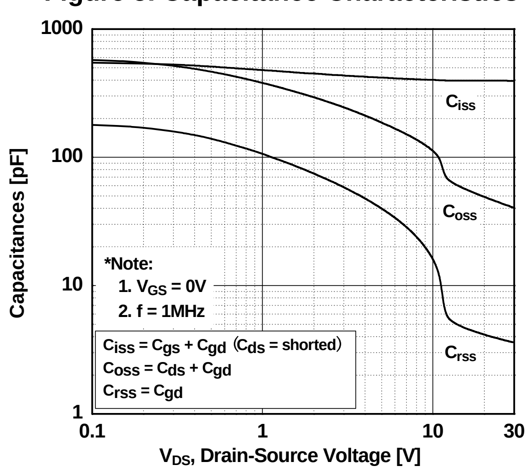
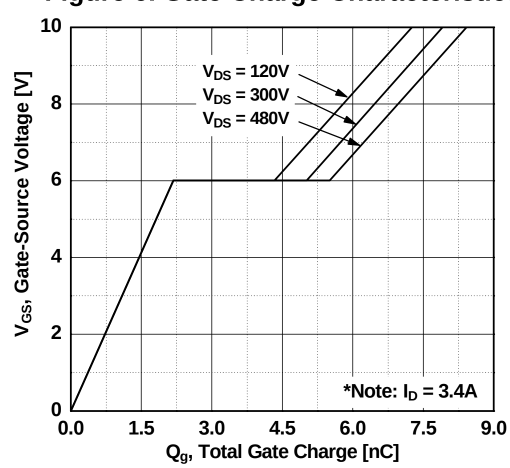


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

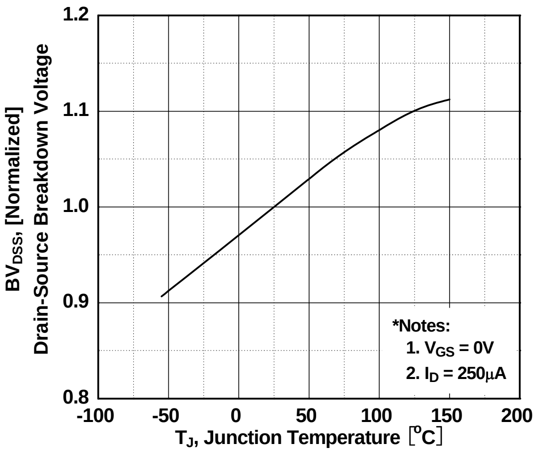


Figure 8. On-Resistance Variation vs. Temperature

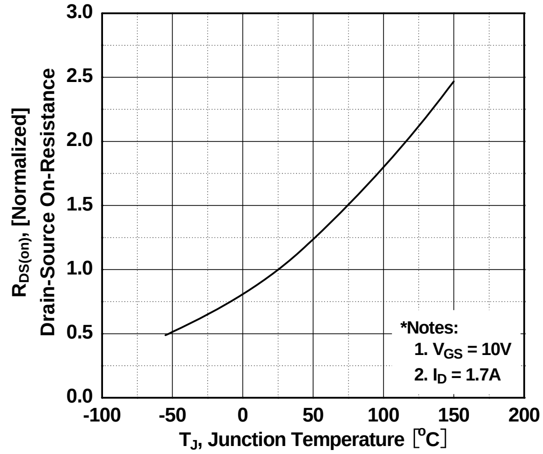


Figure 9. Maximum Safe Operating Area vs. Case Temperature

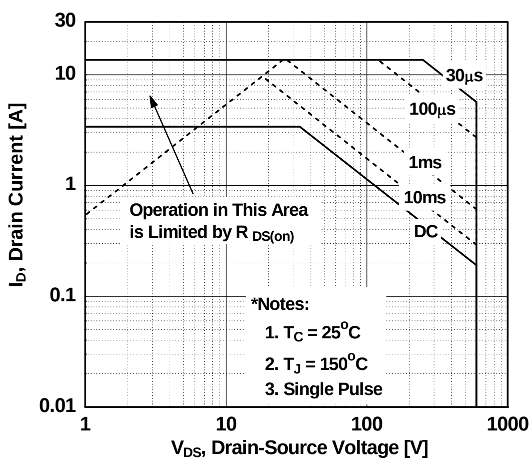


Figure 10. Maximum Drain Current

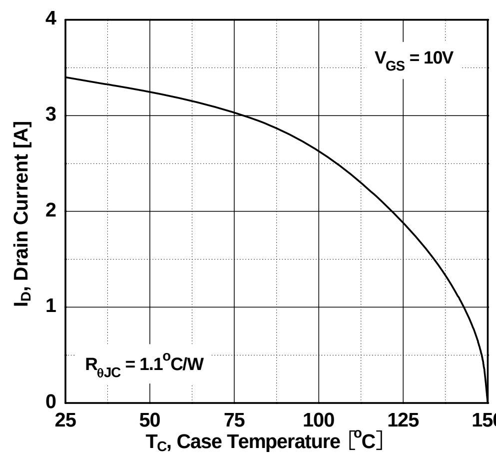
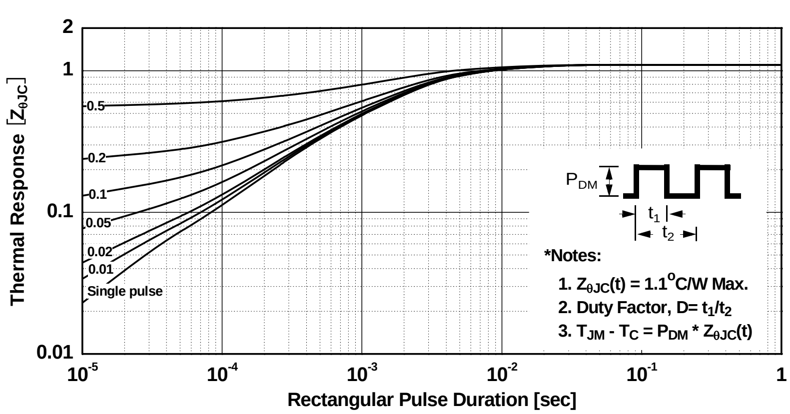
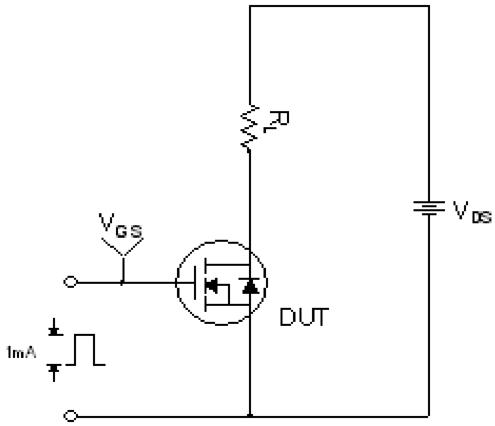
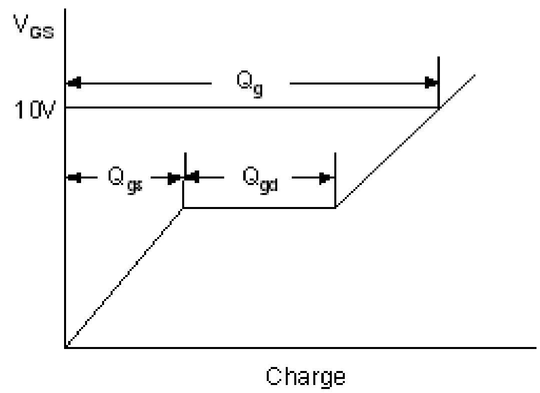


Figure 11. Transient Thermal Response Curve

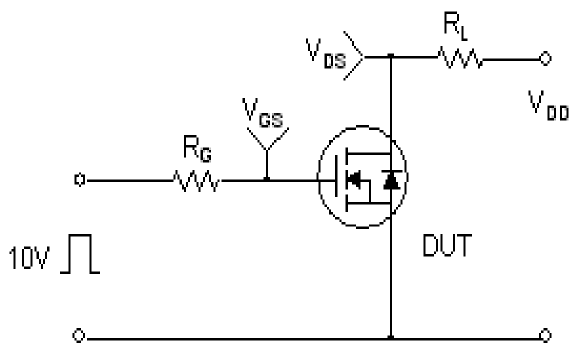


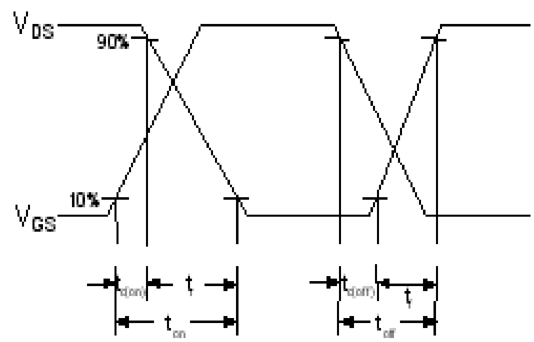
Gate Charge Test Circuit & Waveform



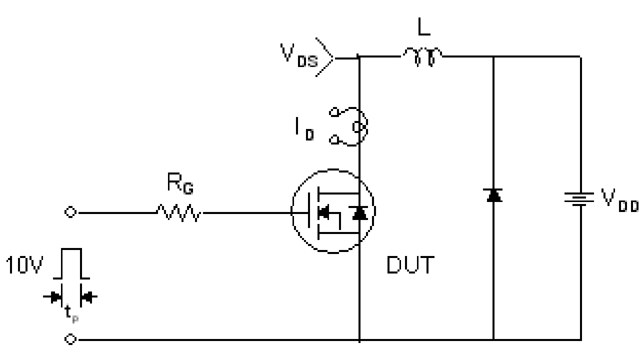


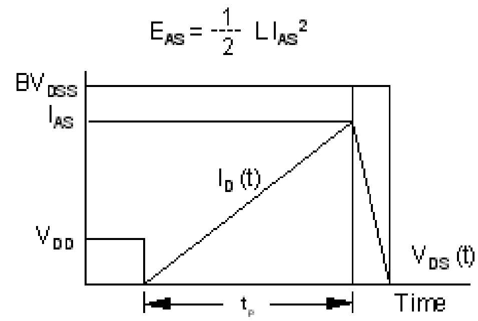
Resistive Switching Test Circuit & Waveforms



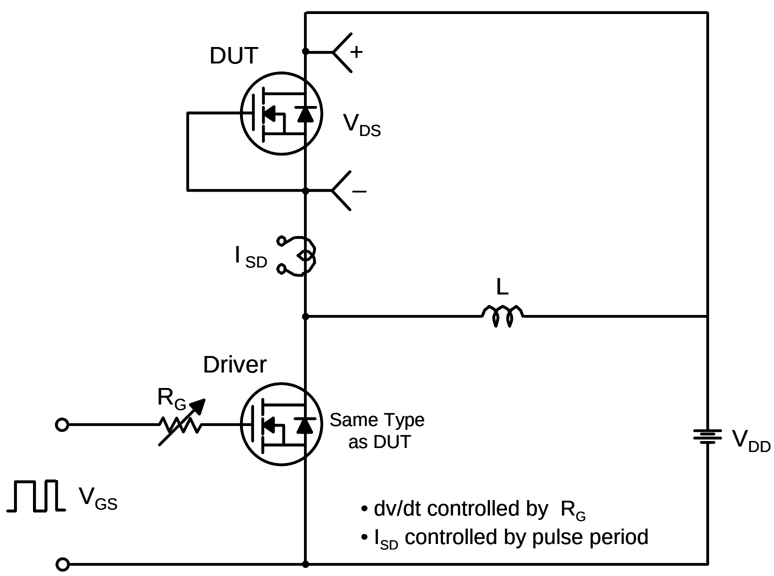


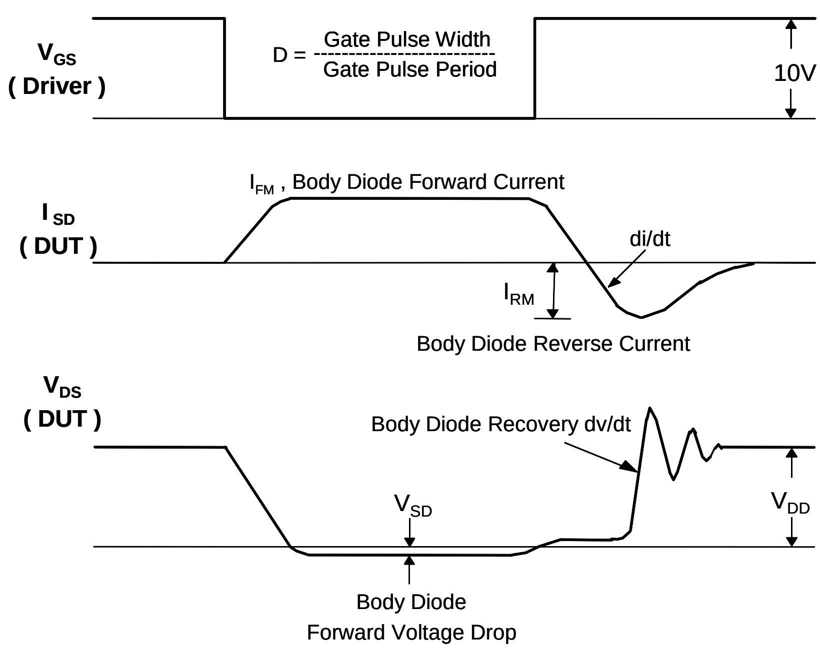
Unclamped Inductive Switching Test Circuit & Waveforms





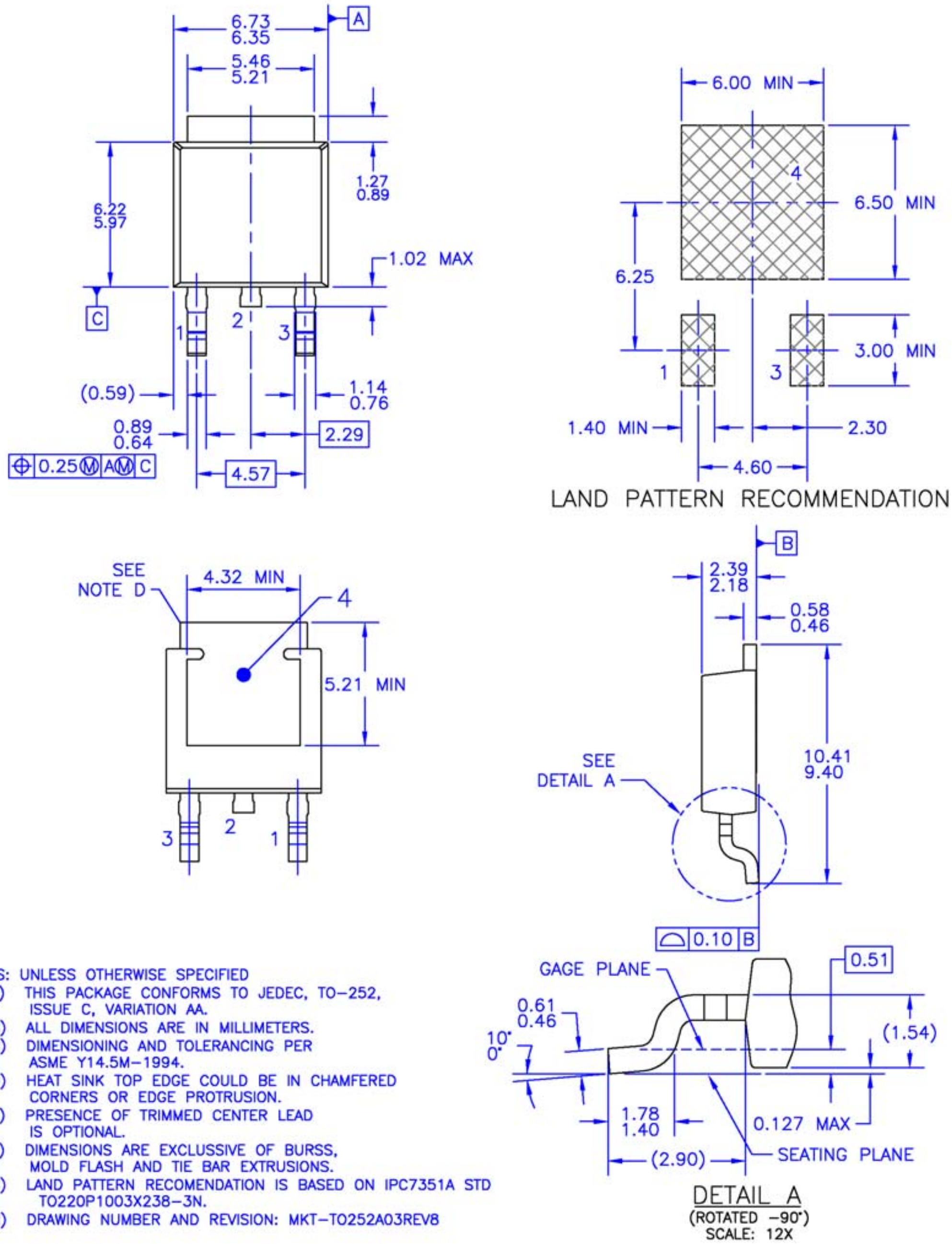
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

D-PAK



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO−252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238−3N.
H) DRAWING NUMBER AND REVISION: MKT−TO252A03REV8

Dimensions in Millimeters

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