QN8035

Single-Chip Low-Power FM Receiver for Portable Devices

Preliminary

General Description

The QN8035 is a high performance, low power; full-featured single-chip stereo FM receiver designed for cell phones, MP3 players. The QN8035 also supports RDS/RBDS data reception.

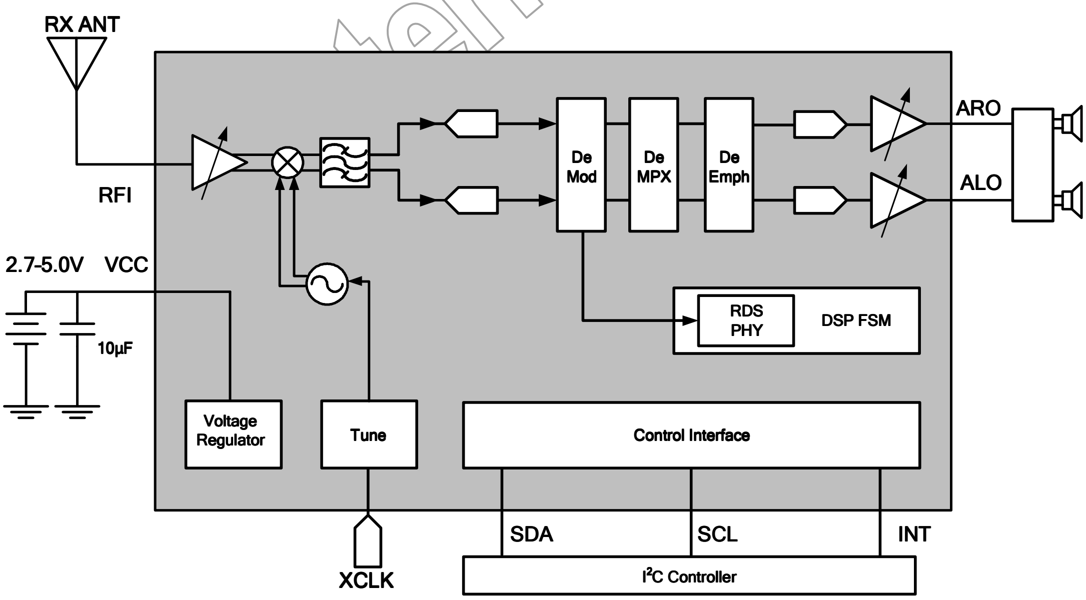
Typical Applications

- *Cell Phones / PDAs / Smart Phones*
- *Portable Audio & Media Players*
- *MP3/MP4 player, PMP, PND*

Key Features

- **Worldwide FM Band Coverage**
  - *60 MHz to 108 MHz full band tuning in 50/100/200 kHz step sizes*
  - *50/75µs de-emphasis*
- **Ease of Integration**
  - *Small footprint, available in 2.5 x2.5 QFN16 and 3x3 MSOP10 packages*
  - *32.768 kHz and multiple MHz clocks input*
  - *I^2C control interface*
- **Very Low Power Consumption**
  - *13 mA typical*
  - *VCC: 2.7~5.0V, integrated LDO, support battery direct connection*
  - *Power saving Standby mode*
  - *Low shutdown leakage current*
  - *Accommodate 1.6~3.6V digital interface*
- **Adaptive Noise Cancellation**
- **Volume Control**
- **High Performance**
  - *Superior sensitivity, better than 1.5 μV_{EMF}*
  - *63dB stereo SNR, 0.03% THD*
  - *Integrated adaptive noise cancellation (SNC, HCC, SM)*
  - *Improved auto channel seek*
  - *L/R separation 45dB*
- **RDS/RBDS**
  1. *Supports US and European data services*
  - *Superior sensitivity, better than 8.9 μV_{EMF}*
- **Robust Operation**
  - *-25^0C to $+85^0C$ operation*
  - *ESD protection on all input and output pads*

QN8035 Functional Blocks:



Ordering Information appears at Section 7.

CONTENTS

REVISION HISTORY

REVISION	CHANGE DESCRIPTION	DATE
0.1	Draft	12/11/09
0.02	Modify the Reg 05h	01/14/10
0.03	1. Modify the Figure 7 I^2C Serial Control Interface Protocol 2. Update the Chapter 5; 3. Update the Table 10 Summary of User Control Registers	01/18/10
0.04	Modify the data in Chapter 2.	01/18/10
0.05	Modify the test conditions in Chapter 2	01/20/10
0.06	Modify the Reg 05h	01/25/10
0.07	Modify the Chapter 5.	02/10/10
0.08	1. Modify the descriotion in Key Features “High Performance”; 2. Modify the figure “QN8035 Functional Blocks”; 3. Add 3 symbols in Table 6: R_{LOAD}, C_{LOAD}, THD_{driver}; 4. Replace the Figure 8 and Figure 9; 5. Modify “Notes: See also PLL_DIV[12:0]” in Table 5 6. Modify some mistakes in Section 5.3 7. Replace Figure15 2.5X2.5 QFN16 Carrier Tape	02/22/10

1 PIN ASSIGNMENT

(Top View)

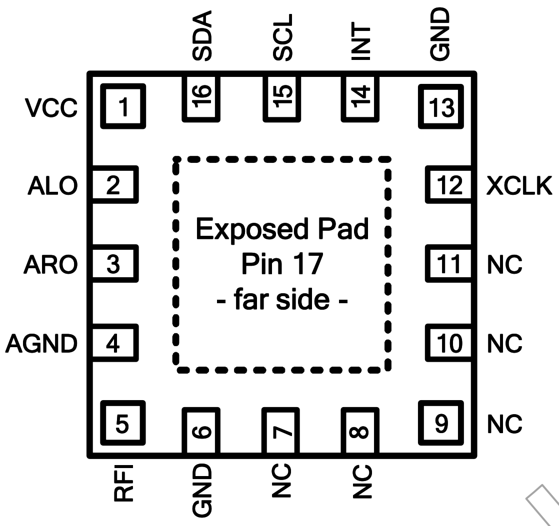


Figure 1 QN8035-NCNA NCNA Pin Out QFN16 2.5x2.5mm

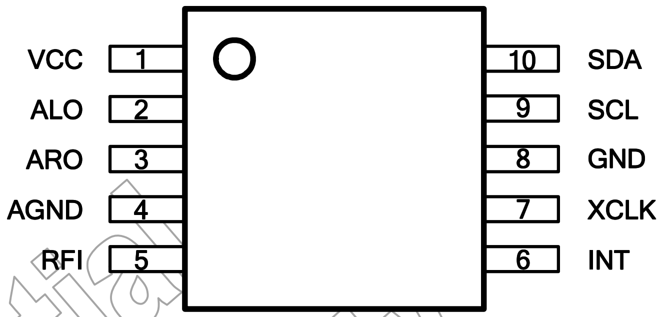


Figure 2 QN8035-SANA Pin Out MSOP10 3x3mm

Table 1: Pin Descriptions

MSOP10	QFN24	NAME	DESCRIPTION
1	1	VCC	Voltage supply
2	2	ALO	Analog audio output – left channel
3	3	ARO	Analog audio output – right channel
4	4	AGND	Ground
5	5	RFI	FM Receiver RF input
	6	GND	RF ground
7	12	XCLK	If using an external clock source, inject from this pin
8	13	GND	Ground
6	14	INT	Interrupt output, active low, need pull-up externally
9	15	SCL	Clock for I^2C serial bus.
10	16	SDA	Bi-directional data line for I^2C serial bus.
	7/8/9/10/ 11	NC	No connect.

2 ELECTRICAL SPECIFICATIONS

Table 2: Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{bat}	Supply voltage	VCC to GND	-0.3	5	V
V_{IO}	Logic signal level	CEN, SCL, SDA, INT to GND	-0.3	3.6	V
T_s	Storage temperature		-55	+150	^oC

Table 3: Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Vcc	Supply voltage	VCC to GND	2.7	3.3	5.0	V
T_A	Operating temperature		-25		+85	^oC
RF_{in}	RF input level[1]	Peak input voltage			0.3	V
V_{IO}	Digital I/O voltage		1.6		3.6	V

Notes:
1. At RF input pin, RFI.

Table 4: DC Characteristics

(Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{RX}	Receive mode supply current			13		mA
I_{IDLE}	Idle mode supply current	Idle mode		TBD		mA
I_{STBY}	Standby mode supply current	Standby mode		TBD		µA
I_{PDN}	Power down leakage current	Power down		TBD		µA
Interface						
V_{OH}	High level output voltage		$0.9*V_{IO}$			V
V_{OL}	Low level output voltage				$0.1*V_{IO}$	V
V_{IH}	High level input voltage		$0.7*V_{IO}$			V
V_{IL}	Low level input voltage				MIN (0.3*VIO , 0.6)	V

Table 5: AC Characteristics

(Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
F_{xtal}	Crystal or Clock frequency		0.032768 -40[1]			MHz
F_{xtal_err}	Crystal frequency accuracy	Over temperature, and aging	-20		20	ppm

Notes:
1. See also PLL_DIV[12:0]

Table 6: Receiver Characteristics

(Typical values are at Vcc = 3.3V, f carrier=88 MHz and T_A = 25°C).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
S_{RX}	FM sensitivity	(S+N)/N = 26dB		TBD		μV_{EMF}
S_{RDS}	RDS sensitivity	BER≤5%, average over 2000 blocks		TBD		μV_{EMF}
IP3	Input referred IP3	At maximum gain		TBD		dBμV
Rej_{AM}	AM suppression			70		dB
R_{in}	RF input impedance	At pin RFI		1		kΩ
S_{RX_Adj}	Adjacent channel rejection	200 kHz offset		50		dB
S_{RX_Alt}	Alternate channel rejection	400 kHz offset		50		dB
SNR_{audio_in}	Audio SNR	MONO, Δf = 22.5 kHz[1]		57		dB
		STEREO, Δf = 67.5 kHz, Δf_{pilot} = 6.75 kHz		63		
THD_{audio_in}	Audio THD	MONO, Δf = 75 kHz		0.03		%
		STEREO, Δf = 67.5 kHz, Δf_{pilot} = 6.75 kHz		0.03		%
α_{LR_in}	L/R separation			40		dB
Att_{Pilot}	Pilot rejection			66		dB
B_{LR}	L/R channel imbalance	L and R channel gain imbalance at 1 kHz offset from DC			1	dB
τ_{emph}[1]	De-emphasis time constant	PETC = 1	71.3	75	78.7	μs
		PETC = 0	47.5	50	52.5	μs
V_{audio_out}	Audio output voltage	Peak-Peak, single ended		1	1.4	V
R_{LOAD}	Audio output Loading Resistance		0.6			kΩ
C_{LOAD}	Audio output loading capacitance				20	pF
$RSSI_{err}$	RSSI uncertainty		-3		3	dB
R_{LOAD}	Audio output Loading Resistance		32			Ω
C_{LOAD}	Audio output loading capacitance				20	pF
THD_{driver}	Audio THD after earphone driver	R_{LOAD}=16Ω , 500mV_p output		53		dB
		R_{LOAD}=32Ω, 500mV_p output		61		dB

Notes:
1. Guaranteed by design.

Table 7: Timing Characteristics

(Typical values are at Vcc = 3.3V and $T_A = 25^oC$).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
τ_{pup}	Chip power-up time [1]	From rising edge of CEN to valid audio output.			0.6	Sec
τ_{astby}	Auto Standby time [2]	TMOUT [1:0] = 00		1		Min
		TMOUT [1:0] = 01		3		
		TMOUT [1:0] = 10		5		
		TMOUT [1:0] = 11		Never		
τ_{chsw}	Channel switching time[1]	From any channel to any channel.			0.12	Sec
Receiver Timing						
τ_{wkup}	Wake-up time from standby to receive	Standby to RX mode.		200		ms
τ_{tune}	Tune time	Per channel during CCA.		5		ms

Notes:
1. Guaranteed by design.
2. Chip automatically goes from IDLE to standby mode; TMOUT = 11 equivalent to auto standby disabled.

Table 8: I²C Interface Timing Characteristics

(Typical values are at Vcc = 3.3V and $T_A = 25^oC$).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	I²C clock frequency				400	kHz
t_{LOW}	Clock Low time		1.3			µs
t_{HI}	Clock High time		0.6			µs
t_{ST}	SCL input to SDA falling edge start [1,3]		0.8			µs
t_{STHD}	SDA falling edge to SCL falling edge start[3]		0.8			µs
t_{rc}	SCL rising edge[3]	Level from 30% to 70%			300	ns
t_{fc}	SCL falling edge[3]	Level from 70% to 30%			300	ns
t_{dtHD}	SCL falling edge to next SDA rising edge[3]		20			ns
t_{dtc}	SDA rising edge to next SCL rising edge[3]				900	ns
t_{stp}	SCL rising edge to SDA rising edge [2,3]		0.6			µs
t_w	Duration before restart[3]		1.3			µs
C_b	SCL, SDA capacitive			10		pF

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
	loading[3]					

Notes:

1. Start signaling of I^2C interface.
2. Stop signaling of I^2C interface.
3. Guaranteed by design.

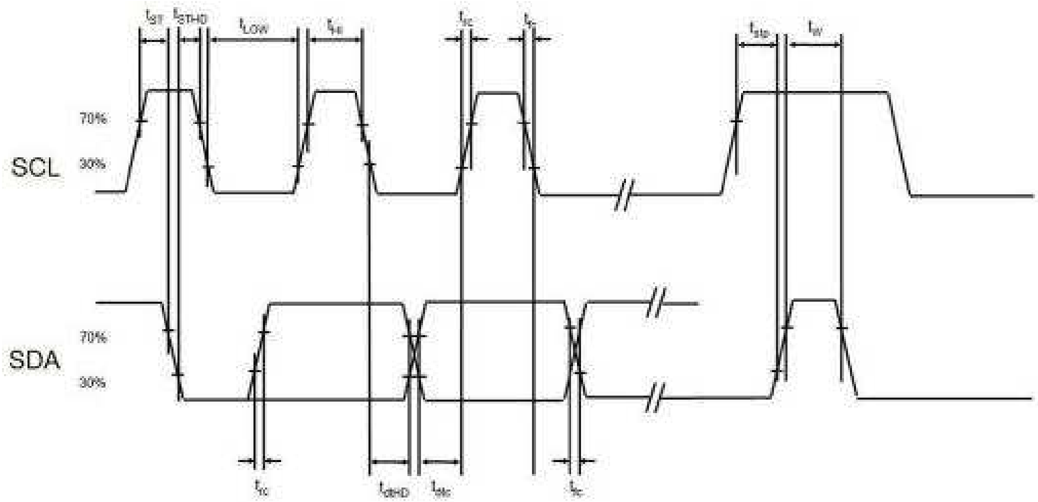


Figure 3 I^2C Serial Control Interface Timing Diagram

3 FUNCTIONAL DESCRIPTION

The QN8035 is a high performance, low power, single chip FM receiver IC that supports worldwide FM broadcast band (60 to 108MHz). RDS/RBDS data service is also supported.

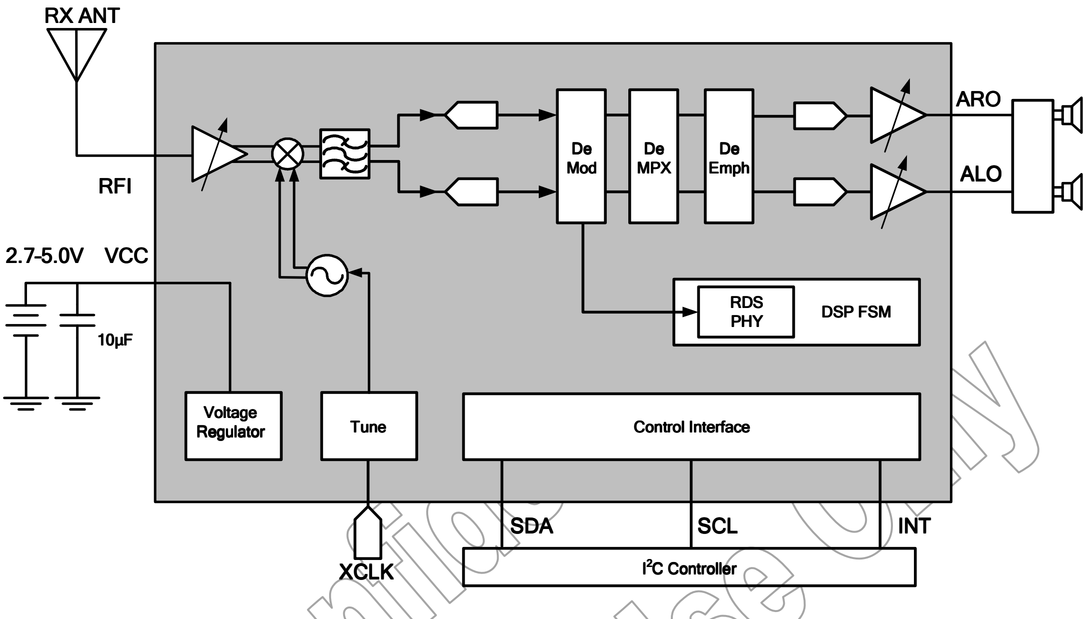


Figure 4 QN8035 Functional Blocks

The QN8035 integrates FM receive functions, including RF front-end circuits (LNA, Mixer and channel selective filter etc), a fully digitized FM demodulator, MPX decoder, de-emphasis and audio processing (SM, HCC, and SNC). Advanced digital architecture enables superior receiver sensitivity and crystal clear audio. The QN8035's Auto Seek function enables automatic channel selection for better sound quality.

The QN8035 supports a small footprint, high level of integration and multiple clock frequencies. These features make it easy to be integrated into a variety of small form-factor, low-power portable applications. Low phase noise digital synthesizers and extensive on-chip auto calibration ensures robust and consistent performance over temperature and process variations. An integrated voltage regulator enables direct connection to a Li-ion battery and provides high PSRR for superior noise suppression. A low-power IDLE and Standby mode extends battery life.

3.1 FM Receiver

The QN8035 receiver uses a highly digitized low-IF architecture, allowing for the elimination of external components and factory adjustments.

The received RF signal is first amplified by an integrated LNA and then down converted to an intermediate frequency (IF) via a quadrature mixer. To improve image rejection (IMR), the quadrature mixer can be programmed to be at high-side or low-side injection. When the RF frequency is greater than the local oscillator (LO), image is at low side; otherwise, image is at high side (Refer to Reg02h for more information). An integrated IF channel filter rejects out-of-channel interference signals. AGC is also performed simultaneously to optimize the signal to noise ratio as well as linearity and interference rejection. The filtered signal is digitized and further processed with a digital FM demodulator and MPX decoder. Audio processing is then performed based on received signal quality and channel condition. Two high-quality audio DACs are integrated on chip to drive the audio output. The RDS signal will also be decoded if RDS reception is enabled.

A receive signal strength indicator (RSSI) is provided and can be read from RSSIDB [7:0]. Figure 5 shows the curve of RSSI vs. different RF input levels. Auto seek utilizes RSSI to search for available channels.

The following figure is measured at FM=88MHz. The RSSI Curve is not varied by FM frequency.

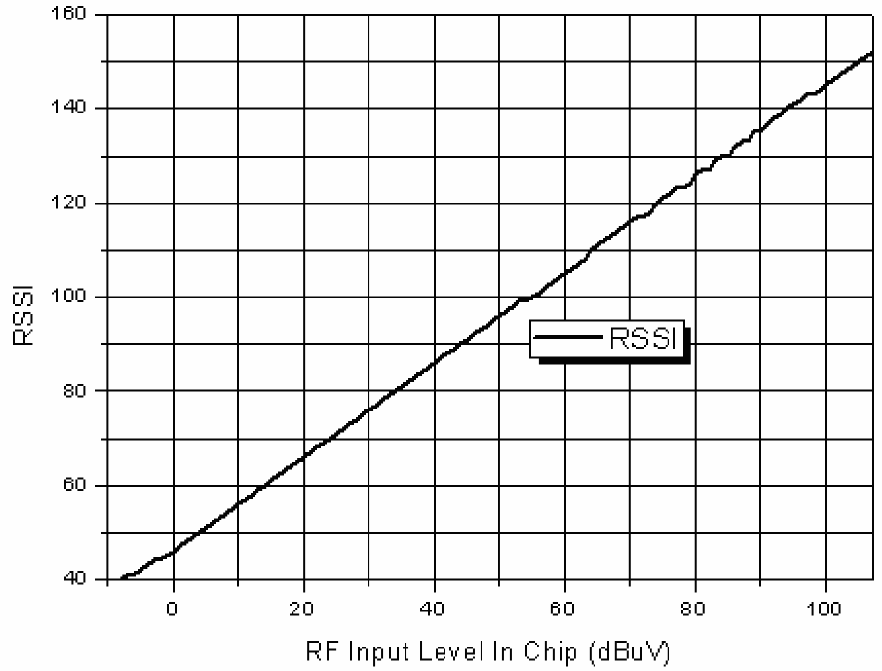


Figure 5 RSSI vs RF Input

3.2 Audio Processing

The MPX signal after FM demodulation is comprised of left and right channel signal, pilot and RDS signal in the following way:

$$m(t) = [L(t) + R(t)] + [L(t) - R(t)]\sin(4\pi ft + 2\theta_0) + \alpha\sin(2\pi ft + \theta_0) + d(t)\sin(6\pi ft + 3\theta_0)$$

Here, L(t) and R(t) correspond to the audio signals on the left and right channels respectively, f = 19 kHz, θ is the initial phase of pilot tone and α is the magnitude of the pilot tone, and d(t) is the RDS signal. In stereo mode, both L and R are recovered by de-MPX. In mono mode, only the L+R portion of audio signal exists. L(t) and R(t) are recovered by de-MPX.

In receive mode, stereo noise cancellation (SNC) for FM only, high cut control (HCC) and soft mute (SM) are supported. Stereo noise suppression is achieved by gradually combining the left and right signals to be a mono signal as the received signal quality degrades. SNC, HCC and SM are controlled by SNR and multipath channel estimation results. The three functions will be archived automatically in the device.

The QN8035 has an integrated mono or stereo audio status indicator. There is also a Read ST_MO_RX (Reg04h [0]) bit to get sound information. In addition, there also is a force mono function to constrain output mono in Reg04h.

To improve the signal-to-noise ratio of the FM receiver by reducing the effect of high frequency interference and noise, the device integrates a technique known as de-emphasis. There are two selectable time constants (75us and 50us) supported.

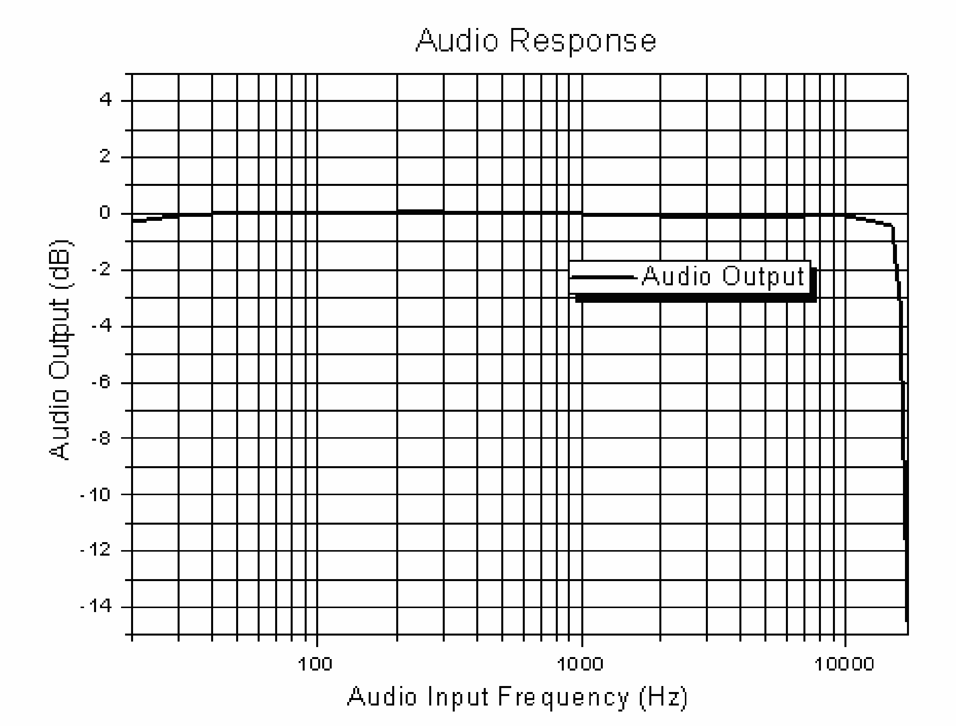


Figure 6 Audio Response

The audio output can be muted with the MUTE_EN (Reg14h[7]) bit and the output can also be replaced by an internally generated 1KHz tone whenever the RFI has a RF signal input.

3.3 RDS/RBDS

The QN8035 supports RDS/RBDS data reception in FM mode, including station ID, Meta data, TMC information, etc. The integrated RDS processor performs all symbol encoding/decoding, block synchronization, error detection and correction functions. RDS/RBDS data communicates with an external MCU through the serial control interface.

3.4 Auto Seek (CCA)

In receive mode, the QN8035 can automatically tune to stations with good signal quality. The auto seek function is referred to CCA (Clear Channel Assessment).

4 CONTROL INTERFACE PROTOCOL

The QN8035 supports the standard I²C serial interfaces. At power-on, all register bits are set to default values.

I²C Serial Control Interface

The I²C bus is a simple bi-directional bus interface. The bus requires only serial data (SDA) and serial clock (SCL) signals. The bus is 8-bit oriented. Each device is recognized with a unique address. Each register is also recognized with a unique address. The I²C bus operates with a maximum frequency of 400 kHz. Each data put on the SDA must be 8 bits long (Byte) from MSB to LSB and each byte sent should be acknowledged by an "ACK" bit. In case a byte is not acknowledged, the transmitter should generate a stop condition or restart the transmission. If a stop condition is created before the whole transmission is completed, the remaining bytes will keep their old setting. In case a byte is not completely transferred, it will be discarded.

Data transfer to and from the QN8035 can begin when a start condition is created. This is the case if a transition from HIGH to LOW on the SDA line occurs while the SCL is HIGH. The first byte transferred represents the address of the IC plus the data direction. The default IC address is 0010000. A LOW LSB of this byte indicates data transmission (WRITE), while a HIGH LSB indicates data request (READ). This means that the first byte to be transmitted to the QN8035 should be "20" for a WRITE operation or "21" for a READ operation.

The second byte is the starting register address (N) for write/read operation. The following bytes are register data for address N, N+1, N+2, etc. There is no limit on the number of bytes in each transmission. A transmission can be terminated by generating a stop condition, which is SDA transition from LOW to HIGH while SCL is HIGH. For write operation, master stops transmission after the last byte. For read operation, master doesn't send ACK after receiving the last read back byte; then stops the transmissio

The timing diagrams below illustrate both write and read operations.

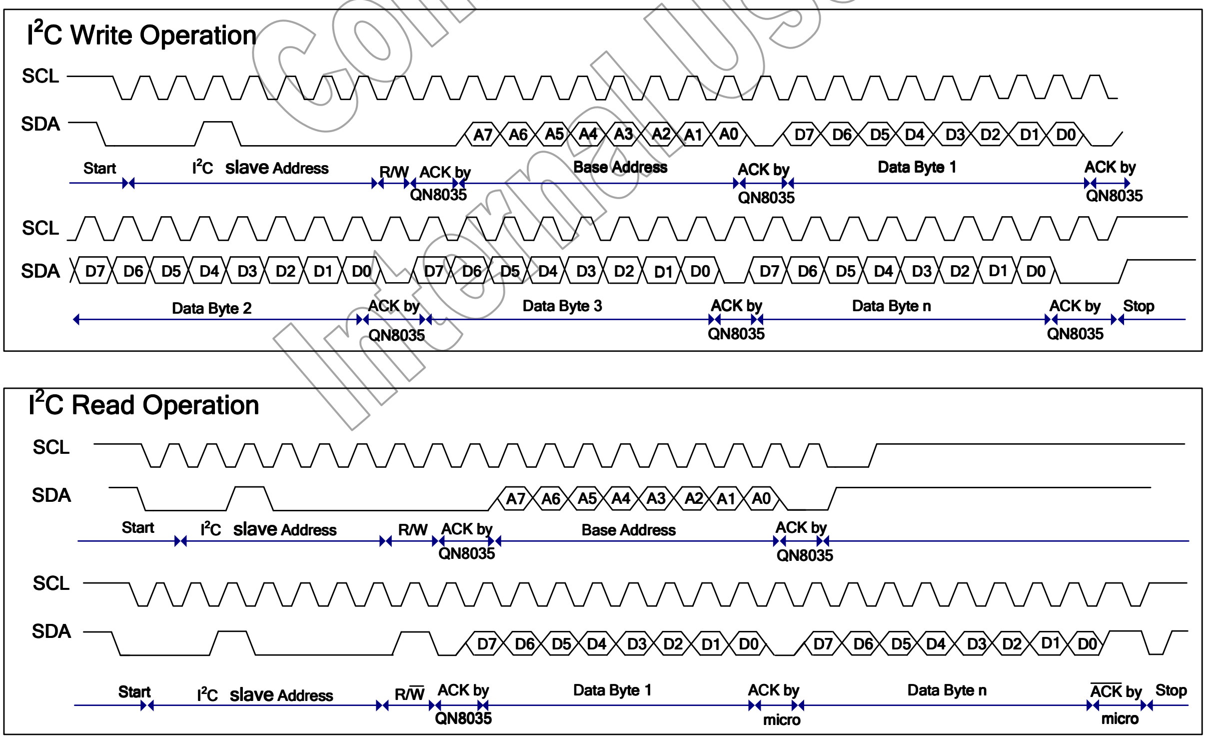


Figure 7 I²C Serial Control Interface Protocol

Notes:

1. The default IC address is 0010000.
2. "20" for a WRITE operation, "21" for a READ operation.

5 APPLICATIONS

5.1 Typical Application Schematic

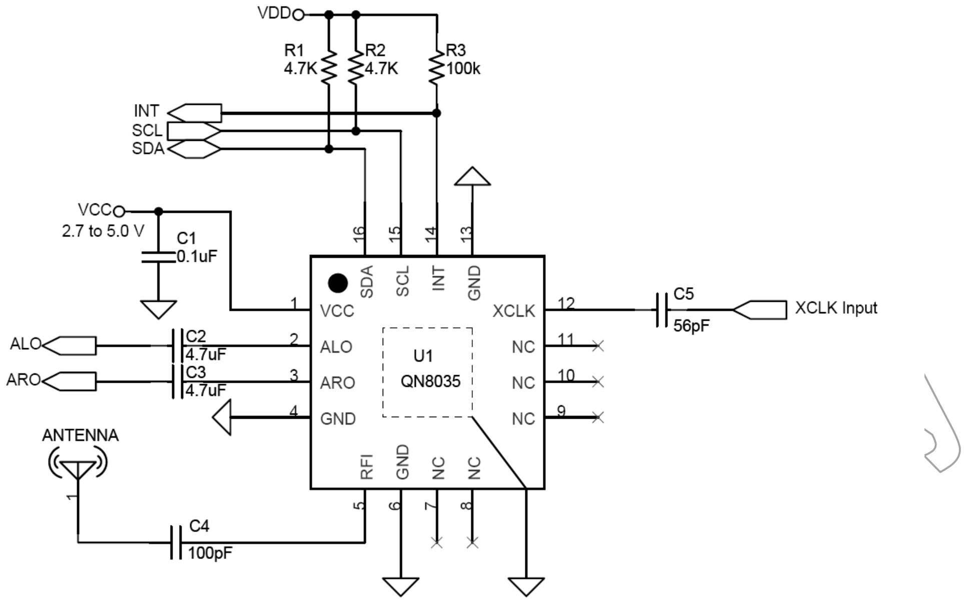


Figure 8 Typical Application Schematic

5.2 Power Supply

The QN8035 provides an integrated voltage regulator that requires only one decoupling capacitor of about 0.1uF on the battery power supply. A 10uF capacitor can be added for best performance. The supported power supply voltage range is 2.7 to 5.0V.

5.3 Clock Selection and Setting

The QN8035 supports various external frequencies clock injection through a coupling capacitor. The following figure shows typical external injection circuit as reference.

1) External Clock Application:

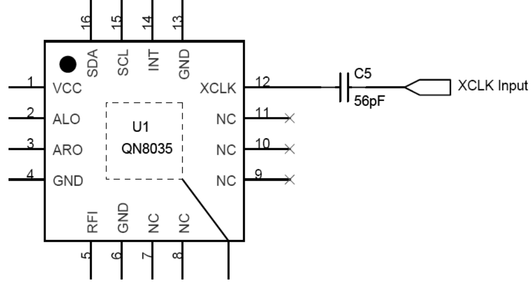


Figure 9 External Clock Input Circuit

Note: 32.768KHz or greater than or equal to 1MHz Clock can be supported

2) XTAL Setting:

XTAL_DIV[10:0] can be computed by the following formula, and then wirte its result to Reg15h and Reg16h[2:0].

XTAL_DIV[10:0] =round($Freq_{xtal}$/32.768KHz).

The default value is 0x01 for 32.768KHz clock.

3) PLL Configuration:

To select the clock frequency, set the PLL frequency divider according to the following formula:

PLL_DLT[12:0=Round(28.5MHz/($Freq_{xtal}$ /XTAL_DIV[10:0]/512))-442368

For example: If clock frequency is 32.768KHZ, then so PLL_DLT[12:0]=Round(28500000/(32768/1/512))-442368 =2945

Translating this numble into a hex result, and then write corresponding value to Reg17h and Reg16h[7:2]. The default value of this parameter PLL_DLT [12:0] is 0xB81 for 32.768 KHz.

5.4 Audio Interface

The QN8035 has a highly flexible analog audio interface. The maximum single-ended audio output level is 1.4V peak-to-peak and is AC coupled to external audio driver. An external audio driver should be used when driving the headphone or speaker directly.

5.5 Antenna

The following circuit is a typical application utilizing the earphone line as a FM antenna. Three ferrite beads are used to prevent interference of the FM signal with the audio signal. A typical ferrite bead value is about 2.5K@100MHz.

For more information on FM antenna design, please refer to related application notes.

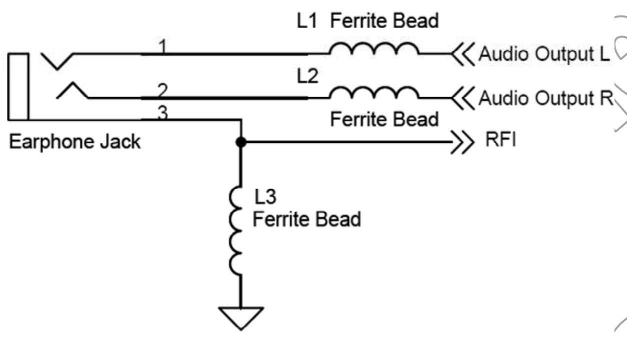


Figure 10 Earphone Line as FM Antenna

5.6 Reset

The QN8035 supports software reset, set Reg00h[7] bit high to reset the device.

After reset, the device will enter standby mode. Before starting receive mode, system initialization should be executed.

5.7 Receive Mode

The QN8035 supports software to enable receiving function from low power consumption state. After powering up, the device will stop at standby mode automatically after going through hardware and software initialization (refer to Section 5.13), set RXREQ (Reg00h [4]) bit high and STNBY(Reg00h[5]) bit low to enter receive mode.

To configure the FM receiver, programmability through registers are provided to select frequency, set channel index, select de-emphasis constants (75us or 50us), enable audio mute and volume control.

5.8 IDLE and Standby Modes

The QN8035 features low power idle and standby modes for fast state transition and power saving. After power up, the QN8035 will enter standby mode automatically.

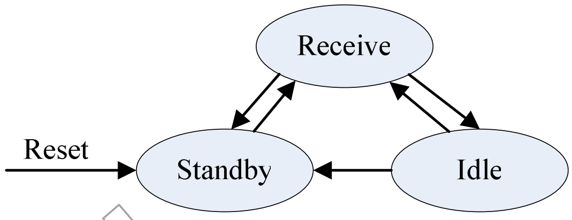


Figure 11 Three Modes Switching

As shown in Figure 11, standby mode can not directly enter idle mode.

Table 9: Mode Switching

Mode \ Bit	STNBY (Reg00h[5])	RXREQ (Reg00h[4])
Receive	0	1
Idle	0	0
Standby	1	x

The Standby mode is the highest priority mode. If STNBY (Reg00h[5]) is low and RXREQ (Reg00h[4]) bits is high, the device will enter the receive mode.

STNBY and RXREQ bits of the Reg00h are used for setting all three modes. Refer to Reg00h for detailed information.

If there is no receiving requirement in a pre-determined time period, the QN8035 should enter standby mode by set register to save power consumption.

5.9 Volume Control

The QN8035 integrates an analog volume controller and a digital volume controller to set audio output gain. The digital gain step is 1dB, and the analog gain step is 6dB. The total gain range is -47 dB to 0 dB. Refer to Reg14h for more descriptions.

5.10 Channel Setting

Manual Channel Setting

By programming channel index CH[9:0], the RF channel can be set to any frequency between 60 MHz ~ 108 MHz in

50 kHz steps. The channel index and RF frequency have the following relationship:

F_{RF} = (60 + 0.05 x *Channel Index), where F_{RF}* is *the RF frequency in MHz.*

For example: To set the receiver to 106.9MHz, the channel index can be calculated with the upper formula as shown in following:

Channel index =(106.9-60)/0.05
=938

This translates into a hex number 0x3AA. So write 0xAA to Reg07h [7:0] and write 0x03 to Reg0Ah[1:0] to tune to the desired channel.

Auto Seek

After setting start frequency, stop frequency, searching step and search threshold, the auto seek function can be enabled by setting CHSC (Reg00h [1]) to one. (Refer to section 5.13-3 for programming guide).

Also, auto-seek supports a hardware interrupt function. Refer to section 5.11 for more descriptions.

5.11 Hardware Interrupt

The QN8035 supports a hardware interrupt function. It can generate an interrupt signal to a MCU during auto seek or RDS reception, in order to relieve the MCU from continuous polling on the QN8035's registers.

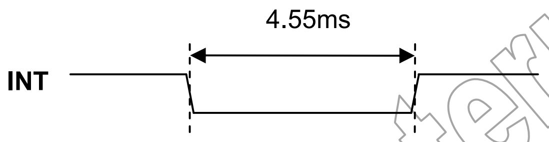


Figure 12 Interrupt Output

If RDS_INT_EN (Reg17h[7])) is set to high, a low pulse of roughly 4.55ms will be produced on the INT pin when a new group of data is received and stored into RDS registers in RDS mode.

Similarly, in CCA mode, after CCA_INT_EN (Reg17h[6]) is set to high, the same low pulse will be generated on the INT pin when a good quality channel is found in the CCA mode.

5.12 RDS/RBDS

In receive mode, setting RDSEN (Reg00h[3]) bit high will enable the RDS function. Once the device receives an RDS signal, the RDSSYNC (Reg13h[4]) will be high. On reception of a RDS signal, if RDS_RXTXTUPD (Reg13h[7]) bit is toggled, or the INT pin will output a 4.55ms low pulse when hardware interrupt function is enabled by RDS_INT_EN, RDS data buffer (Reg0Bh to Reg12h) will be filled.

The results of error check-sum on four RDS blocks are then available in STATUS2[3:0] (Reg13h[3:0]). If any check-sum bit is non-zero, the corresponding RDS block is not valid. Check the register map for detailed definition of STATUS2[3:0].

E_DET bit (Reg13h[6]) is used for distinguishing whether the received RDS group contains E (MMBS) block, and RDSC0C1 (Reg13h[5]) bit is used for judging whether the received group is A group or B group.

5.13 Programming Guide

1) System Initialization:

To initialize the device, the following steps need to be executed.

a. After powering up, execute software reset to the QN8035.

b. Select injection clock type (sine-wave or digital-wave), and set Reg01h[7].

c. Select clock frequency (32.768 KHz or other frequencies), then set XTAL_DLV[10:0] (Reg15h to Reg16h).

d. Set PLL_DLT[12:0] and write the computed result to Reg16h[7:3] and Reg17h. For detailed configuration, refer to section 5.3.

e. Software initialization. Refer to QN8035 application note.

2) Manual Channel Tuning

a. According to the formula on Section 5.10, derive channel index of the desired channel.

b. Write channel index to Reg07h and Reg0Ah[1:0].

c. Set CHCS (Reg00h[1]) bit low to disable the CCA function and select manual operation.

d. Set the CCA_CH_DIS (Reg00h[0]) bit high to select manual tuning channel.

e. Set RXREQ (Reg00[4]) bit high and STNBY (Reg00h[5] bit low to enter receive mode.

3) Auto Seek (CCA)

a. Set start frequency of CCA. Using the formula on Section 5.10, calculate channel index of start frequency, then write its hex value to Reg08h and Reg0Ah[3:2].

b. In the same way calculate channel index of stop frequency, then write its hex value to Reg09h and Reg0Ah[5:4].

c. Select step of CCA, 50KHz, 100KHz or 200KHz, write corresponding value to Reg0Ah[7:6] bits.

d. Write suitable value to RXCCAD [5:0] to set CCA searching threshold in Reg01h.

e. Set CCA_INT_EN (Reg17h [6]) bit high to enable interrupt for CCA. (optional)

f. Set the CCA_CH_DIS (Reg00h [0]) bit low to select CCA result as tuning channel.

g. Set CHSC (Reg00h [1]) bit high to enable CCA.

h. Set RXREQ (Reg00h [4]) bit high STNBY (Reg00h[5] bit low to enter receive mode.

i. Read the CH (Reg07h) and CH_STEP (Reg0Ah[1:0]) after the CHSC (Reg00h[1]) bit is low, or when interrupt function is enabled and the INT pin outputs a low pulse.

j. Read the STATUS1 (Reg04h [3]) bit. If it is low, the CCA result is valid, otherwise, discard the result. **Note**: If interrupt function is used, it is not necessary to check STATUS1 bit.

k. According to the values of CH (Reg07h) and CH_STEP (Reg0Ah [1:0]), calculate channel result of CCA.

l. Repeat step **g** to **k** for scanning all good channels in a frequency band.

Note: When the start frequency is greater than the stop frequency, the device will search down, and when the start frequency is less than the stop frequency, the device will search up.

4) RDS

a. Configure QN8035 channel as described in "Manual Channel Tuning".

b. Set the RDS_INT_EN (Reg17h [7]) bit high to enable the RDS interrupt function. (optional)

c. Set the RDS_ONLY (Reg17h [5]) bit high or low (default is low) to select the RDS working mode. (optional)

d. Set the RDSEN (Reg00h [3]) bit high to enable the RDS function.

e. Check the RDSSYNC (Reg13h [4]) bit. If it is high, the device has received RDS signal, otherwise keep waiting or exit the RDS mode.

f. Look for the RDS reception indicators. Check the RDS_RXTXUPD (Reg13h [7]) bit to monitor whether it is toggled in Reg13h. If the RDS interrupt function is enabled, low pulse on the INT pin is another indicator of the RDS reception. If no RDS reception, keep waiting.

g. After RDS indicators in step **f** are triggered, read out Reg13h [3:0] four bits values to judge whether they are all zeros. If so, RDS data in registers Reg0Bh to Reg12h (RDSD0 ~ RDSD7) are valid.

h. Read out RDS data from registers Reg0Bh to Reg12h (RDSD0 ~ RDSD7) for further decoding.

i. Repeat steps **e** to **h** for continuous reception of RDS data.

6 USER CONTROL REGISTERS

-------- THIS IS A PREVIEW LIST. Number and content of registers subject to change without notice --------

There are 25 user accessible control registers. All registers not listed below are for manufacturing use only.

Table 10: Summary of User Control Registers

REGISTER	NAME	USER CONTROL FUNCTIONS
00h	SYSTEM1	Sets device modes.
01h	CCA	Sets CCA parameters.
02h	SNR	Estimate RF input CNR value
03h	RSSISIG	In-band signal RSSI dBμV value.
04h	STATUS1	System status.
05h	CID1	Device ID numbers.
06h	CID2	Device ID numbers.
07h	CH	Lower 8 bits of 10-bit channel index.
08h	CH_START	Lower 8 bits of 10-bit channel scan start channel index.
09h	CH_STOP	Lower 8 bits of 10-bit channel scan stop channel index.
0Ah	CH_STEP	Channel scan frequency step. Highest 2 bits of channel indexes.
0Bh	RDSD0	RDS data byte 0.
0Ch	RDSD1	RDS data byte 1.
0Dh	RDSD2	RDS data byte 2.
0Eh	RDSD3	RDS data byte 3.
0Fh	RDSD4	RDS data byte 4.
10h	RDSD5	RDS data byte 5.
11h	RDSD6	RDS data byte 6.
12h	RDSD7	RDS data byte 7.
13h	STATUS2	RDS status indicators.
14h	VOL_CTL	Audio controls.
15h	XTAL_DIV0	Frequency select of reference clock source
16h	XTAL_DIV1	Frequency select of reference clock source
17h	XTAL_DIV2	Frequency select of reference clock source
18h	INT_CTRL	RDS control

Register Bit R/W Status:

RO - *R*ead *O*nly: You can not program these bits.
WO - *W*rite *O*nly: You can write and read these bits; the value you read back will be the same as written.
R/W - *R*ead/*W*rite: You can write and read these bits; the value you read back can be different from the value written. Typically, the value is set by the chip itself. This could be a calibration result, AGC FSM result, etc.

Word: SYSTEM1 Address: 00h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
swrst	recal	stnby	rxreq	rdsen	force_mo	chsc	cca_ch_dis
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	SWRST	0	Reset all registers to default values:	
			0	Keep the current values.
			1	Reset to the default values.
6	RECAL	0	Reset the state to initial states and recalibrate all blocks:	
			0	No reset. FSM runs normally.
			1	Reset the FSM. After this bit is de-asserted, FSM will go through all the power up and calibration sequence.
5	STNBY	0	Request immediately to enter Standby mode whatever the chip is in any states. *Note: "stnby" has the highest priority.*	
			0	Non standby mode.
			1	Enter standby mode.
4	RXREQ	0	Receiving request (overwrites STNBY):	
			0	Non RX mode. Either idle mode.
			1	Enter receive mode. *Note: "stnby" must be set to "0" when entering RX mode.*
3	RDSEN	0	RDS enable:	
			0	No RDS.
			1	RDS enable.
2	FORCE_MO	0	Force receiver in MONO mode:	
			0	Not forced. ST/MONO auto selected
			1	Forced in MONO mode
1	CHSC	0	Channel Scan mode enable: Combined with RXREQ, chip scans for occupied channel for receiving. After completing channel scanning, this bit will be cleared automatically. For RX Scan, the FIRST valid channel will be selected. To start CCA, set	

			CHSC (REG0 [1]) =1. CHSC will be reset automatically when CCA is complete. To use the scanned channel, set CCA_CH_DIS=0. (CCA_CH_DIS can be set to 0 at the same time CHSC=1).	
			0	Normal operation
			1	Channel Scan mode operation.
0	CCA_CH_DIS	1	CH (channel index) selection method: See description for CH register at 07h and 0Ah for more information.	
			0	CH is determined by internal CCA (channel scan).
			1	CH is determined by the content in CH [9:0].

Word: CCA **Address: 01h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
XTAL_INJ	imr	rxccad[5]	rxccad[4]	rxccad[3]	rxccad[2]	rxccad[1]	rxccad[0]
wo	rw	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	XTAL_INJ	01	Select the reference clock source	
			0	Inject sine-wave clock
			1	Inject digital clock
6	imr	0	Image Rejection. In CCA disabled mode (CCA_DIS=1), this is user set value. In CCA mode, this is CCA selection read out	
			0	LO<RF, image is in lower side
			1	LO>RF, image is in upper side
5:0	RXCCAD[5:0]	000000	RXCCAD [5:0] is used to set the threshold for RX CCA. Channel with RSSI (dBuV) > (RXCCAD-10) dBuv is selected as valid channel.	

Word: SNR **Address: 02h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
snrdb[7]	snrdb[6]	snrdb[5]	snrdb[4]	snrdb[3]	snrdb[2]	snrdb[1]	snrdb[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	SNRDB	rrrrrrrr	In band signal to noise ratio.

Word: RSSISIG   Address: 03h (RO)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rssidb[7]	rssidb[6]	rssidb[5]	rssidb[4]	rssidb[3]	rssidb[2]	rssidb[1]	rssidb[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RSSIDB[7:0]	rrrr rrrr	In-band signal RSSI (Received Signal Strength Indicator) dBμV value: dBμV = RSSI (with AGC correction) - 43

Word: STATUS1 **Address**: 04h (RO)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
cap_sh	fsm[2]	fsm[1]	fsm[0]	rxcca_fail	rxagcset	rxagcerr	st_mo_rx
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description	
7	CAP_SH	r	Reserved	
6:4	FSM[2:0]	rrr	Top FSM state indicator:	
			FSM[3:0]	FSM status
			000	STBY
			001	RESET
			010	CALI
			011	IDLE
			100	CALIPLL
			101	RECEIVEING
			110	Reserved
			111	RXCCA
3	RXCCA_FAIL	r	RXCCA Status Flag: Indicates whether a valid channel is found during RX CCA. If a valid channel is found, channel index will stay there, and RXCCA_FAIL=0; otherwise, it will stay at the end of scan range and RXCCA_FAIL=1.	
			0	RX CCA successful finds a valid channel.
			1	RX CCA fails to find a valid channel.
2	RXAGCSET	r	RX AGC settling status:	
			0	Not Settled
			1	Settled
1	RXAGCERR	r	RXAGC status:	
			0	No Error
			1	AGC Error
0	ST_MO_RX	r	Stereo receiving status:	
			1	Mono
			0	Stereo

Word: CID1 **Address: 05h (RO)**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
cid0[2]	cid0[1]	cid0[0]	cid1[2]	cid1[1]	cid1[0]	cid2[1]	cid2[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	value	Description	
7:5	CID0[2:0]	rrr	reserved	
4:2	CID1[2:0]	rrr 000	Chip ID for product family:	
			000	FM
			001~111	Reserved
1:0	CID2[1:0]	rr 01	Chip ID for minor revision:	
			00	1
			01	2
			10	3
			11	4

Word: CID2 **Address**: 06h (RO)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
cid3[5]	cid3[4]	cid3[3]	cid3[2]	cid3[1]	cid3[0]	cid4[1]	cid4[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Devault	Description	
7:2	CID3[5:0]	rrrrrr 100001	Chip ID for product ID:	
			0000-0111	Reserved
			100001	QN8035
			100001-111111	Reserved
1:0	CID4[3:0]	rrrr 00	Chip ID for major revision is 1+CID4	
			00	1
			01	2
			10	3
			11	4

Word: CH **Address**: 07h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ch[7]	ch[6]	ch[5]	ch[4]	ch[3]	ch[2]	ch[1]	ch[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	CH[7:0]	00110000	Lower 8 bits of 10-bit Channel index. Channel used for RX has two origins, one is from CH register (REG 07h+REG 0Ah [1:0]), which can be written by the user, another is from CCA/CCS. CCA/CCS selected channel is stored in an internal register, which is physically a different register with CH register, but it can be read out through register CH and be used for RX when CCA_CH_DIS(REG0[0])=0. FM channel: (60+CH*0.05)MHz

Word: **CH_START** **Address**: **08h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ch_sta[7]	ch_sta[6]	ch_sta[5]	ch_sta[4]	ch_sta[3]	ch_sta[2]	ch_sta[1]	ch_sta[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	CH_STA[7:0]	00011100	Lower 8 bits of 10-bit CCA (channel scan) start channel index.

Word: **CH_STOP** **Address**: **09h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ch_stp[7]	ch_stp[6]	ch_stp[5]	ch_stp[4]	ch_stp[3]	ch_stp[2]	ch_stp[1]	ch_stp[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	CH_STP[7:0]	11000000	Lower 8 bits of 10-bit CCA (channel scan) stop channel index.

Word: **CH_STEP** **Address**: **0Ah**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
fstep[1]	fstep[0]	ch_stp[9]	ch_stp[8]	ch_sta[9]	ch_sta[8]	ch[9]	ch[8]
wo	wo	wo	wo	wo	wo	rw	rw

Bit	Symbol	Default	Description	
7:6	FSTEP[1:0]	01	CCA (channel scan) frequency step:	
			00	50 kHz
			01	100 kHz
			10	200 kHz
			11	Reserved
5:4	CH_STP[9:8]	11	Highest 2 bits of 10-bit CCA (channel scan) stop channel index: Stop freq is (60+CH_STP*0.05) MHz.	
3:2	CH_STA[9:8]	10	Highest 2 bits of 10-bit CCA (channel scan) start channel index: Start freq is (60+CH_STA*0.05) MHz.	

1:0	CH[9:8]	10	Highest 2 bits of 10-bit channel index: Channel freq is (60+CH*0.05) MHz.

Word: RDSD0 Address: 0Bh (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd0[7]	rdsd0[6]	rdsd0[5]	rdsd0[4]	rdsd0[3]	rdsd0[2]	rdsd0[1]	rdsd0[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RDSD0[7:0]	xxxxxxxx	RDS data byte 0.

Word: RDSD1 Address: 0Ch (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd1[7]	rdsd1[6]	rdsd1[5]	rdsd1[4]	rdsd1[3]	rdsd1[2]	rdsd1[1]	rdsd1[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RDSD1[7:0]	xxxxxxxx	RDS data byte 1.

Word: RDSD2 Address: 0Dh (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd2[7]	rdsd2[6]	rdsd2[5]	rdsd2[4]	rdsd2[3]	rdsd2[2]	rdsd2[1]	rdsd2[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RDSD2[7:0]	xxxxxxxx	RDS data byte 2.

Word: RDSD3 **Address**: 0Eh (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd3[7]	rdsd3[6]	rdsd3[5]	rdsd3[4]	rdsd3[3]	rdsd3[2]	rdsd3[1]	rdsd3[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RDSD3[7:0]	xxxxxxxx	RDS data byte 3.

Word: RDSD4 **Address**: 0Fh (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd4[7]	rdsd4[6]	rdsd4[5]	rdsd4[4]	rdsd4[3]	rdsd4[2]	rdsd4[1]	rdsd4[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RDSD4[7:0]	xxxxxxxx	RDS data byte 4.

Word: RDSD5 **Address**: 10h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd5[7]	rdsd5[6]	rdsd5[5]	rdsd5[4]	rdsd5[3]	rdsd5[2]	rdsd5[1]	rdsd5[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RDSD5[7:0]	xxxxxxxx	RDS data byte 5.

Word: RDSD6 **Address**: 11h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd6[7]	rdsd6[6]	rdsd6[5]	rdsd6[4]	rdsd6[3]	rdsd6[2]	rdsd6[1]	rdsd6[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RDSD6[7:0]	xxxxxxxx	RDS data byte 6.

Word: RDSD7 **Address**: 12h (RW)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd7[7]	rdsd7[6]	rdsd7[5]	rdsd7[4]	rdsd7[3]	rdsd7[2]	rdsd7[1]	rdsd7[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RDSD7[7:0]	xxxxxxxx	RDS data byte 7.

Word: STATUS2 Address: 13h (RO)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rds_rxtxupd	e_det	rdsc0c1	rdssync	rdsd0err	rdsd1err	rdsd2err	rdsd3err
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description	
7	RDS_RXTXUPD	r	RDS RX: RDS received group updated. Each time a new group is received, this bit will be toggled. If RDS_INT_EN=1, then at the same time this bit is toggled, the interrupt output pin (INT) will output a 4.5 ms low pulse.	
			0->1 or 1->0	A new set (8 bytes) of data is received.
			0->0 or 1->1	New data is in receiving.
6	E_DET	r	'E' block (MMBS block) detected:	
			0	Not Detected
			1	Detected
5	RDSC0C1	r	Type indicator of the RDS third block in one group:	
			0	C0
			1	C1
4	RDSSYNC	r	RDS block synchronous indicator:	
			0	Non-synchronous
			1	Synchronous
3	RDS0ERR	r	Received RDS block 0 status indicator:	
			0	No Error
			1	Error
2	RDS1ERR	r	Received RDS block 1 status indicator:	
			0	No Error
			1	Error
1	RDS2ERR	r	Received RDS block 2 status indicator:	
			0	No Error
			1	Error
0	RDS3ERR	r	Received RDS block 3 status indicator:	
			0	No Error
			1	Error

Word: VOL_CTL Address: 14h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
mute_en	tc	gain_dig[2]	gain_dig[1]	gain_dig[0]	gain_ana[2]	gain_ana[1]	gain_ana[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	MUTE_EN	0	RX audio Mute enable:	
			0	No mute.
			1	Mute
6	TC	1	Pre-emphasis and de-emphasis time constant	
			0	50 us
			1	75 us
5:3	GAIN_DIG[2:0]	000	GAIN_DIG[2:0] set digital volume gain:	
			101	-5 dB
			100	-4 dB
			011	-3 dB
			010	-2 dB
			001	-1 dB
			000	0 dB
2:0	GAIN_ANA[2:0]	111	Lower bits of GAIN_ANA[2:0]: Sets volume control gain of analog portion.	
			111	0 dB
			110	-6 dB
			101	-12 dB
			100	-18 dB
			011	-24 dB
			010	-30 dB
			001	-36 dB
			000	-42 dB

Word: XTAL_DIV0 **Address**: 15h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
xtal_div[7]	xtal_div[6]	xtal_div[5]	xtal_div[4]	xtal_div[3]	xtal_div[2]	xtal_div[1]	xtal_div[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	XTAL_DIV[7:0]	00000001	Lower 8 bits of xtal_div[10:0]. Xtal_div[10:0] = round(freq of xtal/32.768KHz).

Word: XTAL_DIV1 **Address**: 16h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
pll_dlt[4]	pll_dlt[3]	pll_dlt[2]	pll_dlt[1]	pll_dlt[0]	xtal_div[10]	xtal_div[9]	xtal_div[8]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:3	PLL_DLT[4:0]	00001	Lower 5 bits of pll_dlt[12:0].
2:0	XTAL_DIV[10:8]	000	Higher 3 bits of xtal_div[10:0]. Xtal_div[10:0] = round(freq of xtal/32.768KHz)

Word: XTAL _DIV2 **Address**: 17h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
pll_dlt[12]	pll_dlt[11]	pll_dlt[10]	pll_dlt[9]	pll_dlt[8]	pll_dlt[7]	pll_dlt[6]	pll_dlt[5]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	PLL_DLT[12:5]	01011100	Higher 8 bits of pll_dlt[12:0]. Pll_dlt[12:0] = round (28.5MHz / (Freq$_{xtal}$/xtal_div[10:0]/512)) - 442368 .

Word: INT_CTRL   Address: 18h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rds_int_en	cca_int_en	rds_only	s1k_en	rds_4k_en	RSVD	RSVD	RSVD
wo	wo	wo	wo	wo	wo	wo	wo

<table>
<tr><th>Bit</th><th>Symbol</th><th>Default</th><th colspan="2">Description</th></tr>
<tr><td rowspan="4">7</td><td rowspan="4">RDS_INT_EN</td><td rowspan="4">0</td><td colspan="2">RDS RX interrupt enable. When RDS_INT_EN=1, a 4.5ms low pulse will be output from pad din (RX mode) when a new group data is received and stored into RDS0~RDS7 (RX mode).</td></tr>
<tr><td>Rds_int_en</td><td>Status</td></tr>
<tr><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td rowspan="4">6</td><td rowspan="4">CCA_INT_EN</td><td rowspan="4">0</td><td colspan="2">RX CCA interrupt enable. When CCA_INT_EN=1, a 4.5ms low pulse will be output from pad din (RX mode) when a RXCCA (RX mode) is finished.</td></tr>
<tr><td>Cca_int_en</td><td>Status</td></tr>
<tr><td>0</td><td>Disable</td></tr>
<tr><td>1</td><td>Enable</td></tr>
<tr><td rowspan="4">5</td><td rowspan="4">RDS_ONLY</td><td rowspan="4">1</td><td colspan="2">RDS mode</td></tr>
<tr><td>rds_only</td><td>RDS mode selection</td></tr>
<tr><td>0</td><td>Received bit-stream have both RDS and MMBS blocks (‘E’ block)</td></tr>
<tr><td>1</td><td>Received bit-stream has RDS block only, no MMBS block (‘E’ block)</td></tr>
<tr><td rowspan="3">4</td><td rowspan="3">S1K_EN</td><td rowspan="3">0</td><td colspan="2">Internal 1K tone selection. It will be used as DAC output when RXREQ.</td></tr>
<tr><td>0</td><td>Disable</td></tr>
<tr><td>1</td><td>Enable</td></tr>
<tr><td>3</td><td>RDS_4K_EN</td><td>0</td><td colspan="2">Enable RDS 4k mode.</td></tr>
<tr><td>2:0</td><td>RSVD</td><td>000</td><td colspan="2">Reserved.</td></tr>
</table>

7 ORDERING INFORMATION

Part Number	Description	Package
QN8035-NCNA	The QN8035-NCNA is Single-Chip Low-Power FM receiver.	2.5x2.5 mm Body [QFN16]
QN8035-SANA	The QN8035-SANA pin is compatible with the QN8005/8005B.	3x3 mm Body [MSOP10]

8 PACKAGE DESCRIPTION

16-Lead plastic Quad Flat, No Lead Package (ML) – 2.5x2.5 mm Body [QFN]

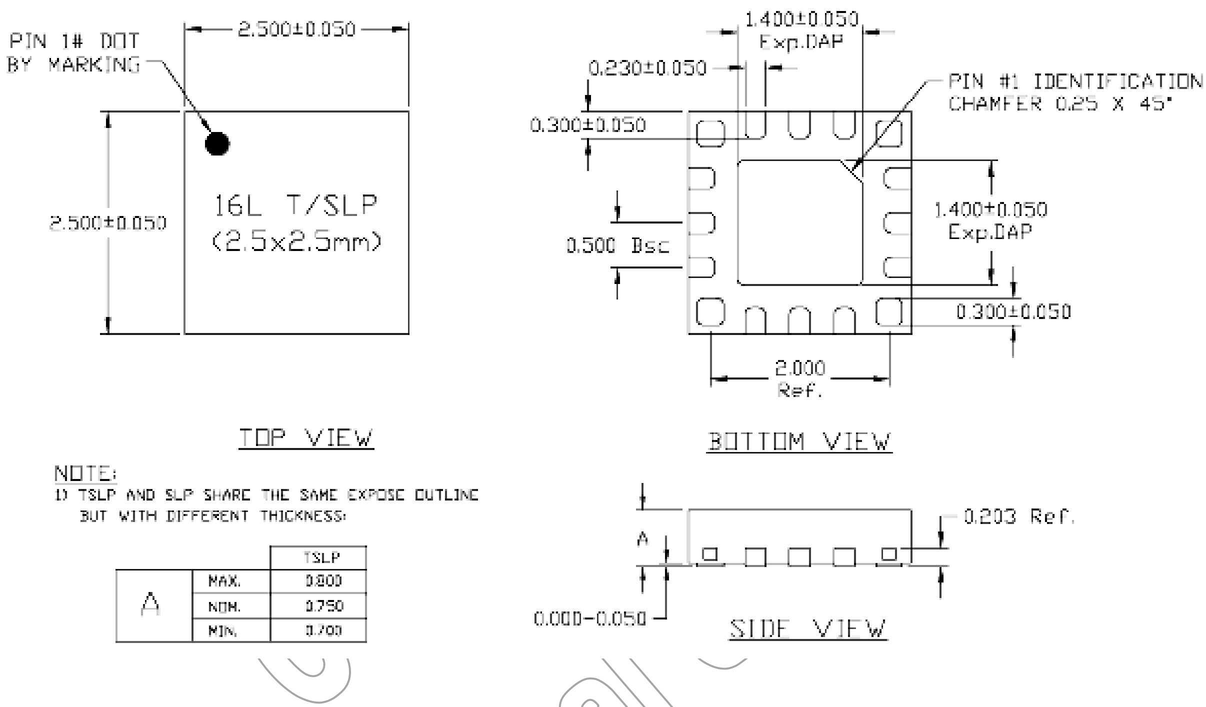


Figure 13 QN8035 Mechanical Drawing

Units	Millimeters		
Dimension Limits	**MIN**	**NOM**	**MAX**
Number of pins		16	
Pitch		0.50 BSC	
Overall Height （SLP）	0.70	0.75	0.80
Standoff	0.00		0.05
Contact Thickness		0.203 REF	
Overall Width		2.50 BSC	
Exposed Pad Width	1.35	1.40	1.45
Overall Length		2.50 BSC	
Exposed Pad Length	1.35	1.40	1.45
Corner Contact Height & Width	0.25	0.30	0.35
Side Contact Width	0.18	0.23	0.28
Side Contact Length	0.25	0.30	0.35
Contact-to-Exposed Pad	-	0.25	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerance per ASME Y 14.5M.
   BSC: Basic Dimension. The theoretically exact value is shown without tolerance.
   REF: Reference Dimension, usually without tolerance, for information purpose only.

10-Lead plastic Quad Flat, No Lead Package (ML) – 3x3 mm Body [QFN]

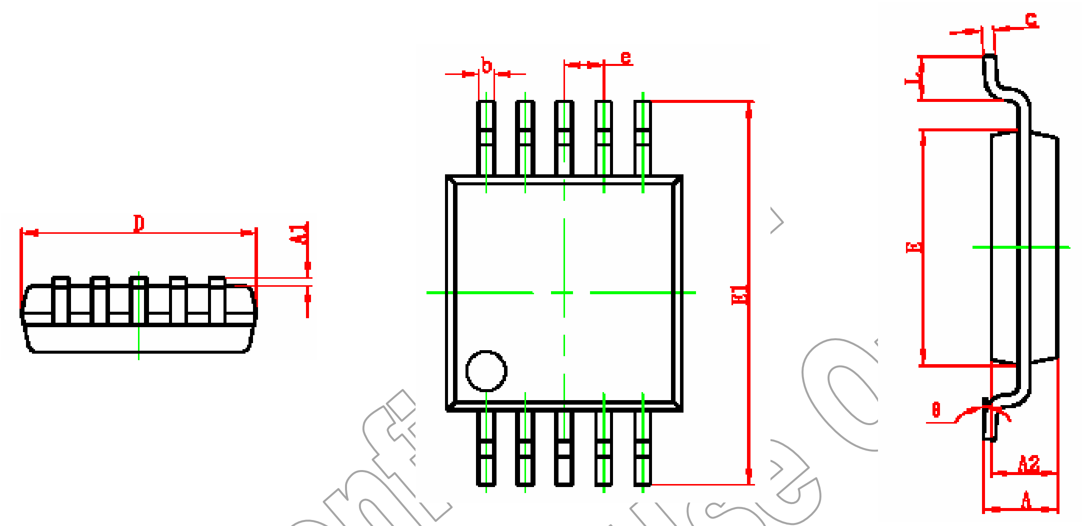


Figure 14 MSOP10 Package Outline Dimensions

Symbol	Description	Millimeters		
		Minimum	Nominal	Maximum
A	Overall package height	0.820	0.95	1.100
A1	Board standoff	0.020	-	0.150
A2	Package thickness	0.750	0.85	0.950
b	Lead width	0.180	0.23	0.280
c	Lead thickness	0.090	-	0.230
D	Package's outside, X-axis	2.900	3.00	3.100
e	Lead pitch	0.50 (BSC)		
E	Package's outside, Y-axis	2.900	3.00	3.100
E1	Lead to lead, Y-axis	4.750	4.90	5.050
L	Foot length	0.400	0.60	0.800
θ	Foot to board angle	0°	-	6°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the area indicated in the drawing.
2. Dimensioning and tolerance per ASME Y 14.5M.
   BSC: Basic Dimension. The theoretically exact value is shown without tolerance.

Carrier Tape Dimensions

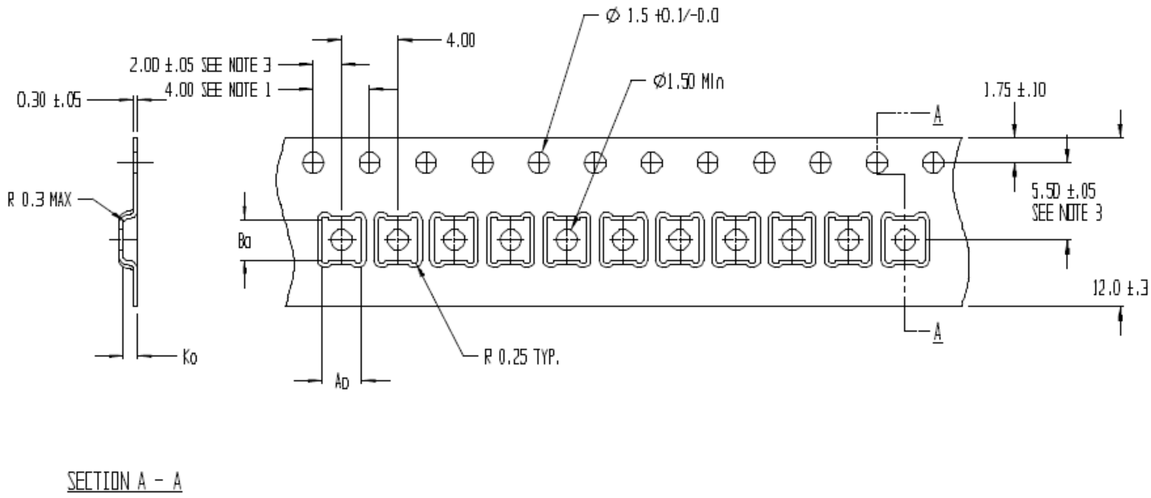


Figure 15 2.5X2.5 QFN16 Carrier Tape

Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
4. A0 = 2.81
   B0 = 2.85
   K0 = 1.00

3X3 MSOP10 Carrier Tape

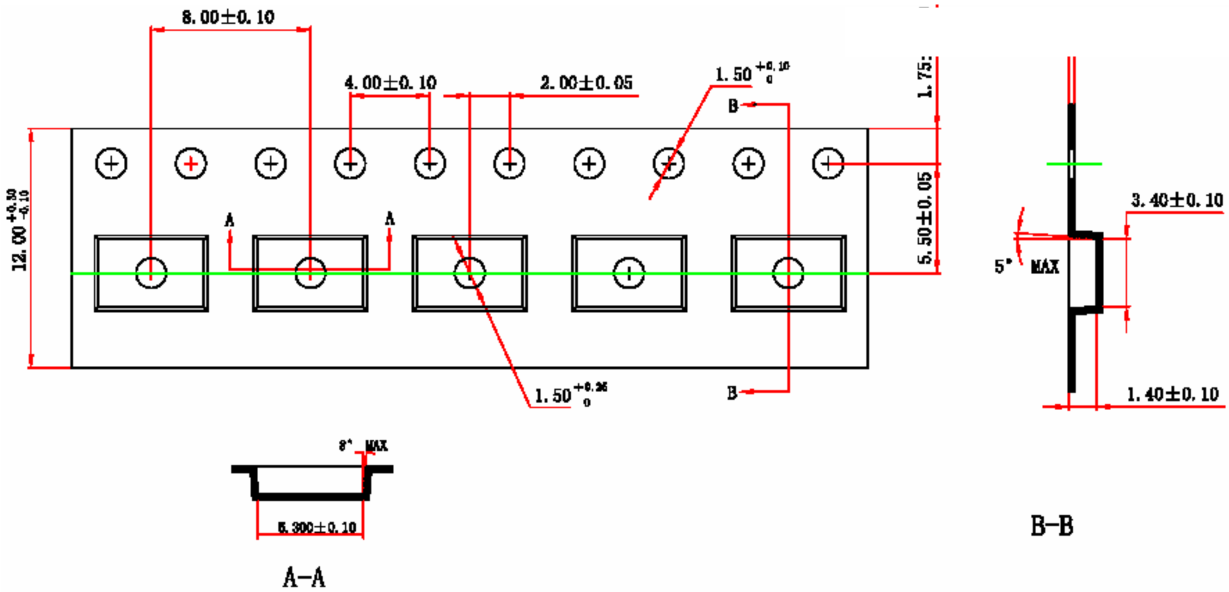


Figure 16 MSOP10 Carrier Tape Drawing

NOTES:

1. 10 sprocket hole pitch cumulative tolerance ±0.2mm maximum.
2. Camber not to exceed 1mm in 100mm: ≤1mm/100mm.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

9 SOLDER REFLOW PROFILE

9.1 Package Peak Reflow Temperature

QN8035 are assembled in a lead-free QFN24 and MSOP10 packages. Since the geometrical size of QN8035 is 4 mm × 4 mm × 0.85 mm, the volume and thickness is in the category of volume<350 mm^3 and thickness<1.6 mm in Table 4-2 of IPC/JEDEC J-STD-020C. The peak reflow temperature is:

$$T_p = 260^{\circ}C$$

The temperature tolerance is +0°C and -5°C. Temperature is measured at the top of the package.

9.2 Classification Reflow Profiles

Profile Feature		Specification*
Average Ramp-Up Rate (tsmax to tP)		3°C/second max.
Pre-heat:	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6°C/second max.
Time 25°C to Peak Temperature		8 minutes max.

*Note: All temperatures are measured at the top of the package.

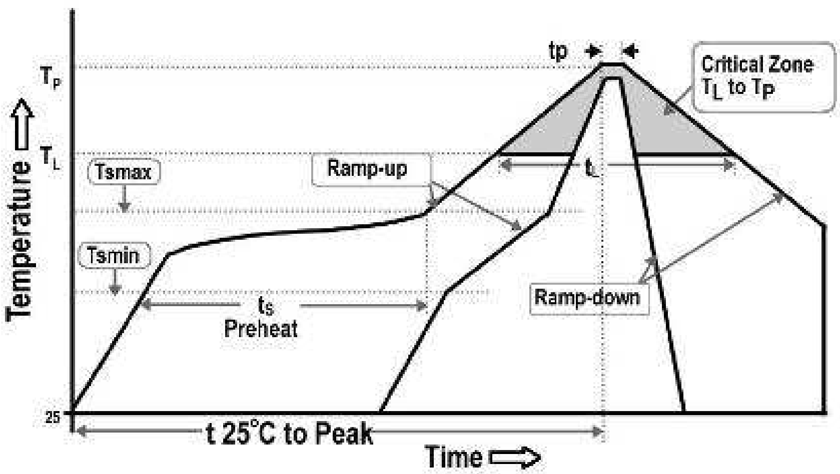


Figure 1: Reflow Temperature Profile

9.3 Maximum Reflow Times

All package reliability tests were performed and passed with a pre-condition procedure that repeat a reflow profile, which conforms to the requirements in Section 9.2, **three (3)** times.

CONTACT INFORMATION

Quintic Corporation (USA)

3211 Scott Blvd., Suite 203
Santa Clara, CA 95054
Tel: +1.408.970.8808
Fax: +1.408.970.8829
Email: support@quinticcorp.com
Web: www.quinticcorp.com

Quintic Microelectronics (China)

Building 8 B-301A Tsinghua Science Park
1st East Zhongguancun Rd, Haidian
Beijing, China 100084
Tel: +86 (10) 8215-1997
Fax: +86 (10) 8215-1570
Web: www.quinticcorp.com