DRAM DIE

4 MEG DRAM

1 MEG x 4, 4 MEG x 1

FEATURES

- Single 5.0V or 3.3V power supply
- Industry-standard timing and functions
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are TTL- and CMOS-compatible
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), HIDDEN
- FAST PAGE MODE access cycle

GENERAL PHYSICAL SPECIFICATIONS

- Wafer thickness = 18.5 mils ±0.5 mils
- Backside wafer surface of polished bare silicon
- Typical metalization thickness 11K angstroms
- Metalization composition: 99.5% Al and 0.5% Cu over titanium
- Typical topside passivation 3K angstroms undoped oxide with 4K angstroms of nitride over oxide
- Typical pad openings: 4.4 x 4.4 mil
  111 x 111 µm

OPTIONS

	ORDER NUMBER	
• Speed probing*	5V	3.3V
No speed probing	None	None
60ns access	-6**	n/a
70ns access	-7**	-7**
80ns access	-8	-8

• Form	
Die	D
Wafer (6" wafer)	W
• Testing levels‡	
Standard probe (0° to 85°C)	C1
Extended Standard probe (0° to 125°C)†	X1
Speed probe (0° to 85°C)	C2

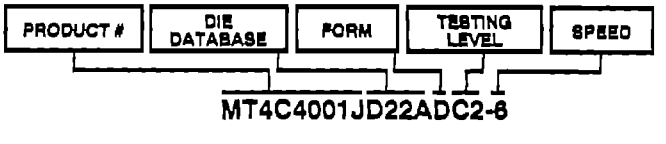
*Refer to "Speed Probing" section of this data sheet. Speed designator should not be included in die part number for C1 level product.
**Available as C2 level product only.
‡Refer to "Die Testing Procedures" section of this data sheet.
†5 volt version only.

ORDER INFORMATION

• 4 Meg x 1 (5V)	MT4C1004JD22A
• 1 Meg x 4 (5V)	MT4C4001JD22A
• 1 Meg x 4 (3.3V)	MT4LC4001JD22A

DIE OUTLINE (Top View)

Die size: 384 x 182 mil
8,992 x 4,623 µm
See Bond Pad Location and Identification Table.



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DIE TESTING PROCEDURES

Micron has established three testing levels for die products. Most Micron products are available with standard probe (C1) level. Selected products are available as speed probe (C2) level. Known-good-die (C3)-level product are available on selected products, as market demand dictates. Level C2 and C3 products generally provide customers with improved assembly yields over level C1.

LEVEL C1

Micron probes wafers at a temperature with limits guardbanded to assure product performance from 0°C to 70°C in Micron's standard package. Since the package environment is not within Micron's control, the user must determine the necessary heat sinking requirements to ensure that the junction die temperature remains within specified limits. A high-voltage functional stress test is performed at probe to assure minimum junction breakdown integrity. V_{BB} (substrate bias voltage) is a forced condition at wafer probe.

Wafer probe consists of various functional and parametric testing of each die. Test patterns, timing, voltage margins, limits and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliabillty, packaged device yield or performance of the product.

LEVEL C2

In addition to the testing performed at C1, Micron also offers C2. Micron's hot chuck speed probe allows Micron to assure the speed performance of die products for the fastest speed grades. Although this additional testing may provide improved assembly yields over a C1 level, the C2-level die has not received burn-in and therefore is also subject to infant mortality failures.

LEVEL C3

In order to provide the customer with fully warranted die product, Micron has developed a known good die process designed to provide customers with die products of equal quality and reliability to packaged product. Micron's KGD™ process allows Micron to fully test and burn-in die product.

FUNCTIONAL SPECIFICATIONS

Please refer to the packaged product data sheets (MT4C1004J, MT4C4001J and MT4LC4001J) found in the applicable Micron data book for functional and parametric specifications. The specifications are provided for reference only on C1- and C2-level die product. On C2-level product ^{t}RAC and ^{t}CAC is guaranteed. C3-level product is warranted to the data sheet.

BONDING INSTRUCTIONS

The D22A DRAM die has 30 bond pads. Refer to the bond pad location and identification table for a complete list of bond pads and coordinates.

The D22A DRAM die has an internal substrate bias generator for normal operation; Bond Pad 24 is used for manufacturing tests only. Normal bonding leaves Bond Pad 24 open (not bonded). Micron requires using a bond wire on each Vcc and Vss bond pad for improved noise immunity. It is important that the back of the die be kept isolated from any other devices sharing a common package or substrate, since the die substrate is internally driven to a negative voltage.

The 4 Meg DRAM device operates from a single +5V (MT4Cxx) or 3.3V (MT4LCxx) power supply and all inputs and outputs are fully TTL- compatible.

PACKAGING

For packaging, Micron utilizes Gel-Pak®. We package all die with the top metallization consistently oriented (refer to Figure 1). External packaging is suitable for electrostatic discharge protection. Each package is individually self-locking or closed with a conductive clip and labeled with the following information:

- Generic device type and data base (Example: 4001JD22A)
- Micron fabrication lot number
- Speed grade of the die (optional)
- Quantity of die in package

STORAGE REQUIREMENTS

Micron die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the Gel-Pak to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

PRODUCT RELIABILITY MONITORS

Reliability of all products is monitored by ongoing QA reliability evaluations. Micron's QA department samples product families on a continuous basis for reliability studies. These studies include high temperature operating life (HTOL) tests for failure in time (FIT) calculations and high temperature steady state (HTSS) tests to monitor electromigration reliability. A summary of these product family evaluations is published on a regular basis.

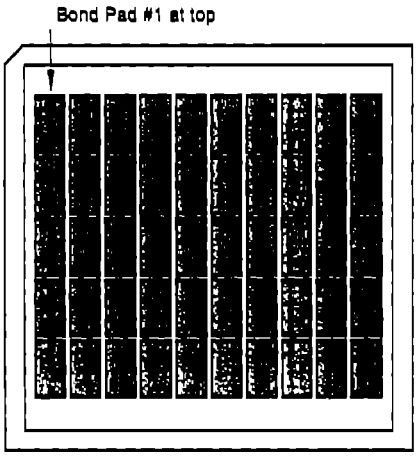
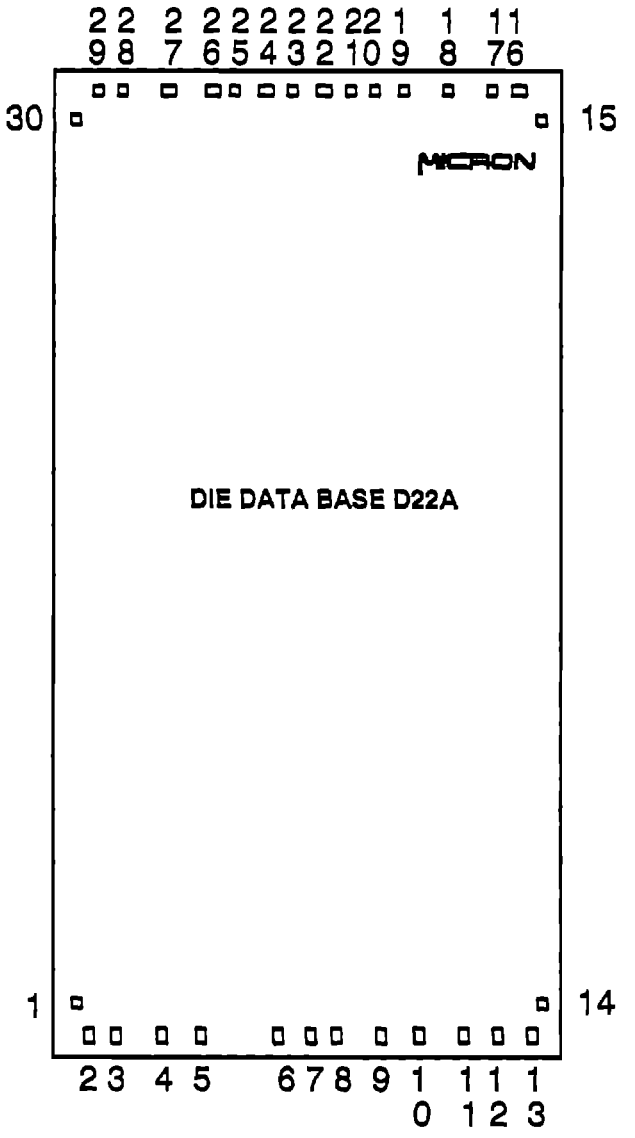


Figure 1
ORIENTATION OF DIE IN GEL-PAK

BOND PAD LOCATION AND IDENTIFICATION TABLE						
			FROM CENTER OF #1			
PAD #	MT4C1004J	MT4C4001J MT4LC4001J	"X" INCHES	"Y" INCHES	"X" MICRONS	"Y" MICRONS
1	A9	OE	0.000	0.000	000	000
2	DNU	DNU	-0.011	-0.004	-279	-102
3	CAS	CAS	-0.011	-0.014	-279	-356
4	DNU	DQ3	-0.011	-0.031	-279	-787
5	DOUT	DQ4	-0.011	-0.044	-279	-1,118
6	Vss	Vss	-0.011	-0.073	-279	-1,854
7	Vss	Vss	-0.011	-0.084	-279	-2,134
8	DIN	DNU	-0.011	-0.094	-279	-2,388
9	DNU	DQ1	-0.011	-0.110	-279	-2,794
10	DNU	DQ2	-0.011	-0.123	-279	-3,124
11	WE	WE	-0.011	-0.139	-279	-3,531
12	RAS	RAS	-0.011	-0.151	-279	-3,835
13	DNU	DNU	-0.011	-0.163	-279	-4,140
14	A10	A9	0.001	-0.167	25	-4,242
15	A0	A0	0.318	-0.167	8,077	-4,242
16	DNU	DNU	0.328	-0.159	8,331	-4,039
17	A1	A1	0.328	-0.150	8,331	-3,810
18	A2	A2	0.328	-0.134	8,331	-3,404
19	A3	A3	0.328	-0.118	8,331	-2,997
20	DNU	Vcc	0.328	-0.108	8,331	-2,743
21	DNU	DNU	0.328	-0.089	8,331	-2,515
22	Vcc	Vcc	0.328	-0.089	8,331	-2,261
23	Vcc	Vcc	0.328	-0.078	8,331	-1,981
24	DNU	DNU	0.328	-0.068	8,331	-1,727
25	A4	A4	0.328	-0.057	8,331	-1,448
26	A5	A5	0.328	-0.049	8,331	-1,245
27	A6	A6	0.328	-0.033	8,331	-838
28	A7	A7	0.328	-0.017	8,331	-432
29	DNU	DNU	0.328	-0.008	8,331	-203
30	A8	A8	0.318	0.000	8,077	000

NOTE: DNU stands for "do not use."

DIE OUTLINE (Top View)



Wafer diameter: 150mm
Wafer thickness: 18.5 mil ±0.5 mil
Die size: 354 x 182 mil (stepping interval) 8,992 x 4,623 µm
Bond pad size: 5.1 x 5.1 mil 128 x 128 µm
Passivation Openings (typical): 4.4 x 4.4 mil 111 x 111 µm