## REVISION HISTORY

| Revision | Description | Issue Date |
|---|---|---|
| Rev. 1.0 | Initial Issued | 2012/2/22 |
| Rev. 1.1 | "CE# ≧$V_{CC}$ - 0.2V" revised as "CE# ≦0.2" for TEST CONDITION of Average Operating Power supply Current Icc1 on page3<br>2.Revised **ORDERING INFORMATION** Page13 | July.19. 2012 |
| Rev. 1.2 | 1. Revise "TEST CONDITION" for VOH, VOL on page 4<br>$I_{OH}$ = -8mA revised as -4mA<br>$I_{OL}$ =4mA revised as 8mA<br>2. Revise VIH(max) & VIL(min) note on page 4<br>VIH(max) = VCC + 2.0V for pulse width less than 6ns.<br>VIL(min) = VSS - 2.0V for pulse width less than 6ns. | June. 04. 2013 |
| Rev. 1.3 | Revised the address pin sequence of TSOP-II pin configuration on page 2 in order to be compatible with industry convention. (No function specifications and applications have been changed and all the characteristics are kept all the same as Rev 1.2 ) | Oct. 30. 2013 |

Lyontek Inc.

# LY61L51216A

Rev. 1.3

**512K X 16 BIT HIGH SPEED CMOS SRAM**

## FEATURES

- Fast access time : 8/10/12ns
- **low power consumption:**
  Operating current:
  90/80/70mA (TYP. 8/10/12ns)
  Standby current:
  3mA(TYP)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
  UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP-II
  48-ball 6mmx8mm TFBGA

## GENERAL DESCRIPTION

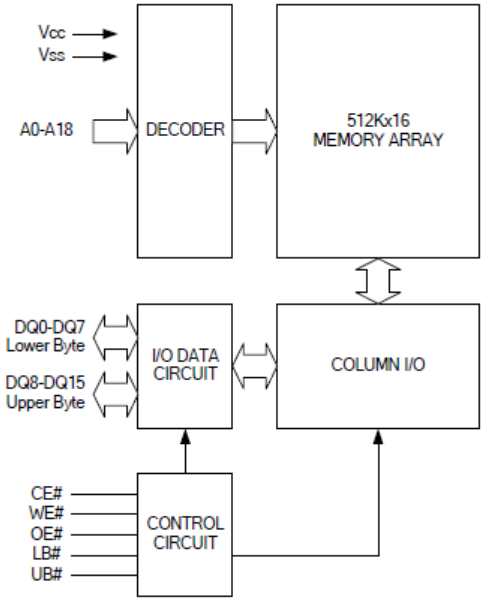
The LY61L51216A is a 8M-bit high speed CMOS static random access memory organized as 512K words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY61L51216A operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

## PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed | Power Dissipation | |
|---|---|---|---|---|---|
| | | | | Standby($I_{SB1}$,TYP.) | Operating($I_{CC1}$,TYP.) |
| LY61L51216A | 0 ~ 70℃ | 3.0 ~ 3.6V | 8/10/12ns | 3mA | 90/80/70mA |
| LY61L51216A(I) | -40 ~ 85℃ | 3.0 ~ 3.6V | 8/10/12ns | 3mA | 90/80/70mA |
| LY61L51216A | 0 ~ 70℃ | 2.7 ~ 3.6V | 10/12ns | 3mA | 80/70mA |
| LY61L51216A(I) | -40 ~ 85℃ | 2.7 ~ 3.6V | 10/12ns | 3mA | 80/70mA |

## FUNCTIONAL BLOCK DIAGRAM




## PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| A0 - A18 | Address Inputs |
| DQ0 – DQ15 | Data Inputs/Outputs |
| CE# | Chip Enable Input |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| LB# | Lower Byte Control |
| UB# | Upper Byte Control |
| $V_{CC}$ | Power Supply |
| $V_{SS}$ | Ground |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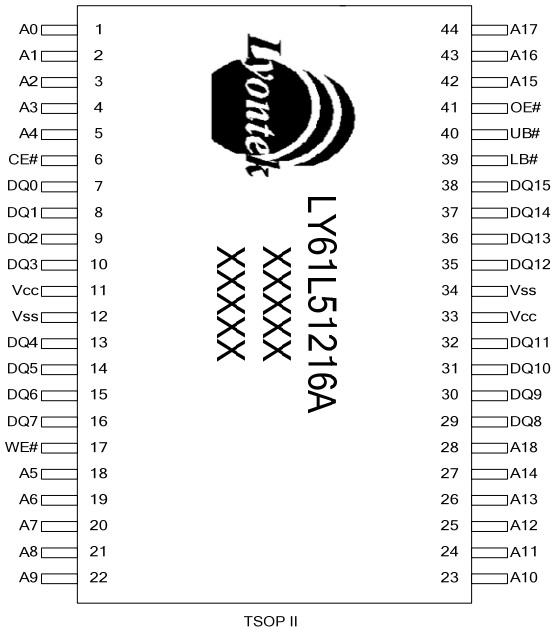
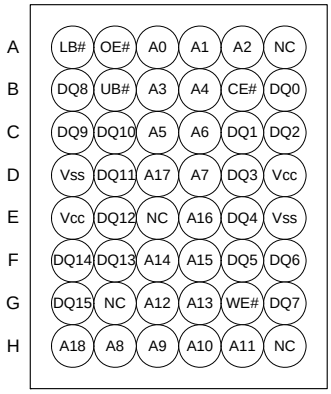
## PIN CONFIGURATION




TSOP II


TFBGA




TFBGA

## ABSOLUTE MAXIMUN RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Terminal Voltage with Respect to $V_{SS}$ | $V_{TERM}$ | -0.5 to 4.6 | V |
| Operating Temperature | $T_A$ | 0 to 70(C grade)<br>-40 to 85(I grade) | ℃ |
| Storage Temperature | $T_{STG}$ | -65 to 150 | ℃ |
| Power Dissipation | $P_D$ | 1 | W |
| DC Output Current | $I_{OUT}$ | 50 | mA |
| Soldering Temperature (under 10 sec) | $T_{SOLDER}$ | 260 | ℃ |

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

## TRUTH TABLE

| MODE | CE# | OE# | WE# | LB# | UB# | I/O OPERATION | | SUPPLY CURRENT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | DQ0-DQ7 | DQ8-DQ15 | |
| Standby | H | X | X | X | X | High – Z | High – Z | $I_{SB1}$ |
| Output Disable | L<br>L | H<br>X | H<br>X | X<br>H | X<br>H | High – Z<br>High – Z | High – Z<br>High – Z | $I_{CC}$ |
| Read | L<br>L<br>L | L<br>L<br>L | H<br>H<br>H | L<br>H<br>L | H<br>L<br>L | $D_{OUT}$<br>High – Z<br>$D_{OUT}$ | High – Z<br>$D_{OUT}$<br>$D_{OUT}$ | $I_{CC}$ |
| Write | L<br>L<br>L | X<br>X<br>X | L<br>L<br>L | L<br>H<br>L | H<br>L<br>L | $D_{IN}$<br>High – Z<br>$D_{IN}$ | High – Z<br>$D_{IN}$<br>$D_{IN}$ | $I_{CC}$ |

Note: H = $V_{IH}$, L = $V_{IL}$, X = Don't care.

## DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | | MIN. | TYP. *4 | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | -8 | 3.0 | 3.3 | 3.6 | V |
| | | | -10/12 | 2.7 | 3.3 | 3.6 | V |
| Input High Voltage | $V_{IH}$ *1 | | | 2.2 | - | $V_{CC}$+0.3 | V |
| Input Low Voltage | $V_{IL}$ *2 | | | - 0.3 | - | 0.8 | V |
| Input Leakage Current | $I_{LI}$ | $V_{CC} \geqq V_{IN} \geqq V_{SS}$ | | - 1 | - | 1 | µA |
| Output Leakage Current | $I_{LO}$ | $V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled | | - 1 | - | 1 | µA |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4mA | | 2.4 | - | - | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ =8mA | | - | - | 0.4 | V |
| Average Operating Power supply Current | Icc | CE# = $V_{IL}$ , $I_{I/O}$ = 0mA ;f=max | -8 | - | 110 | 140 | mA |
| | | | -10 | - | 100 | 130 | mA |
| | | | -12 | - | 90 | 120 | mA |
| | $Icc_1$ | CE# ≦0.2, Other pin is at 0.2V or Vcc-0.2V $I_{I/O}$ = 0mA;f=max | -8 | - | 90 | 120 | mA |
| | | | -10 | - | 80 | 110 | mA |
| | | | -12 | - | 70 | 100 | mA |
| Standby Power Supply Current | Isb | CE# ≧Vih ,Other pin is at Vil or Vih | | - | - | 40 | mA |
| Standby Power Supply Current | $I_{SB1}$ | CE# ≧$V_{CC}$ - 0.2V; Other pin is at 0.2V or Vcc-0.2V | | - | 3 | 25 | mA |

Notes:
1. $V_{IH}$(max) = $V_{CC}$ + 2.0V for pulse width less than 6ns.
2. $V_{IL}$(min) = $V_{SS}$ - 2.0V for pulse width less than 6ns.
3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at $V_{CC}$ = $V_{CC}$(TYP.) and $T_A$ = 25℃

## CAPACITANCE ($T_A$ = 25℃, f = 1.0MHz)

| PARAMETER | SYMBOL | MIN. | MAX | UNIT |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | - | 8 | pF |
| Input/Output Capacitance | $C_{I/O}$ | - | 10 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

## AC TEST CONDITIONS

| | |
|---|---|
| speed | 8ns/10/12ns |
| Input Pulse Levels | 0.2V to Vcc-0.2V |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | $C_L$ = 30pF + 1TTL,<br>$I_{OH}/I_{OL}$ = -4mA/8mA |

## AC ELECTRICAL CHARACTERISTICS

### (1) READ CYCLE

| PARAMETER | SYM. | LY61L51216A-8 | | LY61L51216A-10 | | LY61L51216A-12 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | $t_{RC}$ | 8 | - | 10 | - | 12 | - | ns |
| Address Access Time | $t_{AA}$ | - | 8 | - | 10 | - | 12 | ns |
| Chip Enable Access Time | $t_{ACE}$ | - | 8 | - | 10 | - | 12 | ns |
| Output Enable Access Time | $t_{OE}$ | - | 4.5 | - | 4.5 | - | 5 | ns |
| Chip Enable to Output in Low-Z | $t_{CLZ}$* | 2 | - | 2 | - | 3 | - | ns |
| Output Enable to Output in Low-Z | $t_{OLZ}$* | 0 | - | 0 | - | 0 | - | ns |
| Chip Disable to Output in High-Z | $t_{CHZ}$* | - | 3 | - | 4 | - | 5 | ns |
| Output Disable to Output in High-Z | $t_{OHZ}$* | - | 3 | - | 4 | - | 5 | ns |
| Output Hold from Address Change | $t_{OH}$ | 2 | - | 2 | - | 2 | - | ns |
| LB#, UB# Access Time | $t_{BA}$ | - | 4.5 | - | 4.5 | - | 5 | ns |
| LB#, UB# to High-Z Output | $t_{BHZ}$* | - | 3 | - | 4 | - | 5 | ns |
| LB#, UB# to Low-Z Output | $t_{BLZ}$* | 0 | - | 0 | - | 0 | - | ns |

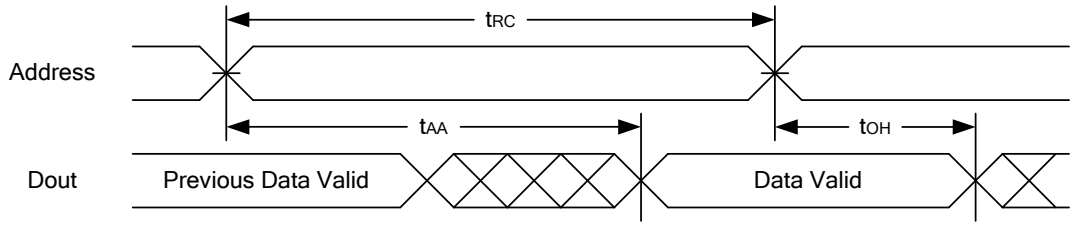
### (2) WRITE CYCLE

| PARAMETER | SYM. | LY61L51216A-8 | | LY61L51216A-10 | | LY61L51216A-12 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | $t_{WC}$ | 8 | - | 10 | - | 12 | - | ns |
| Address Valid to End of Write | $t_{AW}$ | 6.5 | - | 8 | - | 10 | - | ns |
| Chip Enable to End of Write | $t_{CW}$ | 6.5 | - | 8 | - | 10 | - | ns |
| Address Set-up Time | $t_{AS}$ | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | $t_{WP}$ | 6.5 | - | 8 | - | 10 | - | ns |
| Write Recovery Time | $t_{WR}$ | 0 | - | 0 | - | 0 | - | ns |
| Data to Write Time Overlap | $t_{DW}$ | 5 | - | 6 | - | 7 | - | ns |
| Data Hold from End of Write Time | $t_{DH}$ | 0 | - | 0 | - | 0 | - | ns |
| Output Active from End of Write | $t_{OW}$* | 2 | - | 2 | - | 2 | - | ns |
| Write to Output in High-Z | $t_{WHZ}$* | - | 3 | - | 4 | - | 5 | ns |
| LB#, UB# Valid to End of Write | $t_{BW}$ | 6.5 | - | 8 | - | 10 | - | ns |

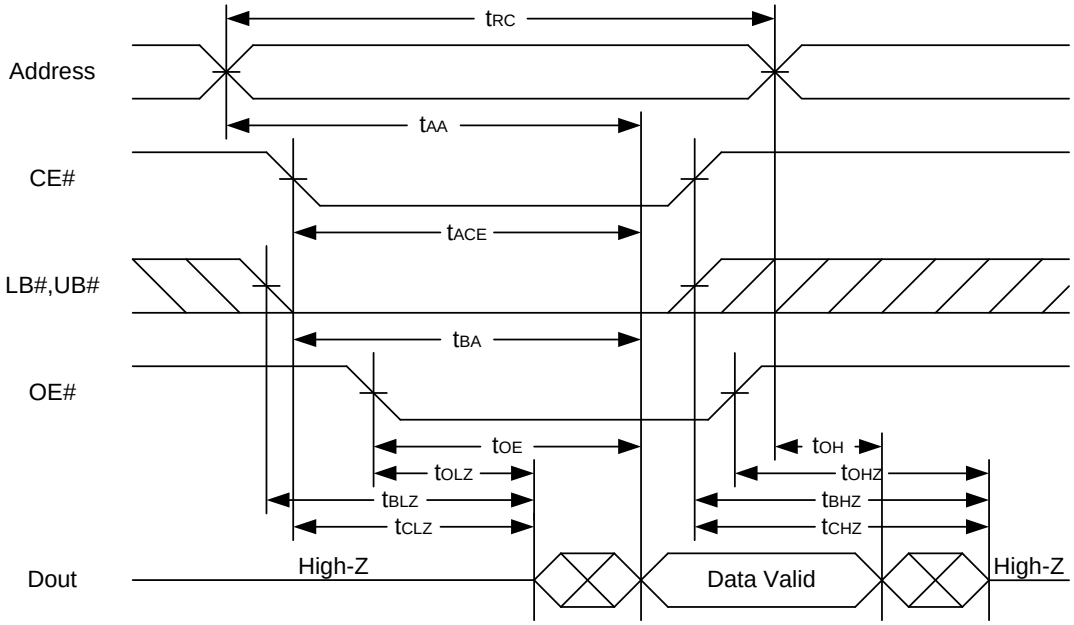
*These parameters are guaranteed by device characterization, but not production tested.

## TIMING WAVEFORMS

**READ CYCLE 1** (Address Controlled) (1,2)

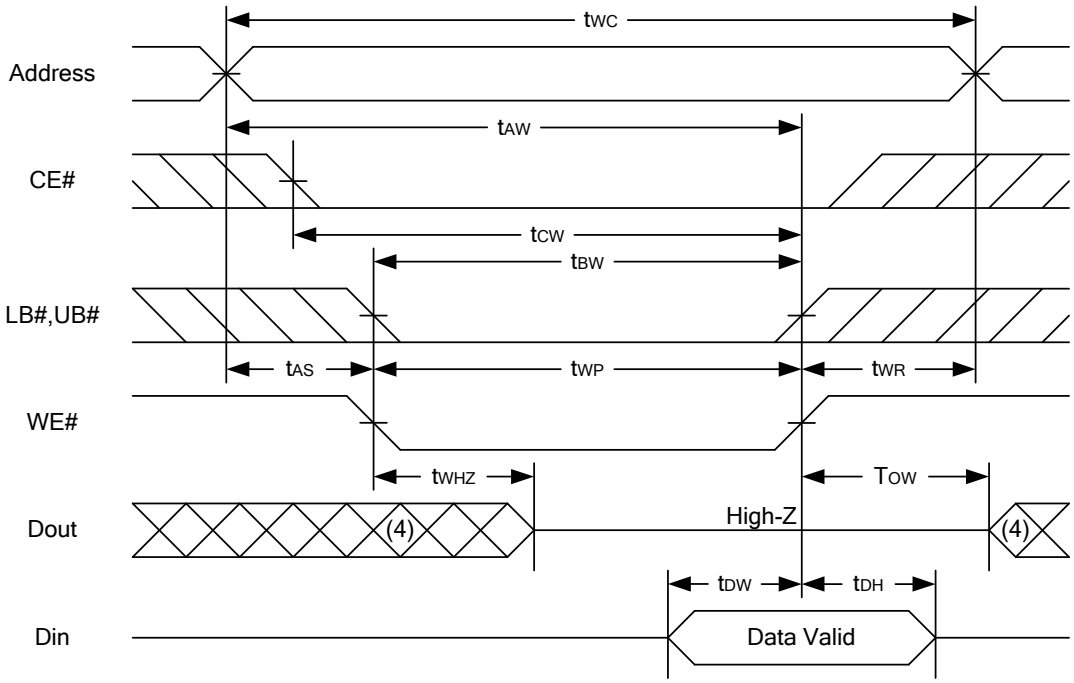



**READ CYCLE 2** (CE# and OE# Controlled) (1,3,4,5)

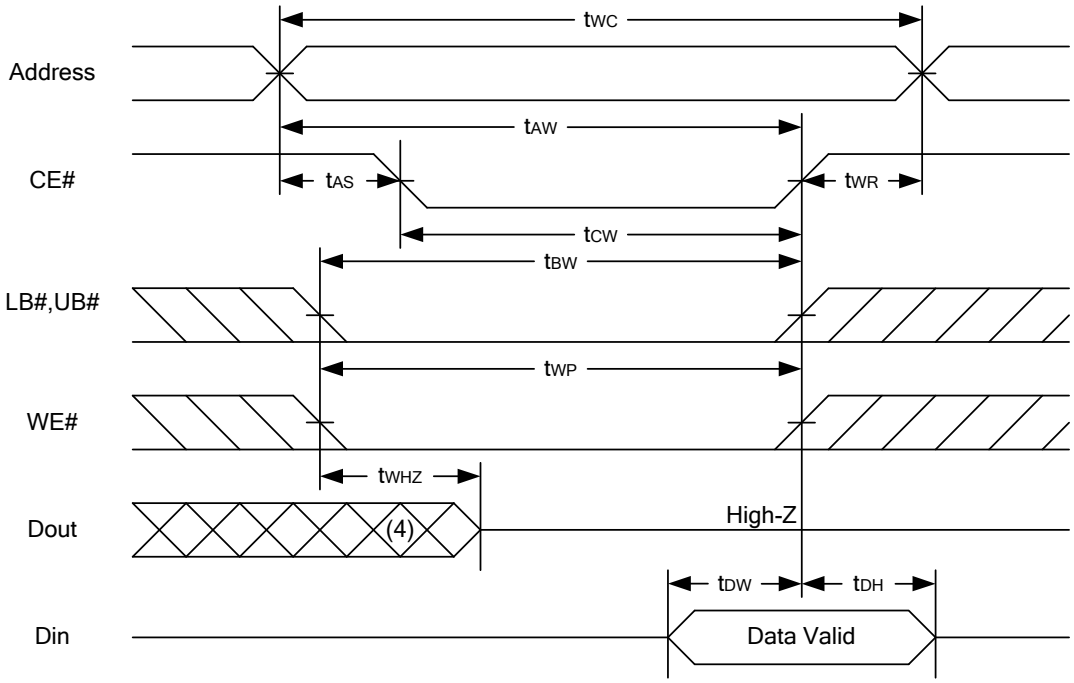



Notes :
1.WE#is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3.Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise $t_{AA}$ is the limiting parameter.
4.$t_{CLZ}$, $t_{BLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{BHZ}$ and $t_{OHZ}$ are specified with $C_L$ = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, $t_{CHZ}$ is less than $t_{CLZ}$ , $t_{BHZ}$ is less than $t_{BLZ}$, $t_{OHZ}$ is less than $t_{OLZ}$.

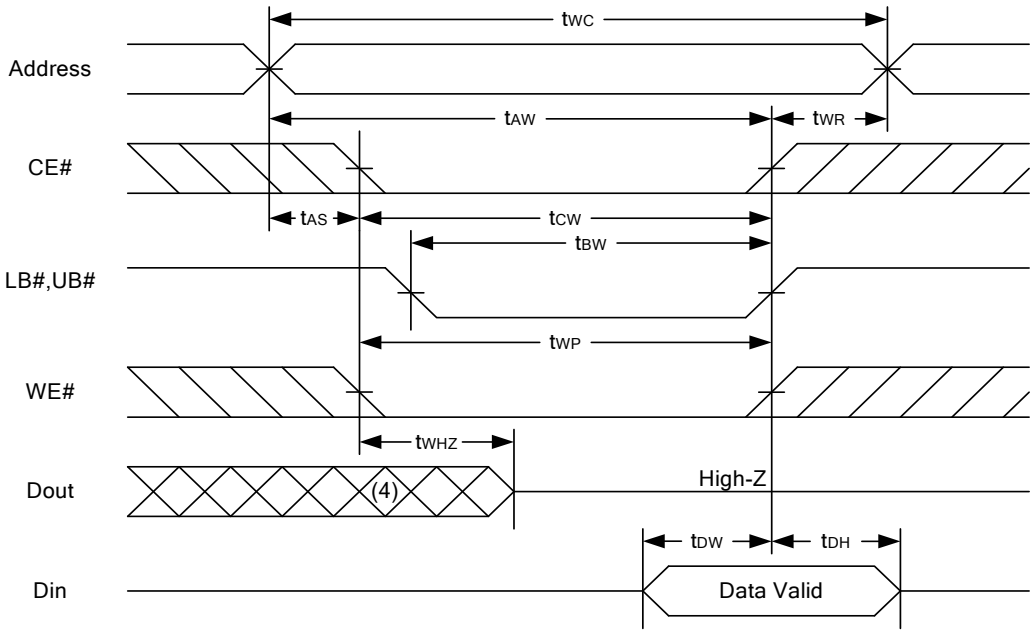
**WRITE CYCLE 1** (WE# Controlled) (1,2,3,5,6)




**WRITE CYCLE 2** (CE# Controlled) (1,2,5,6)



**WRITE CYCLE 3** (LB#,UB# Controlled) (1,2,5,6)



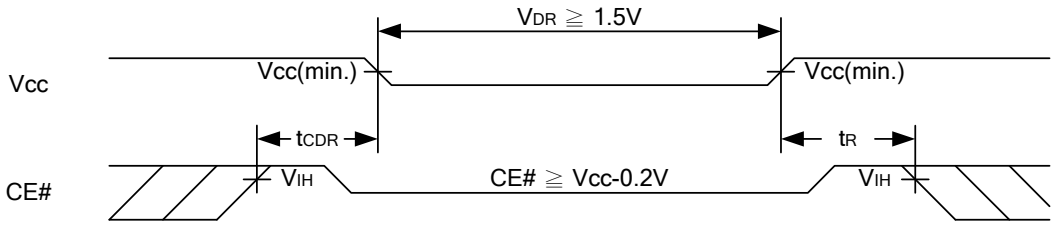

Notes :
1.WE#,CE#, LB#, UB# must be high during all address transitions.
2.A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
3.During a WE# controlled write cycle with OE# low, $t_{WP}$ must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4.During this period, I/O pins are in the output state, and input signals must not be applied.
5.If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.$t_{OW}$ and $t_{WHZ}$ are specified with $C_L$ = 5pF. Transition is measured ±500mV from steady state.

## DATA RETENTION CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ for Data Retention | $V_{DR}$ | CE# ≧ $V_{CC}$ - 0.2V | 1.5 | - | 3.6 | V |
| Data Retention Current | $I_{DR}$ | $V_{CC}$ = 1.5V<br>CE# ≧$V_{CC}$ - 0.2V;<br>Other pin is at 0.2V or Vcc-0.2V | -<br>- | 3 | 25 | mA |
| Chip Disable to Data Retention Time | $t_{CDR}$ | See Data Retention Waveforms (below) | 0 | - | - | ns |
| Recovery Time | $t_R$ | | $t_{RC*}$ | - | - | ns |

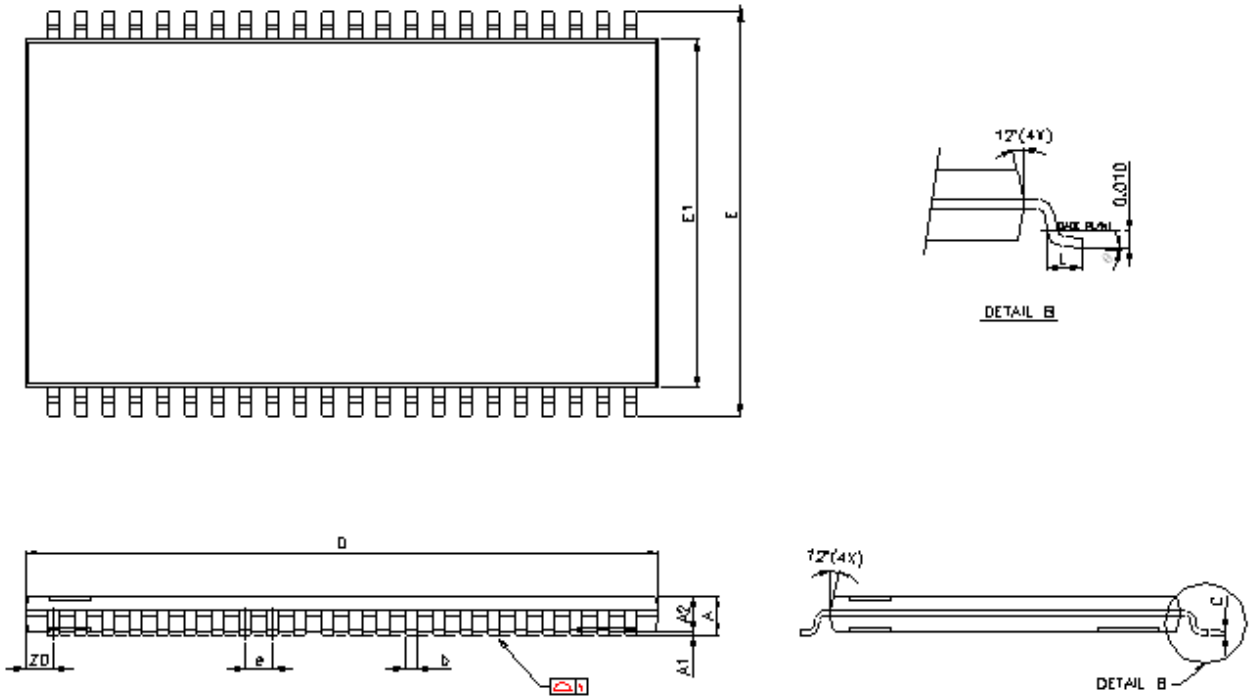
$t_{RC*}$ = Read Cycle Time

## DATA RETENTION WAVEFORM



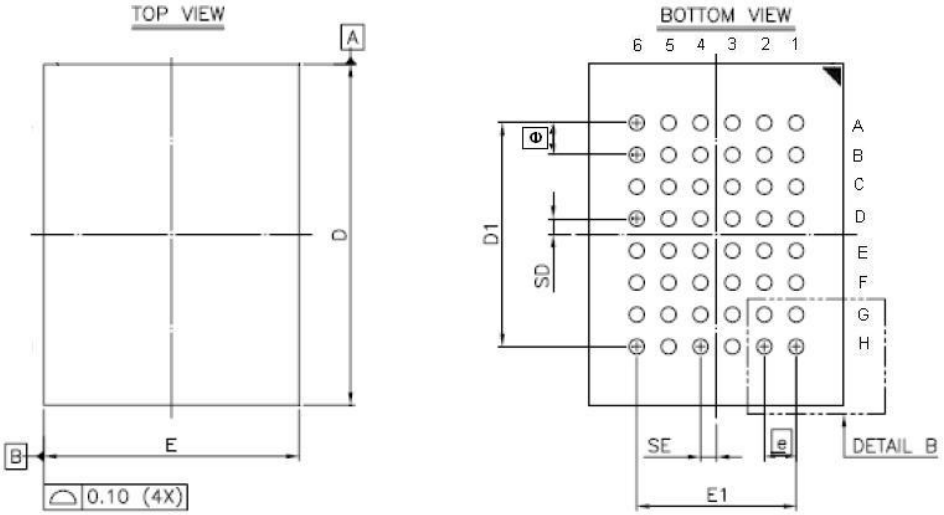
## PACKAGE OUTLINE DIMENSION

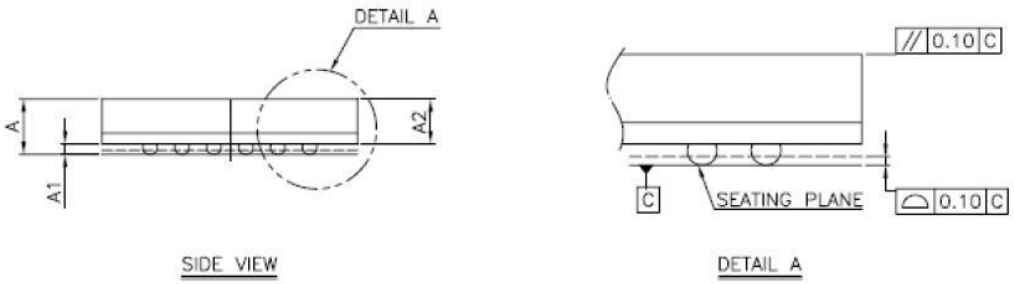
### 44-pin 400mil TSOP-Ⅱ Package Outline Dimension



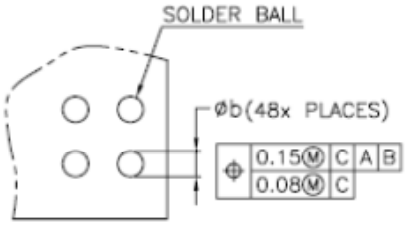

| SYMBOLS | DIMENSIONS IN MILLMETERS | | | DIMENSIONS IN MILS | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | - | - | 1.20 | - | - | 47.2 |
| A1 | 0.05 | 0.10 | 0.15 | 2.0 | 3.9 | 5.9 |
| A2 | 0.95 | 1.00 | 1.05 | 37.4 | 39.4 | 41.3 |
| b | 0.30 | - | 0.45 | 11.8 | - | 17.7 |
| c | 0.12 | - | 0.21 | 4.7 | - | 8.3 |
| D | 18.212 | 18.415 | 18.618 | 717 | 725 | 733 |
| E | 11.506 | 11.760 | 12.014 | 453 | 463 | 473 |
| E1 | 9.957 | 10.160 | 10.363 | 392 | 400 | 408 |
| e | - | 0.800 | - | - | 31.5 | - |
| L | 0.40 | 0.50 | 0.60 | 15.7 | 19.7 | 23.6 |
| ZD | - | 0.805 | - | - | 31.7 | - |
| y | - | - | 0.076 | - | - | 3 |
| Θ | $0^o$ | $3^o$ | $6^o$ | $0^o$ | $3^o$ | $6^o$ |

**48-ball 6mm × 8mm TFBGA Package Outline Dimension**




| SYM. | DIMENSION (mm) | | | DIMENSION (inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.40 | — | — | 0.055 |
| A1 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| A2 | — | — | 1.05 | — | — | 0.041 |
| b | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| D | 7.95 | 8.00 | 8.05 | 0.313 | 0.315 | 0.317 |
| D1 | 5.25 BSC | | | 0.207 BSC | | |
| E | 5.95 | 6.00 | 6.05 | 0.234 | 0.236 | 0.238 |
| E1 | 3.75 BSC | | | 0.148 BSC | | |
| SE | 0.375 TYP | | | 0.015 TYP | | |
| SD | 0.375 TYP | | | 0.015 TYP | | |
| e | 0.75 BSC | | | 0.030 BSC | | |




NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

## ORDERING INFORMATION

| Package Type | Access Time (Speed)(ns) | Temperature Range(℃) | Packing Type | Lyontek Item No. |
|---|---|---|---|---|
| 44Pin(400mil) TSOP-II | 8 | 0℃~70℃ | Tray | LY61L51216AML-8 |
| | | | Tape Reel | LY61L51216AML-8T |
| | | -40℃~85℃ | Tray | LY61L51216AML-8I |
| | | | Tape Reel | LY61L51216AML-8IT |
| | 10 | 0℃~70℃ | Tray | LY61L51216AML-10 |
| | | | Tape Reel | LY61L51216AML-10T |
| | | -40℃~85℃ | Tray | LY61L51216AML-10I |
| | | | Tape Reel | LY61L51216AML-10IT |
| | 12 | 0℃~70℃ | Tray | LY61L51216AML-12 |
| | | | Tape Reel | LY61L51216AML-12T |
| | | -40℃~85℃ | Tray | LY61L51216AML-12I |
| | | | Tape Reel | LY61L51216AML-12IT |
| 48-ball(6mmx8mm) TFBGA | 8 | 0℃~70℃ | Tray | LY61L51216AGL-8 |
| | | | Tape Reel | LY61L51216AGL-8T |
| | | -40℃~85℃ | Tray | LY61L51216AGL-8I |
| | | | Tape Reel | LY61L51216AGL-8IT |
| | 10 | 0℃~70℃ | Tray | LY61L51216AGL-10 |
| | | | Tape Reel | LY61L51216AGL-10T |
| | | -40℃~85℃ | Tray | LY61L51216AGL-10I |
| | | | Tape Reel | LY61L51216AGL-10IT |
| | 12 | 0℃~70℃ | Tray | LY61L51216AGL-12 |
| | | | Tape Reel | LY61L51216AGL-12T |
| | | -40℃~85℃ | Tray | LY61L51216AGL-12I |
| | | | Tape Reel | LY61L51216AGL-12IT |

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