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S1D13717
Mobile Graphics Engine with SD Card Support

Hardware Functional Specification

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1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13717 Mobile Graphics Engine. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

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1.2 General Description

The S1D13717 is an Mobile Graphics Engine solution designed with support for the digital video revolution in mobile products. The S1D13717 contains an integrated camera interface, hardware JPEG encoder/decoder and SD Memory Card interface. Seamlessly connecting to both direct and indirect CPU interfaces, it provides support for up to two LCD panels. The Mobile Graphics Engine supports all standard TFT panel types, eliminating the need for an external timing control IC. The S1D13717, with it's 224K bytes of embedded SRAM and rich feature set, provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring Digital Video, such as Mobile Communications devices and Palm-size PDAs.

Additionally, products requiring a rotated display can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory, transparent to the software application. The S1D13717 also provides support for "Picture-in-Picture Plus" (a variable size window with overlay functions). Higher performance is provided by the Hardware Acceleration Engine which provides 2D BitBLT functions.

The S1D13717 provides impressive support for cellular and other mobile solutions requiring Digital Video support. However, its impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

1.3 Internal Memory

The S1D13717 contains 224K bytes of internal SRAM memory. This internal memory is divided into two physical SRAM banks that contain independent arbitration logic. The boundaries between the memory banks are transparent to the user. Memory Bank1 is 128K bytes and Bank2 is 96K bytes.

The internal memory can be used in 5 distinct ways:

1. **Main Window Display Only**: 224K bytes available. If the JPEG functions and the PIP$^+$ window are not required (therefore disabled), the entire 224K bytes of memory is available for main window image storage. In this case, the image written to the main display window can either come from the Host (RGB data) over the host interface, and/or input by the camera (YUV or RGB data) through the camera interface. The Main Window Display Start Address registers (REG[0212h]-[0214h]) determines where the main window image is stored in memory. Additionally, if the main window image is being updated by a camera, the YUV/RGB Converter Write Start Address registers (REG[0242h]-[0244h]) determines where the camera data is written and typically equals the address of the Main Window Display Start Address.

2. **Main Window and PIP$^+$ Window Display Only**: 224K bytes available. If the JPEG functions are not required (therefore disabled), the entire 224K bytes of memory is available for image storage and must be shared between the Main Window Display Image and the PIP$^+$ Window Display Image. It is recommended that the Main Window and the PIP$^+$ Window be located in different memory banks for improved performance. Since the PIP$^+$ Window is typically smaller than the Main Window, it is recommended that the PIP$^+$ Window Display Image be set to Bank2 using the PIP$^+$ Display Start Address registers (REG[0218h]-[021Ah]), and the Main Window Display Image be set to Bank1 using the Main Window Display Start Address registers (REG[0212h]-[0214h]). As in option 1, the image data for either of these windows can come from the Host or from the camera. Typically, in this setup the camera will input image data to the PIP+ Window and the YUV/RGB Converter Write Start Address registers (REG[0242h]-[0244h]) will equal the PIP$^+$ Display Start Address.

3. **JPEG Functions Enabled**: 192K bytes - JPEG FIFO size available. If either the JPEG Encoder or Decoder is used, segments of Bank1 and Bank2 are automatically reserved for JPEG use only. The JPEG FIFO uses Bank1 and its size is configurable from 4K bytes to 128K bytes using the JPEG FIFO Size bits (REG[09A4h] bits 4-0). The JPEG FIFO starts at address 0 of Bank1 and is accessed using the JPEG FIFO Read/Write register (REG[09A6h]). The JPEG FIFO is used as an interface between the JPEG module and the HOST. When the S1D13717 is encoding a JPEG image, the JPEG FIFO stores JPEG data for the HOST to read. When the S1D13717 is decoding a JPEG file, the JPEG FIFO stores incoming JPEG data from the HOST. The size of the JPEG FIFO should be set to optimize performance based on the HOST operating speed, S1D13717 operating speed, and the size of the JPEG image. The JPEG Line Buffer uses the upper 32K bytes of Bank2, from 2FFFFh - 37FFFh. During an encode operation, the JPEG Line Buffer is used to organize incoming YUV data from the camera and send it to the JPEG Encoder. During a decode operation, the JPEG Line Buffer organizes the YUV data output of the JPEG decoder to be sent to the View Resizer and YUV/RGB Converter for display on the LCD panel.

4. **YUV Data Output**: 192K bytes - JPEG FIFO size available. If YUV data from the camera is directly sent to the HOST, the JPEG Codec is bypassed, however the JPEG FIFO and JPEG Line Buffer are still utilized. The JPEG FIFO and JPEG Line Buffer are used as described for the decode operation in option 3 (JPEG Functions Enabled).

5. **YUV Data Input**: 192K bytes available. If YUV data from the Host is sent directly to the S1D13717, the JPEG Codec and JPEG FIFO are bypassed. YUV data is written directly to the JPEG Line Buffer. In this mode, the JPEG Line Buffer is accessed using the JPEG Line Buffer Write Port register (REG[09E0h]). The JPEG Line Buffer then sends the YUV data to the View Resizer and the YUV/RGB Converter for display on the LCD panel.

All data stored in the internal memory that is intended for display on the LCD panel, must be stored in RGB format. YUV data from the camera interface or from the HOST must be converted to RGB by the YUV/RGB Converter. Color depth data formats of 8/16/32 bit-per-pixel are supported.

1.4 Host CPU Interface

The S1D13717 supports four CPU Host interfaces with 16-bit wide data buses. Each interface can support little or big endian data formats, direct or indirect addressing, and the option to use a wait signal or not. See Section 5.3, “Summary of Configuration Options” on page 42 for a description on how to configure the S1D13717 for these various options. In addition to these four CPU Host interfaces, the S1D13717 also has a serial CPU port which allows the CPU Host to directly control a serial LCD panel connected to the S1D13717.

The Host CPU that is connected to the S1D13717 must meet all specified timing parameters for the Host interface being used, as shown in Section 7.3, “Host Interface Timing” on page 56.

It is recommended that the WAIT# signal be used for all host interfaces as this will ensure that the highest performance is achieved when accessing the S1D13717. When this mode is selected, the WAIT# signal is only asserted when needed (i.e. the S1D13717 cannot accept or present data immediately). If the WAIT# signal is not used, the CPU must guarantee that all cycles meet the maximum cycle length as shown in Table 7-46: “Wait Length,” on page 88.

1.4.1 Direct Addressing Host Interfaces

The direct addressing host interfaces (Direct 80 Type 1, Direct 80 Type 2, Direct 80 Type 3, and Direct 68) are generic asynchronous CPU interfaces that provide addressing along with the data in one transfer. These interfaces only differ in the signals used to interpret the read/write and byte enable command signals. Typically, these interfaces are used to connect to the external memory bus of the host CPU and offer the highest performance when accessing the S1D13717.

The direct addressing host interfaces also have the ability to combine the S1D13717 registers and internal memory into one contiguous memory segment or into separate memory segments. In the contiguous mode (1 CS# mode), only one chip select is used to select the S1D13717 on the host bus. Memory and register accesses are differentiated by the M/R# pin which is typically connected to address pin A19 of the host CPU bus. In the separate memory mode (2 CS# mode), two chip selects select the S1D13717. One chip select is used for memory accesses and the other is used for register accesses. In this mode, the host CPU can be programmed to assign different memory spaces for the memory and registers of the S1D13717.

1.4.2 Indirect Addressing Host Interfaces

The indirect addressing host interfaces (Indirect 80 Type 1, Indirect 80 Type 2, Indirect 80 Type 3, and Indirect 68) are generic asynchronous CPU interfaces that provide addressing and data in two separate transfers. These interfaces only differ in the signals used to interpret the read/write and byte enable command signals. Typically, these interfaces are used when the address and data lines of the host CPU are multiplexed together and two transfers are needed to complete a data transfer.

1.4.3 Serial Port Interface for Serial LCD Control

The S1D13717 also supports a Serial Host Interface that is used to directly control a serial LCD panel connected to the S1D13717. This bypass mode is controlled by the Serial Port Bypass Enable bit (REG[0032h] bit 8). Typically, this interface is used when the S1D13717 is in power save mode and a serial LCD panel is required to show an image such as a status display.

1.5 LCD Controller

The S1D13717 Mobile Graphics Engine contains a versatile LCD controller which supports many LCD panel types and offers a rich feature set. The S1D13717 has four LCD interface modes where either one or two LCD panels (referred to as LCD1 and LCD2) can be connected to the S1D13717. These modes are selected using the Panel Interface bits (REG[0032h] bits 1-0). LCD1 and LCD2 each have their own vertical and horizontal LCD panel size setting and other specific features, in order to easily switch from the LCD1 panel display to the LCD2 panel display or vice versa.

In Mode 1, LCD1 is defined as a TFT RGB type LCD panel. LCD2 is defined as a serial interface type LCD panel with integrated RAM to store the image data.

In Mode 2, LCD1 is defined as a parallel interface LCD panel with integrated RAM to store the image data. LCD2 is defined as a serial interface type LCD panel with integrated RAM to store the image data.

In Mode 3, LCD1 and LCD2 are both defined as parallel interface LCD panels with integrated RAM to store the image data.

In Mode 4, LCD1 is defined as a TFT RGB type LCD panel. LCD2 is defined as a parallel interface LCD panel with integrated RAM to store the image data.

In each mode, only one display at a time (LCD1 or LCD2) can be the active display. A typical application for using two separate LCD panels would be a clamshell type cellular phone where there is a main display and a smaller status display on the outside of the phone. LCD1 would be the main display and LCD2 would be the small status display, typically a serial interface LCD panel. Two images would be stored in the internal memory of the S1D13717 for each LCD display. When each display is selected as active, (LCD1 when the cellular phone is open and LCD2 when the cellular phone is closed) the correct image to be displayed is selected using the Main Window Display Start Address registers (REG[0210h]-[0212h]).

For LCD Interface Pin Mapping refer to Table 5-13: “LCD Interface Pin Mapping,” on page 46.

1.5.1 RGB LCD Interface

The RGB LCD interface supports a wide range of generic TFT panels. TFT panels that can be programmed via various serial type interface are supported and are selected with the LCD1 Serial Data Type bits (REG[0054h] bits 7-5).

The RGB LCD panel data bus width is selectable to support 9/12/16/18-bit panels using the RGB Interface Panel Data Bus Width bits (REG[0032h] bits 6-4). Other configurable options include non-display period times and polarity, width, and position of control signals.

1.5.2 Parallel LCD Interface

The Parallel LCD Interface supports multiple output data formats, providing the flexibility to support various RAM integrated Parallel Interface LCD panels. If a parallel panel is connected to LCD1, the LCD1 Parallel Data Format bits (REG[0056h] bits 2-0) are used to program the output data format, otherwise the LCD2 Parallel Data Format bits (REG[005Eh] bits 2-0) are used.

The LCD panel image can be updated in three different ways. Manual Transfer is accomplished by setting REG[003Ah] bit 1 = 1 which sends one frame of panel data to the Parallel LCD panel. LCD Module VSYNC Manual Transfer mode synchronizes a manual frame transfer to an external VSYNC signal sent by the parallel LCD panel. The VSYNC Input Enable bit for either LCD1 or LCD2 (REG[0056h] bit 7 or REG[005Eh] bit 7) must be set to enable this mode. The last transfer method is Automatic Transfer which sends frames to the LCD panel whenever a camera vertical sync signal is detected. If the VYSNC Input mode is also enabled, an external LCD panel VSYNC must also be detected. Automatic Transfer mode is enabled by setting REG[003Ch] bit 1 = 1. Automatic Transfer mode is intended for displaying a camera image on a serial or parallel interface LCD panel without the need to manually update the panel display.

1.5.3 Serial LCD Interface

The Serial LCD Interface supports serial type LCD panels only on LCD2. Serial Data Type, Data Direction, Data Format, and Serial Clock Phase and Polarity are all selectable and are controlled in the LCD2 Serial Interface Setting register (REG[005Ch]). Serial Interface Panels are updated with image data as described in Section 1.5.2, “Parallel LCD Interface” on page 16.

1.6 Display Features

The S1D13717 contains display features that enhance the functionality of the Mobile Graphics Engine. These features are Picture-in-Picture Plus (PIP$^+$), Overlay, SwivelView, Mirror, and Pixel Doubling.

PIP$^+$ is a sub-window within the Main Window and typically is used to display the camera image or a decoded JPEG image. PIP$^+$ can be used with the overlay functions so that only the part of the PIP$^+$ window that overlaps the overlay color in the Main Window is displayed (according to the overlay function selected). Various overlay functions can be employed such as transparency, averaging, ANDing, ORing, and Inverting. Multiple overlay functions can be enabled, but only the overlay function with the highest priority is processed.

SwivelView is a hardware rotation of the display image by either 90, 180, or 270 degrees. By processing the rotation of the image in hardware, SwivelView offers a performance advantage over software rotation. SwivelView can be used to support portrait sized panels mounted in a landscape orientation or vice versa.

Mirror can be used to mirror the image in either the PIP+ window display, Main Window display, or both. A typical application for mirroring is to support swivelling on a clamshell phone. When the large display is on the outside of the phone and the camera is pointing at the user, mirroring allows the camera image to be displayed properly.

Pixel Doubling is a feature that can be used to double the size of an image in either the PIP+ window display, Main Window display or both. Typical applications for pixel doubling include increasing the displayed size of a decoded JPEG image or using a larger panel size than is supported natively by an operating system. For example, if a 320x320 resolution panel is used with an OS that supports only a main display of 160x160 (such as in many PDAs), pixel doubling can be enabled to utilize the whole display.

1.7 Camera Interface

The S1D13717 supports an 8-bit parallel Camera Interface. The input data format supported is YUV 4:2:2. Embedded sync signals, as defined by the ITU-R BT656 standard, are also supported. A clock is supplied to the camera from the camera interface (CMCLKOUT) and the camera in turn outputs YUV data, horizontal and vertical sync signals, and a pixel clock that the S1D13717 camera interface uses to sample the incoming YUV data. The CMCLKOUT frequencies are controlled by the Camera Clock Divide Select bits (REG[0100h] bits 3-0). The camera interface supports various types of YUV cameras by allowing the selection of different formats of YUV 4:2:2 signals. Features such as YUV Data Format, YUV Data Range, HSYNC and VSYNC polarity, and Camera Pixel Clock Input Polarity are all selectable.

Since the Camera Pixel Clock can be, at most, 1/3 the S1D13715 System Clock , the frames per second of the camera image displayed on the LCD display is dependant on the internal speed of the S1D13717. For example, a setting of 54MHz for the System Clock results in the camera returning a Pixel Clock of 6.5MHz when the S1D13717 Camera Clock Out Divide is set to a divide of 4 (typical cameras use a divide by 2 of the input clock to generate the pixel clock). For CIF resolutions (352x288), this translates into 29 fps. For a Camera Clock Out Divide of 2 and VGA resolutions (640x480), 21 fps is achieved.

1.8 Resizers and YUV/RGB Converter

There are two resizers in the S1D13717: the view resizer and the capture resizer. Both resizers can be used to resize (crop) and/or scale incoming YUV data from the camera interface, from the JPEG Decoder, or from the Host CPU in YUV bypass mode. Once the YUV data has been resized and scaled, it gets converted to RGB data by the YUV/RGB Converter (YRC), so that it can be displayed on the LCD panel. The location in memory where the YRC writes the RGB data is defined by the YUV/RGB Converter Write Start Address registers (REG[0242h]-[0244h]). The output bpp of the YRC must match either the Main Window color depth (bpp) or the PIP+ Window color depth (bpp) setting, depending on which window the image is being displayed in. The YRC color depth (bpp) output is controlled by the YRC Output Bpp Select bits (REG[0240h] bits 11-10). The resizers can support a maximum image size up to 2048 x 2048 pixels.

Although each resizer can be configured to be the source for the YRC using the Output Source Select bit (REG[0940h] bit 3), typically the view resizer is set as the source since only the capture resizer can be the source for the JPEG Encoder or for YUV bypass mode to the Host CPU. A typical application has the view resizer resizing the camera data and has the YRC converting it for display on the LCD panel, while the capture resizer is used to send camera YUV data for JPEG encoding or for raw storage by the Host CPU. When the desired viewed camera image is the same dimensions as the desired captured JPEG or YUV image, only the capture resizer needs to be used.

Note
Only the view resizer can be used to resize YUV data from the JPEG Decoder or from the Host CPU.

1.9 JPEG Encoder / Decoder

The S1D13717 contains a full JPEG Codec capable of encoding an incoming camera data stream or decoding a JPEG image sent from the Host CPU.

1.9.1 Encoder

Either the YUV data stream from the camera interface or the display buffer memory via the RGB to YUV Converter or YUV data from the host can be encoded into a JPEG image. The YUV data from the capture resizer is organized into 8 x 8 blocks in the JPEG Line Buffer, as required for JPEG processing, and then sent to the JPEG Encoder. As the JPEG Encoder is encoding the YUV data, it starts filling up the JPEG FIFO with JPEG data. This data must be read by the Host CPU before the JPEG FIFO overflows. Status flags and interrupts can be used to determine how full the JPEG FIFO is becoming. The JPEG FIFO is accessed through the JPEG FIFO Read/Write register (REG[09A6h]). The JPEG FIFO can be set as large as 128K bytes and typically this will be large enough to contain the whole JPEG image. A smaller JPEG file size can be achieved using the capture resizer's trimming and scaling functions or a higher JPEG compression ratio can be achieved by using different Quantization and Huffman Tables.

As mentioned in Section 1.3, "Internal Memory" on page 12, when the JPEG functions are enabled, 32K bytes of the internal memory is used for the JPEG Line Buffer and from 4K bytes to 64K bytes is used for the JPEG FIFO. The JPEG Encoder can encode YUV 4:2:2, YUV 4:2:0, and YUV 4:1:1 data formats and will convert the incoming YUV data to the desired format. This encoding option is set by the YUV Format Select bits (REG[1000h] bits 1-0). The JPEG file size can be reduced if a smaller UV:Y ratio format is used.

The intended use of the JPEG Encoder is to "take a snapshot" of the currently viewed camera image or display image, or to encode YUV data sent by the Host CPU. This JPEG image is then downloaded to the Host CPU through the JPEG FIFO and stored as a JPEG file.

1.9.2 Decoder

The S1D13717 contains a JPEG Decoder which allows the Host CPU to send a JPEG image file for conversion and display on the LCD panel, or to send the resulting YUV decoded data back to the Host CPU. The incoming JPEG data is written to the JPEP FIFO and then goes to the JPEG Decoder for decoding into YUV format. The YUV format output is based on the original format the JPEG file was encoded from and is reported in the YUV Format Select bits (REG[1000h] bits 1-0). The output of the JPEG Decoder goes to the JPEG Line Buffer which then organizes the 8 x 8 blocks of YUV data into the correct YUV format and sends this data to the view resizer. The view resizer can trim and scale the image and then it is converted by the YRC to be displayed on the LCD panel or sent to the Host CPU.

While writing the JPEG data to the JPEG FIFO, the Host CPU may be interrupted. When this happens, the JPEG Decoder completes decoding the data stored in the JPEG FIFO and the waits for more data from the Host CPU. The decode operation will continue until the JPEG Decoder detects the End-of-File Marker. The JPEG FIFO must not be overflowed by the Host CPU. Status flags and interrupts can be used to determine how full the JPEG FIFO is becoming. The JPEG FIFO is accessed through the JPEG FIFO Read/Write register (REG[09A6h]).

As mentioned in Section 1.3, “Internal Memory” on page 12, when the JPEG functions are enabled, 32K bytes of the internal memory is used for the JPEG Line Buffer and from 4K bytes to 64K bytes is used for the JPEG FIFO. The JPEG Decoder can decode YUV 4:4:4, YUV 4:2:2, YUV 4:2:0, and YUV 4:1:1 data formats.

1.10 2D BitBLT Engine

The purpose of the 2D BitBLT Engine is to improve the overall system performance by off-loading the work of the Host CPU in moving display data between the CPU and display memory. There are five BitBLTs (Bit Block Load Transfer) that can move display data from one location to another. Additionally, data functions can be performed that manipulate the source and/or destination data. For more information on the 2D BitBLT Engine, see Section 16, “2D BitBLT Engine” on page 320.

2 Features

2.1 Internal Memory

- Embedded 224K byte SRAM memory used for:
  - Display Buffer
  - JPEG FIFO
  - JPEG Line Buffer

2.2 Host CPU Interface

- Four generic asynchronous CPU interfaces
- 16-bit data bus
  - 16-bit register and FIFO access
  - 8/16-bit display buffer access
- Direct / Indirect addressing
- Little / Big endian support
- Registers are memory-mapped
  - M/R# input selects between memory and register address space
  - M/R# and CS# inputs select between memory and register address space in 2 CS# mode
- CPU serial port for direct control of a serial LCD
- CPU parallel port for direct control of a parallel LCD

2.3 Display Support

- Active Matrix TFT displays: 9/12/18-bit interface
  - TFT with u-Wire interface
  - a-Si TFT interface
  - Epson ND-TFD interface
- 8/9-bit serial interface LCDs with integrated RAM
- 8/16/18-bit MPU parallel interface LCDs with integrated RAM
- Supports a maximum of 2 panels (LCD1 and LCD2 can’t be refreshed simultaneously)

2.4 Display Modes

- Supports three panel interface modes which each allow two LCDs (LCD1 and LCD2) to be connected to the S1D13717. Only one LCD can be active at a time.
  - Mode 1:
    - LCD1: RGB type panel
    - LCD2: Serial interface panel
  - Mode 2:
    - LCD1: Parallel interface panel
    - LCD2: Serial interface panel
  - Mode 3:
    - LCD1: Parallel interface panel
    - LCD2: Parallel interface panel
  - Mode 4:
    - LCD1: RGB type panel
    - LCD2: Parallel interface panel
- Host CPU can directly control serial interface panels on LCD2
- Host CPU can directly control parallel interface panels on LCD1 or LCD2
- 8/16/32 bit-per-pixel (bpp) color depths
- Separate Look-up Tables (LUTs) for the Main Window and the PIP$^+$ Window
- LUTs can be bypassed

2.5 Display Features

- Overlay functions
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image
- Mirror Display: provides a “mirror” image of the display
- Virtual display support: displays images larger than the panel size through the use of panning and scrolling
- Picture-in-Picture Plus (PIP$^+$): displays a variable size window overlaid over background image
- Pixel Doubling
- Video Invert: Data output to the LCD is inverted

2.6 Camera Interface

- 8-bit Camera Interface (YUV Multi Out)
- Supports YUV 4:2:2 format
- Supports ITU-R BT.656 format
- MPU type interface camera support on Camera interface
- Strobe control function

2.7 Digital Video Features

- Hardware JPEG codec based on the JPEG baseline standard
  - JPEG Encode supports YUV 4:2:2, YUV 4:2:0, YUV4:1:1 formats
  - JPEG Decode supports YUV 4:4:4, YUV 4:2:2, YUV 4:2:0, YUV4:1:1 formats
  - Arithmetic accuracy satisfies the compatibility test of JPEG Part-2
  - Software control of image size
  - Maximum horizontal image size for JPEG encoding (YUV 4:2:2 format: up to 2880 pixels)
- Two resizers: View resizer receives YUV data from the camera interface, or from the JPEG decoder, or from the Host CPU. Capture resizer receives YUV data only from the camera interface.
  - YUV Data can be resized (trimmed and scaled) then:
    - Converted to RGB data for display on the LCD
    - Converted to JPEG data and read by the CPU Host via the JPEG FIFO
    - Read by the Host CPU directly (YUV format)
- YUV to RGB Converter (YRC): YUV data from the View Resizer or Capture Resizer is converted to RGB format to be displayed on the LCD.

2.8 Picture Input / Output Functions

- The YUV data from Camera Interface can be:
  - Stored in the display buffer after resizing and conversion to RGB format.
  - Transferred to the Host CPU via the JPEG FIFO after resizing and encoding to JPEG format.
  - Transferred to the Host CPU via the JPEG FIFO after resizing and conversion to YUV format (4:2:2, 4:2:0).
- The JPEG file downloaded from the Host CPU can be:
  - Decoded by the internal JPEG decoder, resized, scaled, converted to RGB and stored in the display buffer memory for display on the LCD.
  - Decoded by the internal JPEG decoder, resized, scaled, and downloaded to the Host CPU via the JPEG FIFO.
- YUV data (format 4:2:2 or 4:2:0) downloaded from the Host CPU can be:
  - Resized, scaled, converted to RGB and stored in the display buffer memory for display on the LCD.
  - Encoded by the internal JPEG encoder, resized, scaled, and downloaded to the Host CPU via the JPEG FIFO.
- RGB data in the display buffer can be:
  - Converted to YUV, then transferred to the Host CPU via the JPEG FIFO after resizing and encoding to JPEG format.

2.9 2D BitBLT Acceleration

- 2D BitBLT engine including: (this function does not support 32 bpp modes)

Move BitBLT	Transparent Move BitBLT
Solid Fill BitBLT	Read BitBLT
Pattern Fill BitBLT	Move BitBLT with Color Expansion

2.10 SD Memory Card Interface

- SD Memory Card interface compatible with the SD Memory Card Physical Layer version 1.0 specification
  - 4-bit or 1-bit interface (SPI mode is not supported)
  - No security functions
  - Card Detect and Write Protect inputs

2.11 Clock

- Internal PLL driven by a single external reference clock, 32.768KHz
- 40 - 55MHz PLL output
- PLL bypass mode for external clock input

2.12 Power Save

- Software initiated power save mode
- Software initiated display blank

2.13 Miscellaneous

- General Purpose Input/Output pins are available
- FCBGA 161-pin package

3 System Diagrams

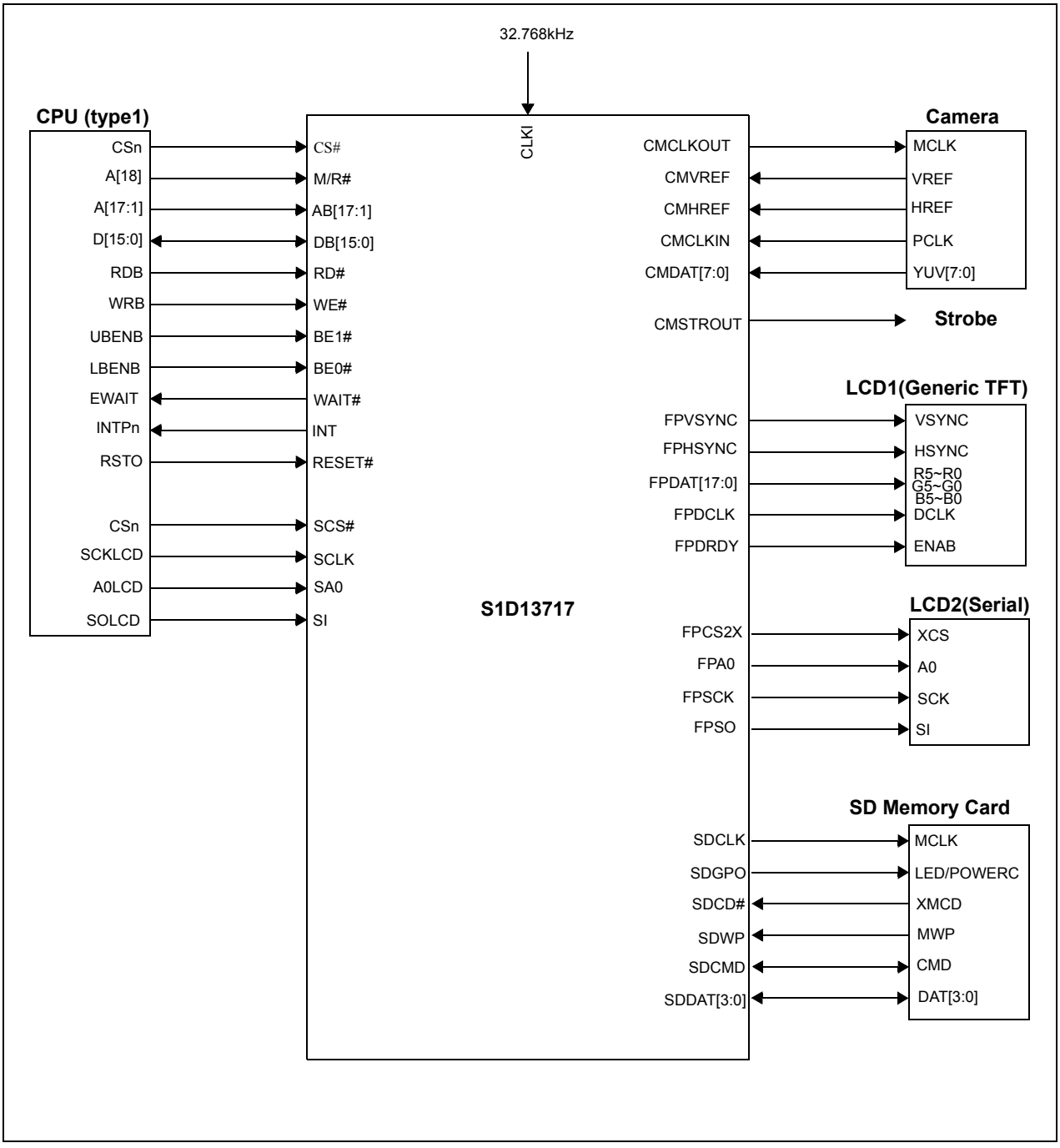


Figure 3-1: S1D13717 System Diagram 1

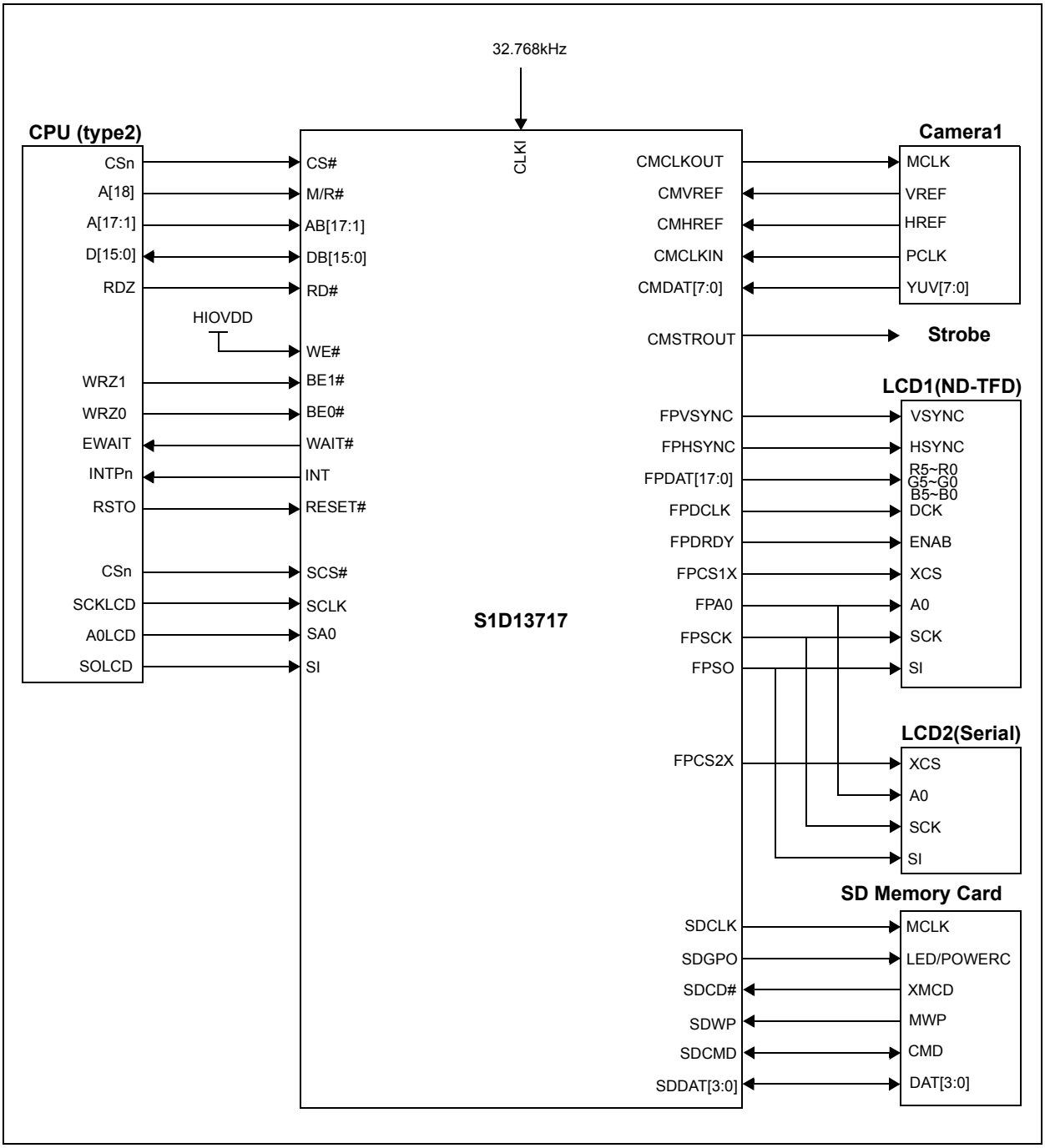


Figure 3-2: S1D13717 System Diagram 2

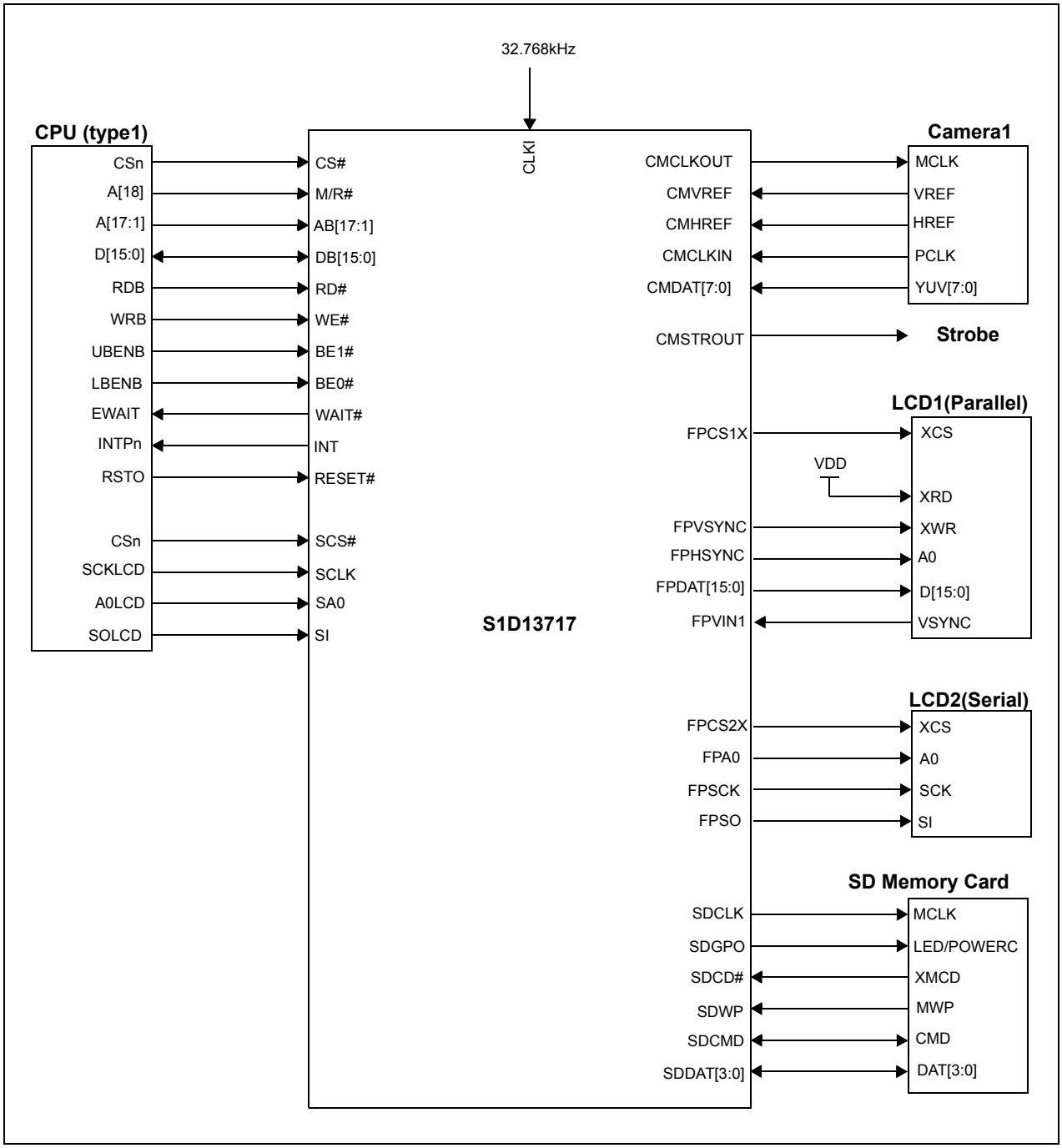


Figure 3-3: S1D13717 System Diagram 3

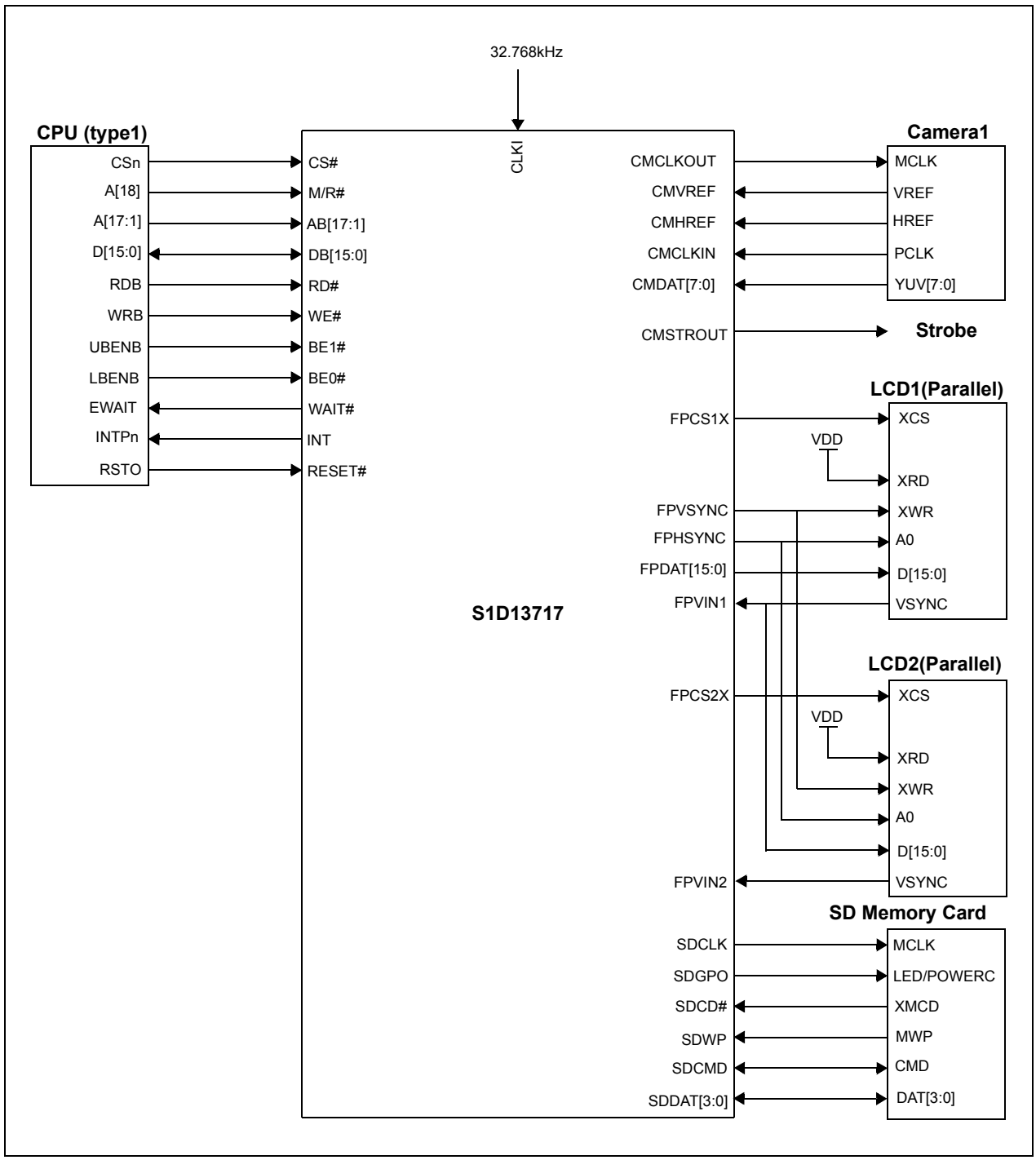


Figure 3-4: S1D13717 System Diagram 4

4 Block Diagram

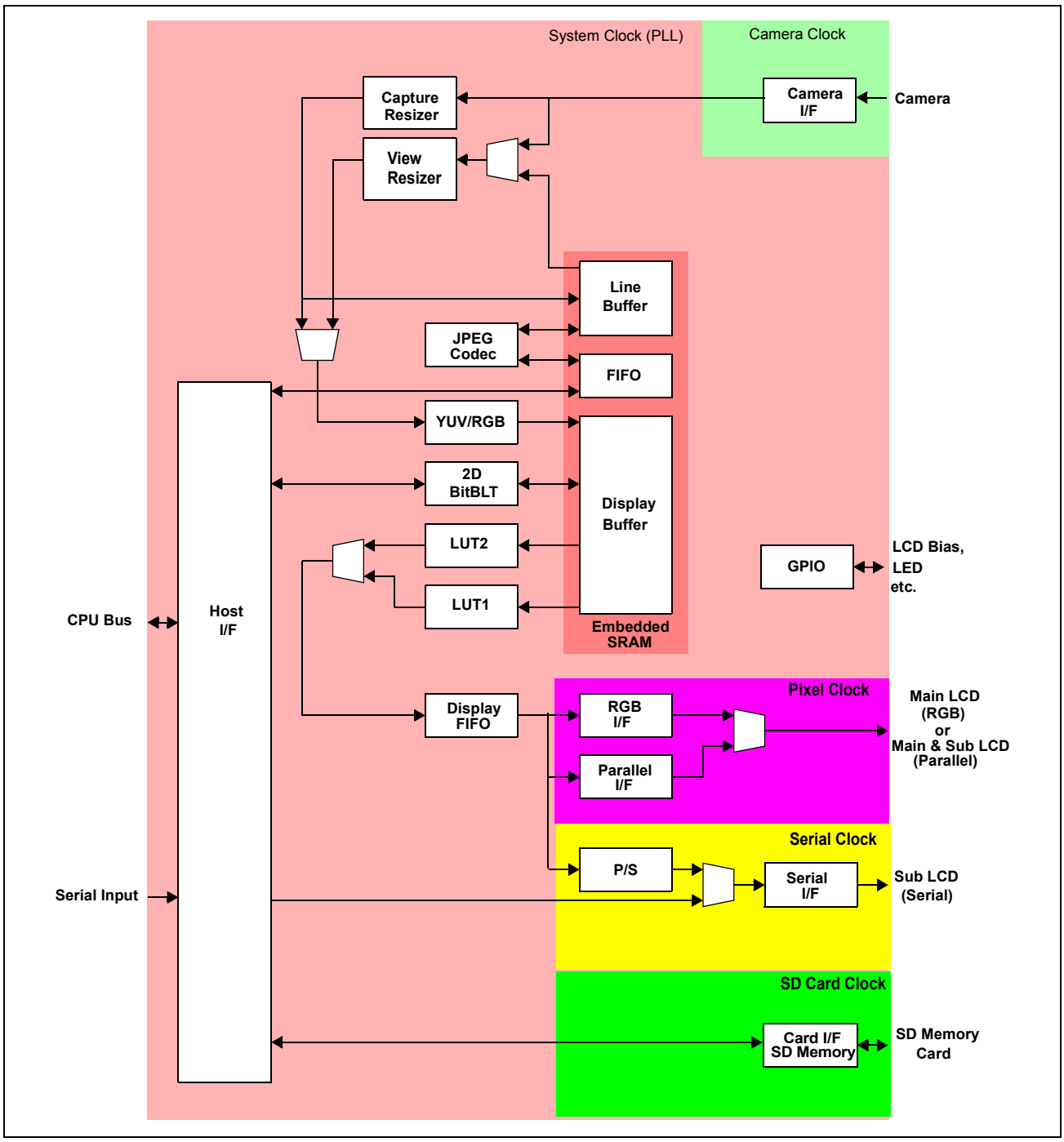


Figure 4-1: S1D13717 Block Diagram

5 Pins

5.1 S1D13717 Pinout Diagram (FCBGA-161)

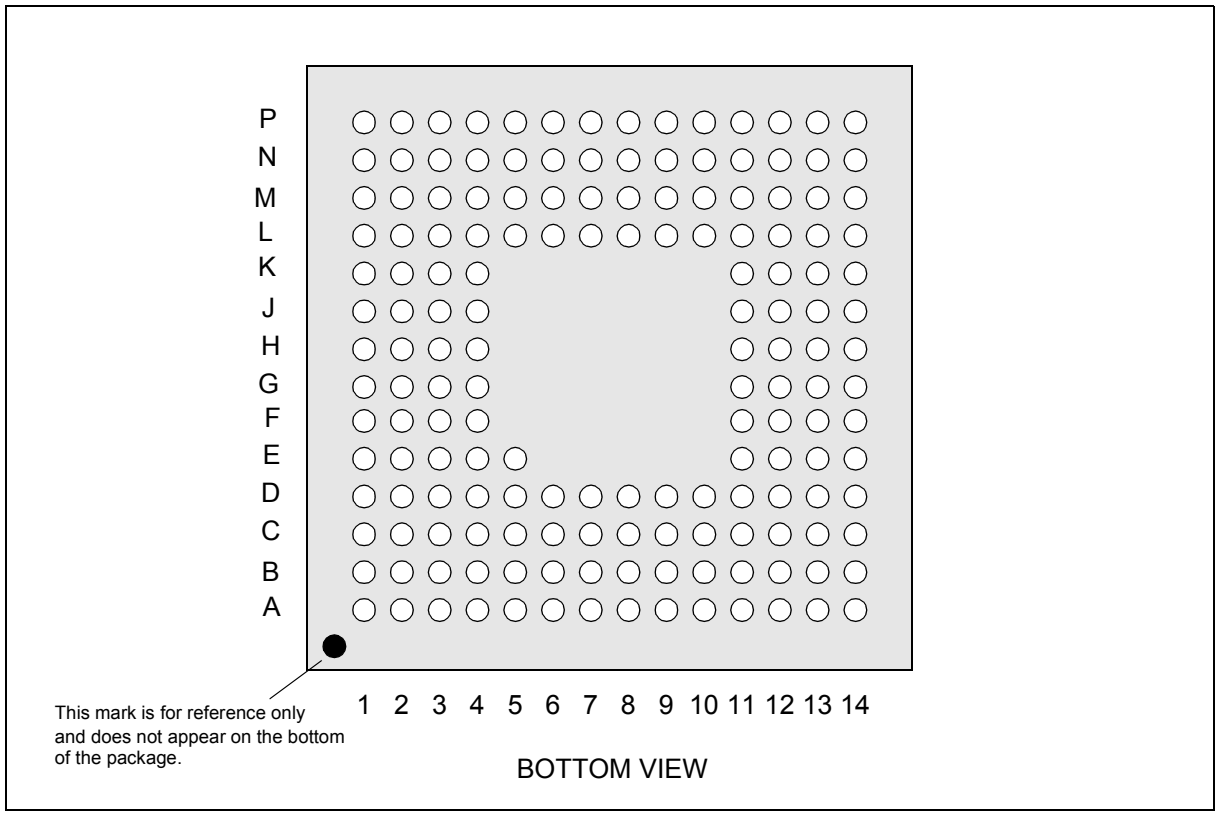


Figure 5-1: S1D13717 FCBGA-161 Pin Mapping

Table 5-1: S1D13717 FCBGA-161 Pin Mapping

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	NC	NC	CMSTROUT	SDCMD	SDDAT1	SDDAT3	SDGPO	COREVDD	CMDAT3	CMDAT4	CIOVDD	VSS	NC	NC
N	NC	NC	VSS	VSS	SDDAT0	VSS	CMCLKOUT	CMHREF	CMDAT1	CMDAT5	CNF3	CNF4	NC	NC
M	TESTEN	COREVDD	SDWP	SDCLK	SIOVDD	SIOVDD	CMCLKIN	CMVREF	CMDAT2	CMDAT6	CNF5	CNF6	PLLVSS	VCP
L	CNF0	CNF2	SCANEN	GPIO3	SDCD#	SDDAT2	VSS	CMDAT0	VSS	CMDAT7	SCLK	CLKI	PLLVDD	COREVDD
K	VSS	GPIO2	CNF1	GPIO0							INT	SI	SCS#	SA0
J	FPDAT17	PIOVDD	GPIO1	FPDAT16							BE0#	RESET#	WAIT#	VSS
H	VSS	FPDAT14	FPDAT15	FPDAT13							RD#	BE1#	WE#	M/R#
G	FPDAT12	FPDAT10	FPDAT9	FPDAT11							CS#	DB1	DB0	HIOVDD
F	FPDAT8	FPDAT7	FPDAT5	COREVDD							DB2	DB5	DB3	VSS
E	FPDAT3	FPDAT4	FPDAT1	FPDAT6	NC						DB4	DB9	COREVDD	DB7
D	FPDAT2	FPDAT0	FPFRAME	VSS	FPA0	FPVIN2	HIOVDD	AB9	AB6	VSS	DB6	DB10	VSS	DB8
C	FPLINE	PIOVDD	DRDY	FPCS2#	FPSO	AB16	AB13	VSS	AB7	AB3	DB15	HIOVDD	DB12	DB11
B	NC	NC	FPCS1#	VSS	FPVIN1	AB15	AB12	AB11	AB8	AB4	AB1	DB14	NC	NC
A	NC	NC	FPSHIFT	FPSCLK	COREVDD	AB17	AB14	AB10	COREVDD	AB5	AB2	DB13	NC	NC

5.2 Pin Descriptions

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
Z	=	High Impedance
L	=	Low level output
H	=	High level output
0	=	Pull-down control on input
1	=	Pull-up control on input

Table 5-2: Cell Descriptions

Item	Description
IC	LVCMOS[1] input
ICU	LVCMOS input with pull-up resistor (60KΩ@3.0V)
ICD	LVCMOS input with pull-down resistor (60KΩ@3.0V)
IHCS	H System LVCMOS level Schmitt input
ILCS	L System LVCMOS level Schmitt input
OLN35	Low noise output buffer (3.5mA/-3.5mA@3.0V)
OLN35T	Low noise Tri-state output buffer (3.5mA/-3.5mA@3.0V)
BLNC35	Low noise LVCMOS IO buffer (3.5mA/-3.5mA@3.0V)
BLNC35D	Low noise LVCMOS IO buffer (3.5mA/-3.5mA@3.0V) with pull-down resistor (60KΩ@3.0V)
BLNC35DS	Low noise LVCMOS Schmitt IO buffer (3.5mA/-3.5mA@3.0V) with pull-down resistor (60KΩ@3.0V)
ITD	Test mode control input with pull-down resistor (60KΩ@3.0V)
ILTR	Low Voltage Transparent Input
IHTR	High Voltage Transparent Input
OHTR	High Voltage Transparent Output

1. LVCMOS is Low Voltage CMOS (see Section 6, “D.C. Characteristics” on page 49).

5.2.1 Unused Pins

All unused input pins should be connected to their inactive state if an internal pull-down resistor is not present.
All unused output pins should be left unconnected.
All unused bi-directional pins should be connected to a 100KΩ pull-down/up resistor if an internal pull-down resistor is not present.

5.2.2 Host Interface

Many of the host interface pins have different functions depending on the selection of the host bus interface (see configuration of CNF[4:2] pins in Table 5-10: "Summary of Power-On/Reset Options," on page 42). For a summary of host interface pins, see Table 5-11: "Host Interface Pin Mapping (1 CS# mode)," on page 44 and Table 5-12: "Host Interface Pin Mapping (2 CS# mode)," on page 45.

Table 5-3: Host Interface Pin Descriptions

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
AB[17:2]	I	A6,C6,B6, A7,C7,B7, B8,A8,D8, B9,C9,D9, A10,B10, C10,A11, B11	IC	HIOVDD	Z	System address bits 17:2. • For Indirect Host Bus Interfaces, these pins must be connected to V_{SS}.
AB1	I	B11	IC	HIOVDD	Z	System address bit 1. • For Indirect Host Bus Interfaces, this pin is the command/data signal.
DB[15:0]	IO	C11,B12, A12,C13, C14,D12, E12,D14, E14,D11, F12,E11, F13,F11, G12,G13	BLNC35	HIOVDD	Z	System data bus.
CS#	I	G11	IC	HIOVDD	Z	This input pin has multiple functions. • For 1 CS# mode, this pin inputs the chip select signal (CS#). • For 2 CS# mode, this pin inputs the memory chip select signal (CSM#).
M/R#	I	H14	IC	HIOVDD	Z	This input pin has multiple functions. • For 1 CS# mode, this pin selects between the display buffer and register address spaces. When M/R# is set high, the display buffer is accessed and when M/R# is set low the registers are accessed. • For 2 CS# mode, this pin inputs the register chip select (CSR#). • For Indirect Host Bus Interfaces, this pin must be connected to V_{SS}.

Table 5-3: Host Interface Pin Descriptions (Continued)

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
RD#	I	H11	IC	HIOVDD	Z	This input pin has multiple functions. • For Indirect and Direct 68, this pin must be connected to $HIOV_{DD}$. • For Indirect and Direct 80 Type 1 and Type 2, this pin is the read enable signal (RD#). • For Indirect and Direct 80 Type 3, this pin is the DB[7:0] lower byte read enable signal (RDL#).
WE#	I	H13	IC	HIOVDD	Z	This input pin has multiple functions. • For Indirect and Direct 68, this pin is the read/write signal (R/W#). • For Indirect and Direct 80 Type 1, this pin is the write enable signal (WE#). • For Indirect and Direct 80 Type 2, this pin must be connected to $HIOV_{DD}$. • For Indirect and Direct 80 Type 3, this pin is the DB[7:0] lower byte write enable signal (WEL#).
BE1#	I	H12	IC	HIOVDD	Z	This input pin has multiple functions. • For Indirect and Direct 68, this pin is the D[15:8] upper data strobe (UDS#). • For Indirect and Direct 80 Type 1, this pin is the D[15:8] upper byte enable signal (UBE#). • For Indirect and Direct 80 Type 2, this pin is the DB[15:8] upper byte write enable signal (WEU#). • For Indirect and Direct 80 Type 3, this pin is the DB[15:8] upper byte read enable signal (RDU#).
BE0#	I	J11	IC	HIOVDD	Z	This input pin has multiple functions. • For Indirect and Direct 68, this pin is the D[7:0] lower data strobe (LDS#). • For Indirect and Direct 80 Type 1, this pin is the D[7:0] lower byte enable signal (LBE#). • For Indirect and Direct 80 Type 2, this pin is the DB[7:0] lower byte write enable signal (WEL#). • For Indirect and Direct 80 Type 3, this pin is the DB[15:8] upper byte write enable signal (WEU#).
WAIT#	O	J13	OLN35T	HIOVDD	Z	During a data transfer, WAIT# is driven active (low) to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. WAIT# is released to a high impedance state after the data transfer is complete. This pin can be masked using the CNF0 pin.
INT	O	K11	OLN35	HIOVDD	L	Interrupt output. When an internal interrupt occurs, this output pin is driven high. If the Host CPU clears the internal interrupt, this pin is driven low.

Table 5-3: Host Interface Pin Descriptions (Continued)

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
RESET#	I	J12	IHCS	HIOVDD	Z	This active low input sets all internal registers to their default state and forces all signals to their inactive states.
SCS#	I	K13	ICU	HIOVDD	1	This input pin has multiple functions. • For Serial Bypass Mode, this pin is the serial chip select input for the Host CPU serial interface. When Serial Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial interface LCD. •
SCLK	I	L11	ICD	HIOVDD	0	This input pin has multiple functions. • For Serial Bypass Mode, this pin is the serial clock input for the Host CPU serial interface. When Serial Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial interface LCD. •
SA0	I	K14	ICD	HIOVDD	0	This input pin has multiple functions. • For Serial Bypass Mode, this pin is the serial A0 command input for the Host CPU serial interface. When Serial Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial interface LCD. •
SI	I	K12	ICD	HIOVDD	0	This input pin has multiple functions. • For Serial Bypass Mode, this pin is the serial data input for the Host CPU serial interface. When Serial Bypass Mode is enabled, the Host CPU can directly control the LCD2 serial interface LCD. •

5.2.3 LCD Interface

Many of the LCD Interface pins have different functions depending on the configured panel interface mode. See Table 5-13: “LCD Interface Pin Mapping,” on page 46 for more details on the pin functions.

- Mode 1 is LCD1: RGB, LCD2: Serial
- Mode 2 is LCD1: Parallel, LCD2: Serial
- Mode 3 is LCD1: Parallel, LCD2: Parallel
- Mode 4 is LCD1: RGB, LCD2: Parallel

For further information on the three panel interface modes, see the bit description for REG[0032h] bits 1-0.

Table 5-4: LCD Interface Pin Descriptions

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
FPDAT[17:0]	O	J1,J4,H3, H2,H4,G1, G4,G2, G4,F1,F2, E4,F3,E2, E1,D1,E3, D2	OLN35	PIOVDD	L	These output pins have multiple functions. • For Mode 1 and Mode 4 RGB interfaces, these pins are the LCD1 RGB data outputs. • For Mode 2, Mode 3 and Mode 4 parallel interfaces, FPDAT[17:0] are the parallel interface data outputs. • When REG[0056h] bit 13 = 1 or REG[005Eh] bit 13 = 1, these pins are controlled with tri-state. • For Parallel Bypass Mode, these pins output the Host CPU data. See Table 5-14: “Serial Bypass Pin Mapping,” on page 47.
FPFRAME	O	D3	OLN35	PIOVDD	L (H)	This output pin has multiple functions. • For Mode 1 and Mode 4 RGB interfaces, this pin is the LCD1 frame pulse output. • For Mode 2, Mode 3 and Mode 4 parallel interfaces, this pin is the write command output. • For Parallel Bypass Mode, this pin outputs the Host CPU XWR signal.
FPLINE	O	C1	OLN35	PIOVDD	L	This output pin has multiple functions. • For Mode 1 and Mode 4 RGB interfaces, this pin is the LCD1 line pulse output. • For Mode 2, Mode 3 and Mode 4 parallel interfaces, this pin is the A0 output. • For Parallel Bypass Mode, this pin outputs the Host CPU A0 signal.
FPSHIFT	O	A3	OLN35	PIOVDD	L	This output pin has multiple functions. • For Mode 1 and Mode 4, this pin is the LCD1 pixel clock output. • For all other cases, this pin is not used.

Table 5-4: LCD Interface Pin Descriptions (Continued)

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
DRDY	O	C3	OLN35	PIOVDD	L	This output pin has multiple functions. • For Mode 1 and Mode 4, this pin is the LCD1 DRDY output. • For all other cases, this pin is not used.
FPCS1#	O	B3	OLN35	PIOVDD	L (H)	This output pin has multiple functions. • For Mode 1 and Mode 4, this pin is the LCD1 serial interface chip select output. • For Mode 2 and Mode 3, this pin is the LCD1 parallel interface chip select output. • For Parallel Bypass Mode, this pin outputs the Host CPU NCS1 signal.
FPCS2#	O	C4	OLN35	PIOVDD	L (Mode 3 = H)	This output pin has multiple functions. • For Mode 1, this pin is the LCD2 serial interface chip select output. When power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SCS# pin. • For Mode 2, this pin is the LCD2 serial interface chip select output. When power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SCS# pin. • For Mode 3 and 4, this pin is the LCD2 parallel interface chip select output. • For Serial or Parallel Bypass Mode, this pin outputs the Host CPU NCS2 signal.
FPSCLK	O	A4	OLN35	PIOVDD	L	This output pin has multiple functions. • For Mode 1, this pin is the LCD1 and LCD2 serial interface clock output. For Mode 4, this pin is the LCD1 serial interface clock output. For LCD2, when power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SCLK pin. • For Mode 2, this pin is the LCD2 serial interface clock output. When power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SCLK pin. • For Mode 3, this pin is not used. • For Serial Bypass Mode, this pin outputs the Host CPU SCK signal.

Table 5-4: LCD Interface Pin Descriptions (Continued)

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
FPA0	O	D5	OLN35	PIOVDD	L	This output pin has multiple functions. • For Mode 1, this pin is the LCD1 and LCD2 serial interface A0 output. For Mode 4, this pin is the LCD1 serial interface A0 output. For LCD2, when power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SA0 pin. • For Mode 2, this pin is the LCD2 serial interface A0 output. When power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SA0 pin. • For Mode 3, this pin is not used. • For Serial Bypass Mode, this pin outputs the Host CPU A0 signal.
FPSO	O	C5	OLN35	PIOVDD	L	This output pin has multiple functions. • For Mode 1, this pin is the LCD1 and LCD2 serial interface data output. For Mode 4, this pin is the LCD1 serial interface data output. For LCD2, when power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SI pin. • For Mode 2, this pin is the LCD2 serial interface data output. When power save is enabled or when Serial Bypass Mode is enabled, this pin outputs the state of the SI pin. • For Mode 3, this pin is not used. • For Serial Bypass Mode, this pin outputs the Host CPU SI signal.
FPVIN1	I	B5	IC	PIOVDD	Z	This input pin has multiple functions. • For Mode 2, Mode 3 and Mode 4, this pin is the parallel interface LCD1 vertical sync input from the LCD panel. If this pin is not used, it must be connected to ground (VSS).
FPVIN2	I	D6	IC	PIOVDD	Z	This input pin has multiple functions. • For Mode 1 and Mode 2, this pin is the LCD2 serial interface vertical sync input from the LCD panel. • For Mode 3 and Mode 4, this pin is the LCD2 parallel interface vertical sync input from the LCD panel. If this pin is not used, it must be connected to ground (VSS).

5.2.4 Camera Interface

The Camera Interface supports a Type 1, 8-bit bus Camera interface. See Table 5-16: "Camera Interface Pin Mapping," on page 48 for details on the connections for the Camera Interface.

Table 5-5: Camera Interface Pin Descriptions

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
CMDAT[7:0]	IO	L10,M10, N10,P10, P9,M9,N9, L8	BLNC35D	CIOVDD	0	For the Camera interface, these pins are the 8-bit data input (CAMDAT[7:0]).
CMVREF	IO	M8	BLNC35D	CIOVDD	0	For the Camera interface, this pin is the vertical sync input (VREF).
CMHREF	IO	N8	BLNC35D	CIOVDD	0	For the Camera interface, this pin is the horizontal sync input (HREF).
CMCLKOUT	O	N7	OLN35	CIOVDD	L	For the Camera interface, this pin is the Master clock output (CAMMCLK).
CMCLKIN	IO	M7	BLNC35DS	CIOVDD	0	For the Camera interface, this pin is the camera pixel clock input (CAMPCLK).
CMSTROUT	O	P3	OLN35	CIOVDD	see note	This output pin is the camera interface strobe (flash).

Note

On RESET# this output drives low when RESET# is low, then drives high once RESET# goes high.

5.2.5 SD Memory Card Interface

Table 5-6: SD Memory Card Interface Pin Descriptions

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
SDDAT[3:0]	IO	P6,L6,P5, N5	BLNC35D	SIOVDD	0	These input/output pins are the SD memory card data IO.
SDCMD	IO	P4	BLNC35D	SIOVDD	0	This input/output pin is the SD memory card command IO.
SDCLK	IO	M4	BLNC35D	SIOVDD	0	This input/output pin is the SD memory card clock output.
SDCD#	I	L5	IHCSD	SIOVDD	0	This input pin is the SD memory card detect.
SDWP	I	M3	IHCSD	SIOVDD	0	This input pin is the SD memory card write protection input.
SDGPO	O	P7	OLN35	SIOVDD	L	This output pin is the SD memory card general purpose output port.

5.2.6 Clock Input

Table 5-7: Clock Input Pin Descriptions

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
CLKI	I	L12	ILCS	HIOVDD	Z	This input pin has multiple functions. • When the internal PLL is used, this pin is the input reference clock for the internal PLL (32.768KHz). • When the PLL is bypassed, this pin is the digital clock input for the system clock (SYSCLK).

5.2.7 Miscellaneous

Table 5-8: Miscellaneous Pin Descriptions

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
CNF[6:3]	I	M12,M11, N12,N11	IC	CIOVDD	Z	These inputs are used for configuring the S1D13717 and must be connected to either CIOVDD or VSS. The states of these pins are latched at RESET#. For more information, see Table 5-10: “Summary of Power-On/Reset Options,” on page 42.
CNF[2:0]	I	L2,K3,L1	IC	PIOVDD	Z	These inputs are used for configuring the S1D13717 and must be connected to either PIOVDD or VSS. The states of these pins are latched at RESET#. For more information, see Table 5-10: “Summary of Power-On/Reset Options,” on page 42.
GPIO[3:0]	IO	L4,K2,J3, K4	BLNC35D	PIOVDD	see note	These pins are general purpose input/output pins. Their default configuration (input or output) is controlled using CNF1.
TESTEN	I	M1	ITD	PIOVDD	0	Test Enable input used for production test only. This pin should be left unconnected for normal operation.
SCANEN	I	L3	ICD	PIOVDD	0	Scan Enable input used for production test only. This pin should be left unconnected for normal operation.
VCP	I	M14	ILTR	COREVDD	—	PLL output monitor pin used for production test only. This pin should be left unconnected for normal operation.

Note

When CNF1 = 0 (GPIO pins are outputs), the reset state of GPIO[3:0] is 0.
When CNF1 = 1 (GPIO pins default to inputs), the reset state of GPIO[3:0] is Hi-Z.

5.2.8 Power And Ground

Table 5-9: Power And Ground Pin Descriptions

Pin Name	Type	FCBGA Pin#	Cell	Power	RESET# State	Description
HIOVDD	P	C12, D7, G14	P	—	—	IO power supply for the host interface
PIOVDD	P	C2, J2	P	—	—	IO power supply for the panel interface
CIOVDD	P	P11	P	—	—	IO power supply for the camera interface
SIOVDD	P	M5, M6	P	—	—	IO power supply for the SD memory card interface
COREVDD	P	A5, A9, E13, F4, L14, M2, P8	P	—	—	Core power supply
VSS	P	B4, C8, D4, D10, D13, F14, H1, J14, K1, L7, L9, N3, N4, N6, P12	P	—	—	GND for HIOVDD, PIOVDD, CIOVDD and COREVDD
PLLVDD	P	L13	P	—	—	PLL power supply. This supply should be isolated from the other supplies.
PLLVSS	P	M13	P	—	—	GND for PLLVDD. This ground should be isolated from the other grounds.

5.3 Summary of Configuration Options

These pins are used for configuration of the chip and must be connected directly to PIOVDD or VSS. The state of CNF[6:0] are latched on the rising edge of RESET#. Changing state at any other time has no effect.

Table 5-10: Summary of Power-On/Reset Options

<table>
<tr><th rowspan="2">Configuration Input</th><th colspan="2">Power-On/Reset State</th></tr>
<tr><th>1
(CNF[6:3] connected to CIOVDD,
CNF[2:0] connected to PIOVDD)</th><th>0
(connected to VSS)</th></tr>
<tr><td>CNF6</td><td>2 CS# mode</td><td>1 CS# mode</td></tr>
<tr><td>CNF5</td><td>Big Endian</td><td>Little Endian</td></tr>
<tr><td>CNF[4:2]</td><td colspan="2">Select host bus interface as follows:
CNF4 CNF3 CNF2 Host Bus
0 0 0 Direct 80 Type 2
0 0 1 Direct 80 Type 3
0 1 0 Indirect 80 Type 2
0 1 1 Indirect 80 Type 3
1 0 0 Direct 80 Type 1
1 0 1 Direct 68
1 1 0 Indirect 80 Type 1
1 1 1 Indirect 68</td></tr>
<tr><td>CNF1</td><td>All GPIO pins (GPIO[3:0]) are configured as inputs.

Note: When CNF1=1 at RESET#, REG[0300h]-REG[0302h] can be used to change individual GPIO pins between inputs/outputs.</td><td>All GPIO pins (GPIO[3:0] are configured as outputs.

Note: When CNF1=0 at RESET#, REG[0300h]-REG[0302h] are ignored and the GPIO pins are always outputs.</td></tr>
<tr><td rowspan="4">CNF0</td><td colspan="2">For Direct Host Bus Interface Types (see CNF[4:2])</td></tr>
<tr><td>WAIT# is used.
The setup/hold time of A[17:1], UBE#, LBE# from the RD# edge is not 0 and the setup time of CS# edge from RD# is not 0 (Direct 80 Types, see Section 7.3, “Host Interface Timing” on page 56 for the signal names for other Direct host bus interfaces).

Note: When WAIT# is used (CNF0 = 1), WAIT# may not be asserted for all cycles. WAIT# is only asserted when needed.</td><td>WAIT# is not used.
The setup/hold time of A[17:1], UBE#, LBE# from the RD# edge is 0 and the setup time of CS# edge from RD# is 0 (Direct 80 Types, see Section 7.3, “Host Interface Timing” on page 56 for the signal names for other Direct host bus interfaces).

Note: When WAIT# is not used (CNF0 = 0), WAIT# is never asserted for any cycles and the Host CPU must insert software wait states as needed to guarantee cycle length as outlined in Section 7.3.9, “WAIT Length” on page 88.</td></tr>
<tr><td colspan="2">For Indirect Host Bus Interface Types (see CNF[4:2])</td></tr>
<tr><td>WAIT# is not used.

The setup/hold time of A[2:1], UBE#, LBE# from the RD# edge is not 0 and the setup time of CS# edge from RD# is not 0 (Indirect 80 Types, see Section 7.3, “Host Interface Timing” on page 56 for the signal names for other Indirect host bus interfaces).</td><td>WAIT# is not used.

The setup/hold time of A[2:1], UBE#, LBE# from the RD# edge is 0 and the setup time of CS# edge from RD# is 0 (Indirect 80 Types, see Section 7.3, “Host Interface Timing” on page 56 for the signal names for other Indirect host bus interfaces).</td></tr>
</table>

Note

When WAIT# is used (CNF0 = 1), WAIT# may not be asserted for all cycles. WAIT# is only asserted when needed. When WAIT# is not used (CNF0 = 0), WAIT# is never asserted for any cycles and the Host CPU must insert software wait states as needed to guarantee cycle length as outlined in Section 7.3.9, “WAIT Length” on page 88.

5.4 Host Interface Pin Mapping

Table 5-11: Host Interface Pin Mapping (1 CS# mode)

Pin Name	Direct 68	Direct 80 Type 1	Direct 80 Type 2	Direct 80 Type 3	Indirect 68	Indirect 80 Type 1	Indirect 80 Type 2	Indirect 80 Type 3	Serial
AB[17:2]	A[17:2]	A[17:2]	A[17:2]	A[17:2]	Low				—
AB1	A1	A1	A1	A1	A1	A1	A1	A1	—
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	—
CS#	CS#	CS#	CS#	CS#	CS#	CS#	CS#	CS#	—
M/R#	External Decode				Low				—
RD#	High	RD#	RD#	RDL#	High	RD#	RD#	RDL#	—
WE#	R/W#	WE#	High	WEL#	R/W#	WE#	High	WEL#	—
BE#[1]	UDS#	UBE#	WEU#	RDU#	UDS#	UBE#	WEU#	RDU#	—
BE#[0]	LDS#	LBE#	WEL#	WEU#	LDS#	LBE#	WEL#	WEU#	—
WAIT#	WAIT#	WAIT#	WAIT#	WAIT#	WAIT#	WAIT#	WAIT#	WAIT#	—
INT	—	—	—	—	—	—	—	—	—
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	—
SCS#	—	—	—	—	—	—	—	—	CS#
SCLK	—	—	—	—	—	—	—	—	Serial Clock
SA0	—	—	—	—	—	—	—	—	A0
SI	—	—	—	—	—	—	—	—	Serial Data

Table 5-12: Host Interface Pin Mapping (2 CS# mode)

Pin Name	Direct 68	Direct 80 Type 1	Direct 80 Type 2	Direct 80 Type 3	Indirect 68	Indirect 80 Type 1	Indirect 80 Type 2	Indirect 80 Type 3	Serial
AB[17:2]	A[17:2]	A[17:2]	A[17:2]	A[17:2]	Indirect Host Bus Interfaces always function in 1 CS# (CNF6 setting is ignored). See Table 5-12: "Host Interface Pin Mapping (2 CS# mode)," on page 45.				—
AB1	A1	A1	A1	A1					—
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]					—
CS#	CSM#	CSM#	CSM#	CSM#					—
M/R#	CSR#	CSR#	CSR#	CSR#					—
RD#	High	RD#	RD#	RDL#					—
WE#	R/W#	WE#	High	WEL#					—
BE#[1]	UDS#	UBE#	WEU#	RDU#					—
BE#[0]	LDS#	LBE#	WEL#	WEU#					—
WAIT#	WAIT#	WAIT#	WAIT#	WAIT#					—
INT	—	—	—	—					—
RESET#	RESET#	RESET#	RESET#	RESET#					—
SCS#	—	—	—	—					CS#
SCLK	—	—	—	—					Serial Clock
SA0	—	—	—	—					A0
SI	—	—	—	—					Serial Data

5.5 LCD Interface Pin Mapping

Table 5-13: LCD Interface Pin Mapping

Pin Name	Mode 1					Mode 2		Mode 3		Mode 4	
	LCD1				LCD2	LCD1	LCD2	LCD1	LCD2	LCD1	LCD2
	RGB Interface										
	General TFT	ND-TFD	a-Si TFT	TFT with uWIRE I/F	Serial I/F	Parallel I/F	Serial I/F	Parallel I/F	Parallel I/F	RGB Interface	Parallel I/F
FPFRAME	VSYNC	VSYNC	VSYNC	VSYNC		XWR		XWR	XWR		XWR
FPLINE	HSYNC	HSYNC	HSYNC	HSYNC		A0		A0	A0		A0
FPSHIFT	DCLK	DCK	DCLK	CLK							
DRDY	DRDY	ENAB	ENAB								
FPDAT0	R5	R5				D0		D0	D0		D0
FPDAT1	R4	R4	R4	R4		D1		D1	D1		D1
FPDAT2	R3	R3	R3	R3		D2		D2	D2		D2
FPDAT3	G5	G5	G5	G5		D3		D3	D3		D3
FPDAT4	G4	G4	G4	G4		D4		D4	D4		D4
FPDAT5	G3	G3	G3	G3		D5		D5	D5		D5
FPDAT6	B5	B5				D6		D6	D6		D6
FPDAT7	B4	B4	B4	B4		D7		D7	D7		D7
FPDAT8	B3	B3	B3	B3		D8		D8	D8		D8
FPDAT9	R2	R2	R2	R2		D9		D9	D9		D9
FPDAT10	R1	R1	R1	R1		D10		D10	D10	See LCD1 for Mode 1	D10
FPDAT11	R0	R0	R0	R0		D11		D11	D11		D11
FPDAT12	G2	G2	G2	G2		D12		D12	D12		D12
FPDAT13	G1	G1	G1	G1		D13		D13	D13		D13
FPDAT14	G0	G0	G0	G0		D14		D14	D14		D14
FPDAT15	B2	B2	B2	B2		D15		D15	D15		D15
FPDAT16	B1	B1	B1	B1		D16		D16	D16		D16
FPDAT17	B0	B0	B0	B0		D17		D17	D17		D17
FPCS1#		XCS	SSTB	LCDCS		NCS1		NCS1			
FPCS2#					NCS2		NCS2		NCS2		NCS2
FPSCLK		SCK	SCLK	SCLK	SCK		SCK				
FPA0		A0			A0		A0				
FPSO		SI	SDATA	SDO	SI		SI				
FPVIN1						VIN1		VIN1			
FPVIN2					VIN2		VIN2		VIN2		VIN2

Table 5-14: Serial Bypass Pin Mapping

		LCD I/F Mode 1		LCD I/F Mode 2	
REG[0032h] bits 1-0		**00**		**10**	
REG[0032h] bit 8		**1**	**0**	**1**	**0**
LCD1, LCD2 Panel Types		**LCD1: RGB LCD2: Serial**		**LCD1: Parallel (16/18-bit) LCD2: Serial**	
Pin Name	**Type**	**Serial Bypass**	**Bypass Disabled**	**Serial Bypass**	**Bypass Disabled**
SCS#	I	SCS#		SCS#	
SCLK	I	SCLK		SCLK	
SA0	I	SA0		SA0	
SI	I	SI		SI	
FPFRAME	O	RGB	RGB	XWR	XWR
FPLINE	O	RGB	RGB	A0	A0
FPSHIFT	O	RGB	RGB	—	—
DRDY	O	RGB	RGB	—	—
FPDAT0	O	RGB	RGB	D0	D0
FPDAT1	O	RGB	RGB	D1	D1
FPDAT2	O	RGB	RGB	D2	D2
FPDAT3	O	RGB	RGB	D3	D3
FPDAT4	O	RGB	RGB	D4	D4
FPDAT5	O	RGB	RGB	D5	D5
FPDAT6	O	RGB	RGB	D6	D6
FPDAT7	O	RGB	RGB	D7	D7
FPDAT8	O	RGB	RGB	D8	D8
FPDAT9	O	RGB	RGB	D9	D9
FPDAT10	O	RGB	RGB	D10	D10
FPDAT11	O	RGB	RGB	D11	D11
FPDAT12	O	RGB	RGB	D12	D12
FPDAT13	O	RGB	RGB	D13	D13
FPDAT14	O	RGB	RGB	D14	D14
FPDAT15	O	RGB	RGB	D15	D15
FPDAT16	O	RGB	RGB	D16	D16
FPDAT17	O	RGB	RGB	D17	D17
FPCS1#	O	RGB	RGB	NCS1	NCS1
FPCS2#	O	NCS2	NCS2	NCS2	NCS2
FPSCLK	O	RGB or SCK	RGB	SCK	SCK
FPA0	O	RGB or A0	RGB	A0	A0
FPSO	O	RGB or SI	RGB	SI	SI
FPVIN1	I	RGB	RGB	VIN1	VIN1
FPVIN2	I	VIN2	VIN2	VIN2	VIN2

	Input port when bypass is used
	Output port when bypass is used
	When bypass is not used, pull-up/pull-down resistors can be set using REG[0014h] bit 4

1. RGB refers to the signals used for RGB panels.

Table 5-15: LCD Interface Mode 1/2 Bypass Endian/Data Width Pin Mapping

Panel Mode	**LCD I/F Mode 1**		**LCD I/F Mode 2**	
Serial Bypass Enabled (REG[0032h] bit 8)	**1**		**1**	
Input/Output	**Input**	**Output**	**Input**	**Output**
Pin Mapping	SCS#	FPCS2#	SCS#	FPCS2#
	SCLK	FPSCLK	SCLK	FPSCLK
	SA0	FPA0	SA0	FPA0
	SI	FPSO	SI	FPSO

5.6 Camera Interface Pin Mapping

Table 5-16: Camera Interface Pin Mapping

Pin Name	Type 1 Camera
CMDAT[7:0]	CAMDAT[7:0]
CMVREF	VREF
CMHREF	HREF
CMCLKOUT	CAMMCLK
CMCLKIN	CAMPCLK

6 D.C. Characteristics

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Core Supply Voltage	V_{SS} - 0.3 ~ 2.5	V
PLL V_{DD}	PLL Supply Voltage	V_{SS} - 0.3 ~ 2.1	V
HIO V_{DD}	Host IO Supply Voltage	Core V_{DD} ~ 4.0	V
PIO V_{DD}	Non-Host IO Supply Voltage	Core V_{DD} ~ 4.0	V
CIO V_{DD}	Camera IO Supply Voltage	Core V_{DD} ~ 4.0	V
SIO V_{DD}	SD Card IO Supply Voltage	Core V_{DD} ~ 4.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 ~ IO V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 ~ IO V_{DD} + 0.5	V

Table 6-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Core Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
PLL V_{DD}	PLL Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
HIO V_{DD}	Host IO Supply Voltage	V_{SS} = 0 V	2.75	3.00	3.25	V
PIO V_{DD}	Non-Host IO Supply Voltage	V_{SS} = 0 V	2.75	3.00	3.25	V
CIO V_{DD}	Camera IO Supply Voltage	V_{SS} = 0 V	2.75	3.00	3.25	V
SIO V_{DD}	SD Card IO Supply Voltage	V_{SS} = 0 V	2.75	3.00	3.25	V
V_{IN}	Input Voltage		V_{SS}		HIO V_{DD}	V
			V_{SS}		PIO V_{DD}	
			V_{SS}		CIO V_{DD}	
			V_{SS}		SIO V_{DD}	
T_{OPR}	Operating Temperature	—	-20	25	70	°C

Table 6-3: Electrical Characteristics for VDD = 3.0V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDSH}	IO Quiescent Current	Quiescent Conditions		10		µA
I_{DDSL}	CORE Quiescent Current	Quiescent Conditions		10		µA
I_{IZ}	Input Leakage Current		-5		5	µA
I_{OZ}	Output Leakage Current		-5		5	µA
$HIOV_{OH}$	High Level Output Voltage	HIOVDD = min I_{OH} = -3.6mA	$HIOV_{DD}$ - 0.4			V
$CIOV_{OH}$	High Level Output Voltage	CIOVDD = min I_{OH} = -3.6mA	$CIOV_{DD}$ - 0.4			V
$PIOV_{OH}$	High Level Output Voltage	PIOVDD = min I_{OH} = -3.6mA	$PIOV_{DD}$ - 0.4			V
$SIOV_{OH}$	High Level Output Voltage	SIOVDD = min I_{OH} = -3.6mA	$SIOV_{DD}$ - 0.4			V
$HIOV_{OL}$	Low Level Output Voltage	HIOVDD = min I_{OL} = 3.6mA			0.4	V
$CIOV_{OL}$	Low Level Output Voltage	CIOVDD = min I_{OL} = 3.6mA			0.4	V
$PIOV_{OL}$	Low Level Output Voltage	PIOVDD = min I_{OL} = 3.6mA			0.4	V
$SIOV_{OL}$	Low Level Output Voltage	SIOVDD = min I_{OL} = 3.6mA			0.4	V
$HIOV_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.95			V
$CIOV_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.95			V
$PIOV_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.95			V
$SIOV_{IH}$	High Level Input Voltage	LVCMOS Level, V_{DD} = max	1.95			V
$HIOV_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.85	V
$CIOV_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.85	V
$PIOV_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.85	V
$SIOV_{IL}$	Low Level Input Voltage	LVCMOS Level, V_{DD} = min			0.85	V
$HIOV_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	1.35		2.5	V
$CIOV_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	1.35		2.5	V
$PIOV_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	1.35		2.5	V
$SIOV_{T+}$	Positive Trigger Voltage	LVCMOS Schmitt	1.35		2.5	V
$HIOV_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.7		1.6	V
$CIOV_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.7		1.6	V
$PIOV_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.7		1.6	V
$SIOV_{T-}$	Negative Trigger Voltage	LVCMOS Schmitt	0.7		1.6	V
R_{PD}	Pull Down Resistance	$V_{IN} = V_{DD}$	30	60	144	kΩ
R_{PU}	Pull Up Resistance	$V_{IN} = V_{DD}$	30	60	144	kΩ
C_I	Input Pin Capacitance	f = 1MHz, V_{DD} = 0V	-	-	8	pF
C_O	Output Pin Capacitance	f = 1MHz, V_{DD} = 0V	-	-	8	pF
C_{IO}	Bi-Directional Pin Capacitance	f = 1MHz, V_{DD} = 0V	-	-	8	pF

7 A.C. Characteristics

Conditions: IO V_{DD} = 3.0V ± 0.25V
T_A = -40° C to 85° C
T_{rise} and T_{fall} for all inputs except CLKI must be ≤ 50 ns (10% ~ 90%)
C_L = 15pF (Host Interface)
C_L = 15pF (Camera Interface)
C_L = 30pF (LCD Panel/GPIO Interface)
C_L = 50pF (SD Card Interface)

7.1 Clock Timing

7.1.1 Input Clocks

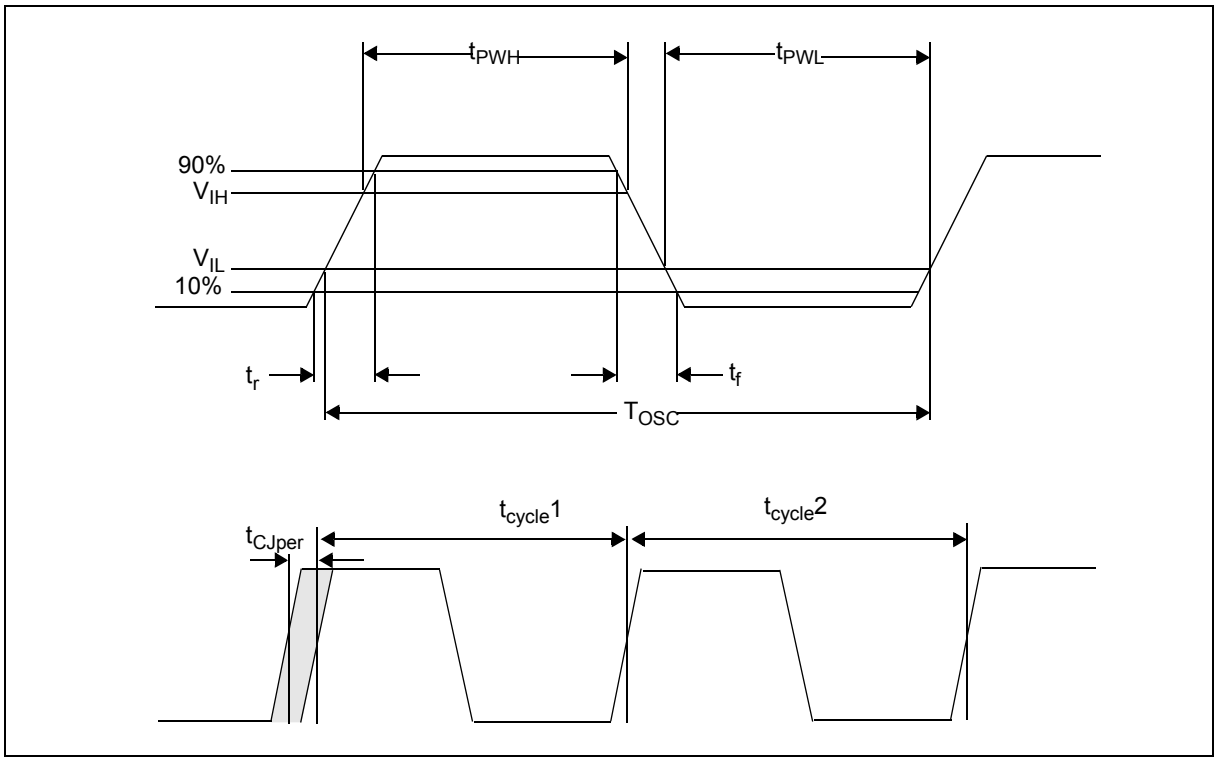


Figure 7-1: Clock Input Requirements (PLL)

Table 7-1: Clock Input Requirements (PLL)

Symbol	Parameter	Min	Typ	Max	Units
f_{OSC}	Input clock frequency	30	32.768	64	KHz
T_{OSC}	Input clock period		$1/f_{OSC}$		us
t_{PWH}	Input clock pulse width high	5			us
t_{PWL}	Input clock pulse width low	5			us
t_r	Input clock rising time (10% - 90%)			5	us
t_f	Input clock falling time (10% - 90%)			5	us
t_{CJper}	Input clock period jitter (see notes 2 and 4)	-100		100	ns
$t_{CJcycle}$ (see note 1)	Input clock cycle jitter (see notes 3 and 4)	-100		100	ns

1. $t_{CJcycle} = t_{cycle}1 - t_{cycle}2$
2. The input clock period jitter is the displacement relative to the center period (reciprocal of the center frequency).
3. The input clock cycle jitter is the difference in period between adjacent cycles.
4. The jitter characteristics must satisfy both the t_{CJper} and $t_{CJcycle}$ characteristics.

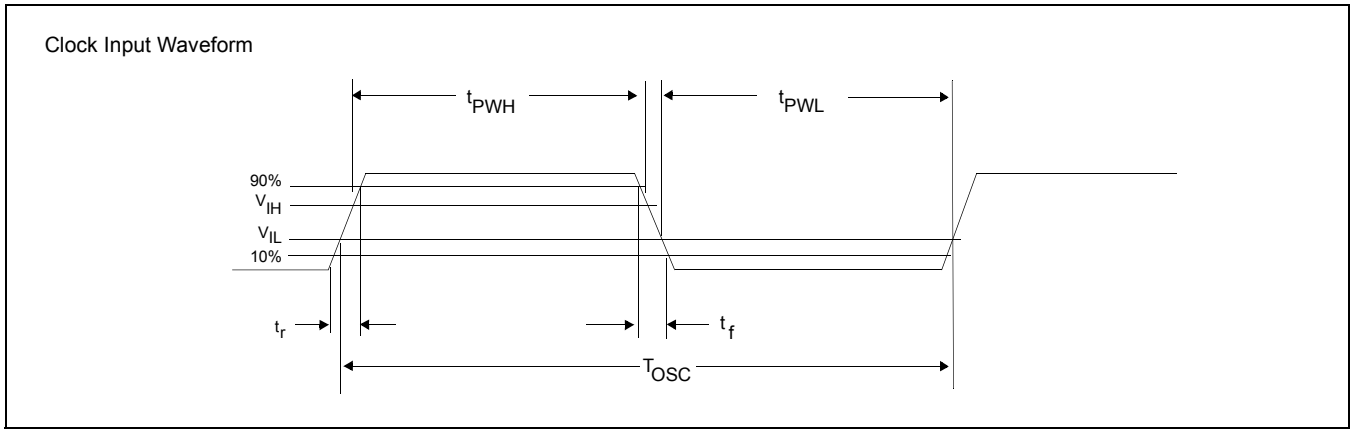


Figure 7-2: Clock Input Requirements (PLL bypassed)

Table 7-2: Clock Input Requirements (PLL bypassed)

Symbol	Parameter	Min	Max	Units
f_{OSC}	Input Clock Frequency (CLKI)		55	MHz
T_{OSC}	Input Clock period (CLKI)	$1/f_{OSC}$		ns
t_{PWH}	Input Clock Pulse Width High (CLKI)	$0.4T_{OSC}$		ns
t_{PWL}	Input Clock Pulse Width Low (CLKI)	$0.4T_{OSC}$		ns
t_r	Input clock rising time (10% - 90%)		5	ns
t_f	Input clock falling time (10% - 90%)		5	ns

7.1.2 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

For example, if noise with a 2KHz frequency modulation is added on PLLVDD, the jitter on the PLL clock output may fluctuate. Measures must be taken to avoid noise within the range of 1KHz to 3KHz.

The specific design should be confirmed to determine the jitter value of a clock. This is because the actual jitter characteristics are affected by a combination of factors, such as the jitter frequency spectrum of CLKI, and amplitude and frequency of the noise on the supplied power. If the jitter of a clock exceeds the requirement of a module, an external oscillator should be used instead of using the internal PLL circuitry.

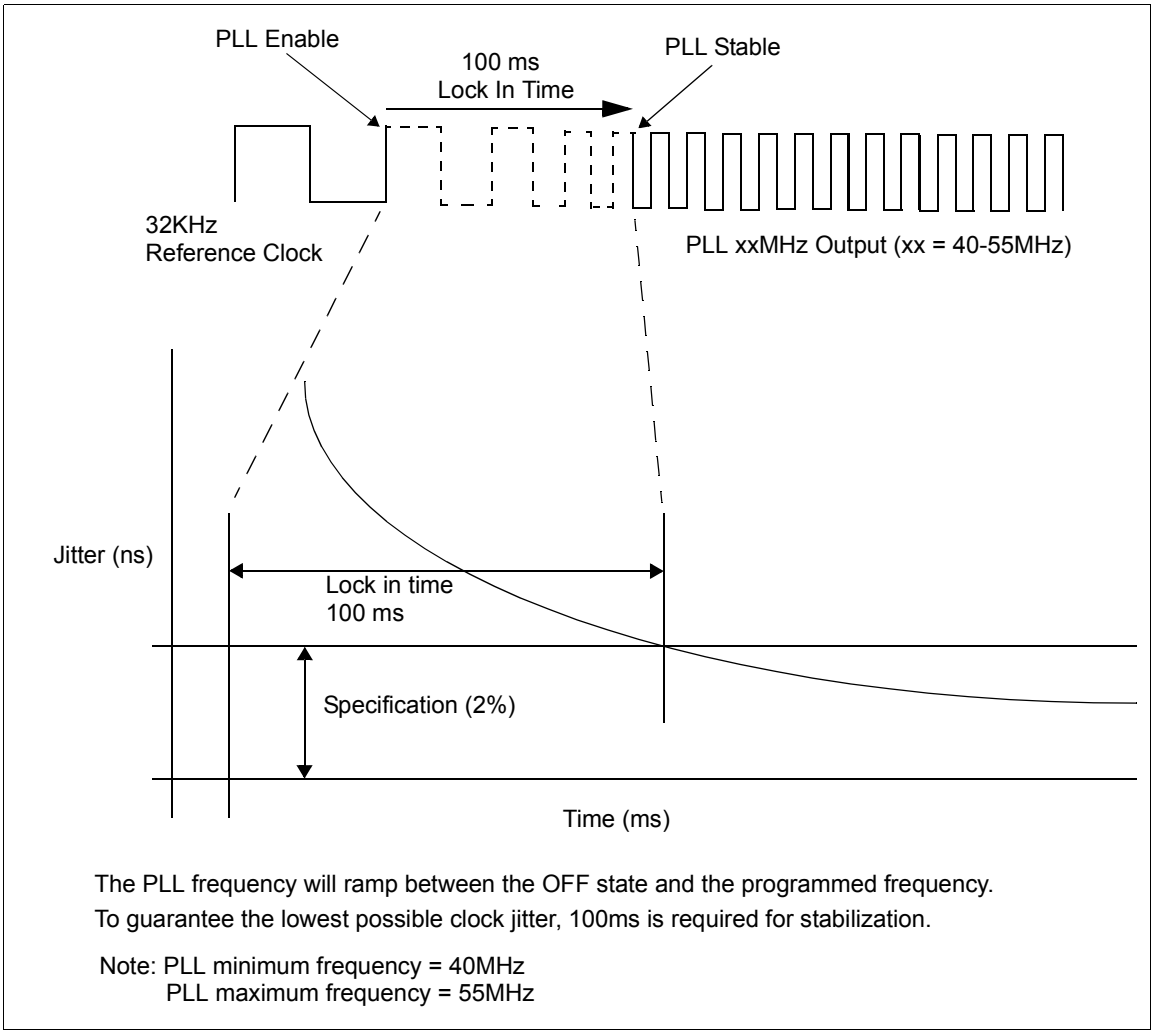


Figure 7-3: PLL Start-Up Time

7.1.3 Internal Clocks

Table 7-3: Internal Clock Requirements

Symbol	Parameter	Min	Max	Units
f_{SYS}	Internal Clock Frequency (System Clock)		55	MHz

7.2 Power Supply Sequence

7.2.1 Power-On Sequence

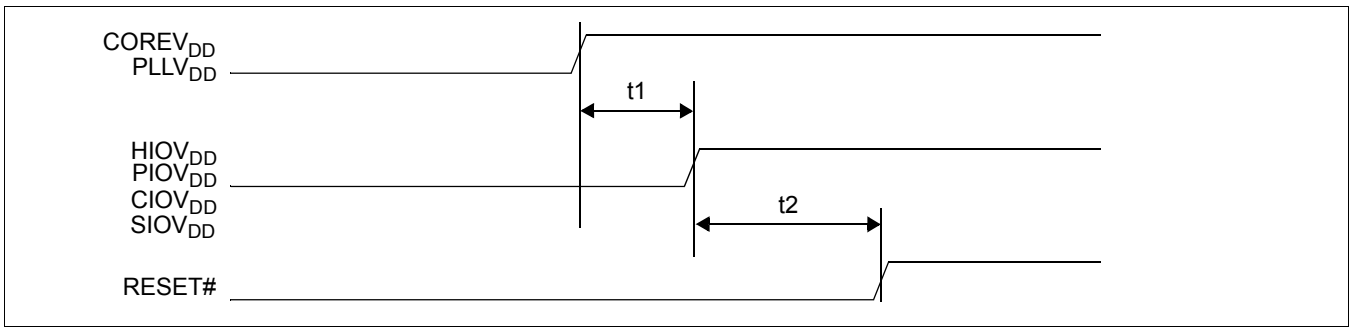


Figure 7-4: Power-On Sequence

Table 7-4: Power-On Sequence

Symbol	Parameter	Min	Max	Units
t1	IOV$_{DD}$ on delay from COREV$_{DD}$ / PLLV$_{DD}$ on	0		ns
t2	RESET# width period	1		CLKI

7.2.2 Power-Off Sequence

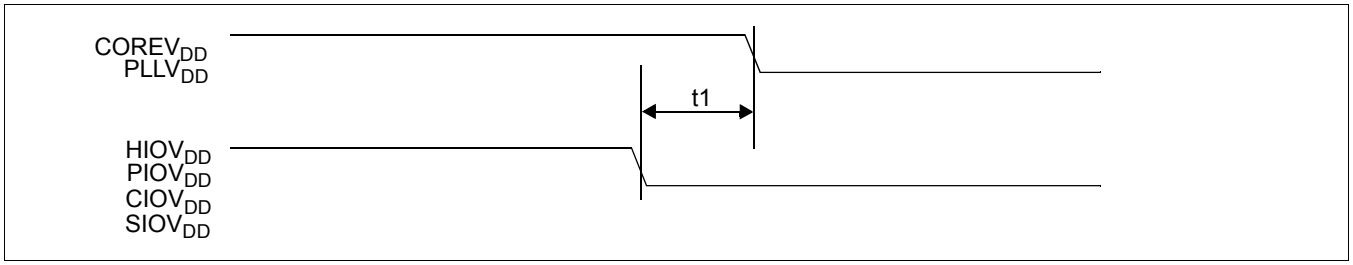


Figure 7-5: Power-Off Sequence

Table 7-5: Power-Off Sequence

Symbol	Parameter	Min	Max	Units
t1	COREV$_{DD}$ / PLLV$_{DD}$ off delay from IOV$_{DD}$ off	0		ns

7.3 Host Interface Timing

7.3.1 Direct 80 Type 1

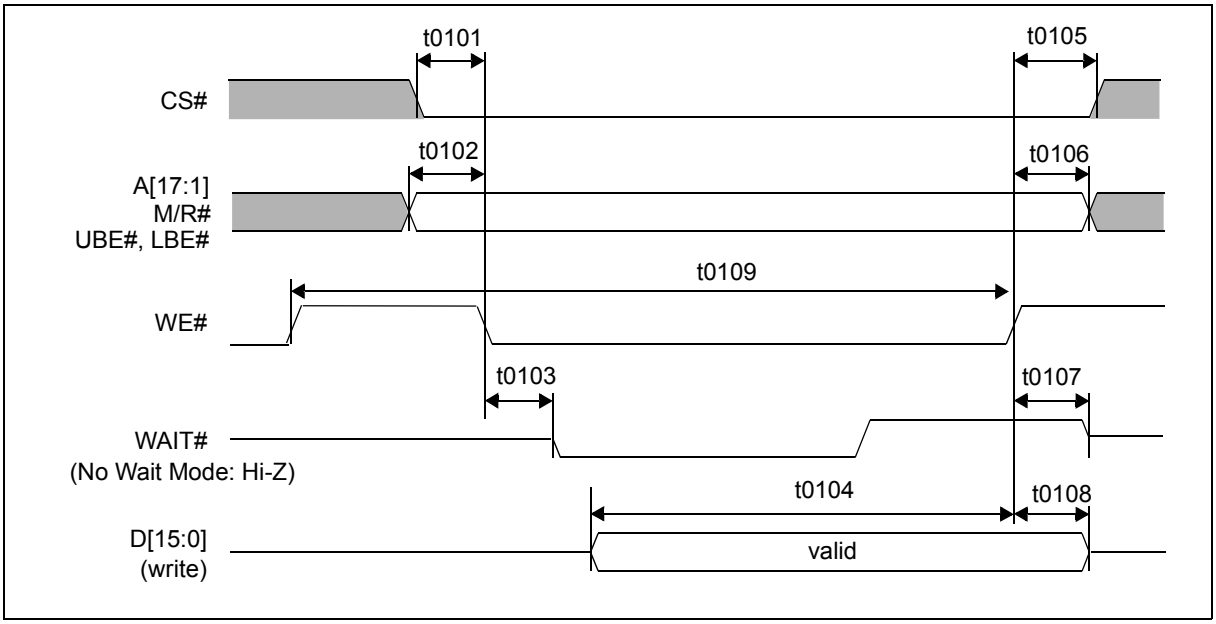


Figure 7-6: Direct 80 Type 1 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-6: Direct 80 Type 1 Interface Write Cycle Timing (Wait/No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0101	CS# setup time	15		ns
t0102	A[17:1], M/R#, UBE#, LBE# setup time	15		ns
t0103	WE# falling edge to WAIT# driven low		10	ns
t0104	D[15:0] setup time to WE# rising edge	10		ns
t0105	CS# hold time from WE# rising edge	5		ns
t0106	A[17:1], M/R#, UBE#, LBE# hold time from WE# rising edge	5		ns
t0107	WE# rising edge to WAIT# high impedance		7	ns
t0108	D[15:0] hold time from WE# rising edge	2		ns
t0109	Cycle time (No wait mode only)	Note2,3		Ts

1. Ts = System clock period.
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
3. t0109min = WAIT Length + 3 Ts.

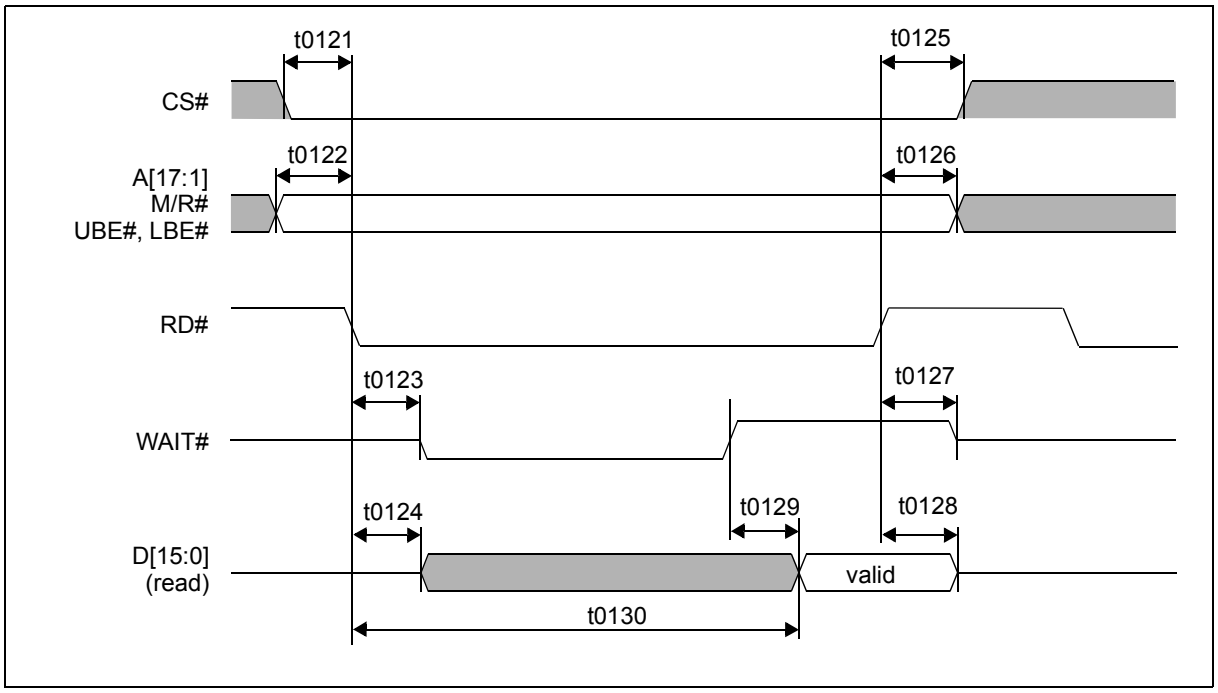


Figure 7-7: Direct 80 Type 1 Interface Read Cycle Timing (Wait Mode)

Table 7-7: Direct 80 Type 1 Interface Read Cycle Timing (Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0121	CS# setup time	15		ns
t0122	A[17:1], M/R#, UBE#, LBE# setup time	15		ns
t0123	RD# falling edge to WAIT# driven low		10	ns
t0124	RD# falling edge to D[15:0] driven	4		ns
t0125	CS# hold time from RD# rising edge	2		ns
t0126	A[17:1], M/R#, UBE#, LBE# hold time from RD# rising edge	2		ns
t0127	RD# rising edge to WAIT# high impedance		7	ns
t0128	D[15:0] hold time from RD# rising edge.	2	8	ns
t0129	WAIT# rising edge to valid Data if WAIT# is asserted		10	ns
t0130	RD# falling edge to valid Data if WAIT# is NOT asserted		17	ns

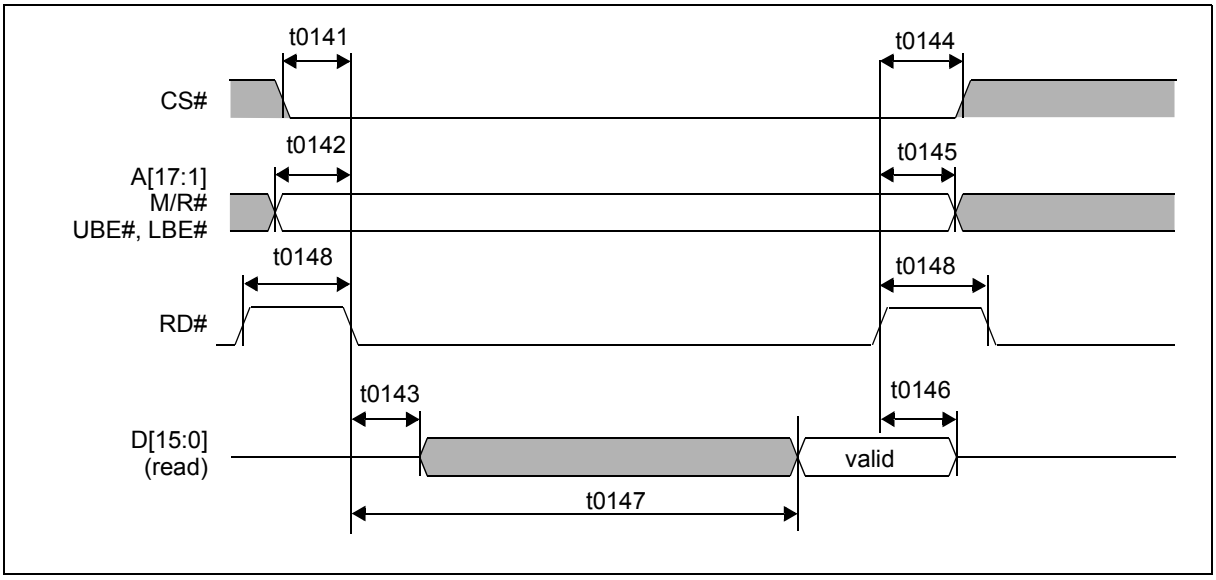


Figure 7-8: Direct 80 Type 1 Interface Read Cycle Timing (No Wait Mode)

Table 7-8: Direct 80 Type 1 Interface Read Cycle Timing (No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0141	CS# setup time	0		ns
t0142	A[17:1], M/R#, UBE#, LBE# setup time	0		ns
t0143	RD# falling edge to D[15:0] driven	4		ns
t0144	CS# hold time from RD# rising edge	0		ns
t0145	A[17:1], M/R#, UBE#, LBE# hold time from RD# rising edge	0		ns
t0146	D[15:0] hold time from RD# rising edge	2	8	ns
t0147	RD# falling edge to valid Data if there are no internal delayed cycles		Note1,2	ns
t0148	RD# pulse width high	10		ns

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
2. t0147max = WAIT Length + 29 ns

Table 7-9: Direct 80 Type 1 Host Interface Truth Table for Little Endian

WE#	RD#	UBE#	LBE#	D[15:8]	D[7:0]	Comments
0	1	0	0	valid	valid	16-bit write
0	1	1	0	-	valid	8-bit write; data on low byte (even byte address[1])
0	1	0	1	valid	-	8-bit write; data on high byte (odd byte address[1])
1	0	0	0	valid	valid	16-bit read
1	0	1	0	-	valid	8-bit read; data on low byte (even byte address[1])
1	0	0	1	valid	-	8-bit read; data on high byte (odd byte address[1])

Table 7-10: Direct 80 Type 1 Host Interface Truth Table for Big Endian

WE#	RD#	UBE#	LBE#	D[15:8]	D[7:0]	Comments
0	1	0	0	valid	valid	16-bit write
0	1	1	0	-	valid	8-bit write; data on low byte (odd byte address[1])
0	1	0	1	valid	-	8-bit write; data on high byte (even byte address[1])
1	0	0	0	valid	valid	16-bit read
1	0	1	0	-	valid	8-bit read; data on low byte (odd byte address[1])
1	0	0	1	valid	-	8-bit read; data on high byte (even byte address[1])

1. Because A0 is not used, all addresses are seen by the S1D13717 as even addresses (16-bit word address aligned on even byte addresses).

7.3.2 Direct 80 Type 2

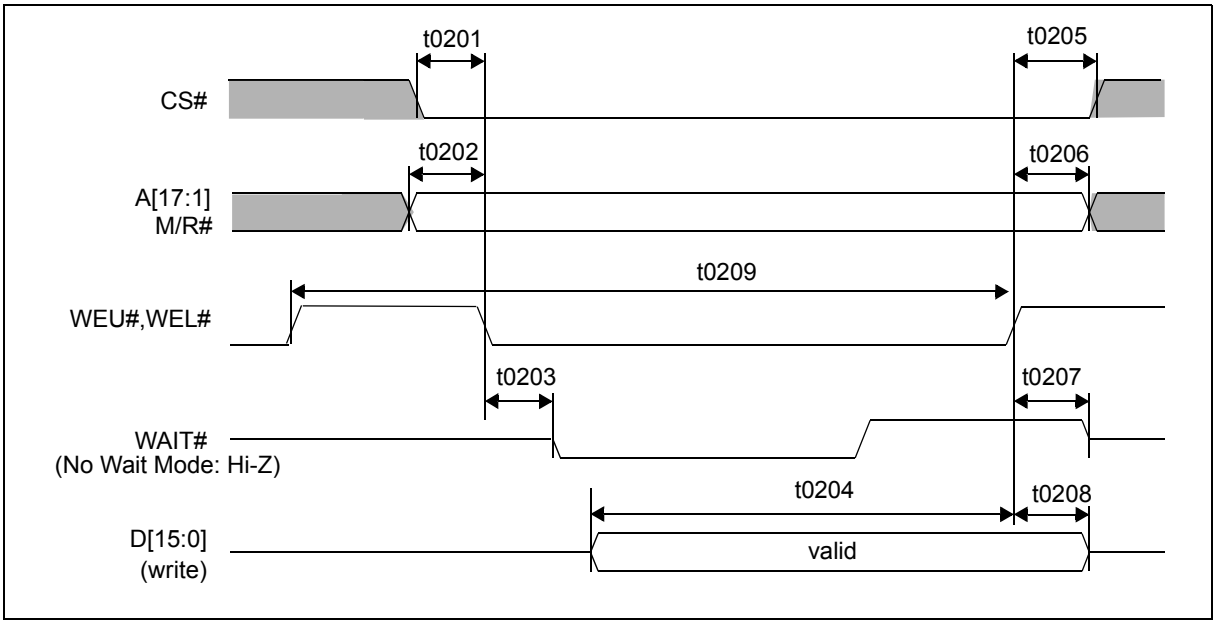


Figure 7-9: Direct 80 Type 2 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-11: Direct 80 Type 2 Interface Write Cycle Timing (Wait/No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0201	CS# setup time	15		ns
t0202	A[17:1], M/R# setup time	15		ns
t0203	WEU#,WEL# falling edge to WAIT# driven low		10	ns
t0204	D[15:0] setup time to WEU#,WEL# rising edge	10		ns
t0205	CS# hold time from WEU#,WEL# rising edge	5		ns
t0206	A[17:1], M/R# hold time from WEU#,WEL# rising edge	5		ns
t0207	WEU#,WEL# rising edge to WAIT# high impedance		7	ns
t0208	D[15:0] hold time from WEU#,WEL# rising edge	2		ns
t0209	Cycle time (No wait mode only)	Note2,3		Ts

1. Ts = System clock period.
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
3. t0209min = WAIT Length + 3 Ts

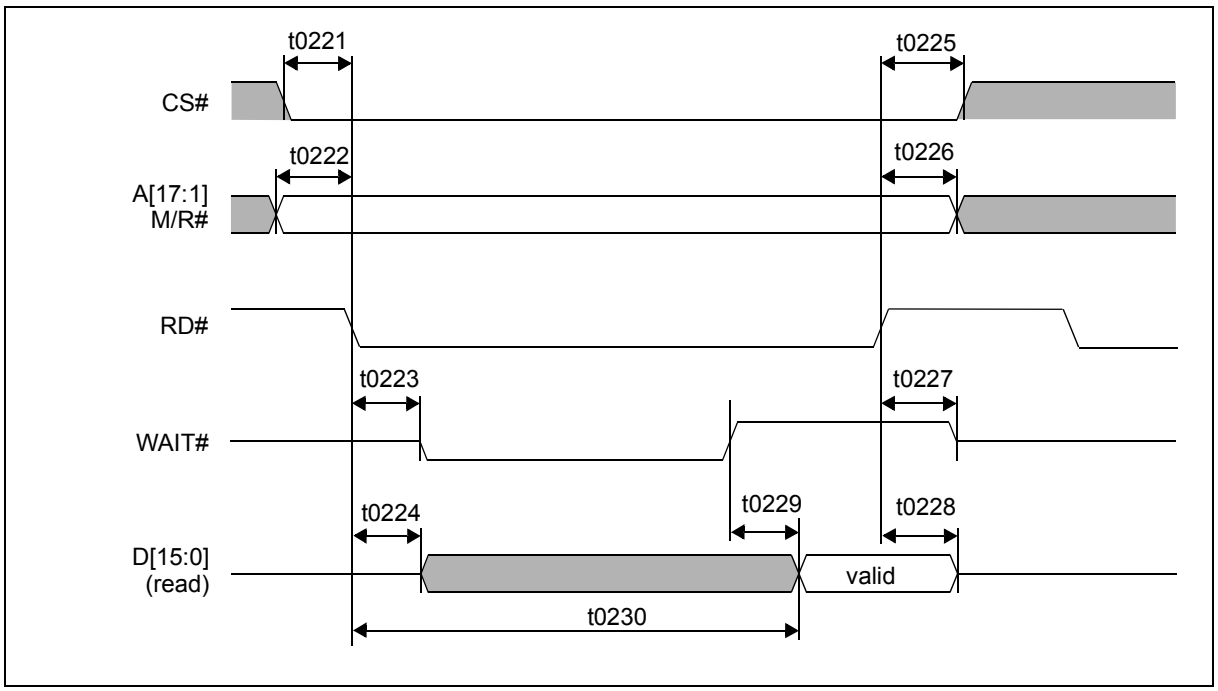


Figure 7-10: Direct 80 Type 2 Interface Read Cycle Timing (Wait Mode)

Table 7-12: Direct 80 Type 2 Interface Read Cycle Timing (Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0221	CS# setup time	15		ns
t0222	A[17:1], M/R# setup time	15		ns
t0223	RD# falling edge to WAIT# driven low		10	ns
t0224	RD# falling edge to D[15:0] driven	4		ns
t0225	CS# hold time from RD# rising edge	2		ns
t0226	A[17:1], M/R# hold time from RD# rising edge	2		ns
t0227	RD# rising edge to WAIT# high impedance		7	ns
t0228	D[15:0] hold time from RD# rising edge.	2	8	ns
t0229	WAIT# rising edge to valid Data if WAIT# is asserted		10	ns
t0230	RD# falling edge to valid Data if WAIT# is NOT asserted		17	ns

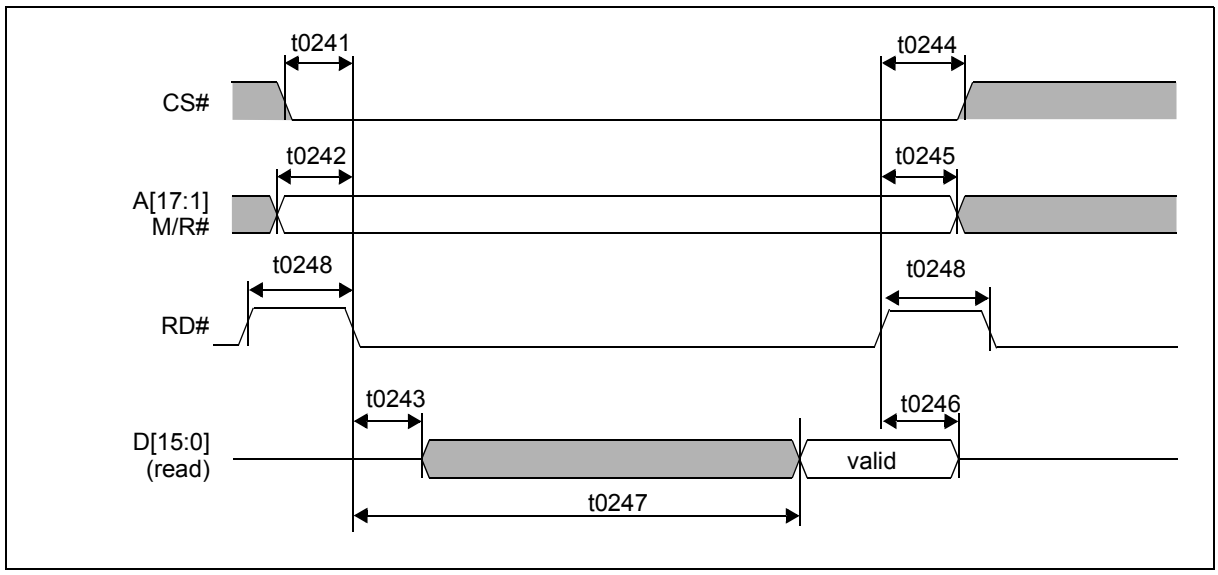


Figure 7-11: Direct 80 Type 2 Interface Read Cycle Timing (No Wait Mode)

Table 7-13: Direct 80 Type 2 Interface Read Cycle Timing (No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0241	CS# setup time	0		ns
t0242	A[17:1], M/R# setup time	0		ns
t0243	RD# falling edge to D[15:0] driven	4		ns
t0244	CS# hold time from RD# rising edge	0		ns
t0245	A[17:1], M/R# hold time from RD# rising edge	0		ns
t0246	D[15:0] hold time from RD# rising edge	2	8	ns
t0247	RD# falling edge to valid Data if there are no internal delayed cycles		Note1,2	ns
t0248	RD# pulse width high	10		ns

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
2. t0247max = WAIT Length + 29 ns

Table 7-14: Direct 80 Type 2 Host Interface Truth Table for Little Endian

RD#	WEU#	WEL#	D[15:8]	D[7:0]	Comments
1	0	0	valid	valid	16-bit write
1	1	0	-	valid	8-bit write; data on low byte (even byte address[1])
1	0	1	valid	-	8-bit write; data on high byte (odd byte address[1])
0	1	1	valid	valid	16-bit read

1. Because A0 is not used, all addresses are seen by the S1D13717 as even addresses (16-bit word address aligned on even byte addresses).

7.3.3 Direct 80 Type 3

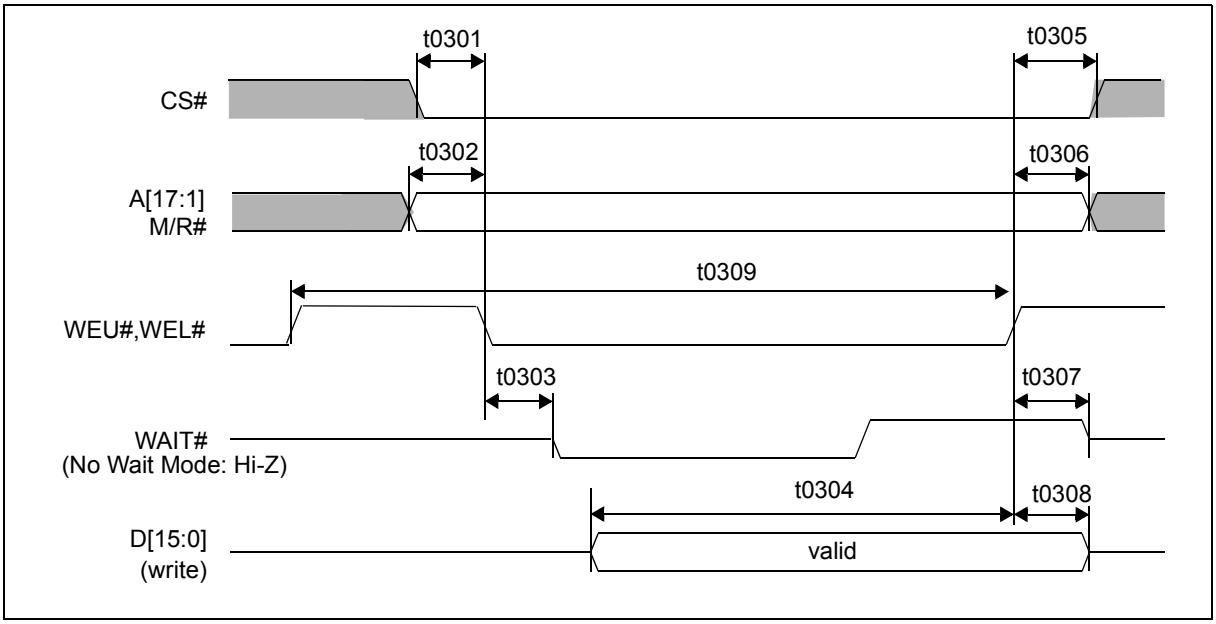


Figure 7-12: Direct 80 Type 3 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-15: Direct 80 Type 3 Interface Write Cycle Timing (Wait/No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0301	CS# setup time	15		ns
t0302	A[17:1], M/R# setup time	15		ns
t0303	WEU#,WEL# falling edge to WAIT# driven low		10	ns
t0304	D[15:0] setup time to WEU#,WEL# rising edge	10		ns
t0305	CS# hold time from WEU#,WEL# rising edge	5		ns
t0306	A[17:1], M/R# hold time from WEU#,WEL# rising edge	5		ns
t0307	WEU#,WEL# rising edge to WAIT# high impedance		7	ns
t0308	D[15:0] hold time from WEU#,WEL# rising edge	2		ns
t0309	Cycle time (No wait mode only)	Note2,3		Ts

1. Ts = System clock period.
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
3. t0309min = WAIT Length + 3 Ts

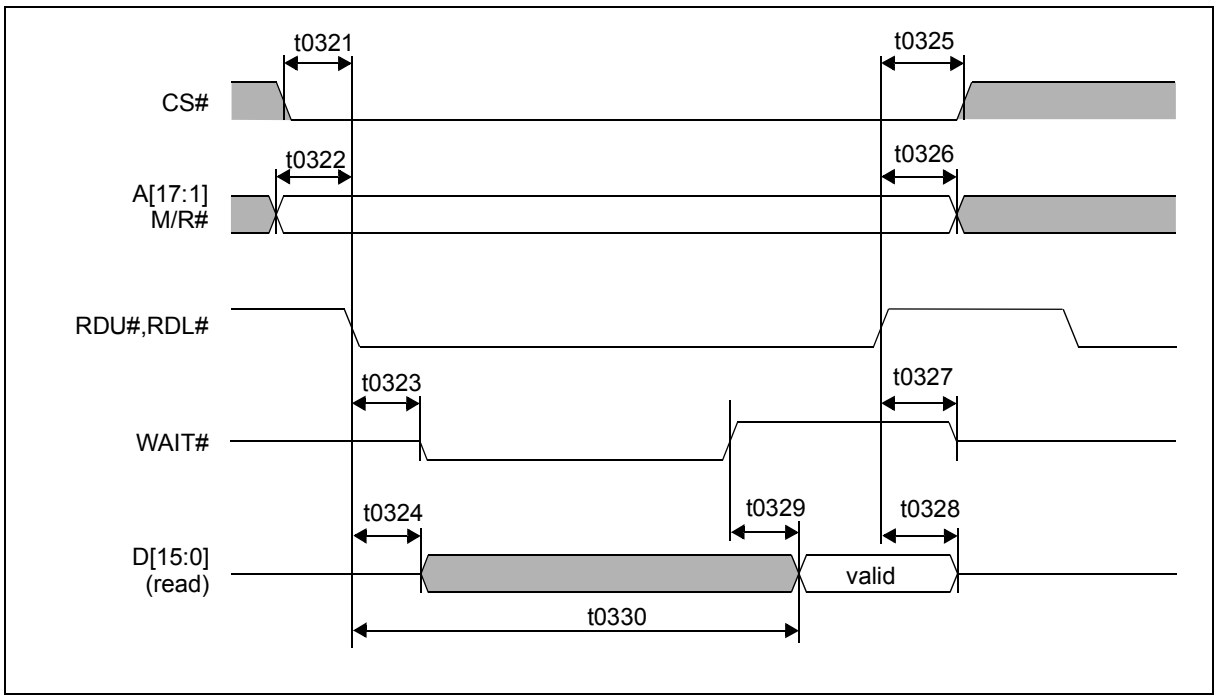


Figure 7-13: Direct 80 Type 3 Interface Read Cycle Timing (Wait Mode)

Table 7-16: Direct 80 Type 3 Interface Read Cycle Timing (Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0321	CS# setup time	15		ns
t0322	A[17:1], M/R# setup time	15		ns
t0323	RDU#,RDL# falling edge to WAIT# driven low		10	ns
t0324	RDU#,RDL# falling edge to D[15:0] driven	4		ns
t0325	CS# hold time from RDU#,RDL# rising edge	2		ns
t0326	A[17:1], M/R# hold time from RDU#,RDL# rising edge	2		ns
t0327	RDU#,RDL# rising edge to WAIT# high impedance		7	ns
t0328	D[15:0] hold time from RDU#,RDL# rising edge.	2	8	ns
t0329	WAIT# rising edge to valid Data if WAIT# is asserted		10	ns
t0330	RDU#,RDL# falling edge to valid Data if WAIT# is NOT asserted		17	ns

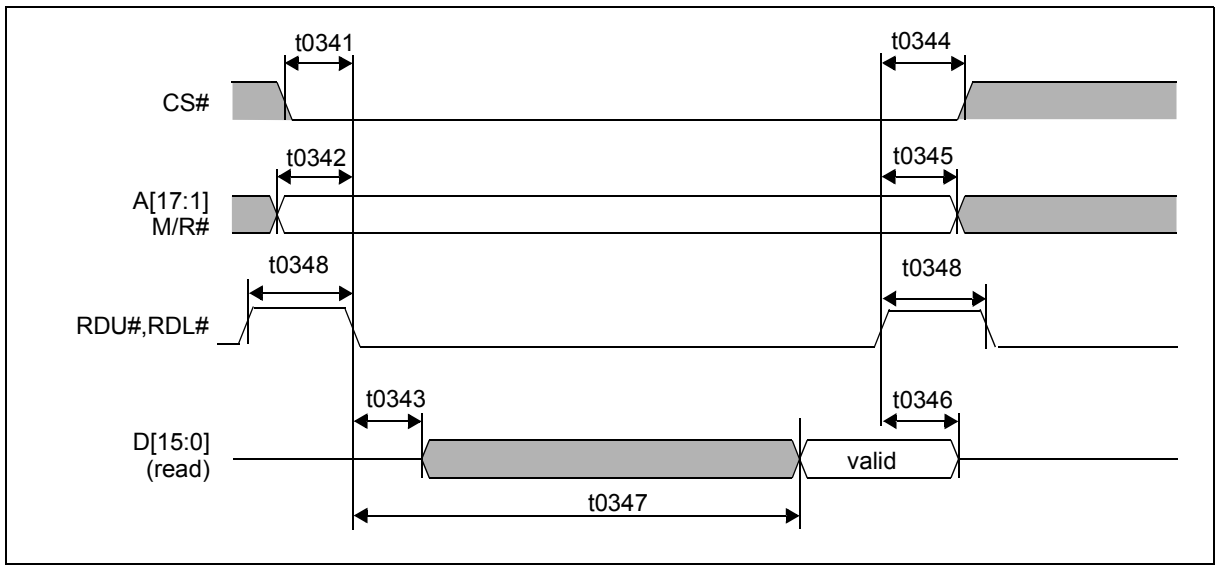


Figure 7-14: Direct 80 Type 3 Interface Read Cycle Timing (No Wait Mode)

Table 7-17: Direct 80 Type 3 Interface Read Cycle Timing (No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0341	CS# setup time	0		ns
t0342	A[17:1], M/R# setup time	0		ns
t0343	RDU#,RDL# falling edge to D[15:0] driven	4		ns
t0344	CS# hold time from RDU#,RDL# rising edge	0		ns
t0345	A[17:1], M/R# hold time from RDU#,RDL# rising edge	0		ns
t0346	D[15:0] hold time from RDU#,RDL# rising edge	2	8	ns
t0347	RDU#,RDL# falling edge to valid Data if there are no internal delayed cycles		Note1,2	ns
t0348	RDU#, RDL# pulse width high	10		ns

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
2. t0347max = WAIT Length + 29 ns

Table 7-18: Direct 80 Type 3 Host Interface Truth Table for Little Endian

WEU#	WEL#	RDU#	RDL#	D[15:8]	D[7:0]	Comments
0	0	1	1	valid	valid	16-bit write
1	0	1	1	-	valid	8-bit write; data on low byte (even byte address[1])
0	1	1	1	valid	-	8-bit write; data on high byte (odd byte address[1])
1	1	0	0	valid	valid	16-bit read
1	1	1	0	-	valid	8-bit read; data on low byte (even byte address[1])
1	1	0	1	valid	-	8-bit read; data on high byte (odd byte address[1])

Table 7-19: Direct 80 Type 3 Host Interface Truth Table for Big Endian

WEU#	WEL#	RDU#	RDL#	D[15:8]	D[7:0]	Comments
0	0	1	1	valid	valid	16-bit write
1	0	1	1	-	valid	8-bit write; data on low byte (odd byte address[1])
0	1	1	1	valid	-	8-bit write; data on high byte (even byte address[1])
1	1	0	0	valid	valid	16-bit read
1	1	1	0	-	valid	8-bit read; data on low byte (odd byte address[1])
1	1	0	1	valid	-	8-bit read; data on high byte (even byte address[1])

1. Because A0 is not used, all addresses are seen by the S1D13717 as even addresses (16-bit word address aligned on even byte addresses).

7.3.4 Direct 68

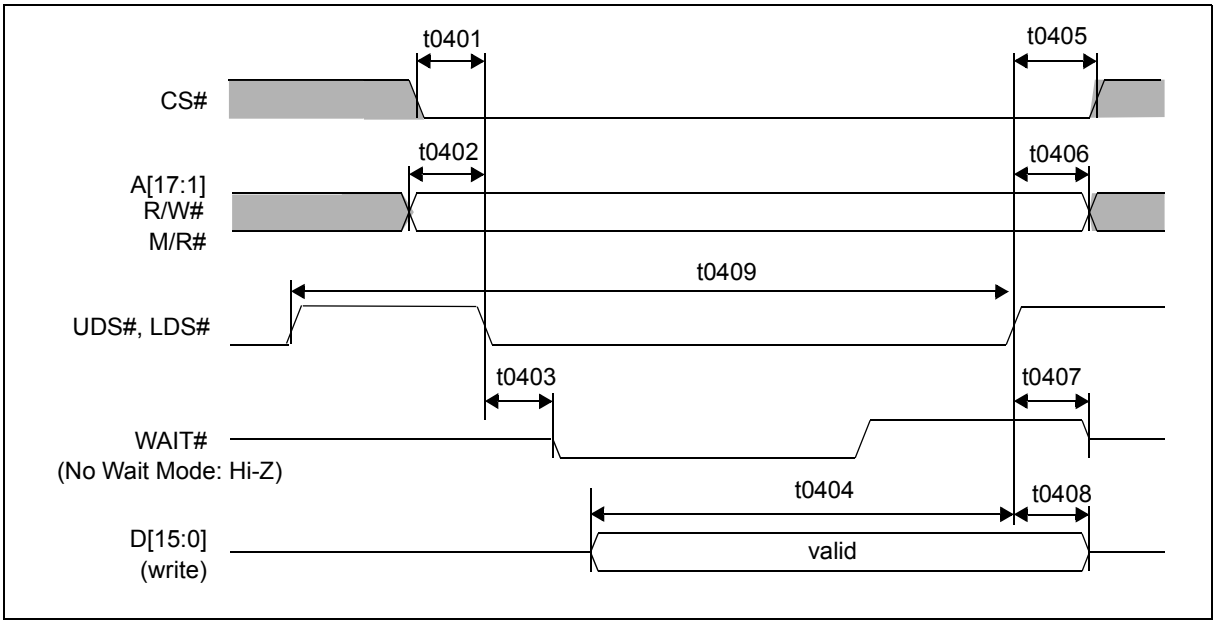


Figure 7-15: Direct 68 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-20: Direct 68 Interface Write Cycle Timing (Wait/No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0401	CS# setup time	15		ns
t0402	A[17:1], R/W#, M/R# setup time	15		ns
t0403	UDS#, LDS# falling edge to WAIT# driven low		10	ns
t0404	D[15:0] setup time to UDS#, LDS# rising edge	10		ns
t0405	CS# hold time from UDS#, LDS# rising edge	5		ns
t0406	A[17:1], R/W#, M/R# hold time from UDS#, LDS# rising edge	5		ns
t0407	UDS#, LDS# rising edge to WAIT# high impedance		7	ns
t0408	D[15:0] hold time from UDS#, LDS# rising edge	2		ns
t0409	Cycle time (No wait mode only)	Note2,3		Ts

1. Ts = System clock period
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
3. t0409min = WAIT Length + 3 Ts

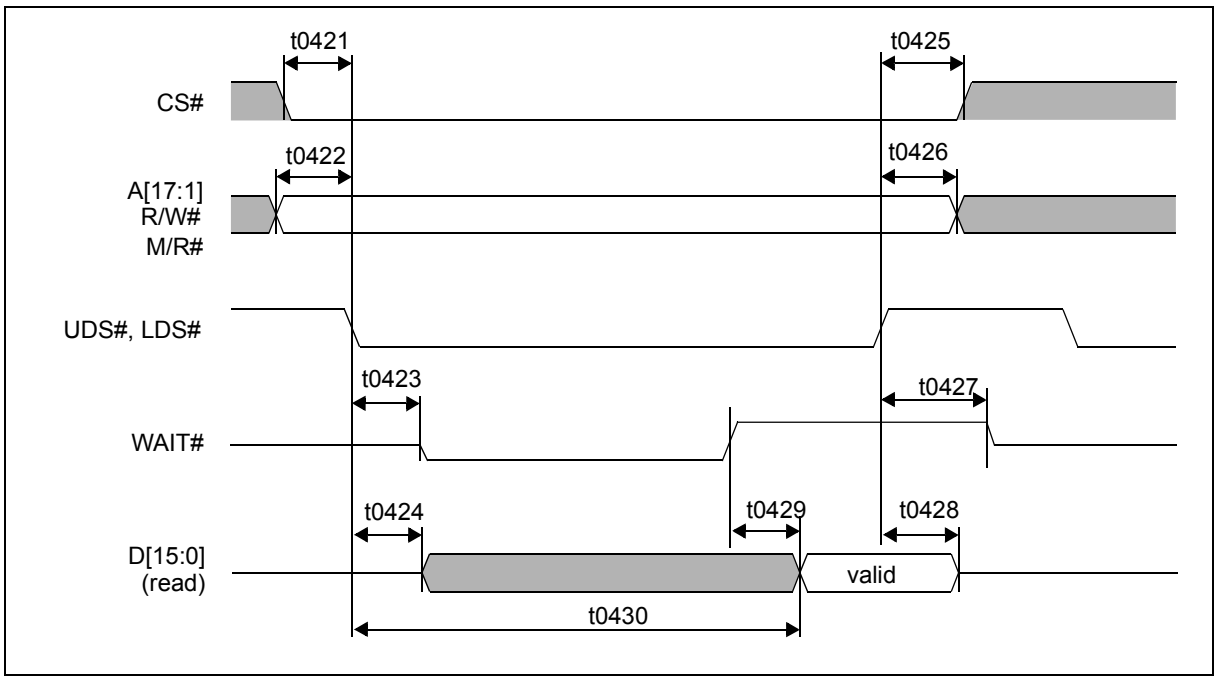


Figure 7-16: Direct 68 Interface Read Cycle Timing (Wait Mode)

Table 7-21: Direct 68 Interface Read Cycle Timing (Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0421	CS# setup time	15		ns
t0422	A[17:1], R/W#, M/R# setup time	15		ns
t0423	UDS#, LDS# falling edge to WAIT# driven low		10	ns
t0424	UDS#, LDS# falling edge to D[15:0] driven	4		ns
t0425	CS# hold time from UDS#, LDS# rising edge	2		ns
t0426	A[17:1], R/W#, M/R# hold time from UDS#, LDS# rising edge	2		ns
t0427	UDS#, LDS# rising edge to WAIT# high impedance		7	ns
t0428	D[15:0] hold time from UDS#, LDS# rising edge	2	8	ns
t0429	WAIT# rising edge to valid Data if WAIT# is asserted		10	ns
t0430	UDS#, LDS# falling edge to valid Data if WAIT# is NOT asserted		17	ns

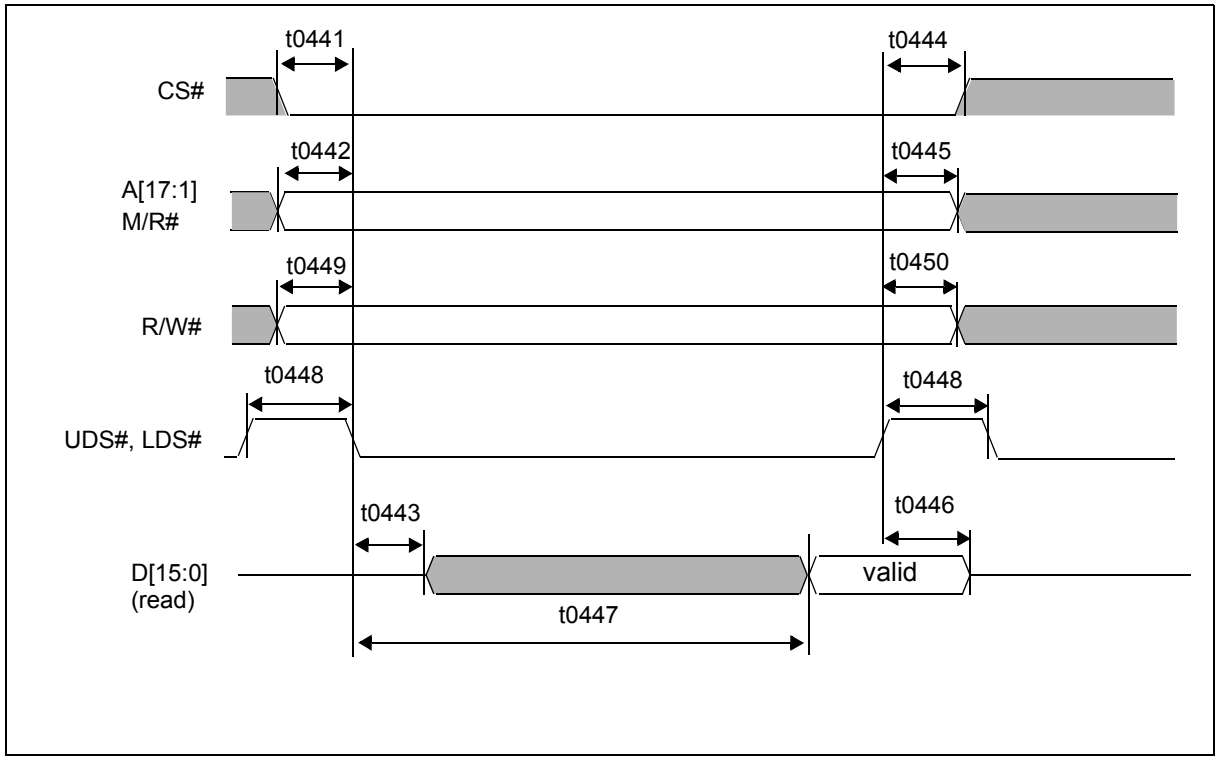


Figure 7-17: Direct 68 Interface Read Cycle Timing (No Wait Mode)

Table 7-22: Direct 68 Interface Read Cycle Timing (No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t0441	CS# setup time	0		ns
t0442	A[17:1], M/R# setup time	0		ns
t0443	UDS#, LDS# falling edge to D[15:0] driven	4		ns
t0444	CS# hold time from UDS#, LDS# rising edge	0		ns
t0445	A[17:1], M/R# hold time from UDS#, LDS# rising edge	0		ns
t0446	D[15:0] hold time from UDS#, LDS# rising edge	2	8	ns
t0447	UDS#, LDS# falling edge to valid Data if there are no internal delayed cycles		Note1,2	ns
t0448	UDS#, LDS# pulse width high	10		ns
t0449	R/W# setup time	5		ns
t0450	R/W# hold time from UDS#, LDS# rising edge	2		ns

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
2. t0447max = WAIT Length + 29 ns

Table 7-23: Direct 68 Host Interface Truth Table for Little Endian

R/W#	UDS#	LDS#	D[15:8]	D[7:0]	Comments
0	0	0	valid	valid	16-bit write
0	1	0	-	valid	8-bit write; data on low byte (even byte address[1])
0	0	1	valid	-	8-bit write; data on high byte (odd byte address[1])
1	0	0	valid	valid	16-bit read
1	1	0	-	valid	8-bit read; data on low byte (even byte address[1])
1	0	1	valid	-	8-bit read; data on high byte (odd byte address[1])

1. Because A0 is not used, all addresses are seen by the S1D13717 as even addresses (16-bit word address aligned on even byte addresses).

7.3.5 Indirect 80 Type 1

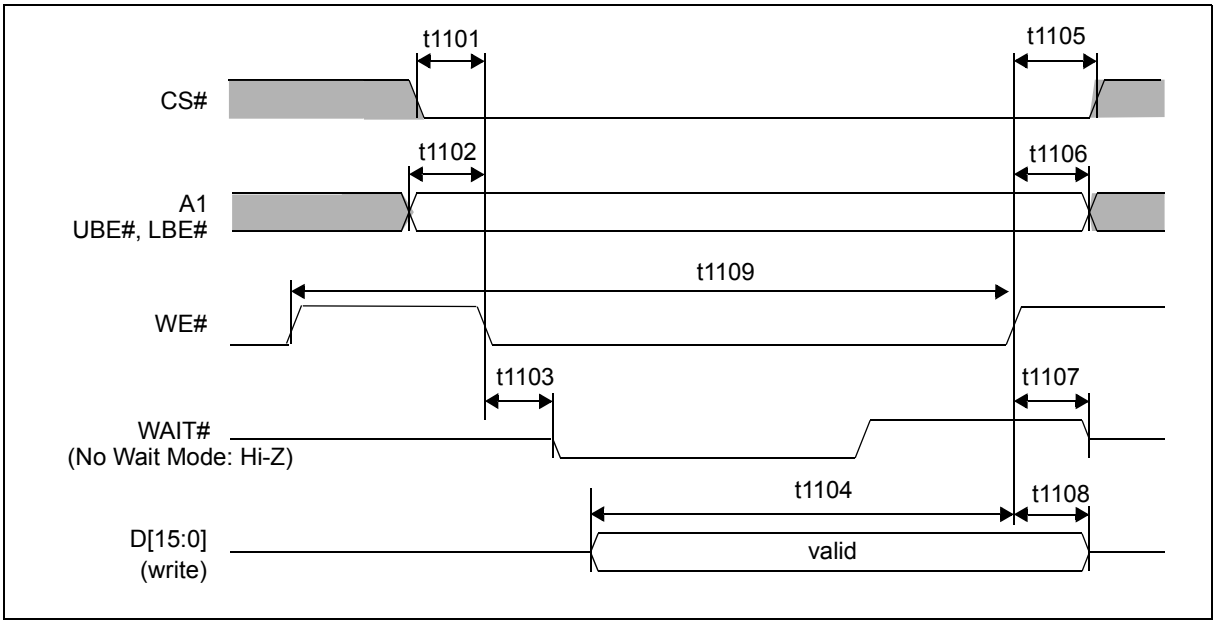


Figure 7-18: Indirect 80 Type 1 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-24: Indirect 80 Type 1 Interface Write Cycle Timing (Wait/No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1101	CS# setup time	15		ns
t1102	A1, UBE#, LBE# setup time	15		ns
t1103	WE# falling edge to WAIT# driven low		10	ns
t1104	D[15:0] setup time to WE# rising edge	10		ns
t1105	CS# hold time from WE# rising edge	5		ns
t1106	A1, UBE#, LBE# hold time from WE# rising edge	5		ns
t1107	WE# rising edge to WAIT# high impedance		7	ns
t1108	D[15:0] hold time from WE# rising edge	2		ns
t1109	Cycle time (No wait mode only)	Note2,3		Ts

1. Ts = System clock period.
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
3. t1109min = WAIT Length + 3 Ts

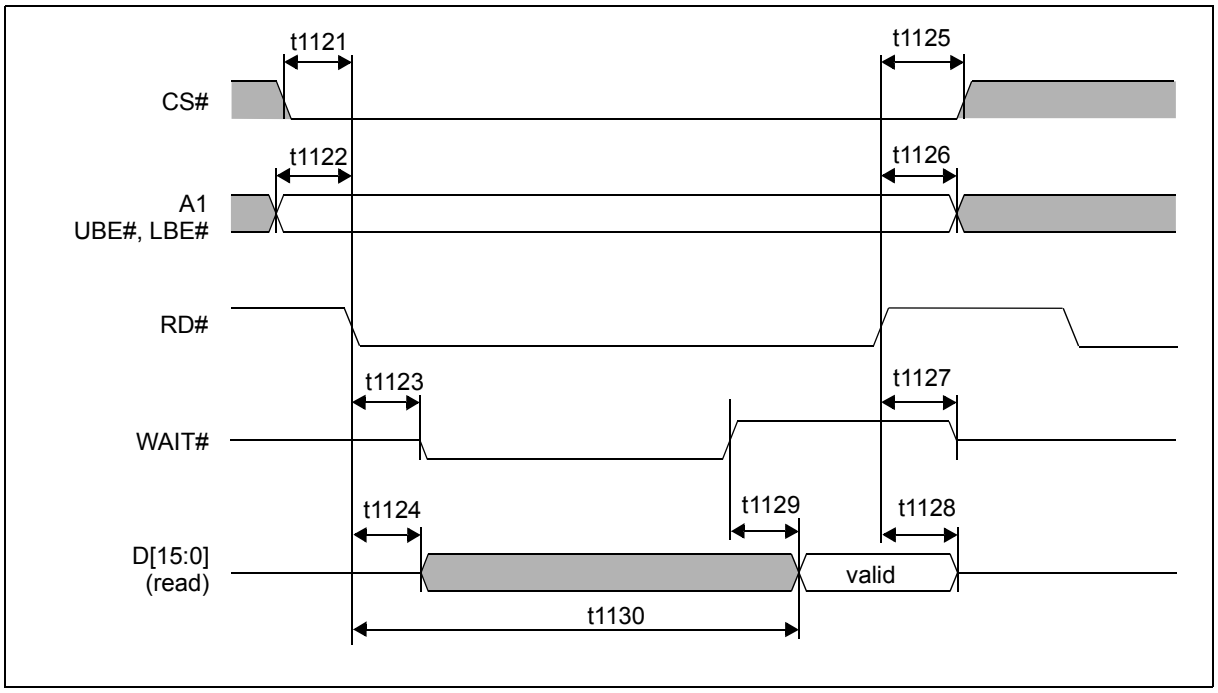


Figure 7-19: Indirect 80 Type 1 Interface Read Cycle Timing (Wait Mode)

Table 7-25: Indirect 80 Type 1 Interface Read Cycle Timing (Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1121	CS# setup time	15		ns
t1122	A1, UBE#, LBE# setup time	15		ns
t1123	RD# falling edge to WAIT# driven low		10	ns
t1124	RD# falling edge to D[15:0] driven	4		ns
t1125	CS# hold time from RD# rising edge	2		ns
t1126	A1, UBE#, LBE# hold time from RD# rising edge	2		ns
t1127	RD# rising edge to WAIT# high impedance		7	ns
t1128	D[15:0] hold time from RD# rising edge.	2	8	ns
t1129	WAIT# rising edge to valid Data if WAIT# is asserted		10	ns
t1130	RD# falling edge to valid Data if WAIT# is NOT asserted		17	ns

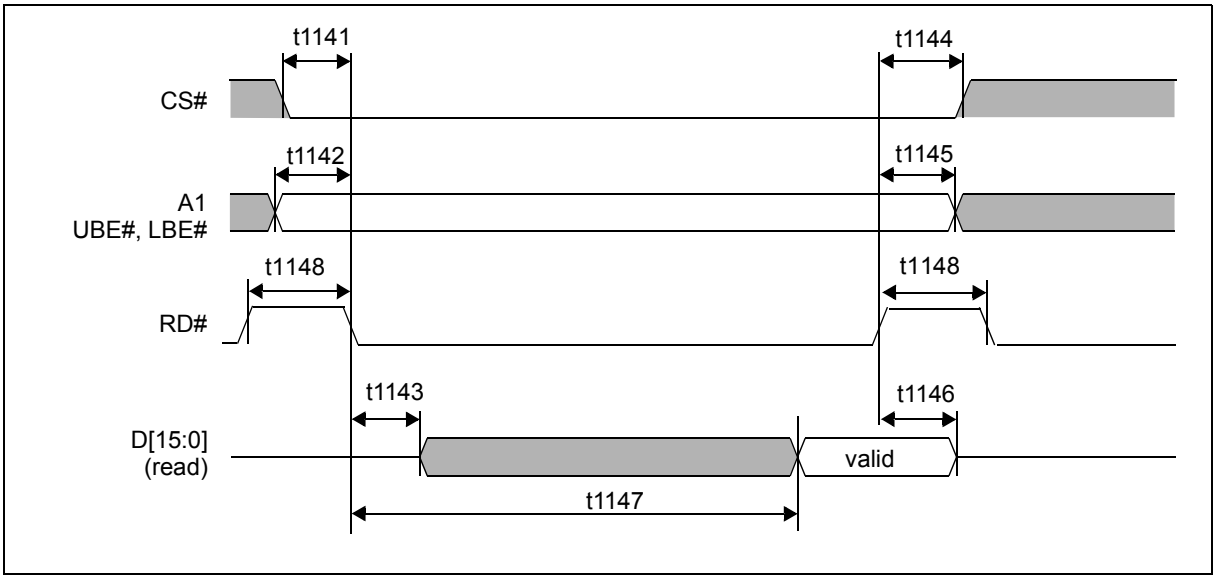


Figure 7-20: Indirect 80 Type 1 Interface Read Cycle Timing (No Wait Mode)

Table 7-26: Indirect 80 Type 1 Interface Read Cycle Timing (No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1141	CS# setup time	0		ns
t1142	A1, UBE#, LBE# setup time	0		ns
t1143	RD# falling edge to D[15:0] driven	4		ns
t1144	CS# hold time from RD# rising edge	0		ns
t1145	A1, UBE#, LBE# hold time from RD# rising edge	0		ns
t1146	D[15:0] hold time from RD# rising edge	2	8	ns
t1147	RD# falling edge to valid Data if there are no internal delayed cycles		Note1,2	ns
t1148	RD# pulse width high	10		ns

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
2. t1147max = WAIT Length + 29 ns

Table 7-27: Indirect 80 Type 1 Host Interface Truth Table for Little Endian

WE#	RD#	UBE#	LBE#	D[15:8]	D[7:0]	Comments
0	1	0	0	valid	valid	16-bit command write or data write
0	1	1	0	-	valid	8-bit data write (memory); data on low byte (even byte address[1])
0	1	0	1	valid	-	8-bit data write (memory); data on high byte (odd byte address[1])
1	0	0	0	valid	valid	16-bit data read
1	0	1	0	-	valid	8-bit data read (memory); data on low byte (even byte address[1])
1	0	0	1	valid	-	8-bit data read (memory); data on high byte (odd byte address[1])

Table 7-28: Indirect 80 Type 1 Host Interface Truth Table for Big Endian

WE#	RD#	UBE#	LBE#	D[15:8]	D[7:0]	Comments
0	1	0	0	valid	valid	16-bit command write or data write
0	1	1	0	-	valid	8-bit data write (memory); data on low byte (odd byte address[1])
0	1	0	1	valid	-	8-bit data write (memory); data on high byte (even byte address[1])
1	0	0	0	valid	valid	16-bit data read
1	0	1	0	-	valid	8-bit data read (memory); data on low byte (odd byte address[1])
1	0	0	1	valid	-	8-bit data read (memory); data on high byte (even byte address[1])

Table 7-29: Indirect 80 Type 1 Host Interface Function Selection

A1	WE#	RD#	Comments
0	0	1	16-bit Command Write (register address)
1	0	1	Data Write (16-bit register data or 8/16-bit memory data)
1	1	0	Data Read (16-bit register data or 8/16-bit memory data)

1. Because A0 is not used, all addresses are seen by the S1D13717 as even addresses (16-bit word address aligned on even byte addresses).

7.3.6 Indirect 80 Type 2

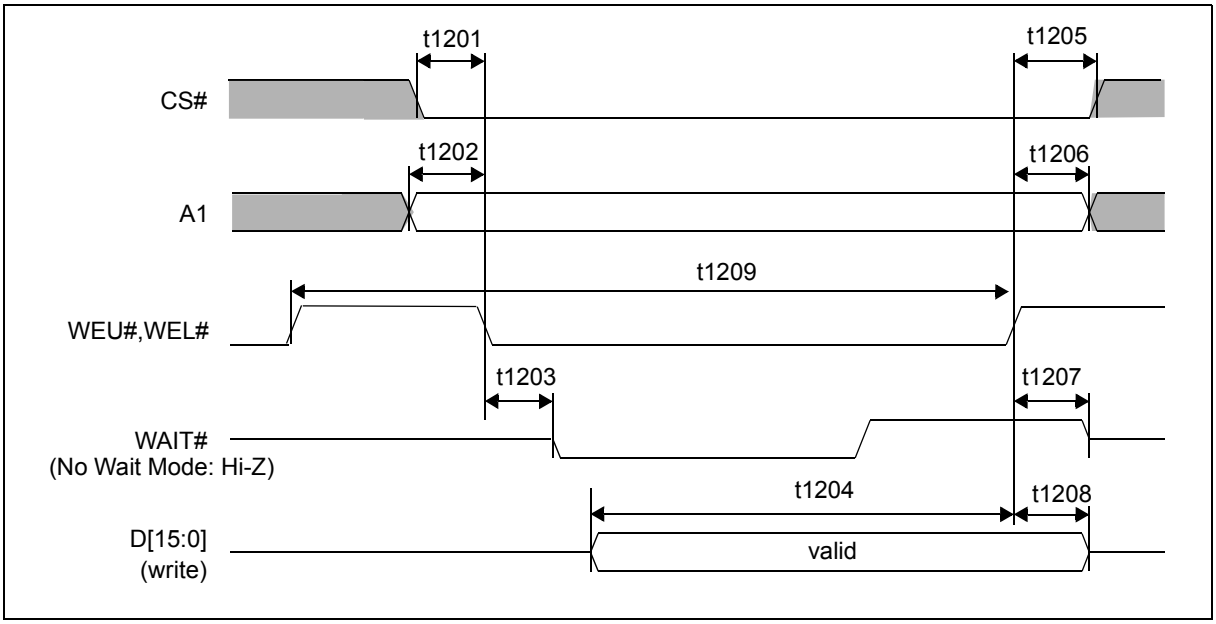


Figure 7-21: Indirect 80 Type 2 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-30: Indirect 80 Type 2 Interface Write Cycle Timing (Wait/No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1201	CS# setup time	15		ns
t1202	A1 setup time	15		ns
t1203	WEU#,WEL# falling edge to WAIT# driven low		10	ns
t1204	D[15:0] setup time to WEU#,WEL# rising edge	10		ns
t1205	CS# hold time from WEU#,WEL# rising edge	5		ns
t1206	A1 hold time from WEU#,WEL# rising edge	5		ns
t1207	WEU#,WEL# rising edge to WAIT# high impedance		7	ns
t1208	D[15:0] hold time from WEU#,WEL# rising edge	2		ns
t1209	Cycle time (No wait mode only)	Note2,3		Ts

1. Ts = System clock period.
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
3. t1209min = WAIT Length + 3 Ts

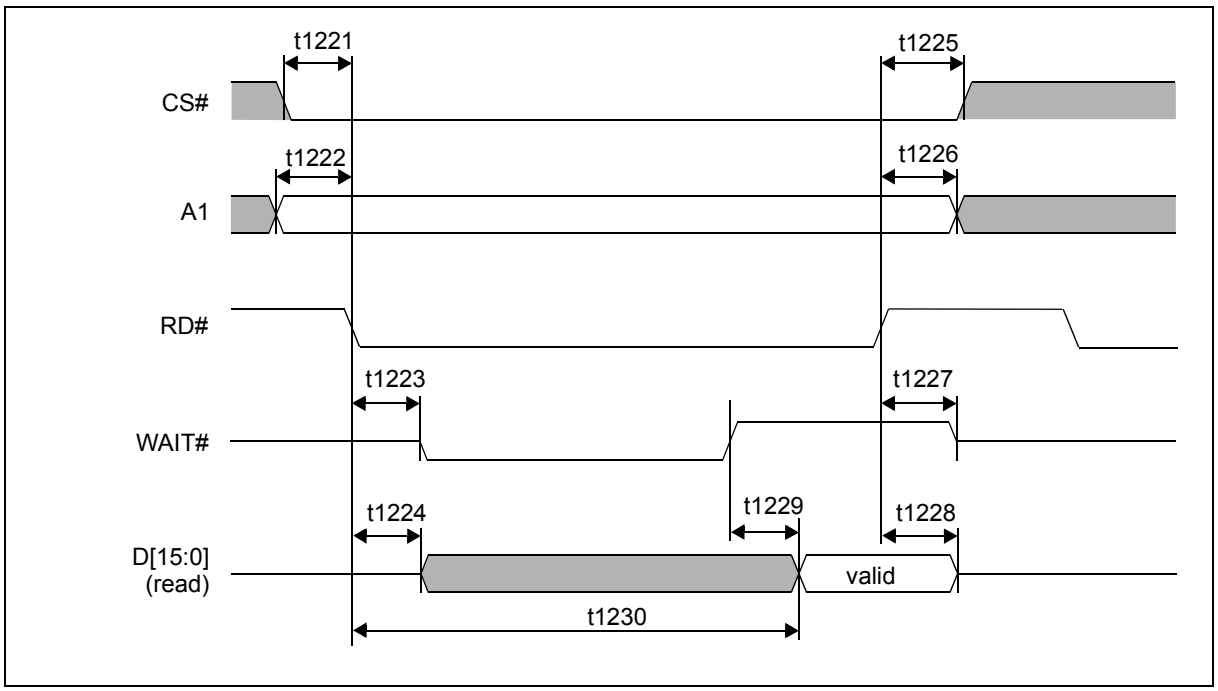


Figure 7-22: Indirect 80 Type 2 Interface Read Cycle Timing (Wait Mode)

Table 7-31: Indirect 80 Type 2 Interface Read Cycle Timing (Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1221	CS# setup time	15		ns
t1222	A1 setup time	15		ns
t1223	RD# falling edge to WAIT# driven low		10	ns
t1224	RD# falling edge to D[15:0] driven	4		ns
t1225	CS# hold time from RD# rising edge	2		ns
t1226	A1 hold time from RD# rising edge	2		ns
t1227	RD# rising edge to WAIT# high impedance		7	ns
t1228	D[15:0] hold time from RD# rising edge.	2	8	ns
t1229	WAIT# rising edge to valid Data if WAIT# is asserted		10	ns
t1230	RD# falling edge to valid Data if WAIT# is NOT asserted		17	ns

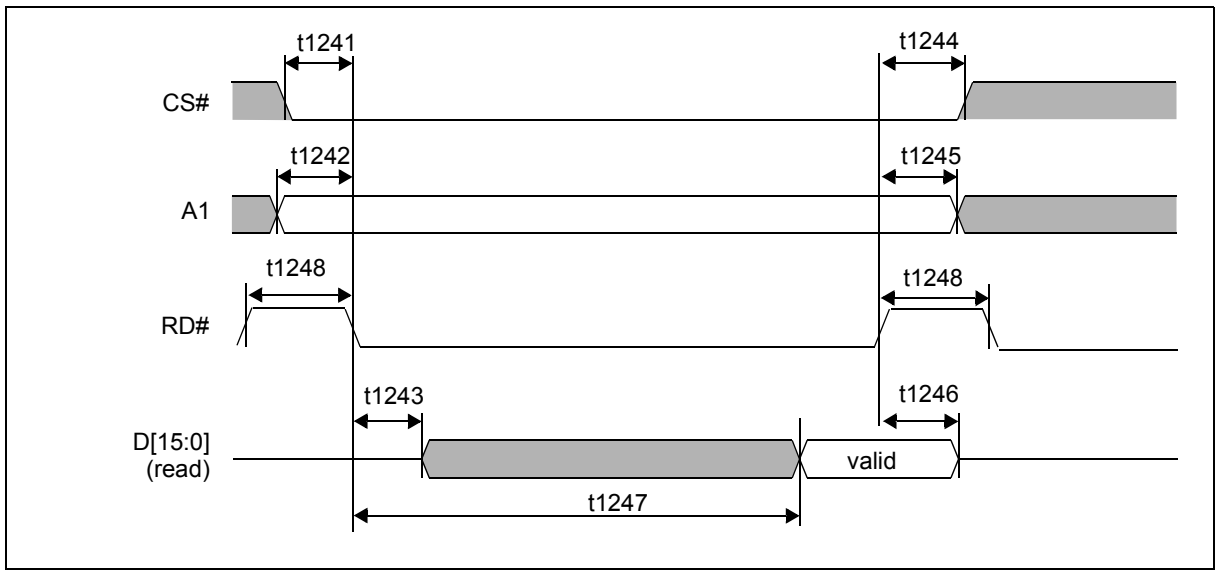


Figure 7-23: Indirect 80 Type 2 Interface Read Cycle Timing (No Wait Mode)

Table 7-32: Indirect 80 Type 2 Interface Read Cycle Timing (No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1241	CS# setup time	0		ns
t1242	A1 setup time	0		ns
t1243	RD# falling edge to D[15:0] driven	4		ns
t1244	CS# hold time from RD# rising edge	0		ns
t1245	A1 hold time from RD# rising edge	0		ns
t1246	D[15:0] hold time from RD# rising edge	2	8	ns
t1247	RD# falling edge to valid Data if there are no internal delayed cycles		Note1,2	ns
t1248	RD# pulse width high	10		ns

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
2. t1247max = WAIT Length + 29 ns

Table 7-33: Indirect 80 Type 2 Host Interface Truth Table for Little Endian

RD#	WEU#	WEL#	D[15:8]	D[7:0]	Comments
1	0	0	valid	valid	16-bit command write or data write
1	1	0	-	valid	8-bit data write (memory); data on high byte (odd byte address[1])
1	0	1	valid	-	8-bit data write (memory); data on high byte (even byte address[1])
0	1	1	valid	valid	16-bit data read

Table 7-34: Indirect 80 Type 2 Host Interface Function Selection

A1	WEU#/WEL#	RD#	Comments
0	0	1	16-bit Command Write (register address)
1	0	1	Data Write (16-bit register data or 8/16-bit memory data)
1	1	0	Data Read (16-bit register data or 16-bit memory data)

1. Because A0 is not used, all addresses are seen by the S1D13717 as even addresses (16-bit word address aligned on even byte addresses).

7.3.7 Indirect 80 Type 3

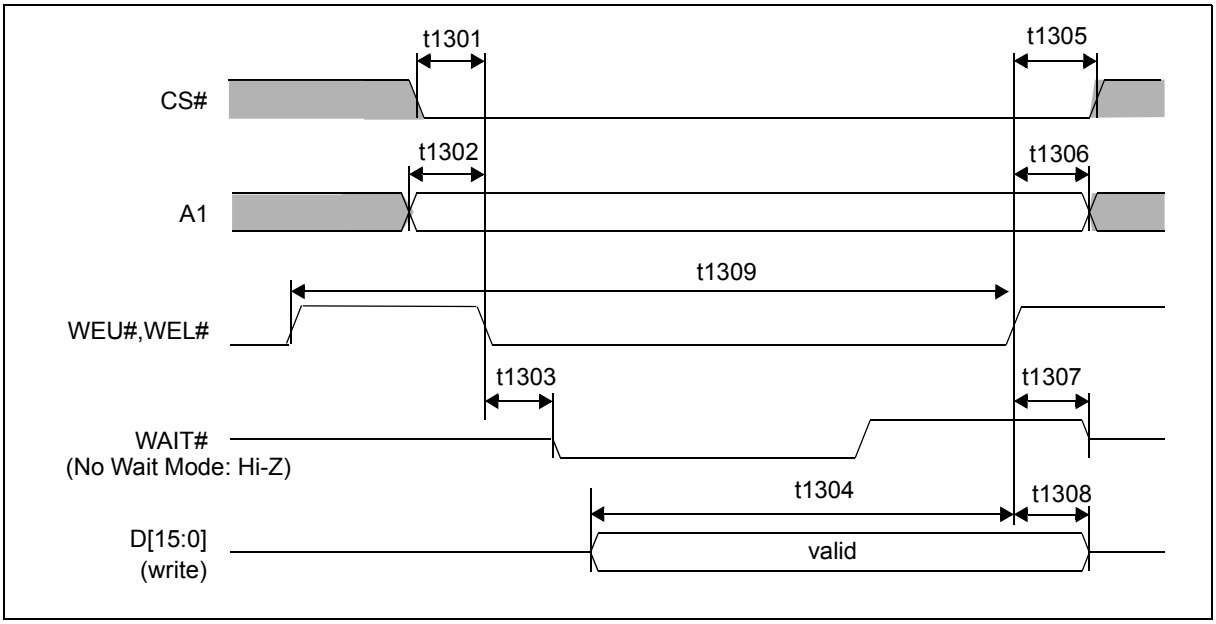


Figure 7-24: Indirect 80 Type 3 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-35: Indirect 80 Type 3 Interface Write Cycle Timing (Wait/No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1301	CS# setup time	15		ns
t1302	A1 setup time	15		ns
t1303	WEU#,WEL# falling edge to WAIT# driven low		10	ns
t1304	D[15:0] setup time to WEU#,WEL# rising edge	10		ns
t1305	CS# hold time from WEU#,WEL# rising edge	5		ns
t1306	A1 hold time from WEU#,WEL# rising edge	5		ns
t1307	WEU#,WEL# rising edge to WAIT# high impedance		7	ns
t1308	D[15:0] hold time from WEU#,WEL# rising edge	2		ns
t1309	Cycle time (No wait mode only)	Note2,3		Ts

1. Ts = System clock period.
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
3. t1309min = WAIT Length + 3 Ts

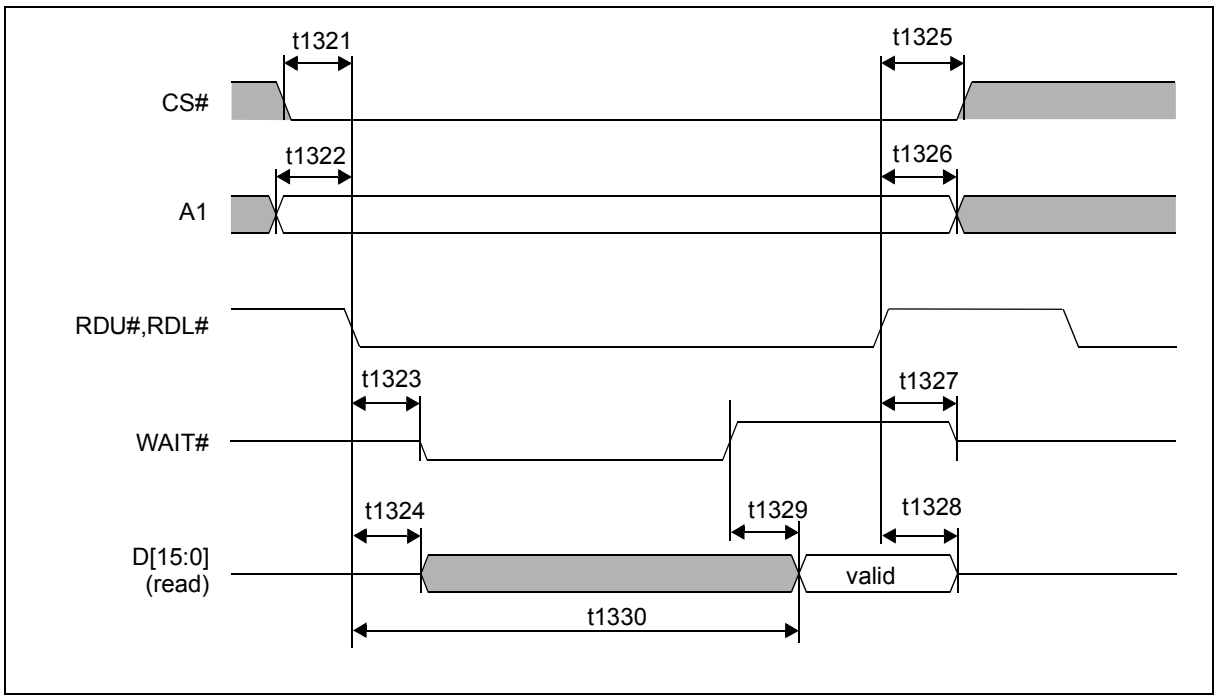


Figure 7-25: Indirect 80 Type 3 Interface Read Cycle Timing (Wait Mode)

Table 7-36: Indirect 80 Type 3 Interface Read Cycle Timing (Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1321	CS# setup time	15		ns
t1322	A1 setup time	15		ns
t1323	RDU#,RDL# falling edge to WAIT# driven low		10	ns
t1324	RDU#,RDL# falling edge to D[15:0] driven	4		ns
t1325	CS# hold time from RDU#,RDL# rising edge	2		ns
t1326	A1 hold time from RDU#,RDL# rising edge	2		ns
t1327	RDU#,RDL# rising edge to WAIT# high impedance		7	ns
t1328	D[15:0] hold time from RDU#,RDL# rising edge.	2	8	ns
t1329	WAIT# rising edge to valid Data if WAIT# is asserted		10	ns
t1330	RDU#,RDL# falling edge to valid Data if WAIT# is NOT asserted		17	ns

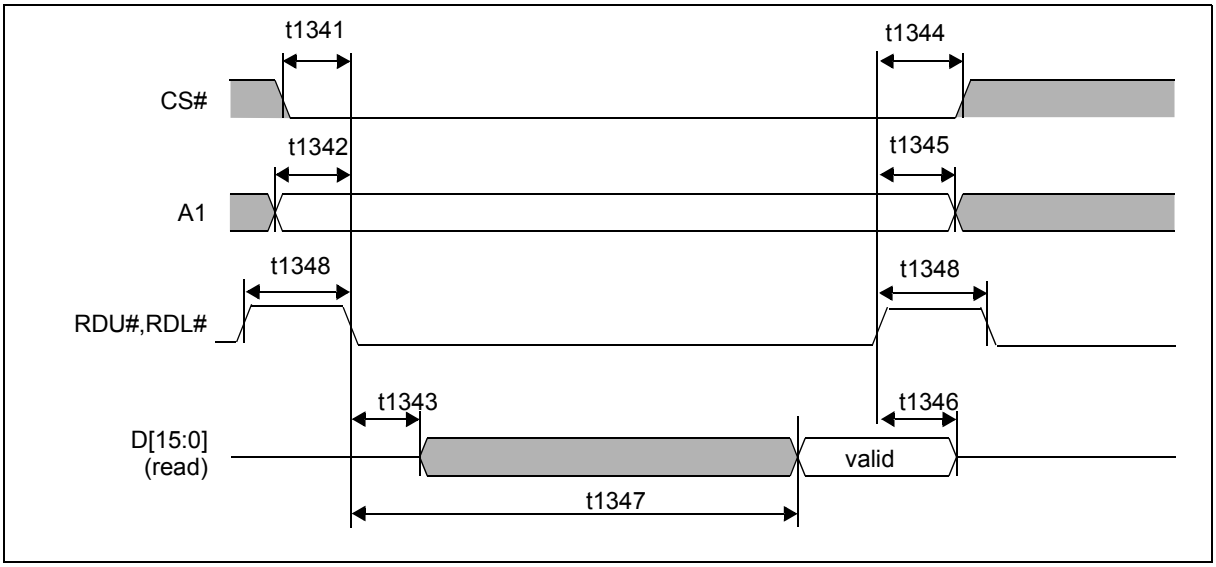


Figure 7-26: Indirect 80 Type 3 Interface Read Cycle Timing (No Wait Mode)

Table 7-37: Indirect 80 Type 3 Interface Read Cycle Timing (No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1341	CS# setup time	0		ns
t1342	A1 setup time	0		ns
t1343	RDU#,RDL# falling edge to D[15:0] driven	4		ns
t1344	CS# hold time from RDU#,RDL# rising edge	0		ns
t1345	A1 hold time from RDU#,RDL# rising edge	0		ns
t1346	D[15:0] hold time from RDU#,RDL# rising edge	2	8	ns
t1347	RDU#,RDL# falling edge to valid Data if there are no internal delayed cycles		Note1,2	ns
t1348	RDU#, RDL# pulse width high	10		ns

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
2. t1347max = WAIT Length + 40 ns

Table 7-38: Indirect 80 Type 3 Host Interface Truth Table for Little Endian

WEU#	WEL#	RDU#	RDL#	D[15:8]	D[7:0]	Comments
0	0	1	1	valid	valid	16-bit command write or data write
1	0	1	1	-	valid	8-bit data write (memory); data on low byte (even byte address[1])
0	1	1	1	valid	-	8-bit data write (memory); data on high byte (odd byte address[1])
1	1	0	0	valid	valid	16-bit data read
1	1	1	0	-	valid	8-bit data read (memory); data on low byte (even byte address[1])
1	1	0	1	valid	-	8-bit data read (memory); data on high byte (odd byte address[1])

Table 7-39: Indirect 80 Type 3 Host Interface Truth Table for Big Endian

WEU#	WEL#	RDU#	RDL#	D[15:8]	D[7:0]	Comments
0	0	1	1	valid	valid	16-bit command write or data write
1	0	1	1	-	valid	8-bit data write (memory); data on low byte (odd byte address[1])
0	1	1	1	valid	-	8-bit data write (memory); data on high byte (even byte address[1])
1	1	0	0	valid	valid	16-bit data read
1	1	1	0	-	valid	8-bit data read (memory); data on low byte (odd byte address[1])
1	1	0	1	valid	-	8-bit data read (memory); data on high byte (even byte address[1])

Table 7-40: Indirect 80 Type 3 Host Interface Function Select

A1	WEU# / WEL#	RDU# / RDL#	Comments
0	0	1	16-bit Command Write (register address)
1	0	1	Data Write (16-bit register data or 8/16-bit memory data)
1	1	0	Data Read (16-bit register data or 8/16-bit memory data)

1. Because A0 is not used, all addresses are seen by the S1D13717 as even addresses (16-bit word address aligned on even byte addresses).

7.3.8 Indirect 68

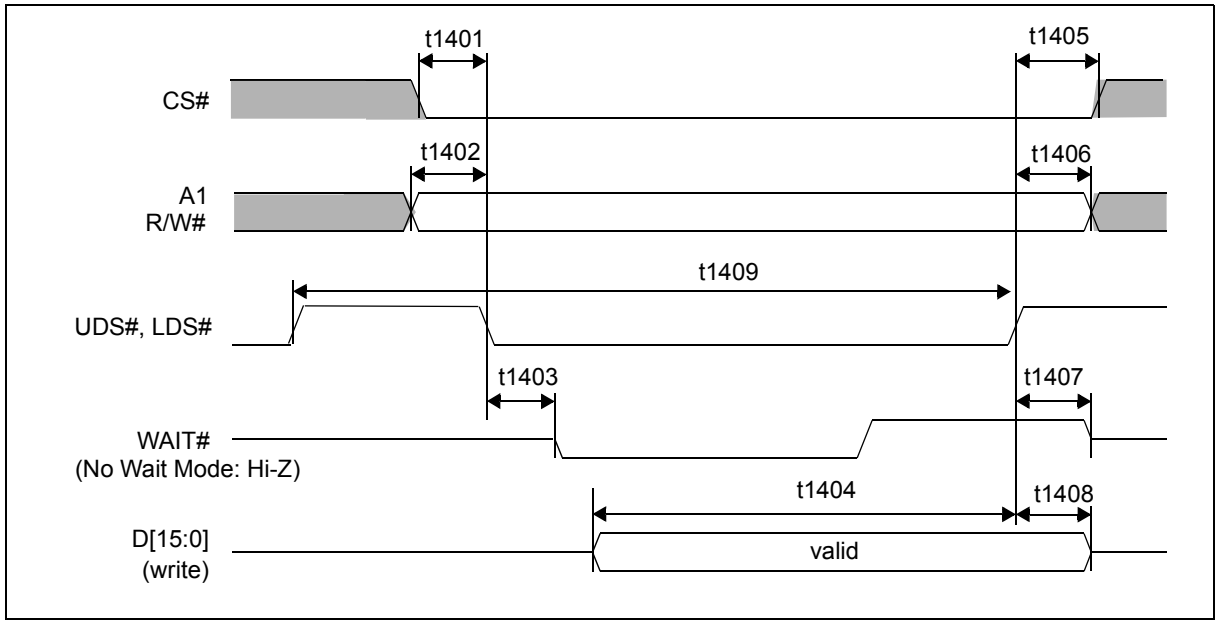


Figure 7-27: Indirect 68 Interface Write Cycle Timing (Wait/No Wait Mode)

Table 7-41: Indirect 68 Interface Write Cycle Timing (Wait/No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1401	CS# setup time	15		ns
t1402	A1, R/W# setup time	15		ns
t1403	UDS#, LDS# falling edge to WAIT# driven low		10	ns
t1404	D[15:0] setup time to UDS#, LDS# rising edge	10		ns
t1405	CS# hold time from UDS#, LDS# rising edge	5		ns
t1406	A1, R/W# hold time from UDS#, LDS# rising edge	5		ns
t1407	UDS#, LDS# rising edge to WAIT# high impedance		7	ns
t1408	D[15:0] hold time from UDS#, LDS# rising edge	2		ns
t1409	Cycle time (No wait mode only)	Note2,3		Ts

1. Ts = System clock period
2. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
3. t1409min = WAIT Length + 3 Ts

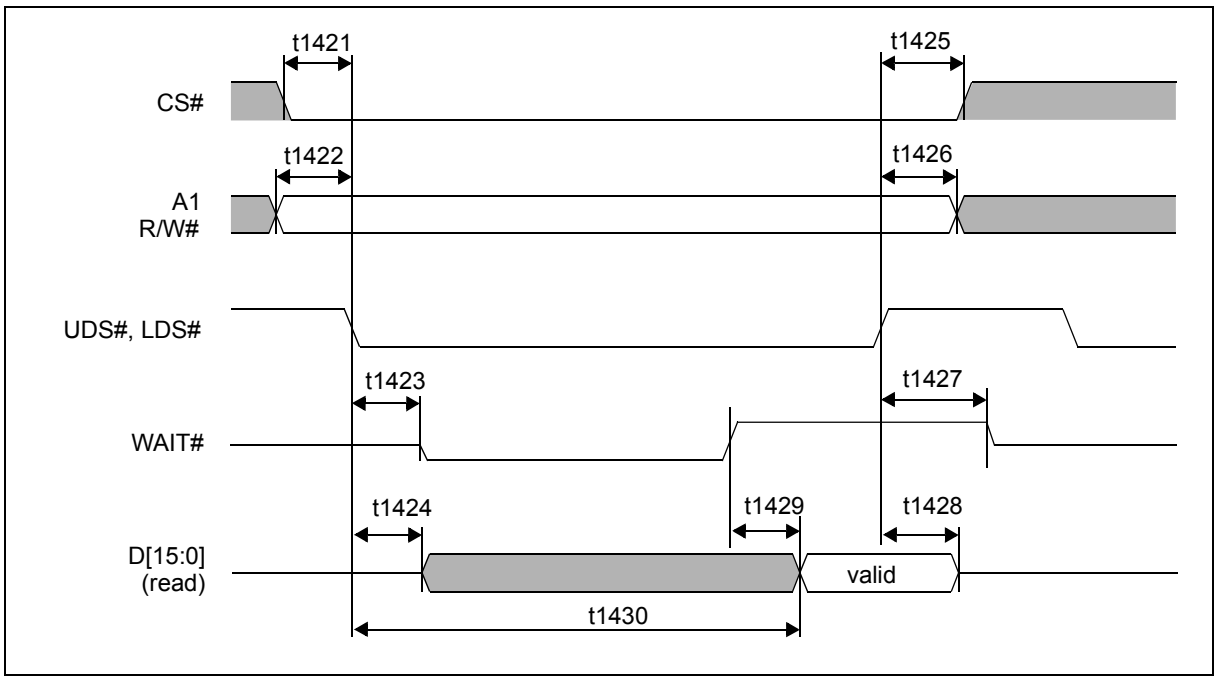


Figure 7-28: Indirect 68 Interface Read Cycle Timing (Wait Mode)

Table 7-42: Indirect 68 Interface Read Cycle Timing (Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1421	CS# setup time	15		ns
t1422	A1, R/W# setup time	15		ns
t1423	UDS#, LDS# falling edge to WAIT# driven low		10	ns
t1424	UDS#, LDS# falling edge to D[15:0] driven	4		ns
t1425	CS# hold time from UDS#, LDS# rising edge	2		ns
t1426	A1, R/W# hold time from UDS#, LDS# rising edge	2		ns
t1427	UDS#, LDS# rising edge to WAIT# high impedance		7	ns
t1428	D[15:0] hold time from UDS#, LDS# rising edge	2	8	ns
t1429	WAIT# rising edge to valid Data if WAIT# is asserted		10	ns
t1430	UDS#, LDS# falling edge to valid Data if WAIT# is NOT asserted		17	ns

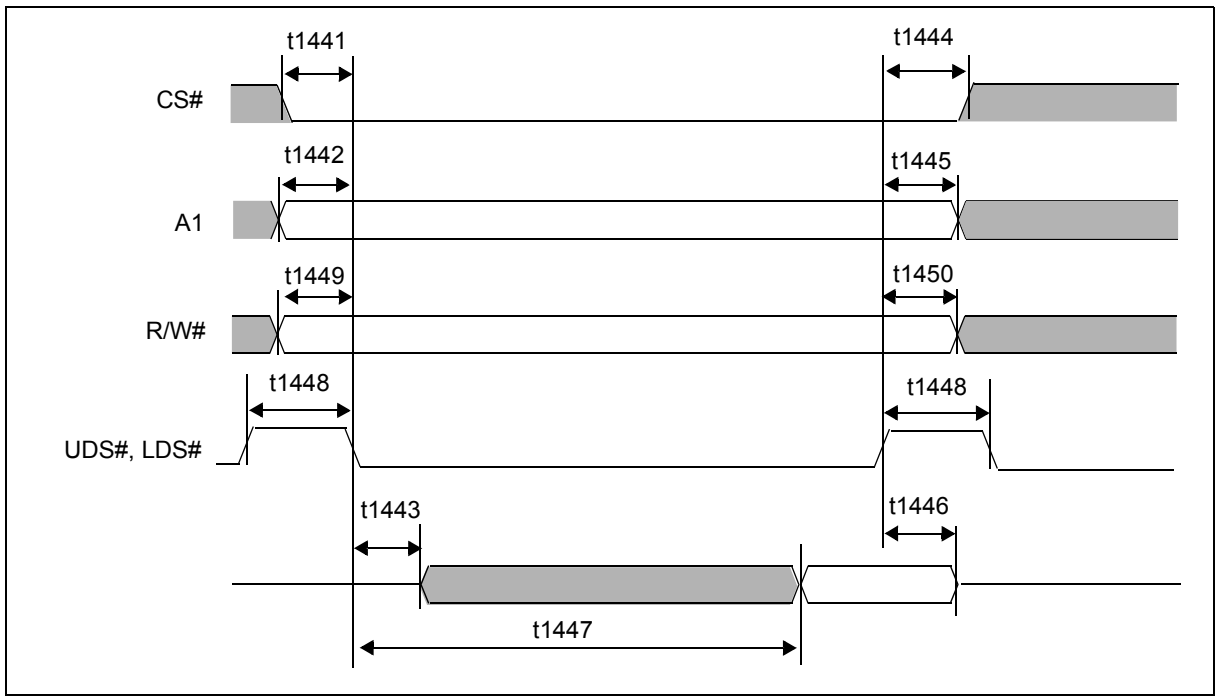


Figure 7-29: Indirect 68 Interface Read Cycle Timing (No Wait Mode)

Table 7-43: Indirect 68 Interface Read Cycle Timing (No Wait Mode)

Symbol	Parameter	3.0 Volt		Units
		Min	Max	
t1441	CS# setup time	0		ns
t1442	A1 setup time	0		ns
t1443	UDS#, LDS# falling edge to D[15:0] driven	4		ns
t1444	CS# hold time from UDS#, LDS# rising edge	0		ns
t1445	A1 hold time from UDS#, LDS# rising edge	0		ns
t1446	D[15:0] hold time from UDS#, LDS# rising edge	2	8	ns
t1447	UDS#, LDS# falling edge to valid Data if there are no internal delayed cycles		Note1,2	ns
t1448	UDS#, LDS# pulse width high	10		ns
t1449	R/W# setup time	5		ns
t1450	R/W# hold time from UDS#, LDS# rising edge	2		ns

1. When no wait mode is selected, the same wait length cycles must be maintained as when wait mode is selected. See Section 7.3.9, “WAIT Length” on page 88.
2. t1447max = WAIT Length + 29 ns

Table 7-44: Indirect 68 Host Interface Truth Table for Little Endian

R/W#	UDS#	LDS#	D[15:8]	D[7:0]	Comments
0	0	0	valid	valid	16-bit command write or data write
0	1	0	-	valid	8-bit data write (memory); data on low byte (even byte address[1])
0	0	1	valid	-	8-bit data write (memory); data on high byte (odd byte address[1])
1	0	0	valid	valid	16-bit data read
1	1	0	-	valid	8-bit data read (memory); data on low byte (even byte address[1])
1	0	1	valid	-	8-bit data read (memory); data on high byte (odd byte address[1])

Table 7-45: Indirect 68 Host Interface Function Select

A1	R/W#	Comments
0	0	16-bit Command Write (register address)
1	0	Data Write (16-bit register data or 8/16-bit memory data)
1	1	Data Read (16-bit register data or 8/16-bit memory data)

1. Because A0 is not used, all addresses are seen by the S1D13717 as even addresses (16-bit word address aligned on even byte addresses).

7.3.9 WAIT Length

The Host CPU interfaces of the S1D13717 are asynchronous. However, the CPU signals are latched internally, synchronous to the system clock. The following table shows the WAIT# length based on the system clock.

In the table, "Single" access means there is enough idle time between accesses. The minimum idle time to guarantee a single access is six system clocks from the rising edge of WE# of the current access to the rising edge of WE# of the next access. "Continuous" access means there is not enough idle time between accesses.

If Host CPU cycles are assumed to be a minimum of *x* clocks in length, the actual cycle length will be "*x* + the value in the following table".

Table 7-46: Wait Length

Description	Min	Typ (Note 4)	Max	Unit
Single Write to the registers, except the JPEG Codec registers		0		Ts (Note1)
Continuous Write to the registers, except the JPEG Codec registers		5		Ts
Single Write to the JPEG Codec registers		0		Ts
Continuous Write to the JPEG Codec registers	4 (Note 3)		6 (Note 2)	Ts
Single Write to the display buffer		0		Ts
Continuous Write to the display buffer		4		Ts
Single Write to the JPEG FIFO (REG09A6h)		0		Ts
Continuous Write to the JPEG FIFO (REG09A6h)		5		Ts
Single/Continuous Read from the registers, except the JPEG Codec registers		5		Ts
Read from the registers after a Write, except the JPEG Codec registers		8		Ts
Single/Continuous Read from the JPEG Codec registers, except the JPEG Codec Table registers	5 (Note 3)		7 (Note 2)	Ts
Read from the JPEG Codec registers after a Write, except the JPEG Codec Table registers	8 (Note 3)		10 (Note 2)	Ts
Single/Continuous Read from the display buffer		5		Ts
Read from the display buffer after a Write		7		Ts
1st access of a JPEG FIFO continuous read		4		Ts
Last 2 accesses of a JPEG FIFO continuous read		4		Ts
Accesses of JPEG FIFO continuous read, except above		0		Ts

1. Ts = System Clock Period
2. Memory arbitration (Camera and JPEG modules are enabled)
3. No memory arbitration (Camera and JPEG modules are disabled)
4. These are typical values. Actual WAIT lengths may be larger than specified when multiple blocks of the S1D13717 are enabled.

7.4 Panel Interface Timing

7.4.1 Generic TFT Panel Timing

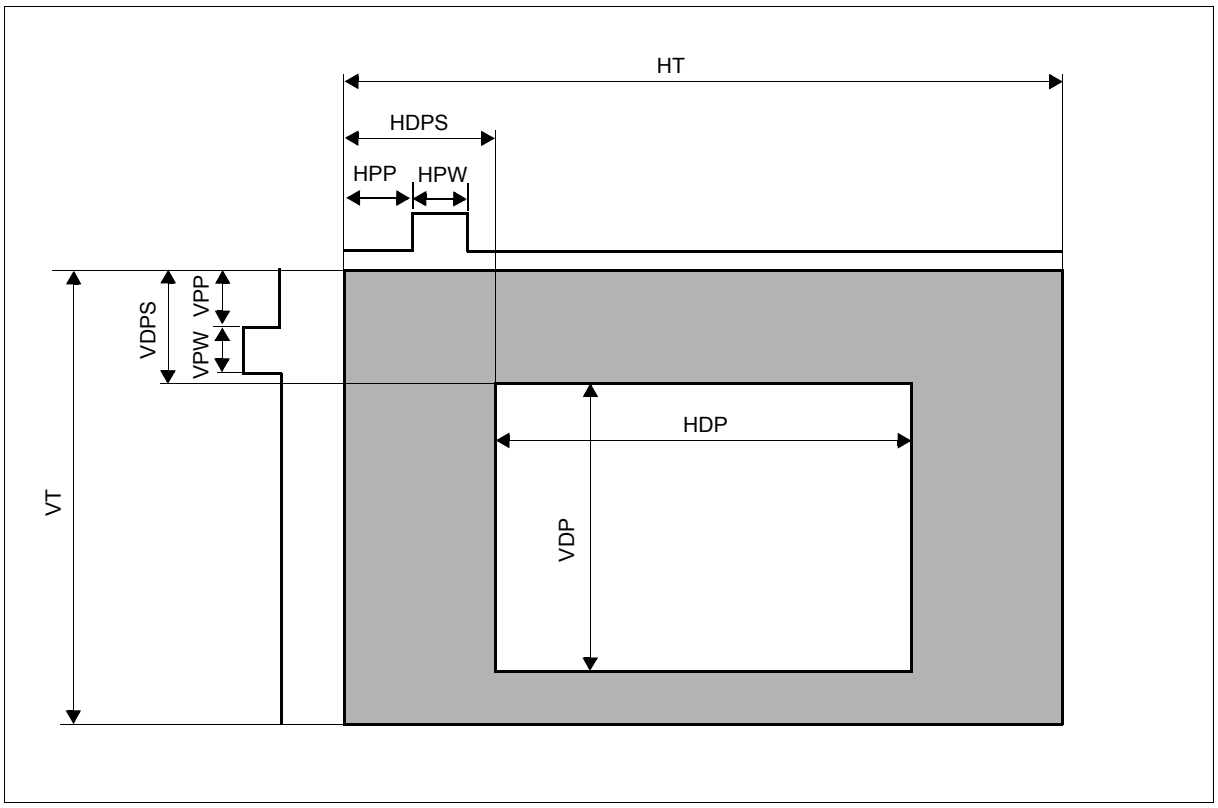


Figure 7-30: Generic TFT Panel Timing

Table 7-47: Generic TFT Panel Timing

Symbol	Description	Derived From	Units
HT	LCD1 Horizontal total	((REG[0040h] bits 6-0) + 1) x 8	Ts
HDP	LCD1 Display Period	((REG[0042h] bits 9-1) + 1) x 2	
HDPS	LCD1 Horizontal Display Period Start Position	((REG[0044h] bits 9-0) + 9	
HPW	LCD1 FPLINE Pulse Width	(REG[0046h] bits 6-0) + 1	
HPP	LCD1 FPLINE Pulse Position (see note 2)	(REG[0048h] bits 9-0) + 1	
VT	LCD1 Vertical Total	(REG[004Ah] bits 9-0) + 1	Lines
VDP	LCD1 Vertical Display Period	(REG[004Ch] bits 9-0) + 1	
VDPS	LCD1 Vertical Display Period Start Position	REG[004Eh] bits 9-0	
VPW	LCD1 FPFRAME Pulse Width	(REG[50h] bits 2-0) + 1	
VPP	LCD1 FPFRAME Pulse Position (see note 2)	REG[0052h] bits 9-0	

1. The following formulas must be valid for all panel timings:
   HDPS + HDP < HT
   VDPS + VDP < VT
2. For generic TFT panel types, the HPP value must be programmed to 1 and the VPP value must be programmed to 0. These values may be used to configure extended TFT types as required.

Generic RGB Type Interface Panel Horizontal Timing

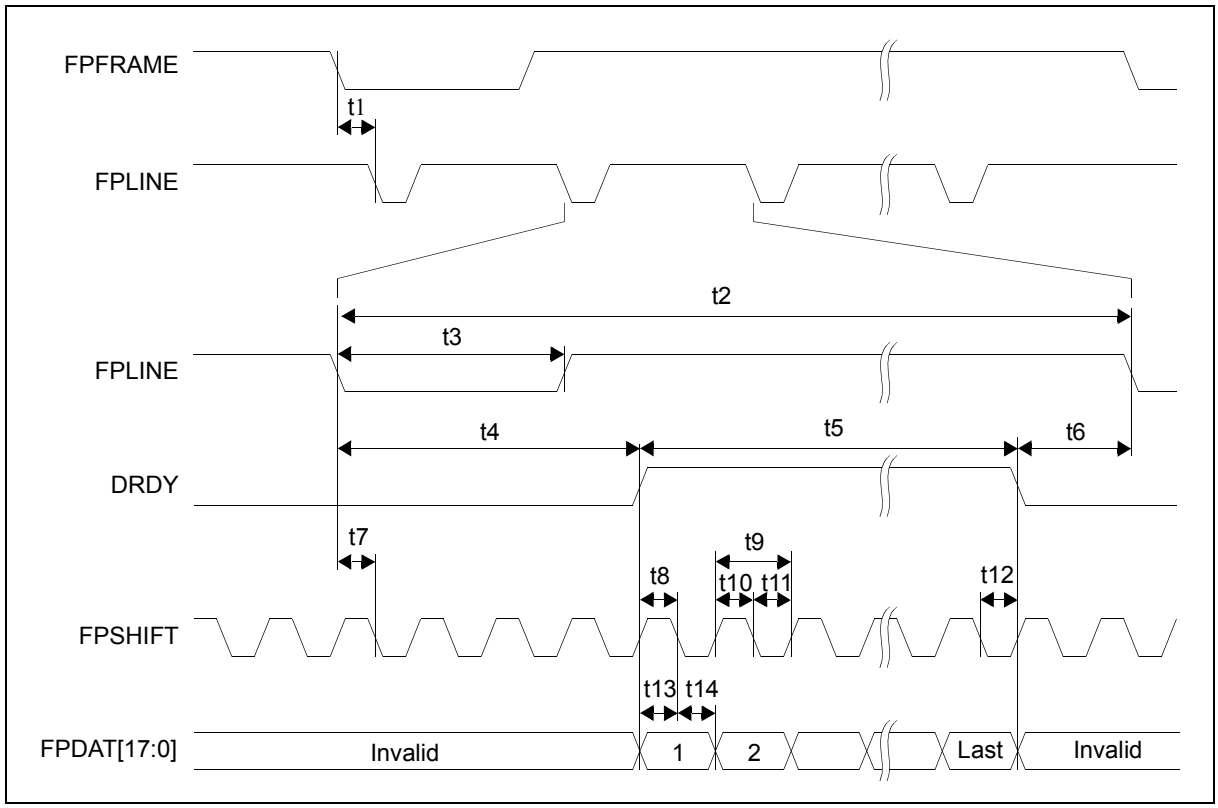


Figure 7-31: Generic RGB Type Interface Panel Horizontal Timing

Table 7-48: Generic RGB Type Interface Panel Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME falling edge to FPLINE falling edge		HPP (note 2)		Ts (note 1)
t2	Horizontal total period		HT		Ts
t3	FPLINE pulse width		HPW		Ts
t4	FPLINE falling edge to DRDY active		HDPS		Ts
t5	Horizontal display period		HDP		Ts
t6	DRDY falling edge to FPLINE falling edge		note 3		Ts
t7	FPLINE setup time to FPSHIFT falling edge		0.5		Ts
t8	DRDY setup to FPSHIFT falling edge		0.5		Ts
t9	FPSHIFT period		1		Ts
t10	FPSHIFT pulse width high		0.5		Ts
t11	FPSHIFT pulse width low		0.5		Ts
t12	DRDY hold from FPSHIFT falling edge		0.5		Ts
t13	Data setup to FPSHIFT falling edge		0.5		Ts
t14	Data hold from FPSHIFT falling edge		0.5		Ts

1. Ts = pixel clock period
2. For generic TFT panel types, the HPP value must be programmed to 1 and the VPP value must be programmed to 0. This values may be used to configure extended TFT types as required.
3. t6typ = t2 - t4 - t5

Note

The Generic TFT timings are based on the following:
FPFRAME Pulse Polarity bit is active low (REG[0050h] bit 7 = 0).
FPLINE Pulse Polarity bit is active low (REG[0046h] bit 7 = 0).

Generic RGB Type Interface Panel Vertical Timing

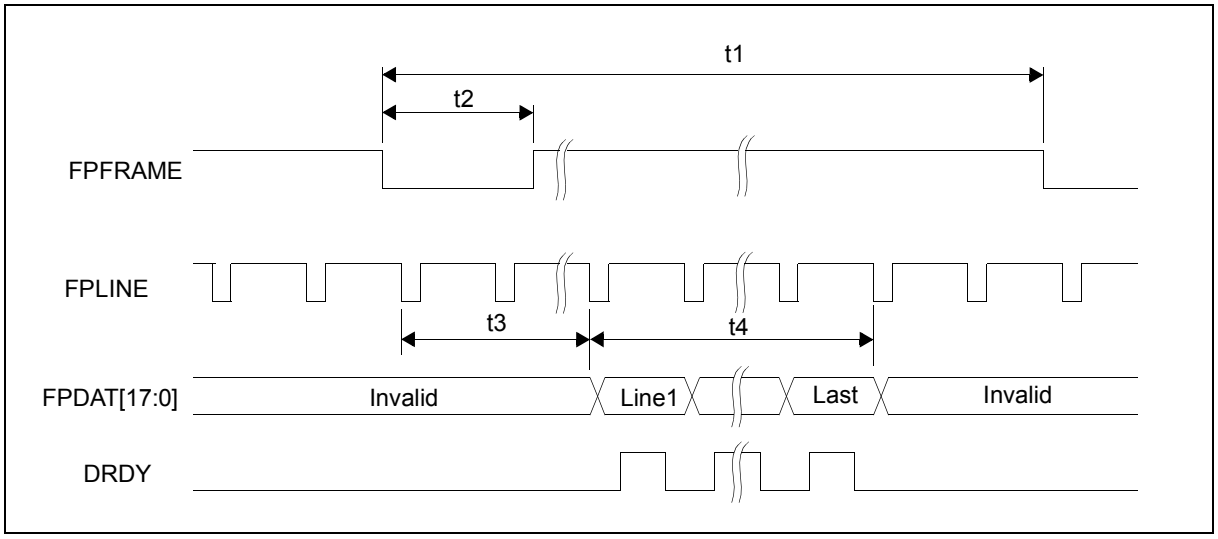


Figure 7-32: Generic RGB Type Interface Panel Vertical timing

Table 7-49: Generic RGB Type Interface Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Vertical total period		VT		Line
t2	FPFRAME pulse width		VPW		Line
t3	Vertical display start position (note 1)		note 2		Line
t4	Vertical display period		VDP		Line

1. t3 is measured from the first FPLINE pulse at the start of the frame to the last FPLINE pulse before FPDAT is valid.
2. t3typ = VDPS - VPP (For generic TFT panel types, the VPP value must be programmed to 0. This value may be used to configure extended TFT types as required.

7.4.2 LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing

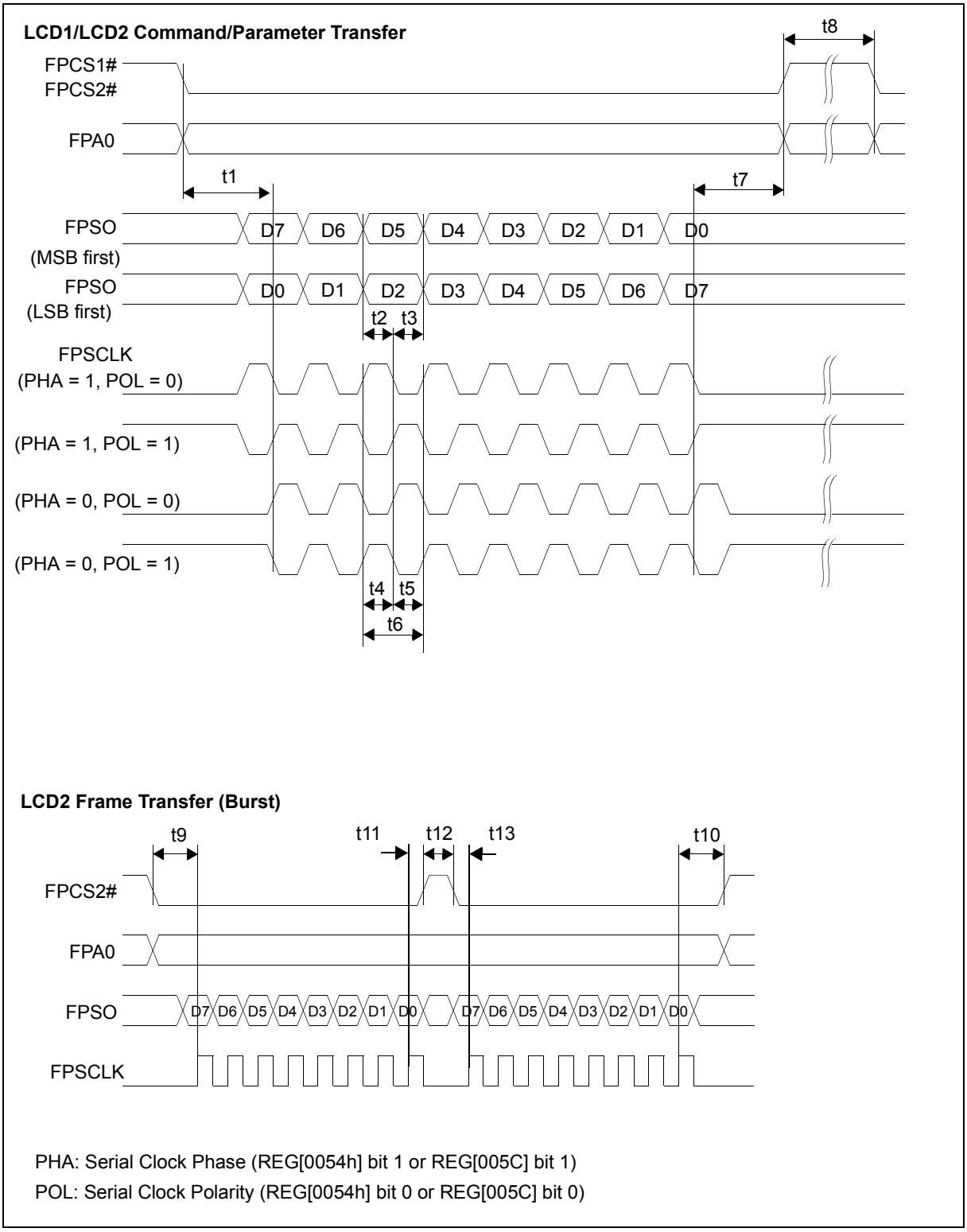


Figure 7-33: LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing

Table 7-50: LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time		1.5		Ts (Note 1)
t2	Data setup time		0.5		Ts
t3	Data hold time		0.5		Ts
t4	Serial clock pulse width low (high)		0.5		Ts
t5	Serial clock pulse width high (low)		0.5		Ts
t6	Serial clock period		1		Ts
t7	Chip select hold time for command/parameter transfer		1.5		Ts
t8	Chip select de-assert to reassert		1		Ts
t9	Chip select setup time at beginning of burst mode		1.5		
t10	Chip select hold time at end of burst mode		2.5		Ts
t11	Chip select hold time during burst mode		0.5		Ts
t12	Chip select interval in burst mode		1		Ts
t13	Chip select setup time during burst mode		0.5		Ts

1. Ts = Serial clock period

7.4.3 LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing

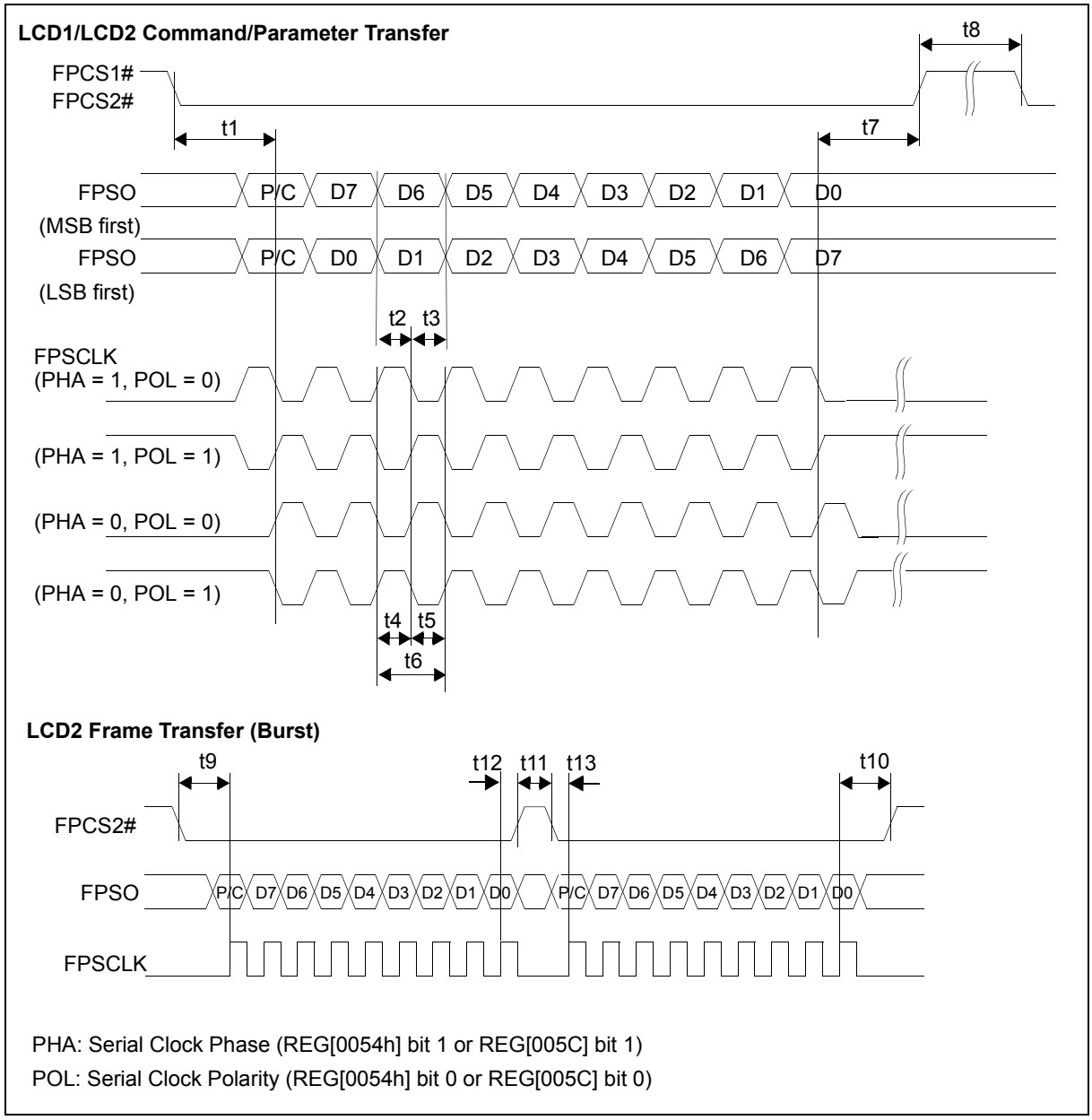


Figure 7-34: LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing

Table 7-51: LCD1 ND-TFD, LCD2 9-Bit Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time		1.5		Ts (Note 1)
t2	Data setup time		0.5		Ts
t3	Data hold time		0.5		Ts
t4	Serial clock pulse width low (high)		0.5		Ts
t5	Serial clock pulse width high (low)		0.5		Ts
t6	Serial clock period		1		Ts
t7	Chip select hold time		1.5		Ts
t8	Chip select de-assert to reassert		1		Ts
t9	Chip select setup time at beginning of burst mode		1.5		
t10	Chip select hold time at end of burst mode		1.5		Ts
t11	Chip select interval in burst mode		1		Ts
t12	Chip select hold time during burst mode		0.5		Ts
t13	Chip select setup time during burst mode		0.5		Ts

1. Ts = Serial clock period

7.4.4 LCD1 a-Si TFT Serial Interface Timing

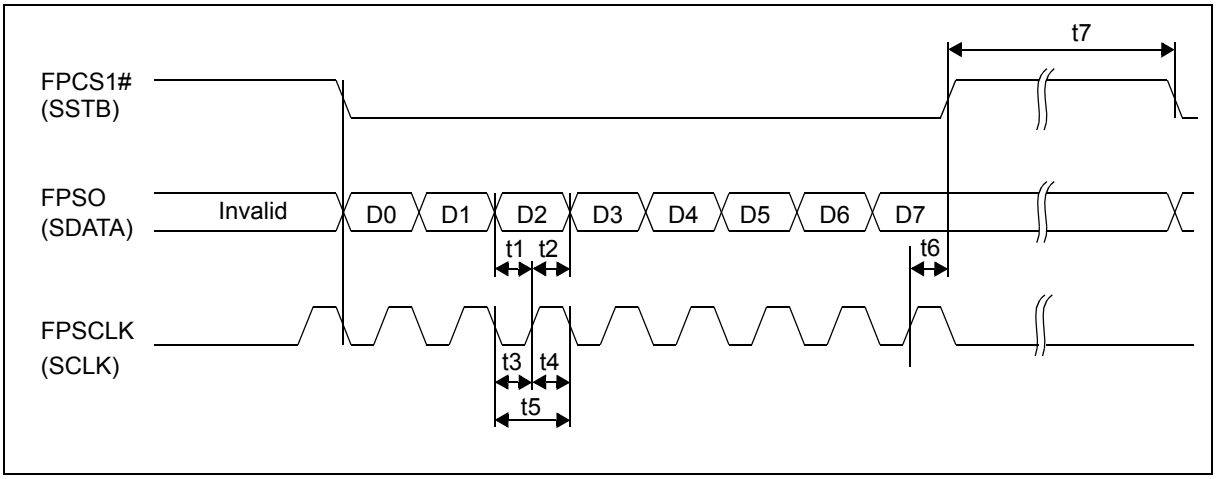


Figure 7-35: LCD1 a-Si TFT Serial Interface Timing

Table 7-52: LCD1 a-Si TFT Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Data Setup Time		0.5		Ts (Note 1)
t2	Data Hold Time		0.5		Ts
t3	Serial clock plus low period		0.5		Ts
t4	Serial clock pulse high period		0.5		Ts
t5	Serial clock period		1		Ts
t6	Chip select hold time		1.5		Ts
t7	Chip select de-assert to reassert		Note 2		Ts

1. Ts = Serial clock period
2. This setting depends on software

7.4.5 LCD1 uWIRE Serial Interface Timing

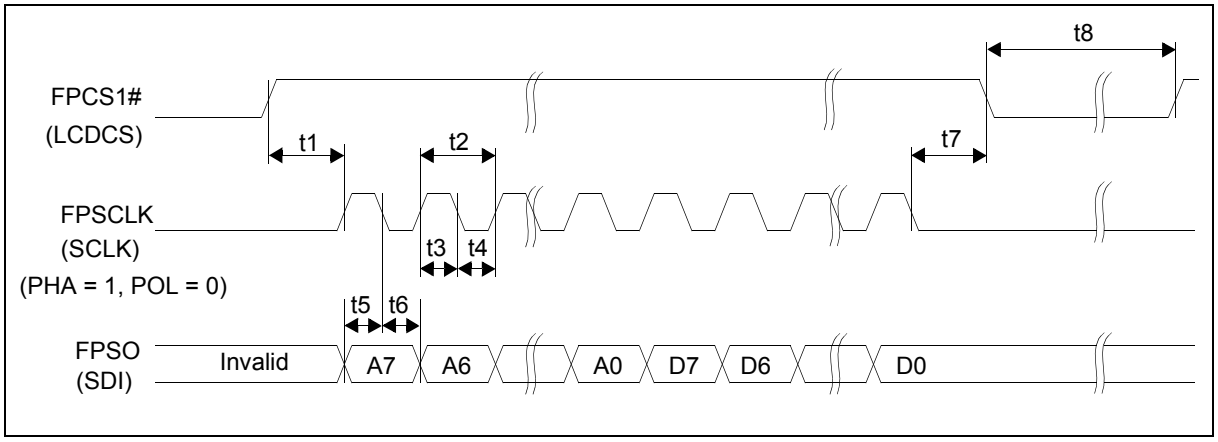


Figure 7-36: LCD1 uWIRE Serial Interface Timing

Table 7-53: LCD1 uWIRE Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time		1		Ts (Note 1)
t2	Serial Clock Period		1		Ts
t3	Serial clock pulse width low		0.5		Ts
t4	Serial clock pulse width high		0.5		Ts
t5	Data setup time		0.5		Ts
t6	Data hold time		0.5		Ts
t7	Chip select hold time		1		Ts
t8	Chip select de-assert to reassert		Note 2		Ts

1. Ts = Serial clock period
2. This setting depends on software

Note

When a uWire panel is selected (REG[0054h] bits 7-5 = 10x), FPCS1# idles high until the first uWire transfer is started. After the first transfer, FPCS1# idles low.

7.4.6 LCD1, LCD2 Parallel Interface Timing (80)

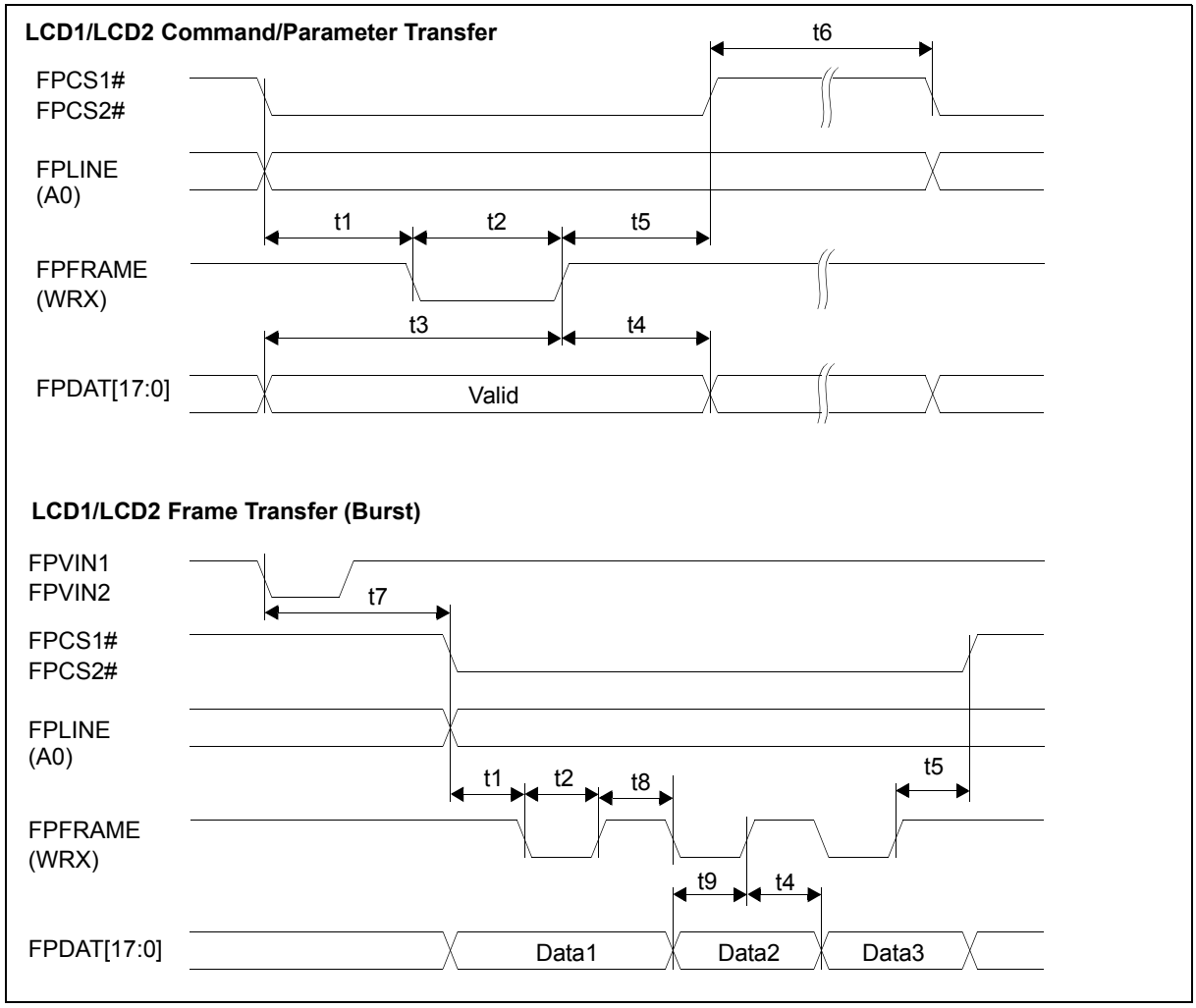


Figure 7-37: LCD1, LCD2 Parallel Interface Timing (80)

Table 7-54: LCD1, LCD2 Parallel Interface Timing (80)

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select falling edge to FPFRAME (WRX) falling edge		1		Ts (Note 1)
t2	FPFRAME (WRX) low period		1		Ts
t3	Data setup time for command/parameter transfers		1		Ts
t4	Data hold time		1		Ts
t5	Write signal rising edge to chip select rising edge		1		Ts
t6	Chip select de-assert to reassert		0		Ts
t7	Vertical sync input falling edge to chip select falling edge			51	Ts
t8	Write signal high period in burst cycle		1		Ts
t9	Data setup time for frame transfers		1		Ts

1. Ts = Pixel clock period

7.4.7 LCD1, LCD2 Parallel Interface Timing (68)

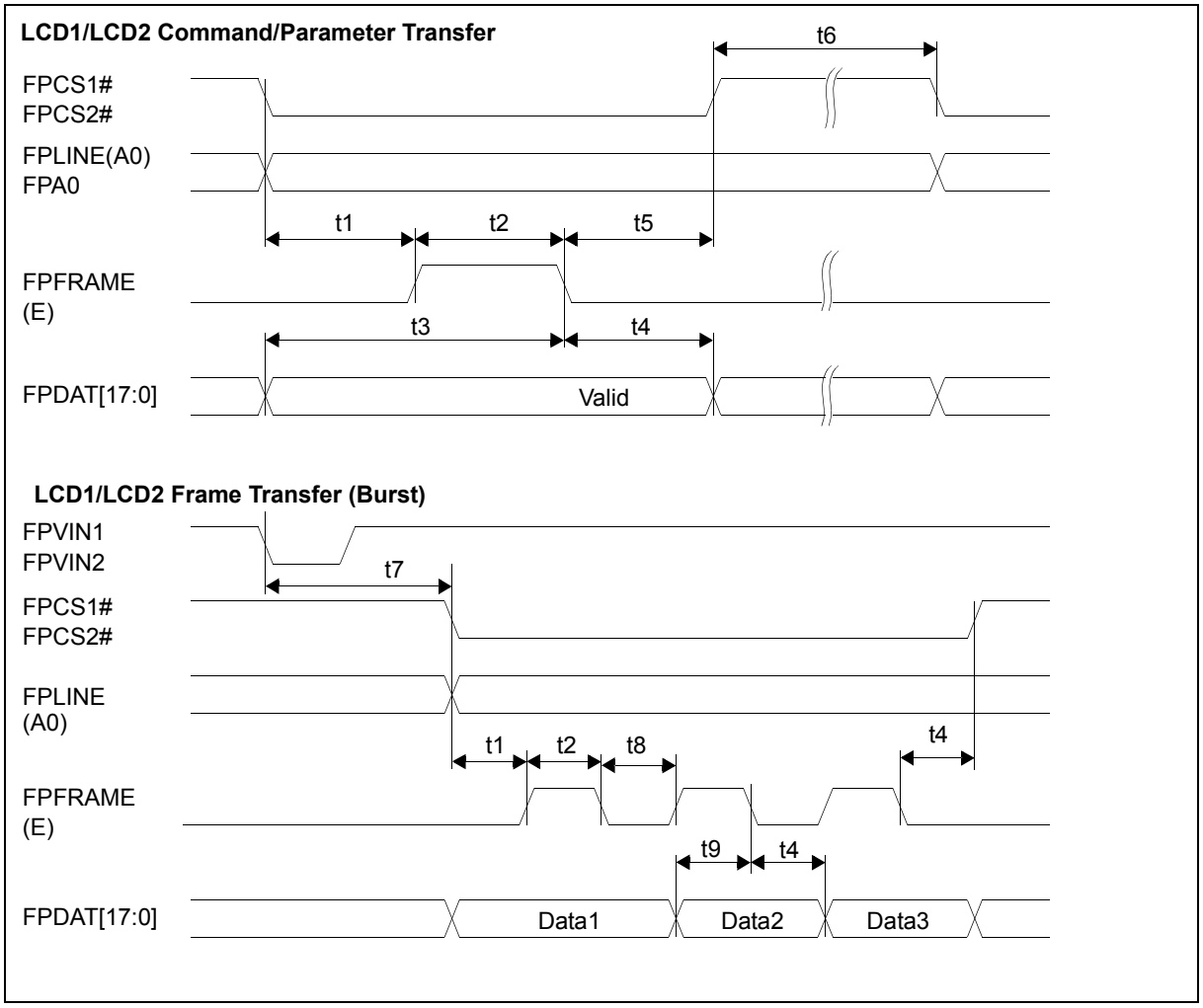


Figure 7-38: LCD1, LCD2 Parallel Interface Timing (68)

Table 7-55: LCD1, LCD2 Parallel Interface Timing (68)

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select falling edge to FPFRAME (E) rising edge		1		Ts (Note 1)
t2	FPFRAME (E) high period		1		Ts
t3	Data setup time for command/parameter transfers		1		Ts
t4	Data hold time		1		
t5	FPFRAME (E) falling edge to Chip select rising edge		1		Ts
t6	Chip select deassert to reassert		0		Ts
t7	Vertical sync input falling edge to chip select falling edge			51	Ts
t8	Enable signal low period in burst cycle		1		Ts
t9	Data setup time for frame transfers		1		Ts

1. Ts = Pixel clock period

7.5 Output Buffer Rise/Fall Time v.s. Capacitance (C_L)

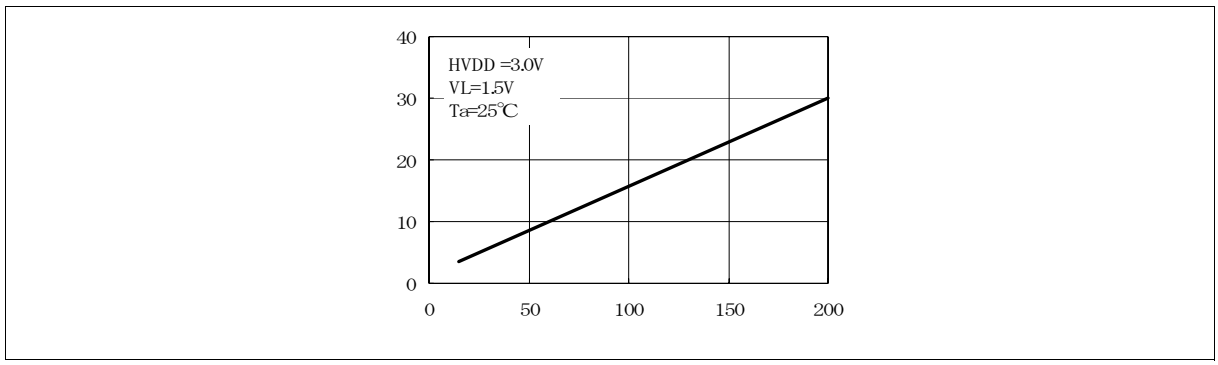


Figure 7-39: Rise Time v.s. Capacitance (C_L)

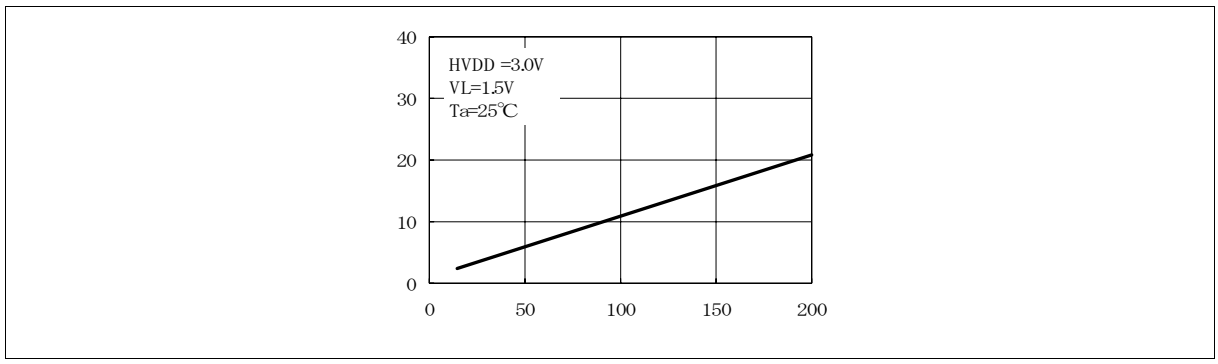


Figure 7-40: Fall Time V.s. Capacitance (C_L)

Table 7-56: Rise/Fall Time v.s. Capacitance (C_L)

C_L (pF)	Rise Time tr (10-90%) [ns]	Fall Time tf (10-90%) [ns]
15	3.413	2.390
50	8.446	5.833
100	15.670	10.840
150	22.910	15.840
200	30.140	20.850

7.6 Camera Interface Timing

7.6.1 Camera Interface Timing

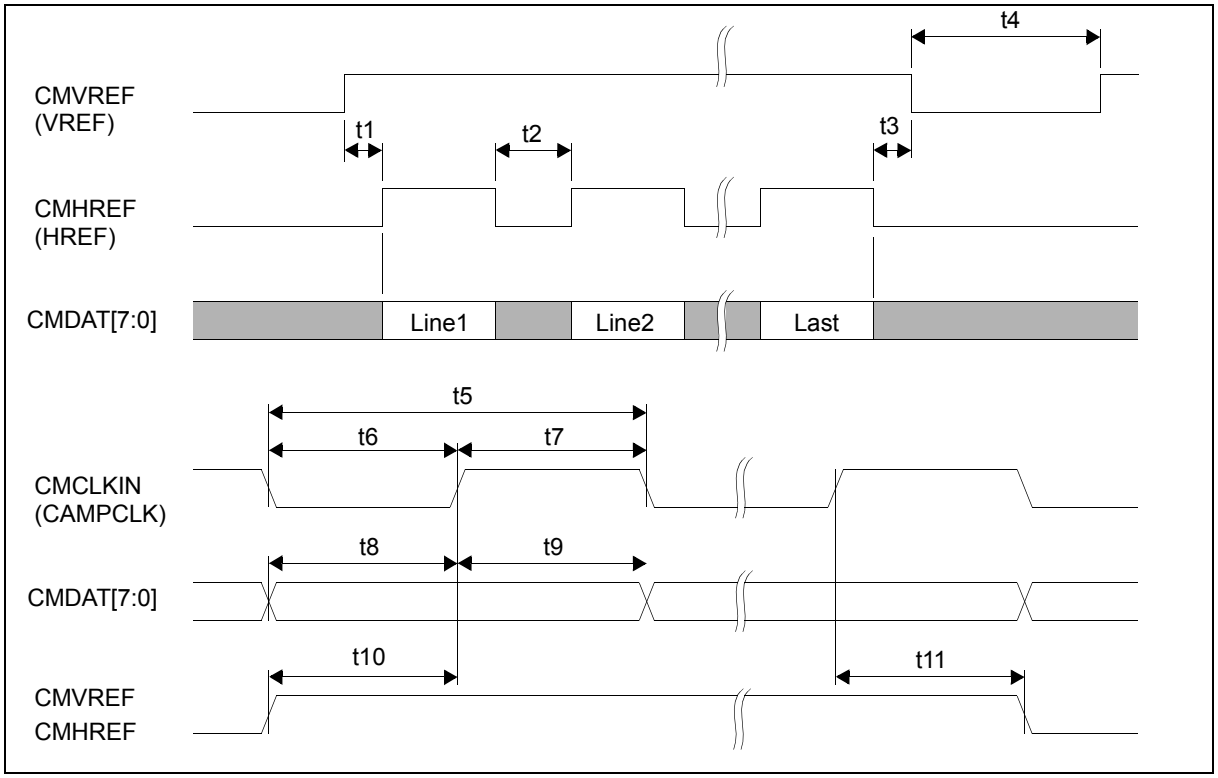


Figure 7-41: Camera Interface Timing

Table 7-57: Camera Interface Timing

Symbol	Parameter	Min	Max	Units
t1	CMVREF rising edge to CMHREF rising edge	0		Tc (note 1)
t2	Horizontal blank period	4		Tc
t3	CMHREF falling edge to CMVREF falling edge	0		Tc
t4	Vertical blank period	1		Line
t5	Camera input clock period	3		Ts (note 2)
t6	Camera input clock pulse width low	1.5		Ts
t7	Camera input clock pulse width high	1.5		Ts
t8	Data setup time	6		ns
t9	Data hold time	6		ns
t10	CMVREF, CMHREF setup time	10		ns
t11	CMVREF, CMHREF hold time	10		ns

1. Ts = System clock period
2. Tc = Camera block input clock period

7.6.2 Camera Clock Output Timing

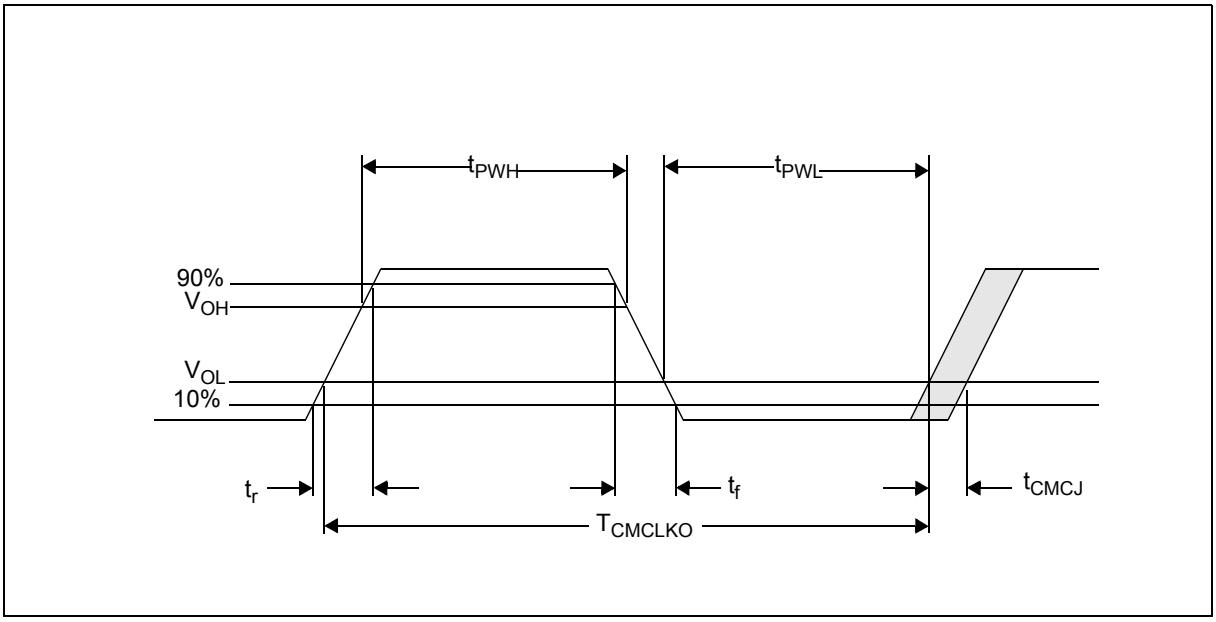


Figure 7-42: Camera Clock Output Timing

Table 7-58: Camera Clock Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{CMCLKO}	Camera output clock frequency			27.5 (Note 1)	MHz
T_{CMCLKO}	Camera output clock period	$1/f_{CMCLKO}$			ns
t_{PWH}	Camera output clock pulse width high	6			ns
t_{PWL}	Camera output clock pulse width low	6			ns
t_r	Camera output clock rising time (10% - 90%)			8 (Note 2)	ns
t_f	Camera output clock falling time (10% - 90%)			8 (Note 2)	ns
t_{CMCJ}	Camera output clock jitter	-2		2	%
t_{CMDUTY}	Camera output clock duty	40 (Note 3)		60 (Note 3)	%

1. System clock = 55MHz, Camera clock divide ratio = 2:1 (REG[0100h] bits 4-0 = 00001b)
2. Refer to Section 7.5, “Output Buffer Rise/Fall Time v.s. Capacitance (CL)” on page 100
3. t_{CMDUTY} Min = 45% and Max. = 55% if the camera clock is less than 13.75MHz (camera clock divide ratio greater than 4:1)

7.6.3 Strobe Timing

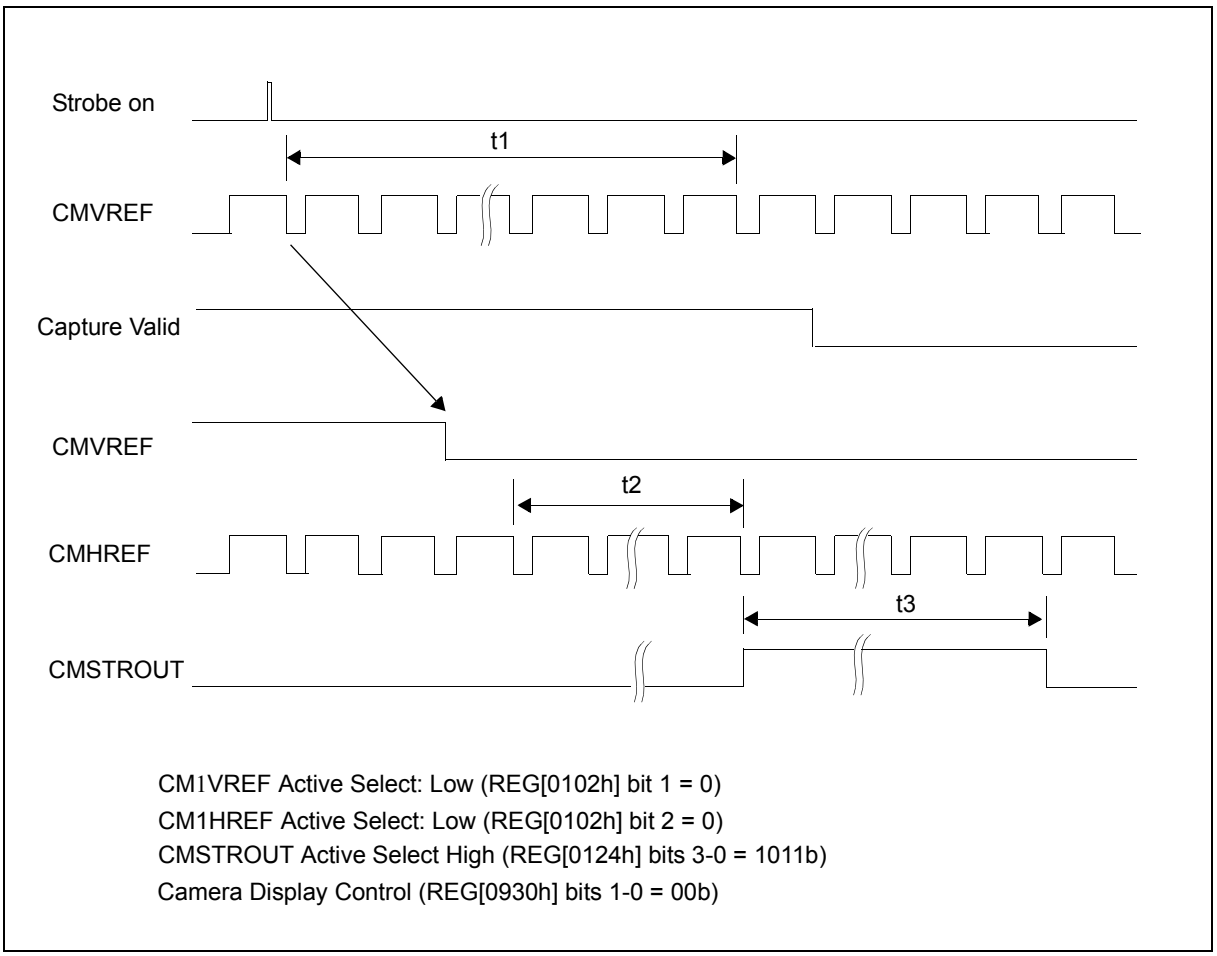


Figure 7-43: Strobe Control Output Timing

Table 7-59: Strobe Control Output Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	CM1VREF delay from strobe on	-	Note 1	-	TCMV
t2	CM1HREF delay from CMVREF active	-	Note 2	-	TCMH
t3	CMSTROUT active pulse width	-	Note 3	-	TCMH

1. This value is determined by REG[1024h]
2. This value is determined by REG[1020h]
3. This value is determined by REG[1022h]

7.7 SD Memory Card Interface

7.7.1 SD Memory Card Access

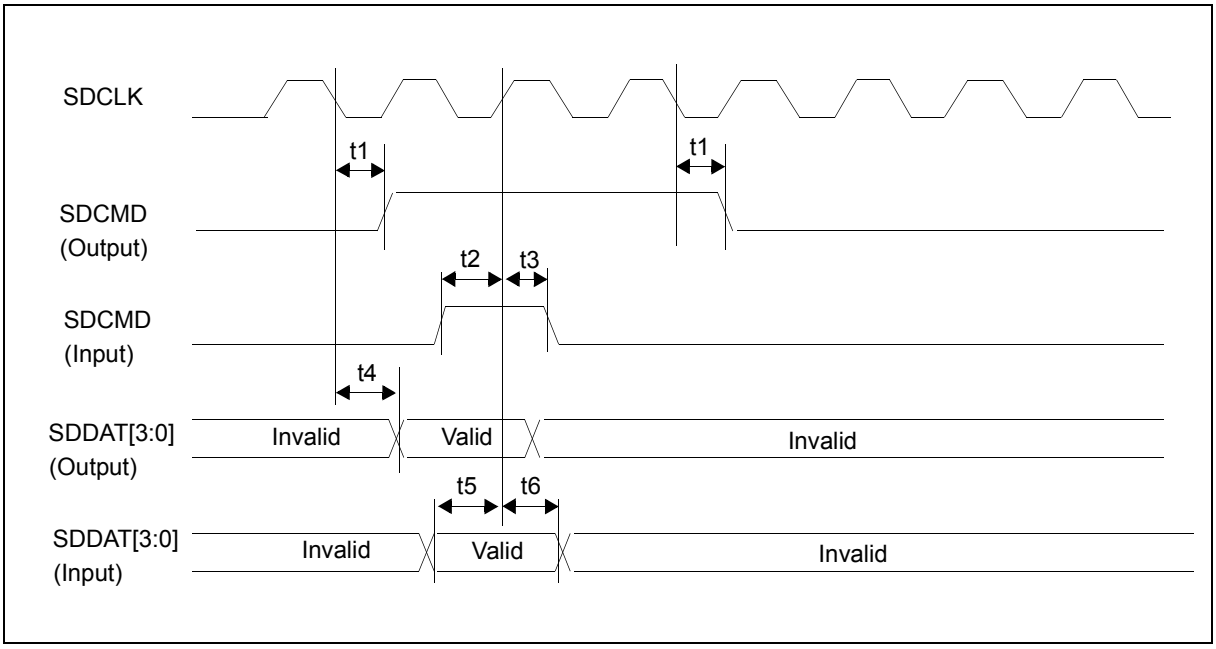


Figure 7-44: SD Memory Card Access Timing

Table 7-60: SD Memory Card Access Timing

Symbol	Parameter	Min	Max	Units
t1	SDCMD output delay time	-	20	ns
t2	SDCMD input setup time	10	-	ns
t3	SDCMD input hold time	5	-	ns
t4	SDDAT[3:0] output delay time	-	20	ns
t5	SDDAT[3:0] input setup time	10	-	ns
t6	SDDAT[3:0] input hold time	5	-	ns

7.7.2 SD Memory Card Clock Output

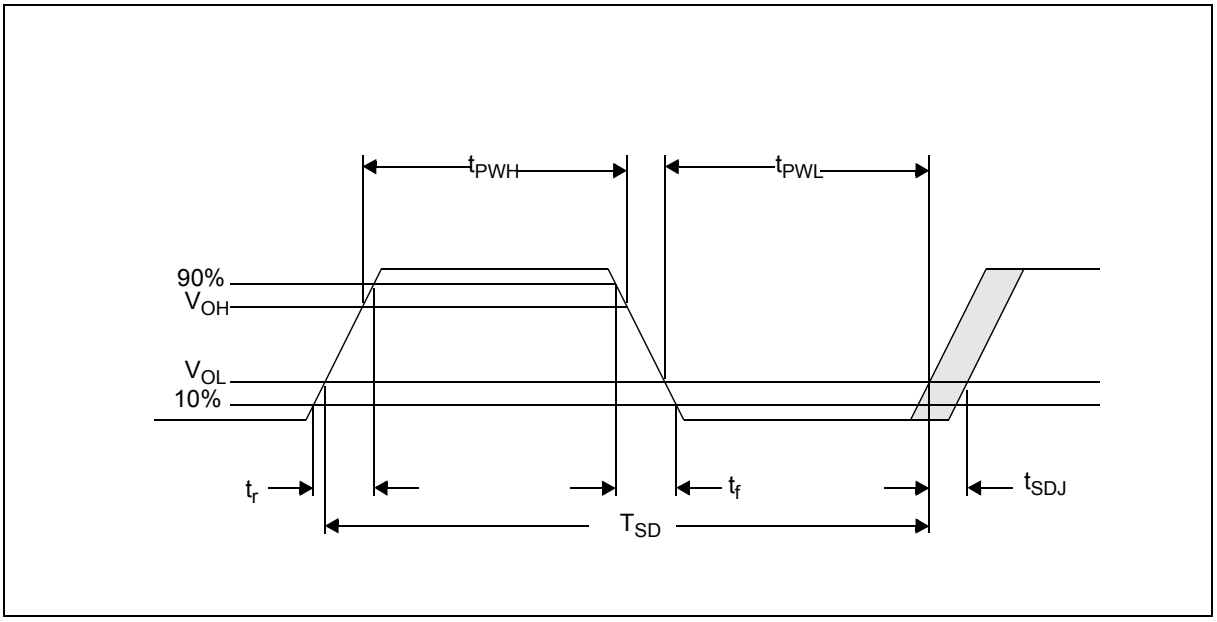


Figure 7-45: SD Memory Card Clock Output Timing

Table 7-61: SD Memory Card Clock Output Timing

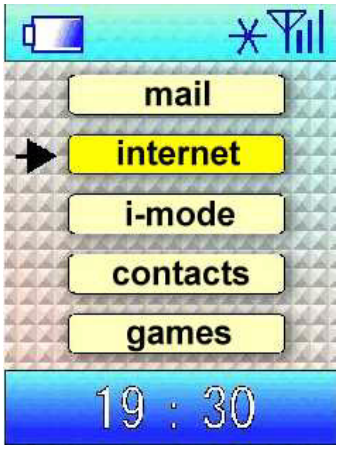
Symbol	Parameter	Min	Typ	Max	Units
f_{SD}	SDCLK frequency	-	-	13.75	MHz
T_{SD}	SDCLK period	-	$1/f_{SD}$	-	ns
t_{PWH}	SDCLK width high	10	-	-	ns
t_{PWL}	SDCLK width low	10	-	-	ns
t_r	SDCLK rising time (10% - 90%)	-	-	10	ns
t_f	SDCLK falling time (10% - 90%)	-	-	10	ns
t_{SDJ}	SDCLK jitter	-3	-	3	%
t_{SDD}	SCLK clock duty	40	-	10	%

8 Memory Allocation

8.1 Main Window Case 1

8.1.1 Environment

- Resolution: 176 x 240
- Color Depth: 8 bpp (LUT 1))
- Data Size: 41.25K bytes
- Image:



Display Image

Figure 8-1: Main Window Case 1 Image

- Memory Map:

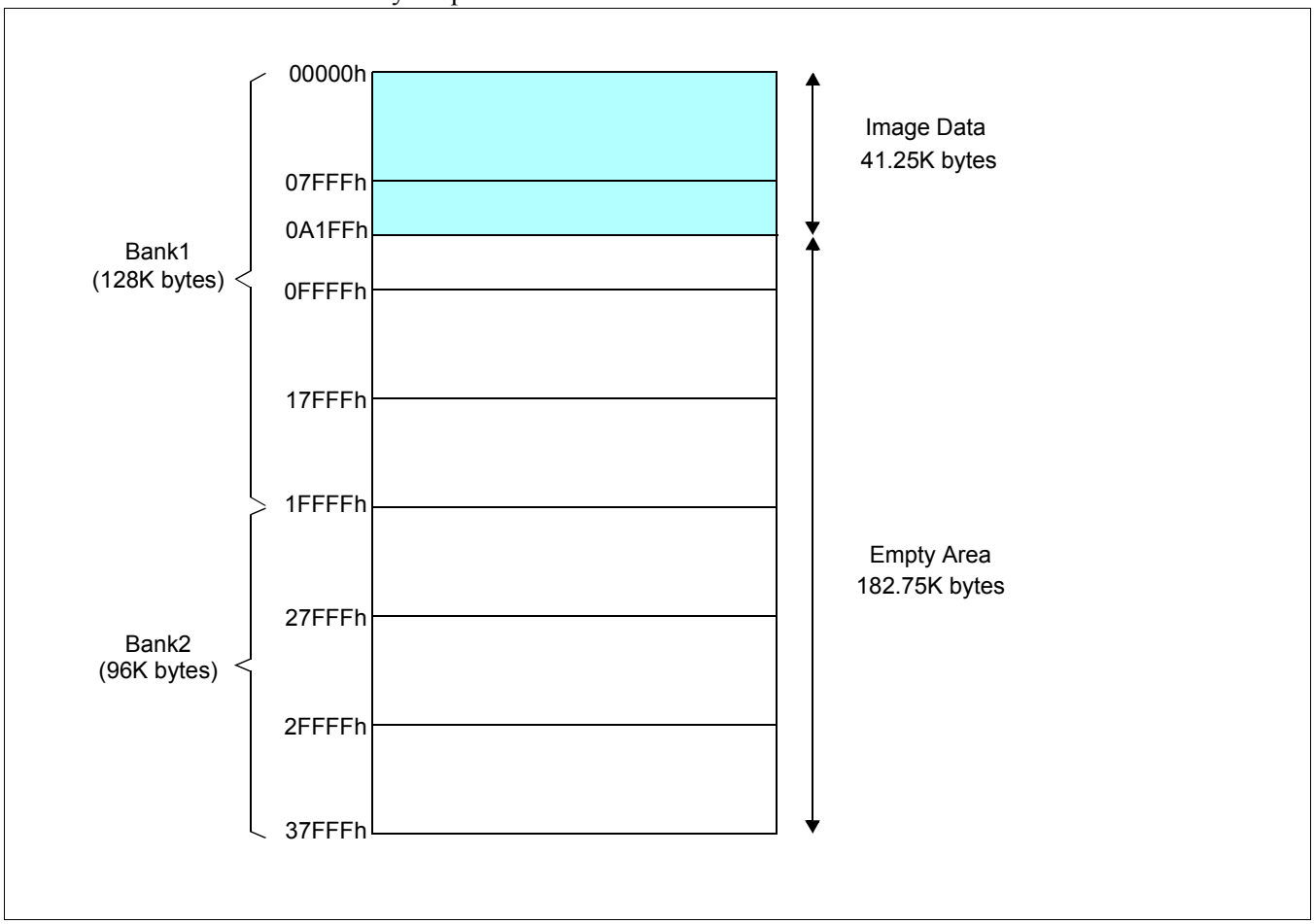


Figure 8-2: Memory Map for Main Window Case 1

8.2 Main Window Case 2

8.2.1 Environment

- Resolution: 176 x 240
- Color Depth: 16 bpp (LUT 1)
- Data Size: 82.5K bytes
- Image:

Display Image

Figure 8-3: Main Window Case 2 Image

- Memory Map:

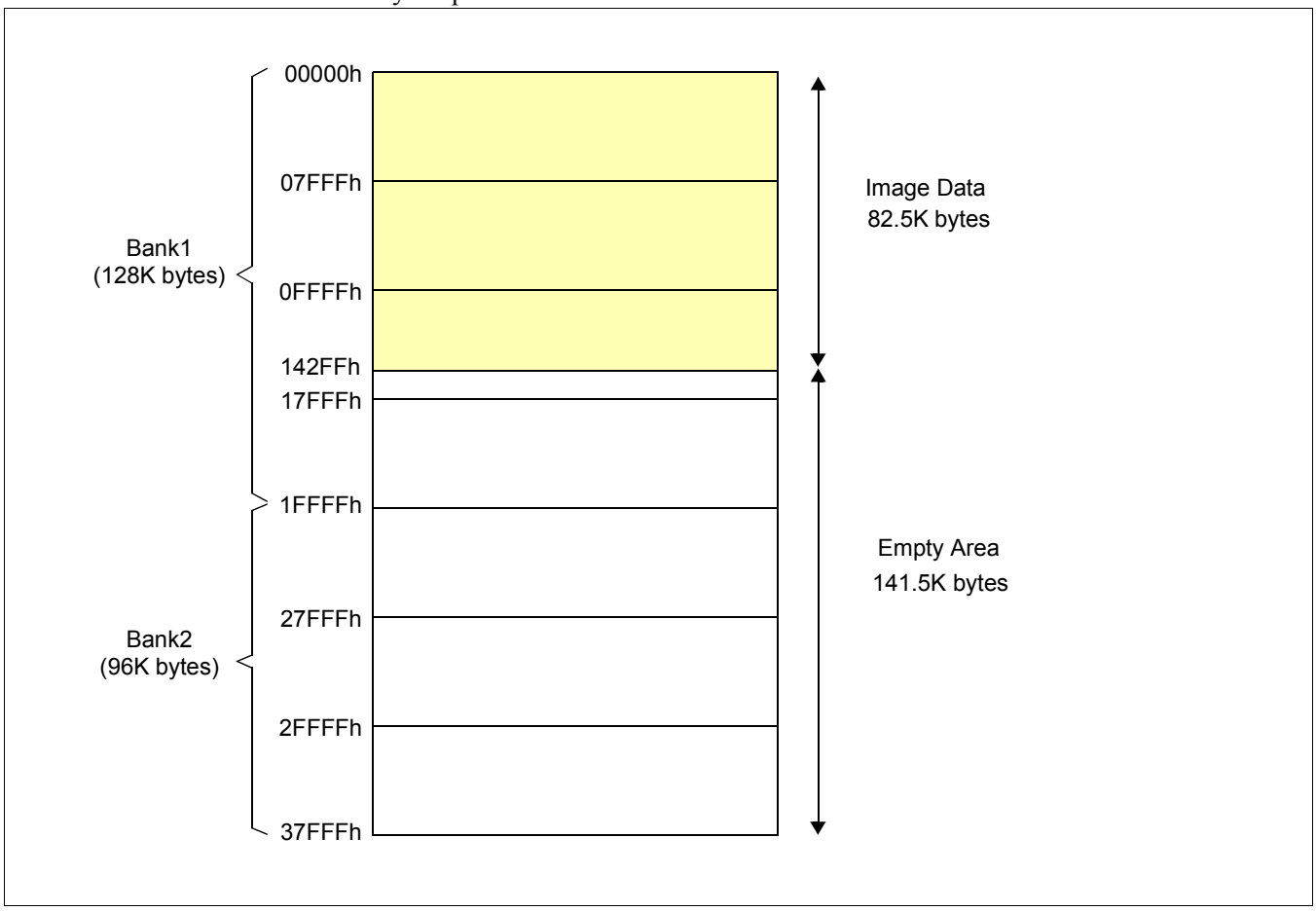


Figure 8-4: Memory Map for Main Window Case 2

8.3 Main Window, PIP+ Window, and Overlay Display

8.3.1 Environment

- Resolution:
  Main Window Image 176 x 240
  PIP+ Window Image 176 x 220
  Other panel sizes may be used within the limits of memory capacity.
- Color Depth:
  Main Window Image 8 bpp (LUT1)
  PIP+ Window Image 16 bpp (LUT2)
- Data Size:
  Main Window Image 41.25K bytes
  PIP+ Window Image 75.625K bytes
- Image:

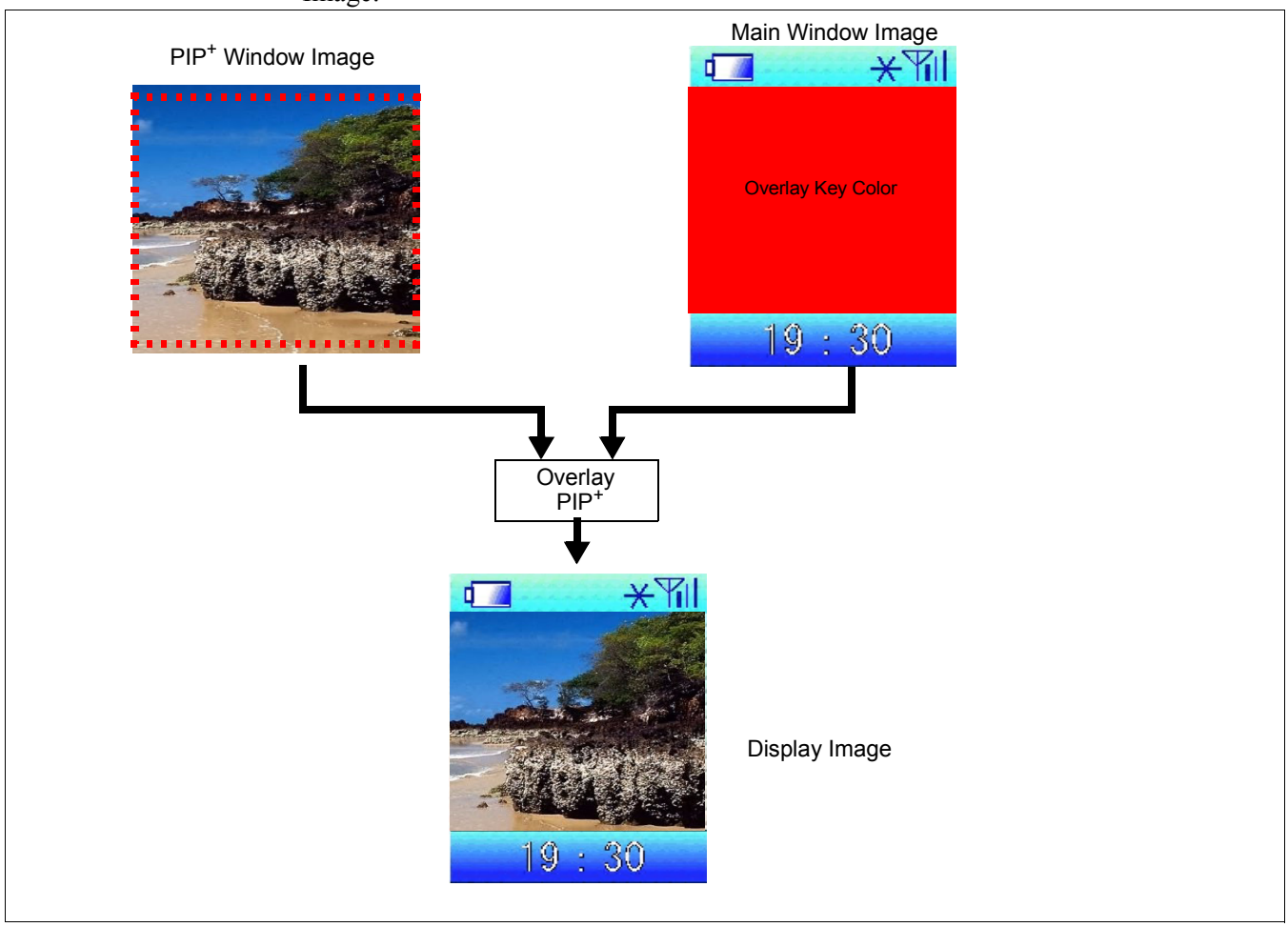


Figure 8-5: Main Window, PIP+ Window, and Overlay Display

- Memory Map:

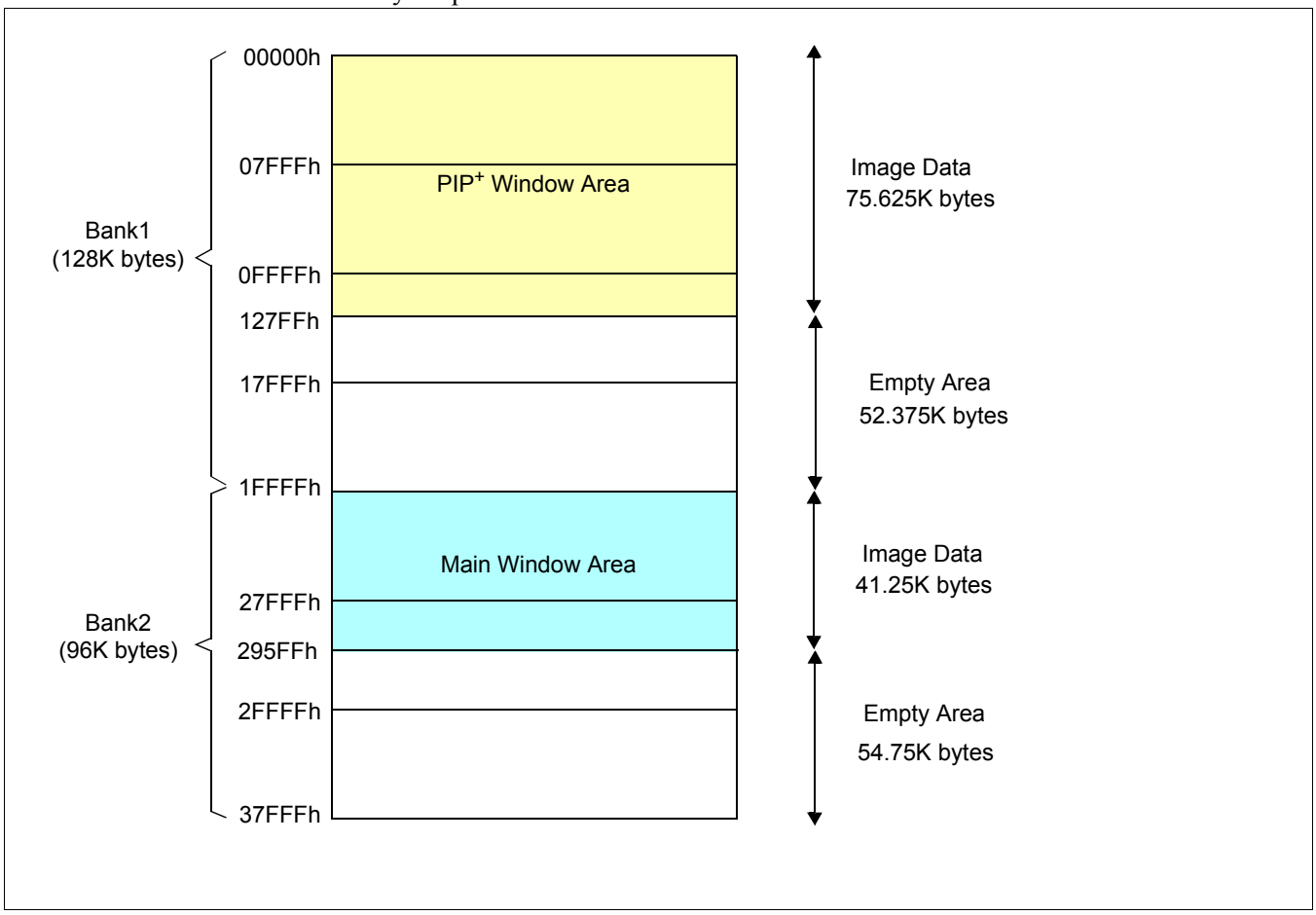


Figure 8-6: Memory Map for Main Window, PIP+ Window, and Overlay Display

8.4 Main Window, PIP+ Window, Overlay, and YUV

8.4.1 Environment

- Resolution:
  Main Window Image 176 x 240
  PIP+ Window Image 176 x 220, from Camera interface and resized
  Other panel sizes may be used within the limits of memory capacity.
- Color Depth:
  Main Window Image 8 bpp (LUT1)
  PIP+ Window Image 16 bpp (LUT2)
- Data Size:
  Main Window Image 41.25K bytes
  PIP+ Window Image 75.625K bytes
- Image:

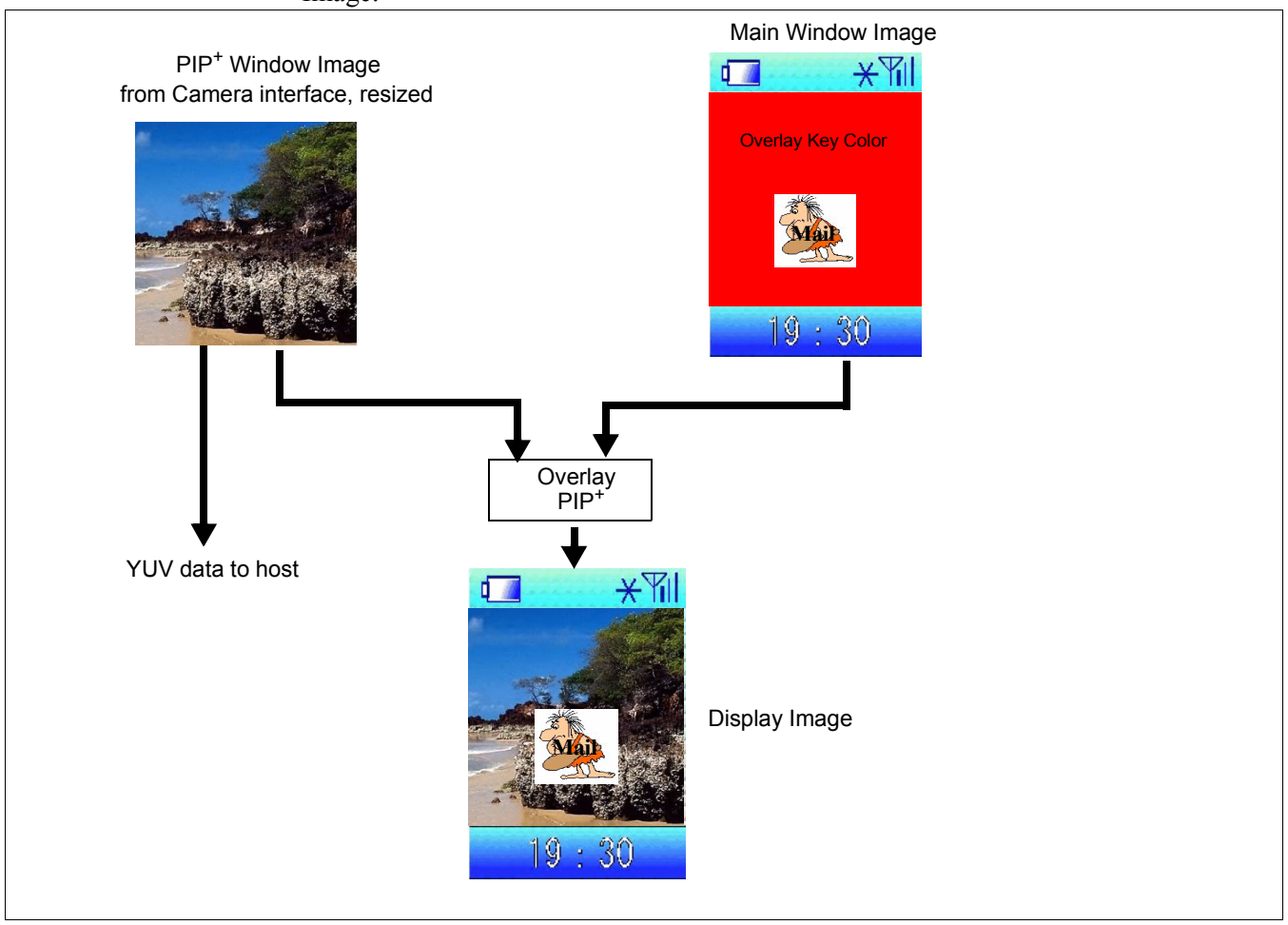


Figure 8-7: Main Window, PIP+ Window, Overlay, and YUV

- Memory Map:

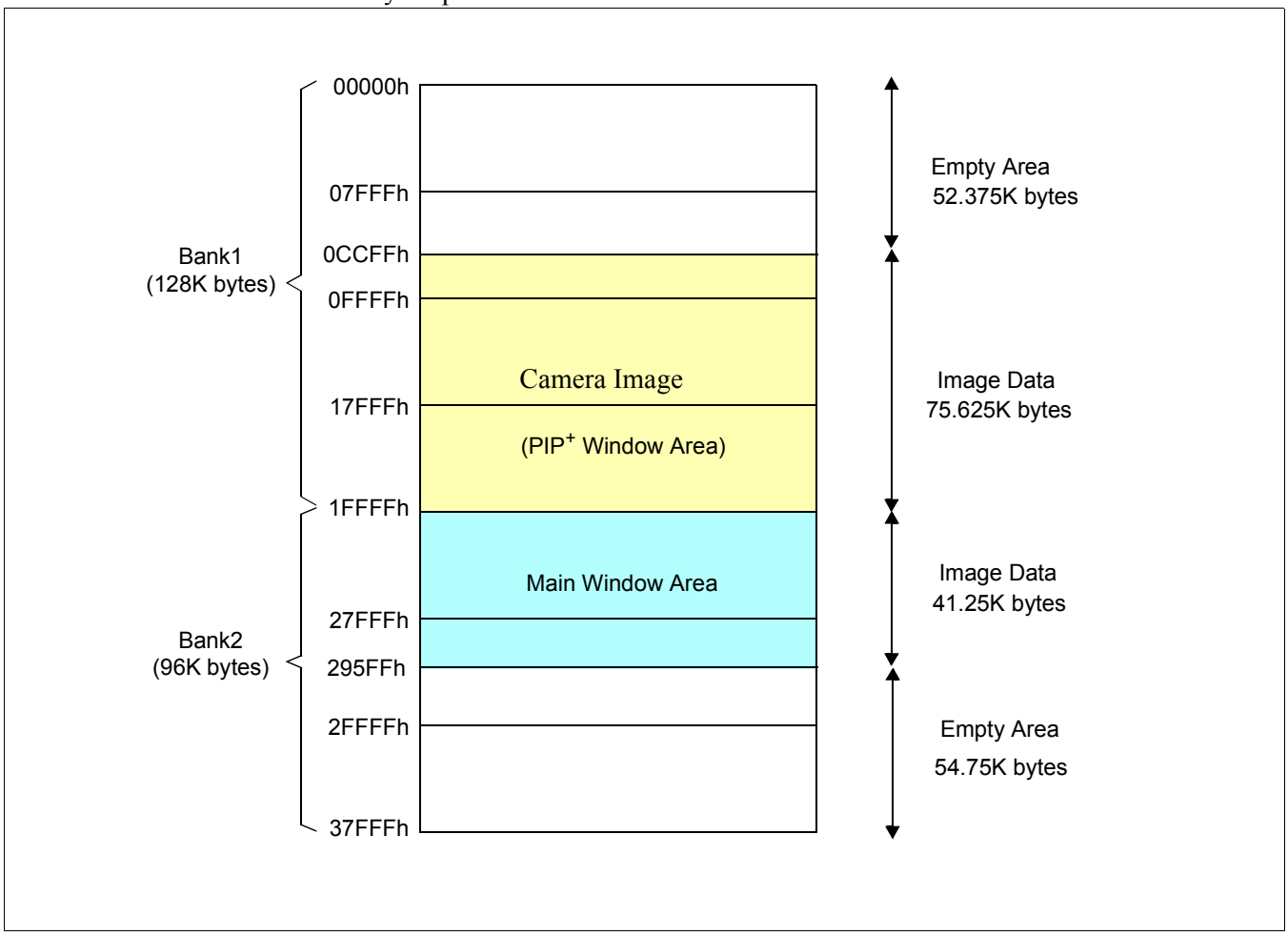


Figure 8-8: Memory Map for Main Window, PIP+ Window, Overlay, and YUV

8.5 Main Window, PIP+ Window, Overlay, and JPEG

8.5.1 Environment

- Resolution:
  Main Window Image 176 x 240
  PIP+ Window Image 176 x 220
  Other panel sizes may be used within the limits of memory capacity.
- Color Depth:
  Main Window Image 8 bpp (LUT1)
  PIP+ Window Image 16 bpp (LUT2)
- Data Size:
  Main Window Image 41.25K bytes
  PIP+ Window Image 75.625K bytes
- Image:

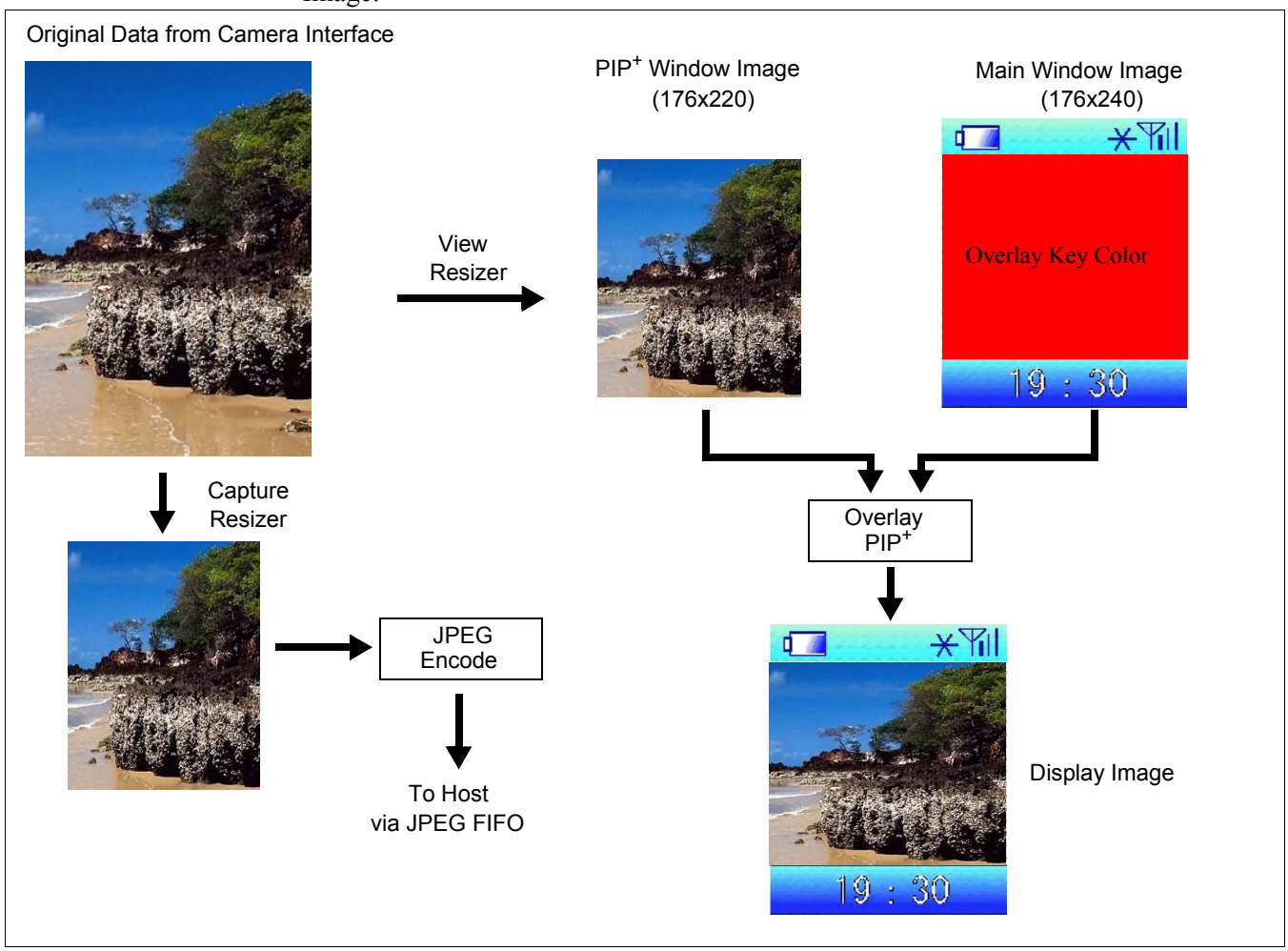


Figure 8-9: Main Window, PIP+ Window, Overlay, and JPEG

- Memory Map:

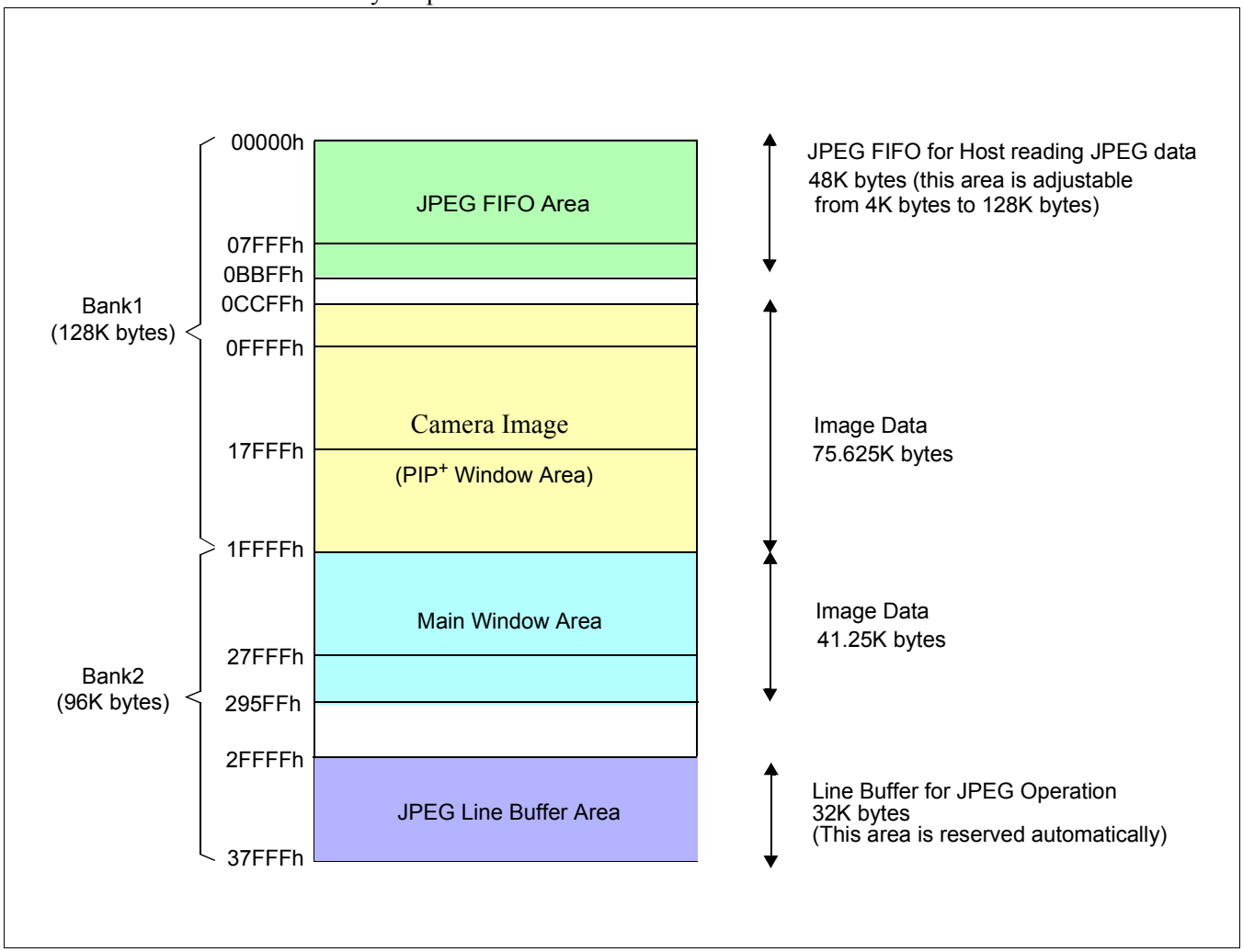


Figure 8-10: Memory Map for Main Window, PIP+ Window, Overlay and JPEG

9 Clocks

9.1 Clock Diagram

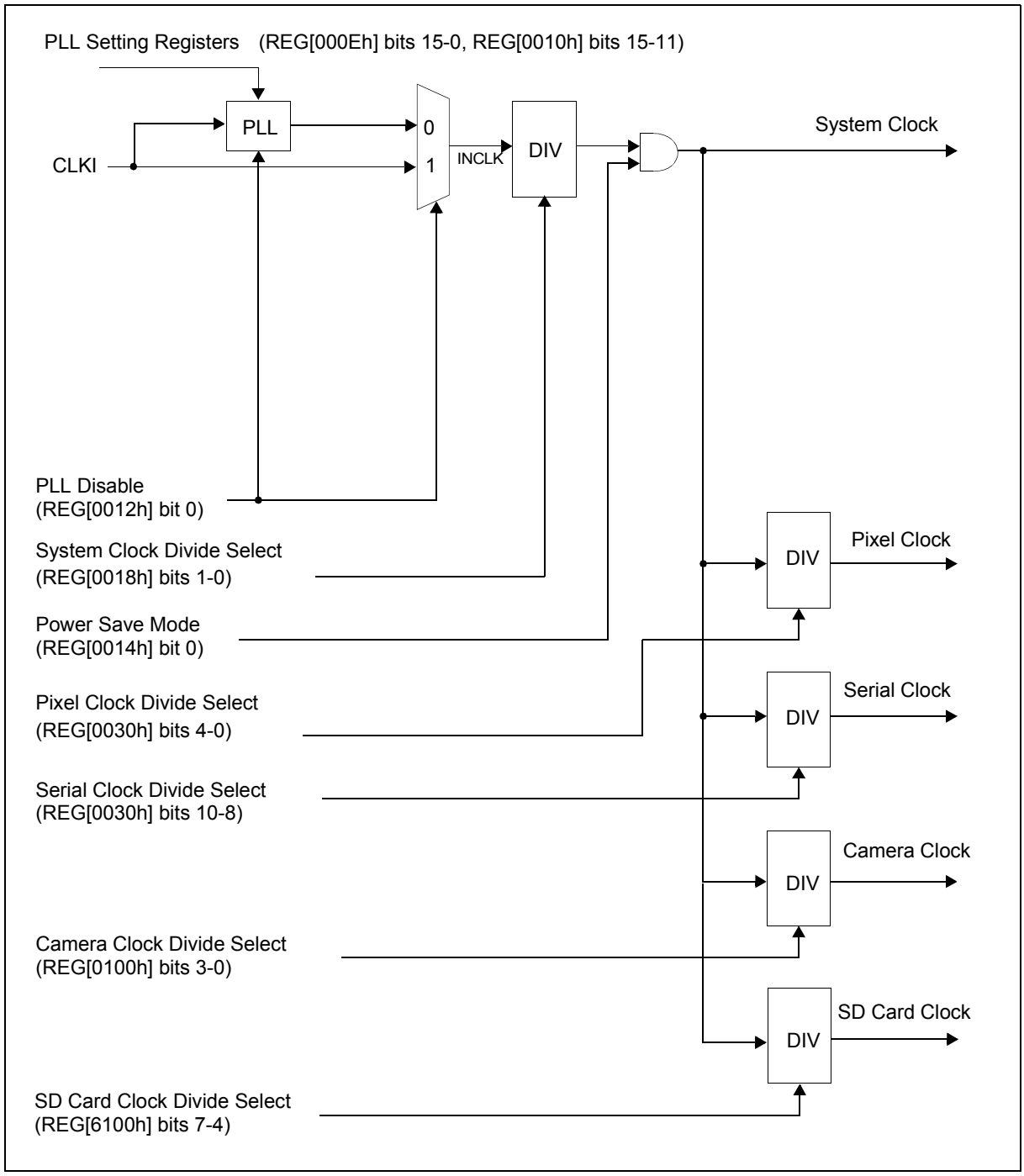


Figure 9-1: Clock Diagram

9.2 Clocks

9.2.1 System Clock

System clock (SYSCLK) is used for the S1D13717 internal main clock. The system clock source can be selected (REG[0012h] bits 2 and 0) from either the internal PLL or an external clock input (CLKI). The System Clock Divide Select bits (REG[0018h] bits 1-0) control this clock division. The system clock can be a divided down version of the output of the PLL or the input of CLKI.

9.2.2 Pixel Clock

Pixel clock (PCLK) is used for the LCD1 shift clock of a RGB type panel and for the LCD1/LCD2 parallel interface timing. The pixel clock source is always the system clock and can be divided using the Pixel Clock Divide Select bits (REG[0030h] bits 4-0).

9.2.3 Serial Clock

Serial clock (SCLK) is used for the LCD1 and LCD2 serial interfaces. The serial clock source is always the system clock and can be divided using the Serial Clock Divide Select bits (REG[0030h] bits 10-8).

9.2.4 Camera Clock

Camera clock (CAMCLK) is used for the Camera interface. The camera clock source is always the system clock and can be divided using the Camera Clock Divide Select bits (REG[0100h] bits 3-0).

Note
This clock can be output on CMCLKOUT to be used as the master clock of an external camera module attached to the Camera interface.

9.2.5 SD Memory Card Clock

The SD Memory Card clock is output to the external SD Memory Card as the SD Card Clock. The SD memory card clock source is always the system clock and can be divided using the SD Memory Card Clock Divide Select bits (REG[6100h] bits 7-4).

10 Registers

10.1 Register Mapping

The S1D13717 registers are memory-mapped. When the system decodes the input pins as CS# = 0 and M/R# = 0 (for 1 CS# mode), or CS# = 1 and M/R# = 0 (for 2 CS# mode), the registers may be accessed. The register space is decoded by AB[17:1] and BE#[1:0], and is mapped as follows.

Table 10-1: S1D13717 Register Mapping

M/R#	Address	Function
1	00000h to 37FFFh	SRAM memory
0	0000h to 0007h	System Configuration Registers
0	000Eh to 0019h	Clock Setting Registers
0	0020h to 002Bh	Indirect Interface Registers
0	0030h to 003Dh	LCD Panel Interface Setting Registers
0	0040h to 0057h	LCD1 Setting Registers
0	0058h to 005Fh	LCD2 Setting Registers
0	0100h to 0125h	Camera Interface Registers
0	0200h to 024Fh	Display Mode Setting Registers
0	0300h to 030Dh	GPIO Registers
0	0310h to 0329h	Overlay Registers
0	0400h to 08FFh	Look-Up Table Registers
0	0930h to 096Fh	Resizer Operation Registers
0	0980h to 098Bh	JPEG Module Registers
0	09A0h to 09BCh	JPEG FIFO Setting Registers
0	09C0h to 09E1h	JPEG Line Buffer Setting Registers
0	0A00h to 0A41h	Interrupt Control Registers
0	0F00h to 0F01h	JPEG Encode Performance Register
0	1000h to 17A3h	JPEG Codec Registers
0	6000h to 613Fh	SD Memory Card Interface Registers
0	8000h to 8033h	2D BitBLT Registers
0	10000h	2D Accelerator Data Port

10.2 Register Set

The S1D13719 registers are listed in the following table.

Table 10-2: S1D13717 Register Set

Register	Pg	Register	Pg
System Configuration Registers			
REG[0000h] Product Information Register	124	REG[0002h] Configuration Pins Status Register	124
REG[0006h] Bus Timeout Setting Register	125		
Clock Setting Registers			
REG[000Eh] PLL Setting Register 0	126	REG[0010h] PLL Setting Register 1	128
REG[0012h] PLL Setting Register 2	128	REG[0014h] Miscellaneous Configuration Register	129
REG[0016h] Software Reset Register	131	REG[0018h] System Clock Setting Register	131
Indirect Interface Registers			
REG[0020h] is Reserved	132	REG[0022h] Indirect Interface Memory Address Register 1	132
REG[0024h] Indirect Interface Memory Address Register 2	132	REG[0026h] Indirect Interface Auto Increment Register	133
REG[0028h] Indirect Interface Memory Access Port Register	133	REG[002Ah] Indirect Interface 2D BitBLT Data Read/Write Port Register	133
LCD Panel Interface Generic Setting Registers			
REG[0030h] LCD Interface Clock Setting Register	134	REG[0032h] LCD Module Clock Setting Register	136
REG[0034h] LCD Interface Command Register	137	REG[0036h] LCD Interface Parameter Register	138
REG[0038h] LCD Interface Status Register	138	REG[003Ah] LCD Interface Frame Transfer Register	139
REG[003Ch] LCD Interface Transfer Setting Register	139		
LCD1 Setting Register			
REG[0040h] LCD1 Horizontal Total Register	141	REG[0042h] LCD1 Horizontal Display Period Register	141
REG[0044h] LCD1 Horizontal Display Period Start Position Register	142	REG[0046h] LCD1 FPLINE Register	142
REG[0048h] LCD1 FPLINE Pulse Position Register	142	REG[004Ah] LCD1 Vertical Total Register	143
REG[004Ch] LCD1 Vertical Display Period Register	143	REG[004Eh] LCD1 Vertical Display Period Start Position Register	143
REG[0050h] LCD1 FPFRAME Register	144	REG[0052h] LCD1 FPFRAME Pulse Position Register	144
REG[0054h] LCD1 Serial Interface Setting Register	145	REG[0056h] LCD1 Parallel Interface Setting Register	146
LCD2 Setting Registers			
REG[0058h] LCD2 Horizontal Display Period Register	148	REG[005Ah] LCD2 Vertical Display Period Register	148
REG[005Ch] LCD2 Serial Interface Setting Register	148	REG[005Eh] LCD2 Parallel Interface Setting Register	149
REG[0070h] through REG[00FEh] are Reserved	150		
Camera Interface Setting Register			
REG[0100h] Camera Clock Setting Register	151	REG[0102h] Camera Signal Setting Register	151
REG[0104h] through REG[010Eh] are Reserved	152	REG[0110h] Camera Mode Setting Register	153
REG[0112h] Camera Frame Setting Register	155	REG[0114h] Camera Control Register	156
REG[0116h] Camera Status Register	157	REG[0120h] Strobe Line Delay Register	159
REG[0122h] Strobe Pulse Width Register	159	REG[0124h] Strobe Control Register	160
REG[0128h] through REG[012Fh] are Reserved	161		

Table 10-2: S1D13717 Register Set

Table 10-2: S1D13717 Register Set

Table 10-2: S1D13717 Register Set

Register	Pg	Register	Pg
SD Memory Card Interface Registers			
REG[6000h] SD Memory Card Configuration Register 0	261	REG[6002h] SD Memory Card Configuration Register 1	262
REG[6004h] SD Memory Card Configuration Register 2	264	REG[6100h] SD Memory Card Control Register 0	266
REG[6102h] SD Memory Card Control Register 1	267	REG[6104h] SD Memory Card Function Register	268
REG[6106h] SD Memory Card Status Register	270	REG[6108h] SD Memory Card Data Length Register 0	272
REG[610Ah] SD Memory Card Data Length Register 1	272	REG[610Ch] SD Memory Card Command Register	272
REG[610Eh] SD Memory Card Timer Register	272	REG[6110h] SD Memory Card Parameter Register 0	273
REG[6112h] SD Memory Card Parameter Register 1	273	REG[6114h] SD Memory Card Parameter Register 2	273
REG[6116h] SD Memory Card Parameter Register 3	273	REG[6118h~611Eh] SD Memory Card Data Register	274
REG[6120h] SD Memory Card Response Register 0	274	REG[6122h] SD Memory Card Response Register 1	274
REG[6124h] SD Memory Card Response Register 2	275	REG[6126h] SD Memory Card Response Register 3	275
REG[6128h] SD Memory Card Response Register 4	275	REG[612Ah] SD Memory Card Response Register 5	275
REG[612Ch] SD Memory Card Response Register 6	276	REG[612Eh] SD Memory Card Response Register 7	276
REG[6130h] SD Memory Card Response Register 8	276	REG[6132h] SD Memory Card Response Register 9	276
REG[6134h] SD Memory Card Response Register A	277	REG[6136h] SD Memory Card Response Register B	277
REG[6138h] SD Memory Card Response Register C	277	REG[613Ah] SD Memory Card Response Register D	277
REG[613Ch] SD Memory Card Response Register E	278	REG[613Eh] SD Memory Card Response Register F	278
2D BitBLT Registers			
REG[8000h] BitBLT Control Register 0	279	REG[8002h] BitBLT Control Register 1	279
REG[8004h] BitBLT Status Register 0	280	REG[8006h] is Reserved	280
REG[8008h] BitBLT Command Register 0	281	REG[800Ah] BitBLT Command Register 1	282
REG[800Ch] BitBLT Source Start Address Register 0	283	REG[800Eh] BitBLT Source Start Address Register 1	283
REG[8010h] BitBLT Destination Start Address Register 0	284	REG[8012h] BitBLT Destination Start Address Register 1	284
REG[8014h] BitBLT Memory Address Offset Register	284	REG[8018h] BitBLT Width Register	284
REG[801Ch] BitBLT Height Register	285	REG[8020h] BitBLT Background Color Register	285
REG[8024h] BitBLT Foreground Color Register	285	REG[8030h] BitBLT Interrupt Status Register	285
REG[8032h] BitBLT Interrupt Control Register	286	REG[10000h] 2D BitBLT Data Memory Mapped Region Register	286

10.3 Register Restrictions

All reserved bits must be set to 0 unless otherwise specified. Writing a value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect.

Some registers are only accessible when certain conditions exist. Any attempts to read/write in-accessible registers are invalid. The following restrictions apply to all registers.

- REG[0000h] - REG[0018h] and REG[0300h] - REG[030Ch] are always accessible.
- REG[0000h] - REG[0018h] are not reset by a Software Reset.
- When power save mode is enabled (REG[0014h] bit 0 = 1), REG[0030h] - REG[0F00h] are not accessible.
- When the JPEG Codec is disabled (REG[0980h] bit 0 = 0), REG[1000h] - REG[17A2h] are not accessible.
- When the SD Card Interface is disabled (REG[6000h] bit 0 = 0), REG[6100h] - REG[613Eh] are not accessible.

10.4 Register Description

10.4.1 System Configuration Registers

REG[0000h] Product Information Register
Default = 3864h — Read Only

15	14	13	12	11	10	9	8
Display Buffer Size bits 7-0							
7	6	5	4	3	2	1	0
Product Code bits 5-0						Revision Code bits 1-0	

bits 15-8 Display Buffer Size bits [7:0] (Read Only)
These bits indicate the size of the SRAM display buffer measured in 4K byte increments. The S1D13717 display buffer is 224K bytes and these bits return a value of 56 (38h).

REG[0000h] bits 15-8 = display buffer size ÷ 4K bytes
= 224K bytes ÷ 4K bytes
= 56 (38h)

bits 7-2 Product Code bits [5:0] (Read Only)
These bits indicate the product code. The product code for the S1D13717 is 011001b (19h).

bits 1-0 Revision Code bits [1:0] (Read Only)
These bits indicate the revision code. The revision code is 00b.

REG[0002h] Configuration Pins Status Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a	CNF[6:0] Status						

bits 6-0 CNF[6:0] Status (Read Only)
These status bits return the status of the configuration pins CNF[6:0]. CNF[6:0] are latched at the rising edge of RESET#. For a functional description of each configuration bit (CNF[6:0]), see Section 5.3, “Summary of Configuration Options” on page 42.

REG[0006h] Bus Timeout Setting Register
Default = 0000h Read/Write

n/a							
15	14	13	13	11	10	9	8
n/a					Bus Timeout Reset Interrupt Status (RO)	Bus Timeout Reset Disable	Bus Timeout Reset Interrupt Disable
7	6	5	4	3	2	1	0

bit 2 Bus Timeout Reset Interrupt Status (Read Only).
This is the status bit for the bus timeout reset function. Bus timeout reset occurs when the WAIT# signal is active for 2 or 3 cycles.
This is the status bit for the bus timeout function.
When this bit = 1, a bus timeout has occurred.
When this bit = 0, a bus timeout has not occurred.

This flag is cleared by the Bus Timeout Reset Interrupt Disable bit (REG[0006h] bit 0).

bit 1 Bus Timeout Reset Disable
This bit controls the Bus Timeout Reset function of the S1D13717. If a bus timeout occurs, the Bus Timeout Reset Interrupt Status is set (REG[0006h] bit 2) and the chip is reset.
When this bit = 0, the bus timeout reset function is enabled (default).
When this bit = 1, the bus timeout reset function is disabled.

Note
When the internal PLL is disabled (REG[0012h] bit 0 = 1), the Bus Timeout function must be disabled (REG[0006h] bit 1 = 1).

bit 0 Bus Timeout Reset Interrupt Disable
This bit controls the bus timeout reset interrupt and is used to clear the Bus Timeout Reset Interrupt Status (REG[0006h] bit 2).
When this bit = 0, the Bus Timeout Interrupt is enabled (default).
When this bit = 1, the Bus Timeout Interrupt is disabled.

When this bit is written as 1, the Bus Timeout Flag (REG[0006h] bit 2) is cleared.

10.4.2 Clock Setting Registers

REG[000Eh] PLL Setting Register 0
Default = 1BE8h — Read/Write

N-Counter bits 3-0				L-Counter bits 9-6			
15	14	13	12	11	10	9	8
L-Counter bits 5-0						V-Divider bits 1-0	
7	6	5	4	3	2	1	0

Note
Before setting this register, power save mode must be enabled (REG[0014h] bit 0 = 1) and the PLL must be disabled (REG[0012h] bit 0 = 1). For more information, see Figure 11-1: "Power-On/Power-Off Sequence," on page 287 or Figure 11-2: "Power Modes," on page 288.

bits 15-12 N-Counter bits [3:0]
bits 11-2 L-Counter bits [9:0]
These bits are used together to configure the PLL Output (in MHz) and must be set according to the following formula.

PLL Output = (N-Counter +1) x (L-Counter +1) x CLKI
= NN x LL x CLKI

Where:
PLL Output is the desired PLL output frequency in MHz (55MHz max)
N-Counter is the value in bits 15-12
L-Counter is the value in bits 11-2
CLKI is the PLL reference frequency (should always be 32.768kHz)

Table 10-3: PLL Setting Example

Target Freq. (MHz)	NN	LL	NN x LL	REG[000Eh]	POUT (MHz)
40	4	305	1220	34C0h	39.98
45	6	229	1374	5390h	45.02
48.76	16	93	1488	F194h	48.76
50	15	122	1830	E1E4h	49.97
54	16	103	1648	F198h	54.00
55	2	839	1678	1D18h	54.98

Note
To optimize power consumption, use the largest NN value possible.

bits 1-0 V-Divider bits [1:0]

These bits are used to fine tune the PLL output jitter. The V-Divider bits represent a value as shown in the following table. The V-Divider bits must be set such that the following formula is valid.

100MHz ≤ PLL Output x V-Divider ≤ 410MHz

Table 10-4: V-Divider

REG[000Eh] bits 1-0	V-Divider
00	see note
01	2
10	4
11	8

Where:

PLL Output in MHz (55MHz max) generated by bits 15-12 (N-Counter) and bits 11-2 (L-Counter)

V-Divide is the value from Table 10-4:

Note

Setting the V-Divider value to 00 provides the lowest possible power consumption, but the most jitter. Specific system design requirements should be considered to achieve the optimal setting.

REG[0010h] PLL Setting Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
VCO Kv Set bits 3-0				n/a			
7	6	5	4	3	2	1	0
n/a							

Note
Before setting this register, power save mode must be enabled (REG[0014h] bit 0 = 1) and the PLL must be disabled (REG[0012h] bit 0 = 1). For more information, see Figure 11-1: "Power-On/Power-Off Sequence," on page 287 or Figure 11-2: "Power Modes," on page 288.

bits 15-12 VCO Kv Set bits [3:0]

These bits are used to fine tune the PLL output jitter. These bits should be set as follows.

If 100MHz ≤ (PLL Output x V-Divider) ≤ 200MHz, set these bits to 0010.
If 200MHz < (PLL Output x V-Divider) ≤ 300MHz, set these bits to 0101.
If 300MHz < (PLL Output x V-Divider) ≤ 410MHz, set these bits to 0111.
All other non-zero values for these bits are reserved.

Where:

PLL Output is the desired PLL output frequency in MHz and is generated using REG[000Eh] bits 15-12 and REG[000Eh] bits 11-2
V-Divide is the value from Table 10-4: and is controlled by REG[000Eh] bits 1-0

Note
Setting the value of these bits to 0000 provides the lowest possible power consumption, but the most jitter. Specific system design requirements should be considered to achieve the optimal setting.

REG[0012h] PLL Setting Register 2
Default = 0001h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a					Reserved	Reserved	PLL Disable

Note
For more information on the PLL and clock structure, see Section 9, "Clocks" on page 116.

bit 2 Reserved
The default value for this bit is 0.

bit 1 Reserved
The default value for this bit is 0.

bit 0 PLL Disable

This bit controls the internal PLL. The PLL must be configured using PLL Setting Register 0 (REG[000Eh]) and PLL Setting Register 1 (REG[0010h]) before enabling this bit.
When this bit = 0, the PLL is enabled. When this option is selected, the PLL output is the source for the system clock divider.
When this bit = 1, the PLL is disabled (default). When this option is selected, the external clock, CLKI is the source for the system clock divider.

Note

There may be up to a 100ms delay before the PLL output becomes stable. The S1D13717 must not be accessed during this time.

REG[0014h] Miscellaneous Configuration Register
Default = 0011h Read/Write

15	14	13	12	11	10	9	8
n/a			Reserved	Reserved	Reserved	LCD2 Serial Bypass Mode Select	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VNDP Status (RO)	Memory Controller Idle Status (RO)	n/a	Serial/Parallel Input Active Pull-up/Pull-down Enable	n/a	Reserved	Reserved	Power Save Enable

bit 12 Reserved

The default value for this bit is 0.

bit 11 Reserved

The default value for this bit is 0.

bit 10 Reserved

The default value for this bit is 0.

bit 9 LCD2 Serial Bypass Mode Select

This bit selects bypass mode for the LCD2 display. This bit must be configured before the Serial/Parallel Port Bypass Enable bit (REG[0032h] bit 8) is set. If REG[0032h] bit 8 is set to 1 when this bits = 0, there is no hardware effect. For bypass mode pin mapping, see Table 5-14: “Serial Bypass Pin Mapping,” on page 47.

When this bit = 0, serial bypass of LCD2 is not possible.
When this bit = 1, serial bypass of LCD2 is possible when Mode 1 (REG[0032h] bits 1-0 = 00b) or Mode 2 (REG[0032h] bits 1-0 = 10b) is selected.

bit 8 Reserved

The default value for this bit is 0.

bit 7 Vertical Non-Display Period Status (Read Only)

If an RGB type panel is selected for LCD1 (Mode 1/Mode 4, see REG[0032h] bits 1-0), this status bit indicates whether the panel is in a Vertical Non-Display Period. This bit has no effect when Mode 2 or Mode 3 is selected.
When this bit = 0, the LCD panel output is in a Vertical Display Period.
When this bit = 1, the LCD panel output is in a Vertical Non-Display Period.

bit 6 Memory Controller Idle Status (Read Only)
This bit indicates the status of the memory controller and must be checked before enabling Power Save Mode (REG[0014h] bit 0) or disabling the PLL (REG[0012h] bit 0). For further information on using this bit, see Figure 11-1: "Power-On/Power-Off Sequence," on page 287 or Figure 11-2: "Power Modes," on page 288.
When this bit = 0, the memory controller is powered up.
When this bit = 1, the memory controller is idling and the system clock source can be disabled.

bit 4 Serial Input Active Pull-up/Pull-down Enable
This bit controls the active pull-up/pull-down resistors on the host serial input pins (SCS#, SCLK, SA0, SI). When the serial input port is unused (Hi-Z), set this bit to 1.
When this bit = 0, the pull-up/pull-down resistors are inactive.
When this bit = 1, the pull-up/pull-down resistors are active and the pins are affected as follows (default).

Table 10-5: Serial Pull-up/Pull-down Resistors

Pin	Type
SCS#	Pull-up
SCLK	Pull-down
SA0	Pull-down
SI	Pull-down

bit 2 Reserved
The default value for this bit is 0.

bit 1 Reserved
The default value for this bit is 0.

bit 0 Power Save Mode Enable
This bit controls the state of the software initiated power save mode. When power save mode is disabled, the S1D13717 is operating normally. When power save mode is enabled, the S1D13717 is in a power efficient state. For more information on the S1D13717 condition during Power Save Mode, see Section 11.2, "Power Save Mode Function" on page 290.
When this bit = 0, power save mode is disabled.
When this bit = 1, power save mode is enabled (default).

Note
For all modes except Mode 1 (see REG[0032h] bits 1-0), the LCD Output Port must be turned off (REG[0202h] bits 12-10 = 000b) before enabling power save mode. For all modes, the Memory Controller Idle Status bit (REG[0014h] bit 6) must return a 1 before enabling power save mode.

REG[0016h] Software Reset Register
Default = not applicable — Write Only

15	14	13	12	11	10	9	8
Software Reset bits 15-8							
7	6	5	4	3	2	1	0
Software Reset bits 7-0							

bits 15-0 Software Reset bits [15:0] (Write Only)
When any value is written to these bits, **all registers are reset to their default values**. A software reset via this register **does not clear the display buffer**. For further information on software reset, see Section 11.1.2, “Reset” on page 289.

REG[0018h] System Clock Setting Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						System Clock Divide Select bits 1-0	

bits 1-0 System Clock Divide Select bits [1:0]
These bits determine the divide ratio for the system clock. The source is selectable, using REG[0012h] bit 0, between either the PLL output (see REG[000Eh]-REG[0012h]) or an external clock source (CLKI).

Table 10-6: System Clock Divide Ratio Selection

REG[0018h] bits 1-0	System Clock Divide Ratio
00b	1:1
01b	2:1
10b	3:1
11b	4:1

Note
For more information on clocks, see Section 9, “Clocks” on page 116.

10.4.3 Indirect Interface Registers

These registers are used for the Indirect Interface only. The indirect interface is selected at RESET# using the configuration bits CNF[4:2] (see Table 5-10: "Summary of Power-On/Reset Options," on page 42). For examples using the Indirect Interface, see Section 22, "Indirect Interface" on page 372.

REG[0020h] is Reserved

This register is Reserved and should not be written.

REG[0022h] Indirect Interface Memory Address Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Indirect Interface Memory Address bits 15-8							
7	6	5	4	3	2	1	0
Indirect Interface Memory Address bits 7-1							n/a

REG[0024h] Indirect Interface Memory Address Register 2
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a					Indirect Interface Memory Address bits 18-16		

REG[0024h] bits 2-0

REG[0022h] bits 15-1 Indirect Interface Memory Address bits [18:1]

This register is used for Indirect Interface modes only.

These bits determine the memory start address for each memory access. After a completed memory access, this register is incremented automatically.

Note

Only 16-bit memory accesses are possible when an indirect interface is selected.

REG[0026h] Indirect Interface Auto Increment Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						Indirect Interface Auto Increment bits 1-0	

bits 1-0 Indirect Interface Auto Increment bits [1:0]

This register is used for Indirect Interface modes only.

These bits determine the method used to auto increment the memory address stored in the Indirect Interface Memory Address registers (REG[0024h]-[0022h]). The Indirect Interface Memory Address registers must be auto incremented after each memory access based on the type of memory accesses being done (byte or word).

Table 10-7: Indirect Interface Auto Increment Selection

REG[0026h] bits 1-0	Indirect Interface Auto Increment
00b (default)	Increment when a high byte access or word access takes place
01b	Increment only when a word access takes place (no increment takes place for byte accesses)
10b	Never increment (Auto increment is disabled)
11b	Reserved

REG[0028h] Indirect Interface Memory Access Port Register
Default = not applicable — Read/Write

15	14	13	12	11	10	9	8
Indirect Interface Memory Access Port bits 15-8							
7	6	5	4	3	2	1	0
Indirect Interface Memory Access Port bits 7-0							

bits 15-0 Indirect Interface Memory Access Port bits [15:0]

This register is used for Indirect Interface modes only.

These bits are the memory read/write port for the Indirect Interface. An Index Write to this register begins (or triggers) a burst read/write to memory.

REG[002Ah] Indirect Interface 2D BitBLT Data Read/Write Port Register
Default = not applicable — Read/Write

15	14	13	12	11	10	9	8
Indirect Interface 2D BitBLT Data Read/Write Port bits 15-8							
7	6	5	4	3	2	1	0
Indirect Interface 2D BitBLT Data Read/Write Port bits 7-0							

bits 15-0 Indirect Interface 2D BitBLT Data Read/Write Port bits [15:0]

This register is used for Indirect Interface modes only.

These bits are the read/write port for 2D BitBLT data when using the Indirect Interface (instead of REG[10000h] for direct addressing).

10.4.4 LCD Panel Interface Generic Setting Registers

REG[0030h] LCD Interface Clock Setting Register
Default = 0000h Read/Write

n/a					Serial Clock Divide Select bits 2-0		
15	14	13	12	11	10	9	8
n/a			Pixel Clock Divide Select bits 4-0				
7	6	5	4	3	2	1	0

bits 10-8 Serial Clock Divide Select bits[2:0]

These bits specify the divide ratio for the serial clock. The clock source for the serial clock is the system clock (see Figure 9-1: “Clock Diagram,” on page 116). If LCD1 or LCD2 is not a serial interface type LCD panel (REG[0032h] bits 1-0) or if Serial Port Bypass is enabled (REG[0032h] bit 8 = 1), these bits are ignored.

Table 10-8: Serial Clock Divide Ratio Selection

REG[0030h] bits 10-8	Serial Clock Divide Ratio
000b	2:1
001b	4:1
010b	6:1
011b	8:1
100b	10:1
101b	12:1
110b	14:1
111b	16:1

bits 4-0 Pixel Clock Divide Select bits[4:0]

These bits specify the divide ratio for the pixel clock. The clock source for the pixel clock is the system clock (see Figure 9-1: "Clock Diagram," on page 116). When LCD1 is an RGB type panel (REG[0032h] bits 1-0 = 00b or 01b), the pixel clock is the same as the shift clock. When LCD1 or LCD2 is a parallel interface type panel (REG[0032h] bits 1-0 = 10b or 11b), the pixel clock is used for the parallel data output timing clock.

Table 10-9: Pixel Clock Divide Selection

REG[0030h] bits 4-0	Pixel Clock Divide Ratio
00000b	2:1
00001b	4:1
00010b	6:1
00011b	8:1
00100b	10:1
00101b	12:1
00110b	14:1
00111b	16:1
01000b	18:1
01001b	20:1
01010b	22:1
01011b	24:1
01100b	26:1
01101b	28:1
01110b	30:1
01111b	32:1
10000b	34:1
10001b	36:1
10010b	38:1
10011b	40:1
10100b	42:1
10101b	44:1
10110b	46:1
10111b	48:1
11000b - 11111b	Reserved

Note

SwivelView should not be used when the 2:1 Pixel Clock Divide Ratio is used (REG[0202h] bits 5-4 = 00b and bits 1-0 = 00b).

REG[0032h] LCD Module Clock Setting Register
Default = 0000h Read/Write

Reserved						n/a	Serial Port Bypass Enable
15	14	13	12	11	10	9	8
FPSHIFT Polarity Select	RGB Interface Panel Data Bus Width bits 2-0			n/a		Panel Interface bits 1-0	
7	6	5	4	3	2	1	0

bits 15-10 Reserved
The default value for these bits is 0.

bit 8 Serial Port Bypass Enable
This bit controls the serial port bypass function. To enable the Serial Port Bypass, set REG[0014h] bit 9 = 1, then REG[0032h] bit 8 =1.

When the serial port bypass is enabled, the host can drive the LCD2 serial interface directly via the Host serial interface. When the serial port bypass is disabled, the LCD2 serial interface is controlled by the S1D13717. For serial bypass pin mapping and input/output port assignments, see Table 5-14: "Serial Bypass Pin Mapping," on page 47.

When this bit = 0, the serial port bypass is disabled.
When this bit = 1, the serial port bypass is enabled.

Note
The LCD Output Port Select bits (REG[0202h] bits 12-10) and Panel Interface bits (REG[0032h] bits 1-0) have no effect in serial bypass mode.

Note
When power save mode is enabled (REG[0014h] bit 0 = 1), the host can drive the LCD2 serial interface directly via the host serial interface automatically. In this situation, the Serial Port Bypass Enable bit does not need to be set.

bit 7 FPSHIFT Polarity Select
This bit sets the polarity of the shift clock for RGB type panels (inverts FPSHIFT).
When this bit = 0, all panel interface signals change at the rising edge of FPSHIFT.
When this bit = 1, all panel interface signals change at the falling edge of FPSHIFT.

bits 6-4 RGB Interface Panel Data Bus Width bits [2:0]
These bits only have an effect when a RGB interface panel is selected (REG[0032h] bits 1-0 = 00b or 01b). These bits determine the RGB Interface Panel Data Bus size. Unused FPDAT[17:0] pins are forced low.

Table 10-10: RGB Interface Panel Data Bus Width Selection

REG[0032h] bits 6-4	RGB Interface Panel Data Bus Width (LCD1)
000b	9-bit
001b	12-bit
010b	16-bit
011b	18-bit
100b - 111b	Reserved

bits 1-0 Panel Interface bits[1:0]
These bits determine the LCD1 and LCD2 interface types.

Table 10-11: Panel Interface Selection

REG[0032h] bits 1-0	Mode	LCD1 Panel Interface	LCD2 Panel Interface
00b	1	RGB Interface	Serial Interface (RAM integrated)
01b	4	RGB Interface	Parallel Interface (RAM integrated)
10b	2	Parallel Interface (RAM integrated)	Serial Interface (RAM integrated)
11b	3	Parallel Interface (RAM integrated)	Parallel Interface (RAM integrated)

REG[0034h] LCD Interface Command Register
Default = 0000h Read/Write

LCD Interface Command Register bits 15-8							
15	14	13	12	11	10	9	8
LCD Interface Command Register bits 7-0							
7	6	5	4	3	2	1	0

bit 15-0 LCD Interface Command Register bits [15:0]
These bits are only for parallel/serial interface panels on LCD1 or LCD2 and have no effect for RGB type panels. These bits form the command register for the LCD1/LCD2 parallel/serial interfaces. For 8-bit parallel or serial interfaces, only the lower byte is used. When the LCD interface is busy (REG[0038h] bit 0 = 1), this register must not be written. When the LCD interface is not busy (REG[0038h] bit 0 = 0), the command transfer starts when this register is written. When the command transfer starts, the FPA0 pin is driven low or high depending on the state of the P/C Polarity Invert Enable bit (REG[003Ch] bit 7).

Note
If the LCD1 serial data type is set to uWIRE (REG[0054h] bits 7-5 = 10xb), the upper byte of REG[0034h] is used for A[7:0] and the lower byte is used for D[7:0].

REG[0036h] LCD Interface Parameter Register
Default = 0000h — Read/Write

LCD Interface Parameter Register bits 15-8							
15	14	13	12	11	10	9	8
LCD Interface Parameter Register bits 7-0							
7	6	5	4	3	2	1	0

bit 15-0 LCD Interface Parameter Register bits [15:0]

These bits are only for parallel/serial interface panels on LCD1 or LCD2 and have no effect for RGB type panels. These bits form the parameter register for the LCD1/LCD2 parallel/serial interfaces. For 8-bit parallel or serial interfaces, only the lower byte is used. When the LCD interface is busy (REG[0038h] bit 0 = 1), this register must not be written. When the LCD interface is not busy (REG[0038h] bit 0 = 0), data transfer starts when this register is written. When the data transfer starts, the FPA0 pin is driven high or low depending on the state of the P/C Polarity Invert Enable bit (REG[003Ch] bit 7).

Note

If the LCD1 serial data type is set to uWIRE (REG[0054h] bits 7-5 = 10xb), the upper byte of REG[0036h] is used for A[7:0] and the lower byte is used for D[7:0].

REG[0038h] LCD Interface Status Register
Default = 0000h — Read Only

n/a							
15	14	13	12	11	10	9	8
n/a							LCD Interface Status
7	6	5	4	3	2	1	0

bit 0 LCD Interface Status (Read Only)

This bit indicates the status of the LCD1 or LCD2 serial/parallel interface.
When this bit = 0, the LCD1 or LCD2 serial/parallel interface is not busy (or ready).
When this bit = 1, the LCD1 or LCD2 serial/parallel interface is busy.

REG[003Ah] LCD Interface Frame Transfer Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							LCD Interface Frame Transfer Trigger

bit 0 LCD Interface Frame Transfer Trigger

This bit is only for parallel/serial interface panels on LCD1 or LCD2 and has no effect for RGB type panels. This bit is the trigger to transfer 1 frame of data to the LCD interface.

When this bit is set to 1 and the LCD interface status is not busy (REG[0038h] bit 0 = 0), 1 frame of data is transferred to the LCD interface. When the data transfer is finished, this bit is cleared automatically.

When this bit is set to 1 and the LCD interface is busy (REG[0038h] bit 0 = 1), the frame transfer request is ignored. Once the LCD interface is no longer busy, this bit is cleared without transferring any data.

Note

When LCD Interface Auto Transfer is enabled (REG[003Ch] bit 0 = 1), this bit remains high (1).

REG[003Ch] LCD Interface Transfer Setting Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
P/C Polarity Invert Enable	n/a						LCD Interface Auto Frame Transfer Enable

bit 7 Parameter/Command Polarity Invert Enable

This bit is only for parallel/serial interface panels on LCD1 or LCD2 and has no effect for RGB type panels. During an LCD Interface Command (REG[0034h]) or LCD Interface Parameter (REG[0036h]) transfer, FPA0 is driven high or low based on the setting of this bit. When LCD1 is a ND-TFD 9-bit panel (REG[0054h] bits 7-5 = 001) or LCD2 is a 9-bit serial panel (REG[005Ch] bit 5 = 1), this bit determines the MSB of the 9-bit data on FPSO.

Table 10-12: Parameter/Command Invert Setting

REG[003Ch] bit 7	FPA0 Signal Output	
	Command	Parameter
0	Low	High
1	High	Low

bit 0

LCD Interface Auto Frame Transfer Enable

This bit is only for parallel/serial interface panels on LCD1 or LCD2 and has no effect for RGB type panels. This bit controls the automatic frame transfer of one frame of display memory to the LCD interface. The frame transfer is triggered and synchronized by the camera interface vertical sync signal (CMVREF). All camera input signals are required to trigger the frame transfer.
When this bit = 0, auto frame transfer is disabled.
When this bit = 1, auto frame transfer is enabled.

When this bit = 1, the LCD Interface Status bit (REG[0038h] bit 0) is always busy. When busy, command/parameter and frame transfers cannot be sent manually. This bit should be disabled before camera input is disabled.

Note

While auto transfer is enabled, the following condition must be met or no frame transfers will take place.

1 Frame transfer cycle (time) < 1 CMVREF period (time)

Note

While auto transfer is enabled, do not vary the PCLK and CM1CLKOUT/CM2CLKOUT frequencies

10.4.5 LCD1 Setting Register

REG[0040h] LCD1 Horizontal Total Register
Default = 0001h — Read/Write

15	14	13	12	11	10	9	8
n/a						Reserved	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	LCD1 Horizontal Total bits 6-0						

bits 9-7 Reserved
The default value for these bits is 0.

bits 6-0 LCD1 Horizontal Total bits [6:0]
These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the LCD1 Horizontal Total period, in 8 pixel resolution. The Horizontal Total is the sum of the Horizontal Display Period and the Horizontal Non-Display Period. The maximum Horizontal Total is 1024 pixels. These bits must not be set to 0.

REG[0040h] bits 6-0 = (Horizontal Total in pixels ÷ 8) - 1

Note
This register must be programmed such that the following formula is valid.

HT ≥ HDP + HNDP

REG[0042h] LCD1 Horizontal Display Period Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							LCD1 HDP bit 8
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LCD1 Horizontal Display Period bits 7-0							

bits 8-0 LCD1 Horizontal Display Period bits [8:0]
These bits specify the LCD1 Horizontal Display Period, in 2 pixel resolution. The Horizontal Display Period must be less than the Horizontal Total to allow for a sufficient Horizontal Non-Display Period.

REG[0042h] bits 8-0 = (Horizontal Display Period in pixels ÷ 2) - 1

Note
For Parallel interface panels (see REG[0032h] bits 1-0), the following formula must be valid.

HDP x VDP ≥ 40 pixels.

REG[0044h] LCD1 Horizontal Display Period Start Position Register
Default = 0000h Read/Write

n/a						LCD1 HDP bits 9-8	
15	14	13	12	11	10	9	8
LCD1 Horizontal Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 LCD1 Horizontal Display Period Start Position bits [9:0]

These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the LCD1 Horizontal Display Period Start Position in 1 pixel resolution.

REG[0044h] bits 9-0 = Horizontal Display Period Start Position in pixels - 9

REG[0046h] LCD1 FPLINE Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
FPLINE Polarity	FPLINE Pulse Width bits 6-0						
7	6	5	4	3	2	1	0

bit 7 FPLINE Pulse Polarity

This bit is for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and has no effect when a serial or parallel interface panel is selected. This bit selects the polarity of the horizontal sync signal (FPLINE).

When this bit = 0, the horizontal sync signal (FPLINE) is active low.

When this bit = 1, the horizontal sync signal (FPLINE) is active high.

bits 6-0 FPLINE Pulse Width bits [6:0]

These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the width of the horizontal sync signal (FPLINE), in 1 pixel resolution.

REG[0046h] bits 6-0 = FPLINE Pulse Width in pixels - 1

REG[0048h] LCD1 FPLINE Pulse Position Register
Default = 0000h Read/Write

n/a						FPLINE Pulse Position bits 9-8	
15	14	13	12	11	10	9	8
FPLINE Pulse Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 FPLINE Pulse Position bits [9:0]

These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the position of the FPLINE pulse.

REG[0048h] bits 9-0 = FPFRAME edge to FPLINE edge in pixels - 1

REG[004Ah] LCD1 Vertical Total Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						LCD1 Vertical Total bits 9-8	
7	6	5	4	3	2	1	0
LCD1 Vertical Total bits 7-0							

bits 9-0 LCD1 Vertical Total bits [9:0]

These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the LCD1 Vertical Total period, in 1 line resolution. The Vertical Total is the sum of the Vertical Display Period and the Vertical Non-Display Period. The maximum Vertical Total is 1024 lines.

REG[004Ah] bits 9-0 = Vertical Total in lines - 1

REG[004Ch] LCD1 Vertical Display Period Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						LCD1 Vertical Display Period bits 9-8	
7	6	5	4	3	2	1	0
LCD1 Vertical Display Period bits 7-0							

bits 9-0 LCD1 Vertical Display Period bits [9:0]

These bits specify the LCD1 Vertical Display period, in 1 line resolution. The Vertical Display Period must be less than the Vertical Total to allow for a sufficient Vertical Non-Display period.

REG[004Ch] bits 9-0 = Vertical Display Period in lines - 1

Note

For Parallel interface panels (see REG[0032h] bits 1-0), the following formula must be valid.

HDP x VDP ≥ 40 pixels

REG[004Eh] LCD1 Vertical Display Period Start Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						LCD1 Vertical Display Period Start Position bits 9-8	
7	6	5	4	3	2	1	0
LCD1 Vertical Display Period Start Position bits 7-0							

bits 9-0 LCD1 Vertical Display Period Start Position bits [9:0]

These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the LCD1 Vertical Display Period Start Position in 1 line resolution.

REG[0050h] LCD1 FPFRAME Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
FPFRAME Polarity	n/a				LCD1 FPFRAME Pulse Width bits 2-0		

bit 7 LCD1 FPFRAME Pulse Polarity

This bit is for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and has no effect when a serial or parallel interface panel is selected. This bit selects the polarity of the vertical sync signal (FPFRAME).
When this bit = 0, the vertical sync signal (FPFRAME) is active low.
When this bit = 1, the vertical sync signal (FPFRAME) is active high.

bits 2-0 LCD1 FPFRAME Pulse Width bits [2:0]

These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the width of the panel vertical sync signal (FPFRAME), in 1 line resolution.

REG[0050h] bits 2-0 = FPFRAME Pulse Width in lines - 1

REG[0052h] LCD1 FPFRAME Pulse Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						LCD1 FPFRAME Pulse Position bits 9-8	

7	6	5	4	3	2	1	0
LCD1 FPFRAME Pulse Position bits 7-0							

bits 9-0 LCD1 FPFRAME Pulse Position bits [9:0]

These bits are for RGB Interface panels only (REG[0032h] bits 1-0 = 00b or 01b) and have no effect when a serial or parallel interface panel is selected. These bits specify the start position of the FPFRAME signal, in 1 line resolution.

REG[0054h] LCD1 Serial Interface Setting Register
Default = 0001h — Read/Write

n/a							
15	14	13	12	11	10	9	8
LCD1 Serial Data Type bits 2-0			LCD1 Serial Data Direction	n/a		LCD1 Serial Clock Phase	LCD1 Serial Clock Polarity
7	6	5	4	3	2	1	0

bit 7-5 LCD1 Serial Data Type bits [2:0]

These bits determine the LCD1 Serial Data Type for RGB displays requiring initialization through a serial interface.

Table 10-13: LCD1 Serial Data Type Selection

REG[0054h] bits 7-5	LCD1 Serial Data Type
000b	ND-TFD 4 pins (8-bit Serial)
001b	ND-TFD 3 pins (9-bit Serial)
01xb	a-Si TFT (8-bit Serial)
10xb	uWIRE (16-bit Serial)
11xb	Reserved

Note
For Mode 2 and Mode 3 configurations (see REG[0032h] bits 1-0), these bits must be set to 000b.

bit 4 LCD1 Serial Data Direction

This bit determines the LCD1 serial data direction for RGB displays requiring initialization through a serial interface.
When this bit = 0, the MSB is first.
When this bit = 1, the LSB is first.

bit 1 LCD1 Serial Clock Phase

This bit specifies the serial clock phase for RGB displays requiring initialization through a serial interface. See Table 10-14: “LCD1 Serial Clock Polarity and Phase Selection”.

Note
For details on timing, see Section 7.4.2, “LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing” on page 92.

bit 0 LCD1 Serial Clock Polarity

This bit determines the LCD1 serial data format for RGB displays requiring initialization through a serial interface.

Table 10-14: LCD1 Serial Clock Polarity and Phase Selection

REG[0054h] bit 1	REG[0054h] bit 0	Serial Data Output Changes	Idling Status of Clock
0	0	falling edge of Serial Clock	Low
	1	rising edge of Serial Clock	High
1	0	rising edge of Serial Clock	Low
	1	falling edge of Serial Clock	High

Note

For details on timing, see Section 7.4.2, "LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing" on page 92.

REG[0056h] LCD1 Parallel Interface Setting Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a		Reserved	Reserved	n/a		Reserved	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LCD1 VSYNC Input Enable	LCD1 Parallel Type Select	n/a			LCD1 Parallel Data Format bits 2-0		

bit 13 Reserved

The default value for this bit is 0.

bit 12 Reserved

The default value for this bit is 0.

bits 9-8 Reserved

These bits are reserved and default to 0.

bit 7 LCD1 VSYNC Input Enable

This bit is not used for RGB type panels.

This bit allows the transfer of a frame of data synced to an external VSYNC input (FPVIN1). When a manual transfer has been initiated, the LCD1 data output will occur on the next falling edge of FPVIN1.

When this bit = 0, the LCD1 data output is independent of an external VSYNC input.

When this bit = 1, the LCD1 data output is synchronous with an external VSYNC input.

Note

The FPVIN1 signal period must be longer than the time it takes to transfer a frame of data. If the FPVIN1 period is shorter than the time it takes to transfer a complete frame to the panel, the current frame transfer is interrupted at the next FPVIN1 falling edge.

Note

Once a manual frame transfer has been initiated (REG[003Ah] bit 0 = 1), the LCD1 VSYNC Input Enable bit must not be disabled before the next VSYNC signal has occurred or the LCD interface will always be busy and subsequent transfers will not occur.

bit 6 LCD1 Parallel Type Select
This bit determines the LCD1 parallel interface type.
When this bit = 0, the parallel interface is type 80.
When this bit = 1, the parallel interface is type 68.

bit 2-0 LCD1 Parallel Data Format bits [2:0]
These bits determine the LCD1 parallel data format. **These bits are not used for RGB Type Panels (REG[0032h] bits 1-0 = 00 or 01)**. For further information on available parallel data formats, see Section 13.4, “Parallel Data Format” on page 299.

Table 10-15: LCD1 Parallel Data Format Selection

REG[0056h] bits 2-0	LCD1 Parallel Data Format	
	Data Bus Width	Data Format
000b	8-bit	RGB = 3:3:2 (1 cycle/pixel)
001b		RGB = 4:4:4 (3 cycle / 2 pixel)
010b	16-bit	RGB = 8:8:8 (3 cycle/2 pixel)
011b	8-bit	RGB = 8:8:8 (3 cycle/pixel)
100b	Reserved	
101b	16-bit	RGB = 4:4:4 (1 cycle/pixel)
110b		RGB = 5:6:5 (1 cycle/pixel)
111b	18-bit	RGB = 6:6:6 (1 cycle/pixel)

10.4.6 LCD2 Setting Registers

REG[0058h] LCD2 Horizontal Display Period Register
Default = 0000h Read/Write

n/a							LCD2 HDP bit 8
15	14	13	12	11	10	9	8
LCD2 Horizontal Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 8-0 LCD2 Horizontal Display Period bits [8:0]

These bits specify the LCD2 Horizontal Display Period, in 2 pixel resolution.

REG[0058h] bits 8-0 = (Horizontal Display Period in pixels ÷ 2) - 1

Note

For Parallel and Serial interface panels (see REG[0032h] bits 1-0), the following formula must be valid.

HDP x VDP ≥ 40 pixels.

REG[005Ah] LCD2 Vertical Display Period Register
Default = 0000h Read/Write

n/a						LCD2 Vertical Display Period bits 9-8	
15	14	13	12	11	10	9	8
LCD2 Vertical Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 LCD2 Vertical Display Period bits [9:0]

These bits specify the LCD2 Vertical Display Period, in 1 line resolution.

REG[005Ah] bits 9-0 = Vertical Display Period in lines - 1

Note

For Parallel and Serial interface panels (see REG[0032h] bits 1-0), the following formula must be valid.

HDP x VDP ≥ 40 pixels.

REG[005Ch] LCD2 Serial Interface Setting Register
Default = 0001h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a		LCD2 Serial Data Type	LCD2 Serial Data Direction	LCD2 Serial Data Format bits 1-0		LCD2 Serial Clock Phase	LCD2 Serial Clock Polarity
7	6	5	4	3	2	1	0

bit 5 LCD2 Serial Data Type

This bit determines the LCD2 serial data type.

Table 10-16: LCD2 Serial Data Type Selection

REG[005Ch] bit 5	LCD2 Serial Data Type
0	4 pins (8-bit)
1	3 pins (9-bit)

bit 4 LCD2 Serial Data Direction
This bit determines the LCD2 serial data direction.
When this bit = 0, the MSB is first.
When this bit = 1, the LSB is first.

bit 3-2 LCD2 Serial Data Format bits[1:0]
These bits determine the LCD2 serial data format. For further information on available serial data formats, see Section 13.5, "Serial Data Format" on page 305.

Table 10-17: LCD2 Serial Data Format Selection

REG[005Ch] bits 3-2	LCD2 Serial Data Format	
	Data Length	Data Format
00b	8-bit	RGB=3.3.2 (1 transfer / pixel)
01b		RGB=4.4.4 (3 transfer / 2 pixel)
10b	Reserved	
11b		

bit 1 LCD2 Serial Clock Phase
This bit specifies the LCD2 serial clock phase. See Table 10-18: "LCD2 Serial Clock Polarity and Phase Selection".

Note
For details on timing, see Section 7.4.2, "LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing" on page 92.

bit 0 LCD2 Serial Clock Polarity
This bit determines the LCD2 serial clock polarity.

Table 10-18: LCD2 Serial Clock Polarity and Phase Selection

REG[005Ch] bit 1	REG[005Ch] bit 0	Serial Data Output Changes	Clock Idling Status
0	0	falling edge of Serial Clock	Low
	1	rising edge of Serial Clock	High
1	0	rising edge of Serial Clock	Low
	1	falling edge of Serial Clock	High

Note
For details on timing, see Section 7.4.2, "LCD1 ND-TFD, LCD2 8-Bit Serial Interface Timing" on page 92.

REG[005Eh] LCD2 Parallel Interface Setting Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a		Reserved	Reserved	n/a			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LCD2 VSYNC Input Enable	LCD2 Parallel Type Select	n/a			LCD2 Parallel Data Format bits 2-0		

bit 13 Reserved
The default value for this bit is 0.

bit 12 Reserved
The default value for this bit is 0.

bit 7 LCD2 VSYNC Input Enable
This bit allows the transfer of a frame of data synced to an external VSYNC input (FPVIN2). When a manual transfer has been initiated, the LCD1 data output will occur on the next falling edge of FPVIN1.
When this bit = 0, the LCD2 data output is independent of an external VSYNC input.
When this bit = 1, the LCD2 data output is synchronous with an external VSYNC input.

Note
The FPVIN2 signal period must be longer than the time it takes to transfer a frame of data. If the FPVIN2 period is shorter than the time it takes to transfer a complete frame to the panel, the current frame transfer is interrupted at the next FPVIN2 falling edge.

bit 6 LCD2 Parallel Type Select
This bit determines the LCD2 parallel interface type.
When this bit = 0, the parallel interface is type 80.
When this bit = 1, the parallel interface is type 68.

bits 2-0 LCD2 Parallel Data Format bits[2:0]
These bits determine the LCD2 Parallel Data Format. For further information on available parallel data formats, see Section 13.4, “Parallel Data Format” on page 299.

Table 10-19: LCD2 Parallel Data Format Selection

REG[005Eh] bits 2-0	LCD2 Parallel Data Format	
	Data Bus Width	Data Format
000b	8-bit	RGB=3.3.2 (1 cycle/pixel)
001b		RGB=4.4.4 (3 cycle / 2 pixel)
011b		RGB=8.8.8 (3 cycle/pixel)
101b	16-bit	RGB=4.4.4 (1 cycle/pixel)
110b		RGB=5.6.5 (1 cycle/pixel)
111b	18-bit	RGB=6.6.6 (1 cycle/pixel)
010b	16-bit	RGB=8.8.8 (3 cycle/2 pixel)
100b	Reserved	

REG[0070h] through REG[00FEh] are Reserved

These registers are Reserved and should not be written.

10.4.7 Camera Interface Setting Register

REG[0100h] Camera Clock Setting Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a			Camera Clock Divide Select bits 4-0				

bits 4-0 Camera Clock Divide Select bits [4:0]
These bits specify the divide ratio used to generate the Camera Clock from the System Clock.

Table 10-20: Camera Clock Divide Ratio Selection

REG[0100h] bits 4-0	Camera Clock Divide Ratio
00000b	1:1
00001b	2:1
00010b	3:1
00011b	4:1
00100b	5:1
00101b	6:1
00110b	7:1
00111b	8:1
01000b	9:1
01001b	10:1
01010b	11:1
01011b	12:1
01100b	13:1
01101b	14:1
01110b	15:1
01111b	16:1

REG[0100h] bits 4-0	Camera Clock Divide Ratio
10000b	17:1
10001b	18:1
10010b	19:1
10011b	20:1
10100b	21:1
10101b	22:1
10110b	23:1
10111b	24:1
11000b	25:1
11001b	26:1
11010b	27:1
11011b	28:1
11100b	29:1
11101b	30:1
11110b	31:1
11111b	32:1

REG[0102h] Camera Signal Setting Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a	Reserved	Camera Clock Mode Select	Camera YUV Data Format Select bits 1-0		Camera HSYNC Active Select	Camera VSYNC Active Select	Camera Valid Input Clock Edge

bit 6 Reserved
The default value for this bit is 0.

bit 5 Camera Clock Mode Select
This bit determines the source of the clock used to sample incoming YUV data on the Camera interface.
When this bit = 0, the external input clock (CMCLKIN) from the camera interface is used to sample incoming YUV data (default).
When this bit = 1, the internally divided system clock is used to sample incoming YUV data.

bits 4-3 Camera YUV Data Format Select bits [1:0]
These bits specify the YUV data format for the Camera interface, in bytes.

Table 10-21: YUV Data Format Selection

REG[0102h] bits 4-3	YUV Data Format (8-bit format)
00b	(1st) UYVY (last)
01b	(1st) VYUY (last)
10b	(1st) YUYV (last)
11b	(1st) YVYU (last)

bit 2 Camera HSYNC Active Select
This bit defines HYSNC for the Camera interface.
When this bit = 0, the Camera HSYNC (CMHREF) is active low and CMHREF high means data is valid.
When this bit = 1, the Camera HSYNC (CMHREF) is active high and CMHREF low means data is valid.

bit 1 Camera VSYNC Active Select
This bit defines VYSNC for the Camera interface.
When this bit = 0, the Camera VSYNC (CMVREF) is active low and CMVREF high means data is valid.
When this bit = 1, the Camera VSYNC (CMVREF) is active high and CMVREF low means data is valid.

bit 0 Camera Valid Input Clock Edge
This bit determines the edge on which Camera data is latched.
When this bit = 0, the S1D13717 latches input data on the rising edge of the clock (CMCLKIN).
When this bit = 1, S1D13717 latches input data on the falling edge of the clock (CMCLKIN).

REG[0104h] through REG[010Eh] are Reserved

These registers are Reserved and should not be written.

REG[0110h] Camera Mode Setting Register
Default = 0000h — Read/Write

Reserved	n/a	Reserved	Camera Active Pull-down Disable	n/a	Camera Clock Sampling Mode	Reserved	YUV Data Offset Enable
15	14	13	12	11	10	9	8
ITU-R BT656 Enable	Reserved			CMCLKOUT Output Disable	Reserved		Camera Module Enable
7	6	5	4	3	2	1	0

bit 15 Reserved
The default value for this bit is 0.bit 13Reserved
The default value for this bit is 0.

bit 12 Camera Active Pull-down Disable
This bit controls the active pull-down resistors on the Camera interface.
When this bit = 0, the active pull-down resistors on the Camera interface are enabled.
When this bit = 1, the active pull-down resistors on the Camera interface are disabled.

bit 10 Camera Clock Sampling Mode
This bit controls the camera clock sampling rate.
When this bit = 0, the sampling rate is “normal mode”.
When this bit = 1, the sampling rate is “fast mode”.

When fast mode is selected the Camera Clock Divide Select bits must be set to 1:1 or 1:2 (REG[0100h] bits 4-0 = 0000b or 0001b).

bit 9 Reserved
The default value for this bit is 0.

bit 8

YUV Data Offset Enable
This bit determines whether the incoming U and V data from the camera interface is internally offset. Typically, camera modules output in YUV or YCbCr offset format, therefore this bit is cleared or set to 0. If the camera data is intended for viewing after the YUV/RGB Converter (YRC), or encoding through the JPEG codec, the resulting YUV data format should be YUV or YCbCr offset.
When this bit = 0, no offset is applied to the incoming U and V camera (UV values are unmodified).
When this bit = 1, an offset is applied to the incoming U and V camera data, the incoming U and V camera data MSB are inverted.

Note
For YUV to RGB Converter (YRC) input requirements, see the bit description for REG[0240h] bit 4.

Table 10-22: YUV/YUV Offset Enable

REG[0110h] bits 8	YUV Data Offset	Input Data Range	Output Data Range
0	No offset is applied	0 ≤ Y ≤ 255	Same as Input
		-128 ≤ U ≤ 127	
		-128 ≤ V ≤ 127	
		16 ≤ Y ≤ 235	
		-113 ≤ U ≤ 112	
		-113 ≤ V ≤ 112	
1	Camera format: YUV Straight range converted to YUV Offset range	0 ≤ Y ≤ 255	0 ≤ Y ≤ 255
		0 ≤ U ≤ 255	-128 ≤ U ≤ 127
		0 ≤ V ≤ 255	-128 ≤ V ≤ 127
	Camera format: YCbCr Straight range converted to YCbCr Offset range	16 ≤ Y ≤ 235	16 ≤ Y ≤ 235
		16 ≤ U ≤ 240	-113 ≤ U ≤ 112
		16 ≤ V ≤ 240	-113 ≤ V ≤ 112

bit 7

ITU-R BT656 Enable
This bit controls the active camera interface type and is valid when the interface type is YUV 4:2:2 8-bit (see REG[0102h] bit 6).
When this bit = 0, the normal camera interface is active. In this mode the HSYNC, VSYNC, clock, and data signals are independent.
When this bit = 1, the ITU-R BT656 camera interface is active. In this mode the HSYNC and VSYNC signals are mixed with the data signals.

bits 6-4

Reserved
The default value for these bits is 0.

bit 3

CMCLKOUT Output Disable
This bit controls (enables/disables) the camera clock output (CMCLKOUT).
When this bit = 0, the camera clock output is enabled (default).
When this bit = 1, the camera clock output is disabled (low output).

bits 2-1 Reserved
The default value for these bits is 0.

bit 0 Camera Module Enable
This bit controls the camera module.
When this bit = 0, the camera module and clock output (CMCLKOUT) are disabled.
When this bit = 1, the camera module and clock output (CMCLKOUT) are enabled.

REG[0112h] Camera Frame Setting Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Camera Frame Capture Interrupt Control	Camera Single Frame Capture Enable	Camera Frame Capture Interrupt Status Always Active	Frame Sampling Control bits 2-0			Camera Frame Capture Interrupt Polarity	Camera Frame Capture Interrupt Enable
7	6	5	4	3	2	1	0

bit 7 Camera Frame Capture Interrupt Control
This bit controls when the camera frame capture interrupt is asserted and depends on the setting of the Camera Single Frame Capture Mode bit (REG[0112h] bit 6) as follows.

For continuous frame capture mode (REG[0112h] bit 6 = 0):
When this bit = 0, the interrupt is generated when a valid frame is captured. This result also depends on the Camera Frame Capture Interrupt Status Always Active bit (REG[0112h] bit 5).
When this bit = 1, the interrupt is generated after a valid frame is captured and the capture is stopped.

For single frame capture mode (REG[0112h] bit 6 = 1):
When this bit = 0, the interrupt is generated when a valid frame is captured. This result also depends on the Camera Frame Capture Interrupt Status Always Active bit (REG[0112h] bit 5).
When this bit = 1, the interrupt is generated when a valid frame is captured.

Note
When this bit = 1, the Camera Frame Capture Interrupt Status Always Active bit (REG[0112h] bit 5) has no effect on camera frame interrupt generation.

bit 6 Camera Single Frame Capture Enable
This bit controls the camera frame capture mode of the camera interface. This bit **must not** be changed while the camera module is enabled (REG[0110h] bit 0 = 1).
When this bit = 0, frames from the camera interface are continuously captured.
When this bit = 1, the next frame from the camera interface is captured when a camera frame capture start command is issued (REG[0114h] bit 2 = 1). The camera frame capture stops after a single frame is captured.

bit 5 Camera Frame Capture Interrupt Status Always Active
When Camera Frame Capture Interrupts are enabled (REG[0112h] bit 0 =1b) this bit enables triggering of the camera frame capture interrupt on all captured camera frames. This bit has no effect if Camera Frame Capture Interrupts are disabled

When this bit = 0, the camera frame capture interrupt flag is only active when the JPEG Start/Stop Control bit is on, REG[098Ah] bit 0 =1.
When this bit = 1, the camera frame capture interrupt flag is active on all captured camera frames.

bits 4-2 Frame Sampling Control Bits [2:0]
These bits control the camera data sampling rate in frames.

Table 10-23: Frame Sampling Control Selection

REG[0112h] bits 4-2	Frame Sampling Mode
000b	Every Frame is sampled
001b	1 Frame is sampled for every 2 Frames
010b	1 Frame is sampled for every 3 Frames
011b	1 Frame is sampled for every 4 Frames
100b	1 Frame is sampled for every 5 Frames
101b	1 Frame is sampled for every 6 Frames
110b	1 Frame is sampled for every 7 Frames
111b	Reserved

bit 1 Camera Frame Capture Interrupt Trigger Polarity
This bit controls the assertion timing of the camera frame capture interrupt.
When this bit = 0, the Camera Frame Capture Interrupt is asserted when VSYNC is active.
When this bit = 1, the Camera Frame Capture Interrupt is asserted when VSYNC is inactive.

bit 0 Camera Frame Capture Interrupt Enable
This bit controls whether a camera frame capture interrupt is generated or not.
When this bit = 0, the camera frame capture interrupt is disabled.
When this bit = 1, the camera frame capture interrupt is enabled.

REG[0114h] Camera Control Register
Default = 0000h Write Only

15	14	13	12	11	10	9	8
n/a						ITU-R BT656 Error Flag 1 Clear	ITU-R BT656 Error Flag 0 Clear
7	6	5	4	3	2	1	0
n/a				Camera Frame Capture Stop	Camera Frame Capture Start	Camera Frame Cap[ture Interrupt Status Clear	Camera Module Software Reset

bit 9 ITU-R BT656 Error Flag 1 Clear (Write Only)
This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit clears the ITU-R BT656 Error Flag 1 (REG[0116h] bit 9).

bit 8 ITU-R BT656 Error Flag 0 Clear (Write Only)
This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit clears the ITU-R BT656 Error Flag 0 (REG[0116h] bit 8).

bit 3 Camera Frame Capture Stop (Write Only)
This bit stops image frame capturing from the camera interface.
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit stops image frame capturing.

bit 2 Camera Frame Capture Start (Write Only)
This bit starts image frame capturing from the camera interface.
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit starts image frame capturing.

bit 1 Camera Frame Capture Interrupt Status Clear (Write Only)
This bit clears the Camera Frame Capture Interrupt Status bit (REG[0116h] bit 1).
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit clears the Camera Frame Capture Interrupt Status.

bit 0 Camera Module Software Reset (Write Only)
This bit initializes the camera module logic. Camera interface registers are not affected.
Writing a 0 to this bit has no hardware effect.
Writing a 1 to this bit initializes the camera module.

REG[0116h] Camera Status Register
Default = 0044h Read Only

n/a						ITU-R BT656 Error Flag 1	ITU-R BT656 Error Flag 0
15	14	13	12	11	10	9	8
n/a	Camera Vsync	Effective Strobe Frame Status	Effective Frame Status	Camera Frame Capture Busy Status	Camera Frame Capture Start/Stop Flag	Camera Frame Capture Interrupt Status	n/a
7	6	5	4	3	2	1	0

bit 9 ITU-R BT656 Error Flag 1 (Read Only)
This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).
When this bit = 0, no error has occurred.
When this bit = 1, a 2-bit error is detected on the reference decode operation.

To clear this bit, see REG[0114h] bit 9.

bit 8 ITU-R BT656 Error Flag 0 (Read Only)
This bit only has an effect when ITU-R BT656 interface mode is active (REG[0110h] bit 7 = 1).
When this bit = 0, no error has occurred.
When this bit = 1, a 1-bit error is detected on the reference decode operation.

To clear this bit, see REG[0114h] bit 8.

bit 6 Camera VSYNC (Read Only)
This bit indicates the current condition of VSYNC from the camera interface.
When this bit = 0, VSYNC is not currently occurring.
When this bit = 1, VSYNC is currently occurring.

bit 5 Effective Strobe Frame Status (Read Only)
This bit indicates the status of the valid data captured when the strobe is enabled (REG[0124h] bit 0 = 1). This bit goes high when the valid frame for the strobe pulse is captured. It will only remain high for one frame and then go low.
This bit returns a 0, when there is no valid data.
This bit returns a 1, when the valid frame for the strobe pulse is captured. It remains high for only one frame and then goes low.

bit 4 Effective Frame Status (Read Only)
This bit indicates whether the current frame from the camera interface is an "effective" frame based on the Frame Sampling Control bits (REG[0112h] bit 4-2).
When this bit = 0, an effective frame is not occurring.
When this bit = 1, an effective frame is occurring.

The following diagram shows an example of the Effective Frame Status bit where the Frame Sampling Control bits are set for 1 frame sampled for every 3 frames (REG[0112h] bits 4-2 = 010b).

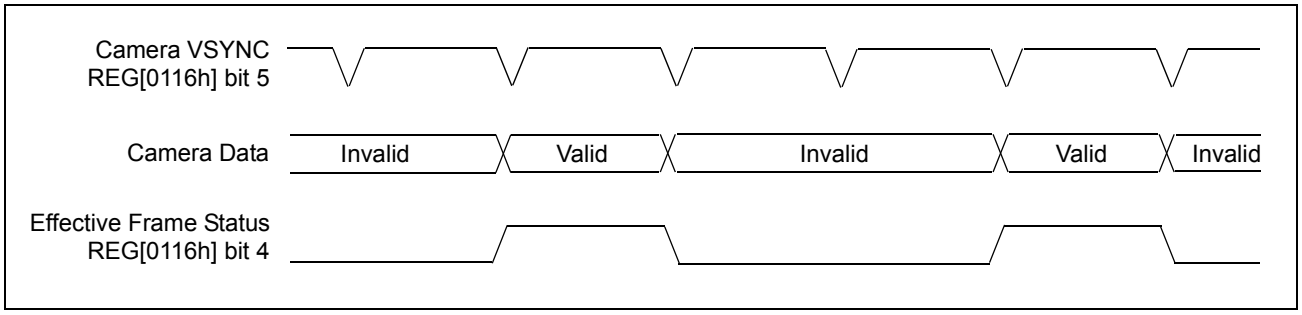


Figure 10-1: Effective Frame Status Bit Example

bit 3 Camera Frame Capture Busy Status (Read Only)
This bit indicates the status of frame capturing from the camera interface.
When this bit = 0, frames are not being captured.
When this bit = 1, frames are being captured.

bit 2 Camera Frame Capture Start/Stop Flag (Read Only)
This bit indicates the current state of the camera frame capture setting in relation to the setting of the Camera Frame Capture Start/Stop bits (REG0114h] bits 3-2).
When this bit = 0, camera frame capturing has been stopped.
When this bit = 1, the camera frame capturing start command has been asserted.

bit 1 Camera Frame Capture Interrupt Status (Read Only)
This bit indicates when a Camera Frame Capture Interrupt has taken place. This bit is masked by the Camera Frame Capture Interrupt Enable bit (REG[0112h] bit 0) and cleared using the Camera Frame Capture Interrupt Status Clear bit (REG[0114h] bit 1).
When this bit = 0, a camera frame capture interrupt has not occurred.
When this bit = 1, a camera frame capture interrupt has occurred.

Note
When the Camera Frame Capture Interrupt is enabled (REG[0112h] bit 0 = 1) and the Camera Frame Capture Interrupt Status Always Active is enabled (REG[0112h] bit 5 = 0), the camera frame capture interrupt is only set at the first camera VREF if continuous capture mode is selected (REG[0112h] bit 6 = 0).

Note
This bit is set regardless of whether the resizers are enabled. Therefore, the Camera Frame Capture Interrupt Status bit cannot be used as an indication that a camera frame has been written to the embedded memory or the JPEG Codec.

REG[0120h] Strobe Line Delay Register
Default = 0000h Read/Write

Strobe Line Delay bits 15-8							
15	14	13	12	11	10	9	8
Strobe Line Delay bits 7-0							
7	6	5	4	3	2	1	0

bit 15-0 Strobe Line Delay bits [15:0]
When the strobe is enabled (REG[0124h] bit 0 = 1), these bits specify the delay, in lines of the camera interface, from the first HSYNC input of a camera frame to the beginning of the Strobe Control Signal. For details on the Strobe Control Signal, see Section 20.2, “Strobe Control Signal” on page 367.

REG[0122h] Strobe Pulse Width Register
Default = 0000h Read/Write

Strobe Pulse Width bits 15-8							
15	14	13	12	11	10	9	8
Strobe Pulse Width bits 7-0							
7	6	5	4	3	2	1	0

bit 15-0 Strobe Pulse Width bits [15:0]
When the strobe is enabled (REG[0124h] bit 0 = 1), these bits specify the pulse width of the Strobe Control Signal, in lines of the camera interface. For details on the Strobe Control Signal, see Section 20.2, “Strobe Control Signal” on page 367.

REG[0124h] Strobe Control Register
Default = 0009h Read/Write

n/a							
15	14	13	12	11	10	9	8
Strobe Capture Delay Control bits 3-0				Strobe Enable	Strobe Port Data	Strobe Control Signal Polarity	Strobe Port Select
7	6	5	4	3	2	1	0

bits 7-4 Strobe Capture Delay Control bits [3:0]
When the strobe is enabled (REG[0124h] bit 0 = 1) and continuous frame capture mode is enabled (REG[0112h] bit 6 = 0), these bits specify the delay, in camera frames, of the captured camera data.

Table 10-24: Strobe Capture Delay Control

REG[0124h] bits 7-4	Delay Value
0000b	No Delay
0001b	1 Frame
0010b	2 Frames
0011b	3 Frames
0100b	4 Frames
0101b	5 Frames
0110b	6 Frames
0111b	7 Frames
1000b	8 Frames
1001b	9 Frames
1010b	10 Frames
1011b	11 Frames
1100b	12 Frames
1101b	13 Frames
1110b	14 Frames
1111b	15 Frames

bit 3 Strobe Enable
This bit enables the Strobe Control Signal (CMSTROUT).
When this bit = 0, the strobe is disabled and CMSTROUT is high (default).
When this bit = 1, the strobe is enabled and CMSTROUT is actively driven (high/low).

bit 2 Strobe Port Data
This bit determines the output of CMSTROUT and only has an effect when the output mode of the strobe port is configured for general purpose output (REG[0124h] bit 0 = 0) and the strobe is enabled (REG[0124h] bit 3 = 1).
When this bit = 0, the output is low (default).
When this bit = 1, the output is high.

bit 1 Strobe Control Signal Polarity
This bit selects output polarity of the Strobe Control Signal.
When this bit = 0, the strobe control signal is active low.
When this bit = 1, the strobe control signal is active high.

bit 0 Strobe Port Select

This bit configures the output mode of the Strobe Port (CMSTROUT).
When this bit = 0, the strobe port is a general purpose output port (default). In this mode CMSTROUT can be used for general purpose data output.
When this bit = 1, the strobe port is configured for the strobe (or flash) function. For further information on this function, see Section 20.2, “Strobe Control Signal” on page 367. In this mode CMSTROUT outputs a strobe pulse triggered by:

- The JPEG Start/Stop Control bit (REG[098Ah] bit 0 = 1)
- The Frame Capture Stop bit for repeat capture mode (REG[0114h] bit 2 = 1)
- The Frame Capture Start bit for single frame capture mode (REG[0114h] bit 3 = 1)

REG[0128h] through REG[012Fh] are Reserved

These registers are Reserved and should not be written.

10.4.8 Display Mode Setting Register

REG[0200h] Display Mode Setting Register 0
Default = 0000h Read/Write

n/a		Double Buffer Window Select	Double Buffer Mode Enable	n/a	Reserved	Display Mode Select bits 1-0	
15	14	13	12	11	10	9	8
LCD Software Reset (WO)	Reserved	LUT2 Bypass Enable	LUT1 Bypass Enable	PIP+ Window Bpp Select bits 1-0		Main Window Bpp Select bits 1-0	
7	6	5	4	3	2	1	0

bit 13 Double Buffer Window Select
This bit controls which window (Main or PIP$^+$) is affected when Double Buffer Mode is enabled (REG[0200h] bit 12 = 1).
When this bit = 0, the PIP$^+$ window area is double buffered.
When this bit = 1, the Main window area is double buffered.

bit 12 Double Buffer Mode Enable
This bit controls double buffer mode. When double buffer mode is enabled, the window to be double buffered must be selected using the Double Buffer Window Select bit (REG[0200h] bit 13). The corresponding Main/PIP$^+$ window area settings, such as the Display Start Address and the Line Address Offset registers, specify the front buffer display start address and line address offset. The back buffer uses the same line address offset as the front buffer, however it's display start address is now controlled by the Back Buffer Display Start Address registers (REG[022Ch]-[022Ah]). The following table summarizes the possible address and offset configurations.
When this bit = 0, double buffer mode is disabled.
When this bit = 1, double buffer mode is enabled.

Table 10-25: Double Buffer Address Registers

Double Buffer Window Select (REG[0200h] bit 13)	Front Buffer		Back Buffer	
	Start Address	Offset	Start Address	Offset
double buffer = Main	REG[0212h]-[0210h]	REG[0216h]	REG[022Ch]-[022Ah]	REG[0216h]
double buffer = PIP$^+$	REG[021Ah]-[0218h]	REG[021Eh]	REG[022Ch]-[022Ah]	REG[021Eh]

Double buffer mode in combination with double buffer write mode (REG[0240h] bit 5 = 1) can be used to enhance the performance of the camera interface, allowing the display to be refreshed from one buffer while the camera interface is writing data to the other buffer.

Note
If double buffer mode is enabled, but single buffer write mode is selected (REG[0240h] bit 5 = 0), only the back buffer image is displayed on the selected window (see REG[0200h] bit 13).

bit 10 Reserved
The default value for this bit is 0.

bit 9-8 Display Mode Select bits[1:0]
These bits determine the display mode for either LCD1 or LCD2 depending on the setting of the LCD Output Port Select bits (REG[0202h] bits 12-10).

Table 10-26: Display Mode Selection

REG[0200h] bits 9-8	Display Mode
00b	Main Window only
01b	Main Window and PIP+
10b	Reserved
11b	Main Window and PIP+ with Overlay

bit 7 LCD Software Reset (Write Only)
When this bit is set to 0, there is no hardware effect.
When this bit is set to 1, a software reset is performed on the LCD interface.

bit 6 Reserved
The default value for this bit is 0.

bit 5 LUT2 Bypass Enable
LUT2 is associated with the PIP+ Window. This bit determines if LUT2 is used for output to the PIP+ Window. For more information on the display format when LUT2 is used or bypassed, see Section 13, “Display Data Formats” on page 295.
When this bit = 0, LUT2 is used.
When this bit = 1, LUT2 is bypassed.

bit 4 LUT1 Bypass Enable
LUT1 is associated with the Main Window. This bit determines if LUT1 is used for output to the Main Window. For more information on the display format when LUT1 is used or bypassed, see Section 13, “Display Data Formats” on page 295.
When this bit = 0, LUT1 is used.
When this bit = 1, LUT1 is bypassed.

bit 3-2 PIP+ Window Bits-per-pixel Select bits[1:0]
These bits determine the color depth for the PIP+ Window. For more information, see Section 13, “Display Data Formats” on page 295.

Table 10-27: LUT2 (PIP+ Window) Color Mode Selection

REG[0200h] bits 3-2	Color Depth	LUT2 Bypass Enable	Color
00b	8 bpp	0	LUT2 color format
		1	Data is handled as follows: R_data={r2, r1, r0, r2, r2, r2, r2, r2} G_data={g2, g1, g0, g2, g2, g2, g2, g2} B_data={b1, b0, b1, b1, b1, b1, b1, b1}
01b	16 bpp	0	LUT2 color format
		1	Data is handled as follows: R_data={r4, r3, r2, r1, r0, r4, r4, r4} G_data={g5, g4, g3, g2, g1, g0, g5, g5} B_data={b4, b3, b2, b1,b0, b4, b4, b4}
10b	Reserved	0	Reserved
		1	
11b	Reserved	0	Reserved
		1	

bit 1-0 Main Window Bits-per-pixel Select bits[1:0]

These bits determine the color depth for the Main Window. For more information, see Section 13, “Display Data Formats” on page 295.

Table 10-28: LUT1 (Main Window) Color Mode Selection

REG[0200h] bits 1-0	Color Depth	LUT1 Bypass Enable	Color
00b	8 bpp	0	LUT1 color format
		1	Data is handled as follows: R_data={r2, r1, r0, r2, r2, r2, r2, r2} G_data={g2, g1, g0, g2, g2, g2, g2, g2} B_data={b1, b0, b1, b1, b1, b1, b1, b1}
01b	16 bpp	0	LUT1 color format
		1	Data is handled as follows: R_data={r4, r3, r2, r1, r0, r4, r4, r4} G_data={g5, g4, g3, g2, g1, g0, g5, g5} B_data={b4, b3, b2, b1,b0, b4, b4, b4}
10b	Reserved	0	Reserved
		1	
11b	Reserved	0	Reserved
		1	

REG[0202h] Display Mode Setting Register 1

Default = 0000h Read/Write

Active LCD Port Status bits 2-0 (RO)			n/a	LCD Output Port Select bits 2-0		SW Video Invert	Display Blank
15	14	13	12	11	10	9	8
PIP+ Window Mirror Enable	Reserved	PIP+ Window Swivel View Mode Select bits 1-0		Main Window Mirror Enable	n/a	Main Window Swivel View Mode Select bits 1-0	
7	6	5	4	3	2	1	0

bits 15-13 Active LCD Port Status bits[2:0] (Read Only)

These bits indicate the selected output port is active. Before sending any commands, parameters, or image data to the port, confirm that the desired port is active.

Note

These bits are read only and are only changed using the LCD Output Port Select bits 2-0 (REG[0202h] bits 12-10).

Table 10-29: Active LCD Port Status

REG[0202h] bits 15-13	Active LCD Port
000b	All Off
001b	LCD1
010b	LCD2
011b - 111b	Reserved

bits 11-10 LCD Output Port Select bits [2:0]

These bits specify the valid output port. Changes to these bits take effect after the end of the current frame. The auto transfer bits (REG[003Ch] bit 0) must be cleared before changing these bits.

Table 10-30: LCD Output Port Selection

REG[0202h] bits 11-10	LCD Output Port
00b	All Off
01b	LCD1
10b	LCD2
11b	Reserved

bit 9 Software Video Invert

This bit determines whether the RGB type panel data output (FPDAT[17:0]) is inverted or left unchanged (normal). This bit has an effect when the display is active and when the display is blanked (see REG[0202h] bit 8). For a summary, see Table 10-31: "LCD Interface Data Output Selection".

When this bit = 0, the panel data output is left unchanged (normal).

When this bit = 1, the panel data output is inverted.

Note

If the Software Video Invert bit is set to 1 when configured for an 8-bit parallel panel, the FPDAT[15:8] pins will toggle.

bit 8 Display Blank

This bit blanks the display of RGB Type panels by disabling the display pipe and forcing all data outputs (FPDAT[17:0]) low (or high). For a summary, see Table 10-31: "LCD Interface Data Output Selection".

When this bit = 0, the display is active.

When this bit = 1, display is blanked and all data outputs are forced low or high based on the setting of the Software Video Invert bit (REG[0202h] bit 9).

Table 10-31: LCD Interface Data Output Selection

REG[0202h] bit 8	REG[0202h] bit 9	LCD Interface Data Output
0	0	normal
	1	inverted
1	0	forced low
	1	forced high

Note

For further details, see Table 5-13: "LCD Interface Pin Mapping," on page 46.

bit 7 PIP$^+$ Window Mirror Enable

This bit controls the Mirror Display function for the PIP$^+$ window. Mirror display is independently controlled for the PIP$^+$ Window and the Main window (see REG[0202h] bit 3).

When this bit = 0, mirror display for the PIP$^+$ window is disabled.

When this bit = 1, mirror display for the PIP$^+$ window is enabled.

bit 6 Reserved

The default value for this bit is 0.

bit 5-4 PIP+ Window SwivelView Mode Select bits[1:0]

These bits select the SwivelView mode of the PIP+ window. The SwivelView mode (orientation) of the PIP+ window is independently controlled for the PIP+ window and the Main window (see bits 1-0). SwivelView is a counter-clockwise hardware rotation of the displayed image. For more information on SwivelView, see Section 14, "SwivelView™" on page 310.

Table 10-32: PIP+ Window SwivelView Mode Selection

REG[0202h] bits 5-4	SwivelView Mode
00b	0° (Normal)
01b	90°
10b	180°
11b	270°

bit 3 Main Window Mirror Enable

This bit controls the Mirror Display function for the Main Window. Mirror display is independently controlled for the PIP+ window (bit 7) and the main window.
When this bit = 0, mirror display for the main window is disabled.
When this bit = 1, mirror display for the main window is enabled.

bits 1-0 Main Window SwivelView Mode Select bits[1:0]

These bits select the SwivelView mode of the Main window. The SwivelView mode (orientation) of the Main window is independently controlled for the Main window and the PIP+ window (see bits 5-4). SwivelView is a counter-clockwise hardware rotation of the displayed image. For more information on SwivelView, see Section 14, "SwivelView™" on page 310.

Table 10-33: Main Window SwivelView Mode Selection

REG[0202h] bits 1-0	SwivelView Mode
00b	0° (Normal)
01b	90°
10b	180°
11b	270°

REG[0204h] Transparent Overlay Key Color Red Data Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Transparent Overlay Key Color Red Data bits 7-0							

bits 7-0 Transparent Overlay Key Color Red Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the red color component of the Transparent Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0206h] Transparent Overlay Key Color Green Data Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Transparent Overlay Key Color Green Data bits 7-0							

bits 7-0 Transparent Overlay Key Color Green Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the green color component of the Transparent Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0208h] Transparent Overlay Key Color Blue Data Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Transparent Overlay Key Color Blue Data bits 7-0							

bits 7-0 Transparent Overlay Key Color Blue Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the blue color component of the Transparent Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0210h] Main Window Display Start Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Main Window Display Start Address bits 15-8							
7	6	5	4	3	2	1	0
Main Window Display Start Address bits 7-0							

REG[0212h] Main Window Display Start Address Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a					Reserved	Main Window Display Start Address bits 17-16	

REG[0212h] bits 2-0
REG[0210h] bits 15-0 Main Window Display Start Address bits [18:0]
These bits specify the Main window starting address for the LCD image in the display buffer. At a color depth of 8 bpp, this register is incremented in 8-bit steps. At 16 bpp, this register should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and this register should be set to an even number.

REG[0212h] bit 2 Reserved
The default value for this bit is 0.

REG[0214h] Main Window Start Address Status Register
Default = 0001h — Read Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							Main Window Start Address Status

bit 0 Main Window Start Address Status (Read Only)
When Double Buffer Mode is disabled (REG[0200h] bit 12 = 0), this bit indicates the current main window frame status. This bit is updated only after the Main Window Display Start Address has been changed.
When this bit = 1, the current frame is using the latest Main Window Display Start Address values (REG[0210h] - REG[0212h].
When this bit = 0, the next frame will use the latest Main Window Display Start Address values (REG[0210h] - REG[0212h]).

When Double Buffer Mode is enabled (REG[0200h] bit 12 = 1) and the Main Window is used for the front buffer (REG[0200h] bit 13 = 1), this bit indicates which buffer is currently displayed.
When this bit = 0, the back buffer as defined by the Back Buffer Display Start Address registers (REG[022Ah] - REG[022Ch]) is being displayed.
When this bit = 1, the front buffer which corresponds to the Main window area (REG[0210h] - REG[0212h]) is being displayed.

REG[0216h] Main Window Line Address Offset Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a		Main Window Vertical Pixel Doubling Enable	Main Window Horizontal Pixel Doubling Enable	Main Window Line Address Offset bits 11-8			
Main Window Line Address Offset bits 7-0							
7	6	5	4	3	2	1	0

bit 13 Main Window Vertical Pixel Doubling Enable

This bit controls the pixel doubling feature for the vertical dimension or height of the panel (i.e. 160 pixel high data doubles for a 320 pixel high panel).
When this bit = 0, there is no hardware effect.
When this bit = 1, pixel doubling in the vertical dimension (height) is enabled.

When vertical pixel doubling of the main window is enabled, the main window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 1-0) using the following formulas.
For SwivelView 0°
Address = 0
For SwivelView 90°
Address = (main window height - (bpp/8))
For SwivelView 180°
Address = ((main window height - 1) x (main window width)) - (bpp/8)
For SwivelView 270°
Address = main window line offset x ((main window width ÷ 2) - 1

bit 12 Main Window Horizontal Pixel Doubling Enable

This bit controls the pixel doubling feature for the horizontal dimension or width of the panel (i.e. 160 pixel wide data doubles for a 320 pixel wide panel)
When this bit = 0, there is no hardware effect.
When this bit = 1, pixel doubling in the horizontal dimension (width) is enabled.

When horizontal pixel doubling of the main window is enabled, the main window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 1-0) using the following formulas.
For SwivelView 0°
Address = 0
For SwivelView 90°
Address = (main window height - (bpp/8))
For SwivelView 180°
Address = ((main window height - 1) x (main window width)) - (bpp/8)
For SwivelView 270°
Address = main window line offset x ((main window width ÷ 2) - 1

bits 11-0 Main Window Line Address Offset bits [11:0]
These bits specify the offset from the beginning of one display line to the beginning of the next display line in the memory used for the main window. At a color depth of 8 bpp, these bits should be incremented by 8-bit steps. At 16 bpp, these bits should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and these bits should be set to an even number.

Calculate the Line Address Offset as follows (valid for both pixel doubling enabled and disabled).

REG[0216h] bits 11-0 = Line width in pixels x bpp ÷ 8

REG[0218h] PIP+ Display Start Address Register 0
Default = 0000h Read/Write

PIP+ Display Start Address bits 15-8							
15	14	13	12	11	10	9	8
PIP+ Display Start Address bits 7-0							
7	6	5	4	3	2	1	0

REG[021Ah] PIP+ Display Start Address Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a					Reserved	PIP+ Display Start Address bits 17-16	
7	6	5	4	3	2	1	0

REG[021Ah] bits 1-0
REG[0218h] bits 15-0 PIP+ Display Start Address bits [17:0]
These bits specify the PIP+ window starting address for the LCD image in the display buffer. When the PIP+ function is disabled (REG[0200h] bits 9-8 = 00b), this register is ignored. At a color depth of 8 bpp, this register is incremented in 8-bit steps. At 16 bpp, this register should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and this register should be set to an even number. At 32 bpp, this register should be incremented by 32-bit steps.

REG[021Ah] bit 2 Reserved
The default value for this bit is 0.

REG[021Ch] PIP+ Window Start Address Status Register
Default = 0001h — Read Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							PIP+ Window Start Address Status

bit 0 PIP+ Window Start Address Status (Read Only)
When Double Buffer Mode is disabled (REG[0200h] bit 12 = 0), this bit indicates the current PIP+ window frame status. This bit is updated only after the PIP+ Window Display Start Address has been changed.
When this bit = 0, the next frame will use the latest PIP+ Window Display Start Address values (REG[0218h] - REG[021Ah]).
When this bit = 1, the current frame is using the latest PIP+ Window Display Start Address values (REG[0218h] - REG[021Ah].

When Double Buffer Mode is enabled (REG[0200h] bit 12 = 1) and the PIP+ Window is used for the front buffer (REG[0200h] bit 13 = 0), this bit indicates which buffer is currently displayed.
When this bit = 0, the back buffer as defined by the Back Buffer Display Start Address registers (REG[022Ah] - REG[022Ch]) is being displayed.
When this bit = 1, the front buffer which corresponds to the PIP+ window area (REG[0218h] - REG[021Ah]) is being displayed.

REG[021Eh] PIP+ Window Line Address Offset Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a		PIP+ Window Pixel Doubling Vertical Enable	PIP+ Window Pixel Doubling Horizontal Enable	PIP+ Window Line Address Offset bits 11-8			
7	6	5	4	3	2	1	0
PIP+ Window Line Address Offset bits 7-0							

bit 13 PIP+ Window Pixel Doubling Vertical Enable

This bit controls the pixel doubling feature for the vertical dimension or height of the panel (i.e. 160 pixel high data doubles for a 320 pixel high panel).
When this bit = 0, there is no hardware effect.
When this bit = 1, pixel doubling in the vertical dimension (height) is enabled.

When vertical pixel doubling of the PIP+ window is enabled, the PIP+ window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 5-4) using the following formulas.
For SwivelView 0°
Address = 0
For SwivelView 90°
Address = (PIP+ window height - (bpp/8))
For SwivelView 180°
Address = ((PIP+ window height - 1) x (PIP+ window width)) - (bpp/8)
For SwivelView 270°
Address = PIP+ window line offset x ((PIP+ window width ÷ 2) - 1

bit 12 PIP+ Window Pixel Doubling Horizontal Enable

This bit controls the pixel doubling feature for the horizontal dimension or width of the panel (i.e. 160 pixel wide data doubles for a 320 pixel wide panel)
When this bit = 0, there is no hardware effect.
When this bit = 1, pixel doubling in the horizontal dimension (width) is enabled.

When horizontal pixel doubling of the PIP+ window is enabled, the PIP+ window display start address must be adjusted according to the selected SwivelView mode (see REG[0202h] bits 5-4) using the following formulas.
For SwivelView 0°
Address = 0
For SwivelView 90°
Address = (PIP+ window height - (bpp/8))
For SwivelView 180°
Address = ((PIP+ window height - 1) x (PIP+ window width)) - (bpp/8)
For SwivelView 270°
Address = PIP+ window line offset x ((PIP+ window width ÷ 2) - 1

bits 11-0 PIP+ Window Line Address Offset bits [11:0]

This register specifies the offset from the beginning of one display line to the beginning of the next display line in the memory of the PIP+ window. At a color depth of 8 bpp, these bits should be incremented by 8-bit steps. At 16 bpp, these bits should be incremented by 16-bit steps. 16 bpp pixel data should be mapped from even memory addresses, and these bits should be set to an even number.

Calculate the Line Address Offset as follows (valid for both pixel doubling enabled and disabled).

REG[021Eh] bits 11-0 = Line width in pixels x bpp ÷ 8

Note

When the camera image is being displayed in the PIP+ window, the PIP+ window size must equal the resulting camera frame dimensions after it has been sized and scaled by the resizer.

REG[0220h] PIP+ X Start Positions Register

Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						PIP+ X Start Position bits 9-8	
PIP+ X Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP+ Window X Start Position bits [9:0]

These bits determine the X start position of the PIP+ window in relation to the origin of the panel (in pixels).

Note

When the camera image is being displayed in the PIP+ window, the PIP+ window size must equal the resulting camera frame dimensions after it has been sized and scaled by the resizer.

REG[0222h] PIP+ Y Start Positions Register

Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						PIP+ Y Start Position bits 9-8	
PIP+ Y Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP+ Window Y Start Position bits [9:0]

These bits determine the Y start position of the PIP+ window in relation to the origin of the panel (in pixels).

REG[0224h] PIP+ X End Positions Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP+ X End Position bits 9-8	
7	6	5	4	3	2	1	0
PIP+ X End Position bits 7-0							

bits 9-0 PIP+ Window X End Position bits [9:0]
These bits determine the X end position of the PIP+ window in relation to the origin of the panel (in pixels).

Note
These bits must be set such that the following formula is valid.
REG[0224h] bits 9-0 < Horizontal Display Period

Note
When the camera image is being displayed in the PIP+ window, the PIP+ window size must equal the resulting camera frame dimensions after it has been sized and scaled by the resizer.

REG[0226h] PIP+ Y End Positions Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP+ Y End Position bits 9-8	
7	6	5	4	3	2	1	0
PIP+ Y End Position bits 7-0							

bits 9-0 PIP+ Window Y End Position bits [9:0]
These bits determine the Y end position of the PIP+ window in relation to the origin of the panel (in pixels).

Note
These bits must be set such that the following formula is valid.
REG[0226h] bits 9-0 < Vertical Display Period

Note
When the camera image is being displayed in the PIP+ window, the PIP+ window size must equal the resulting camera frame dimensions after it has been sized and scaled by the resizer.

REG[0228h] is Reserved

This register is Reserved and should not be written.

REG[022Ah] Back Buffer Display Start Address Register 0
Default = 0000h — Read/Write

Buck Buffer Display Start Address bits 15-8							
15	14	13	12	11	10	9	8
Back Buffer Display Start Address bits 7-0							
7	6	5	4	3	2	1	0

REG[022Ch] Back Buffer Display Start Address Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a					Reserved	Back Buffer Display Start Address bits 17-16	
7	6	5	4	3	2	1	0

REG[022Ch] bits 1-0
REG[022Ah] bits 15-0 Back Buffer Display Start Address bits [17:0]
These bits specify the Back Buffer window starting address for the LCD image in the display buffer. When the Double Buffer function is disabled (REG[0200h] bit 12 = 0), this register is ignored.

REG[022Ch] bit 2 Reserved
The default value for this bit is 0.

REG[0240h] YUV/RGB Translate Mode Register
Default = 0405h — Read/Write

YUV/RGB Converter Bypass Enable	YUV/RGB Converter Reset	UV Fix bits 1-0		YRC Output Bpp Select bits 1-0		n/a	YUV Output Data Format Select
15	14	13	12	11	10	9	8
Reserved	YUV/RGB Rectangular Write Mode Enable	Frame Buffer Writing Mode Select	YUV Input Data Type Select	n/a	YUV/RGB Transfer Mode bits 2-0		
7	6	5	4	3	2	1	0

bit 15 YUV/RGB Converter Bypass Enable
When YUV/RGB Converter (YRC) bypass mode is enabled, YUV data from the camera interface or JPEG decoder, or Host goes directly into the internal memory. When the YRC is enabled (bypass mode is disabled), incoming YUV data is converted to RGB format and stored in the display buffer to be displayed by the LCD panel.
When this bit = 0, YUV/RGB Converter bypass mode is disabled (default).
When this bit = 1, YUV/RGB Converter bypass mode is enabled.

Note
The YUV/RGB converter swaps the incoming byte data when it is disabled. To change the YUV data back to normal, set the YRC Output Data Format Select bit (REG[0240h] bit 8) to 1. Disabling the YRC is useful for cameras that can output RGB data.

bit 14 YUV/RGB Converter Reset

This bit is resets the YUV/RGB Converter (YRC). It has no effect on the YRC registers. The YRC should be reset after any changes are made to the Resizer Operation registers (REG[0930h]-[096Eh] and before performing a Memory Image JPEG Encode operation.
When this bit is set to 0, the YRC is available for use.
When this bit is set to 1, the YUV/RGB Converter is reset. This bit must be set back to 0 before the YUV/RGB Converter can be used again.

bits 13-12 UV Fix Select bits [1:0]

These bits control the UV input to the YUV/RGB Converter (YRC). The setting of these bits has an effect on the UV data even when the YRC is disabled (REG[0240h] bit 15 = 1)..

Table 10-34: UV Fix Selection

REG[0240h] bits 13-12	UV Input to the YUV/RGB Converter
00b	Original U data, original V data
01b	U data = REG[024Ah] bits 15-8, original V data
10b	Original U data, V data = REG[024Ah] bits 7-0
11b	U data = REG[024Ah] bits 15-8, V data = REG[024Ah] bits 7-0

bits 11-10 YRC Output Bpp Select bits [1:0]

These bits specify the color depth in bits-per-pixel (bpp) for the YUV/RGB Converter output.

Table 10-35: YUV/RGB Converter Output Bpp Selection

REG[0240h] bits 11-10	YUV/RGB Converter Output Bpp
00b	16 bpp
01b (default)	
10b	Reserved
11b	Reserved

bit 8 YRC Output Data Format Select

This bit selects the output data format of the YUV/RGB Converter (YRC) when it is disabled (REG[0240h] bit 15 = 1). This bit has no effect when the YRC is enabled (REG[0240h] bit 15 = 0).
When this bit = 0, VYUY format is selected. See Table 10-36: “VYUY Output Data Format (REG[0240h] bit 8 = 0),” on page 178.
When this bit = 1, YUYV format is selected. See Table 10-37: “YUYV Output Data Format Select (REG[0240h] bit 8 = 1),” on page 178.

Table 10-36: VYUY Output Data Format (REG[0240h] bit 8 = 0)

Cycle Count	1	2	3	4	...	2n+1	2n+2
D15	V_0^7	U_0^7	V_2^7	U_2^7	...	V_{2n}^7	U_{2n}^7
D14	V_0^6	U_0^6	V_2^6	U_2^6	...	V_{2n}^6	U_{2n}^6
D13	V_0^5	U_0^5	V_2^5	U_2^5	...	V_{2n}^5	U_{2n}^5
D12	V_0^4	U_0^4	V_2^4	U_2^4	...	V_{2n}^4	U_{2n}^4
D11	V_0^3	U_0^3	V_2^3	U_2^3	...	V_{2n}^3	U_{2n}^3
D10	V_0^2	U_0^2	V_2^2	U_2^2	...	V_{2n}^2	U_{2n}^2
D9	V_0^1	U_0^1	V_2^1	U_2^1	...	V_{2n}^1	U_{2n}^1
D8	V_0^0	U_0^0	V_2^0	U_2^0	...	V_{2n}^0	U_{2n}^0
D7	Y_1^7	Y_0^7	Y_3^7	Y_2^7	...	Y_{2n+1}^7	Y_{2n}^7
D6	Y_1^6	Y_0^6	Y_3^6	Y_2^6	...	Y_{2n+1}^6	Y_{2n}^6
D5	Y_1^5	Y_0^5	Y_3^5	Y_2^5	...	Y_{2n+1}^5	Y_{2n}^5
D4	Y_1^4	Y_0^4	Y_3^4	Y_2^4	...	Y_{2n+1}^4	Y_{2n}^4
D3	Y_1^3	Y_0^3	Y_3^3	Y_2^3	...	Y_{2n+1}^3	Y_{2n}^3
D2	Y_1^2	Y_0^2	Y_3^2	Y_2^2	...	Y_{2n+1}^2	Y_{2n}^2
D1	Y_1^1	Y_0^1	Y_3^1	Y_2^1	...	Y_{2n+1}^1	Y_{2n}^1
D0	Y_1^0	Y_0^0	Y_3^0	Y_2^0	...	Y_{2n+1}^0	Y_{2n}^0

Table 10-37: YUYV Output Data Format Select (REG[0240h] bit 8 = 1)

Cycle Count	1	2	3	4	...	2n+1	2n+2
D15	Y_0^7	Y_1^7	Y_2^7	Y_3^7	...	Y_{2n}^7	Y_{2n+1}^7
D14	Y_0^6	Y_1^6	Y_2^6	Y_3^6	...	Y_{2n}^6	Y_{2n+1}^6
D13	Y_0^5	Y_1^5	Y_2^5	Y_3^5	...	Y_{2n}^5	Y_{2n+1}^5
D12	Y_0^4	Y_1^4	Y_2^4	Y_3^4	...	Y_{2n}^4	Y_{2n+1}^4
D11	Y_0^3	Y_1^3	Y_2^3	Y_3^3	...	Y_{2n}^3	Y_{2n+1}^3
D10	Y_0^2	Y_1^2	Y_2^2	Y_3^2	...	Y_{2n}^2	Y_{2n+1}^2
D9	Y_0^1	Y_1^1	Y_2^1	Y_3^1	...	Y_{2n}^1	Y_{2n+1}^1
D8	Y_0^0	Y_1^0	Y_2^0	Y_3^0	...	Y_{2n}^0	Y_{2n+1}^0
D7	U_0^7	V_0^7	U_2^7	V_2^7	...	U_{2n}^7	V_{2n+1}^7
D6	U_0^6	V_0^6	U_2^6	V_2^6	...	U_{2n}^6	V_{2n+1}^6
D5	U_0^5	V_0^5	U_2^5	V_2^5	...	U_{2n}^5	V_{2n+1}^5
D4	U_0^4	V_0^4	U_2^4	V_2^4	...	U_{2n}^4	V_{2n+1}^4
D3	U_0^3	V_0^3	U_2^3	V_2^3	...	U_{2n}^3	V_{2n+1}^3
D2	U_0^2	V_0^2	U_2^2	V_2^2	...	U_{2n}^2	V_{2n+1}^2
D1	U_0^1	V_0^1	U_2^1	V_2^1	...	U_{2n}^1	V_{2n+1}^1
D0	U_0^0	V_0^0	U_2^0	V_2^0	...	U_{2n}^0	V_{2n+1}^0

bit 7 Reserved
The default value for this bit is 0.

bit 6 YUV/RGB Rectangular Write Mode Enable

When this bit = 0, continuous write mode is selected. In continuous write mode, data is written to the frame buffer continuously based on the YUV/RGB Converter Frame Buffer Write Start Address registers (REG[0242h]-[0244h]).

When this bit = 1, rectangular write mode is selected. In rectangular write mode, data is written based on the X Pixel Size register (REG[024Ch]) and the Frame Buffer Line Address Offset register (REG[024Eh]).

Note

YUV/RGB Rectangular Write Mode may only be enabled when Single Buffer Writing Mode is selected (REG[0240h] bit 5 = 0).

bit 5 Frame Buffer Writing Mode Select

This bit determines the write mode used by the YRC when writing YUV data to the frame buffer.

When this bit = 0, single buffer write mode is selected. In single buffer write mode, frames of data are written only to the memory section defined by REG[0244h] - REG[0242h].

When this bit = 1, double buffer write mode is selected. In double buffer write mode, frames of data are written alternately between the memory section defined by REG[0244h] - REG[0242h] and the the memory section defined by REG[0248h] - REG[0246h]. This mode can be used with double buffer mode (REG[0200h] bit 12 = 1) to prevent “tearing” of the camera image for fast moving images.

bit 4 YRC Input Data Type Select

This bit specifies the data type of the YUV input to the YUV to RGB Converter (YRC).

Table 10-38: YUV Data Type Selection

REG[0240h] bit 4	YRC Input Data Type	YRC Input Data Range
0	YUV Offset	$0 \le Y \le 255$ $-128 \le U \le 127$ $-128 \le V \le 127$
1	YCbCr Offset	$16 \le Y \le 235$ $-113 \le U \le 112$ $-113 \le V \le 112$

bits 2-0 YUV/RGB Transfer Mode bits [2:0]

These bits specify the YUV/RGB Transfer mode. Recommended settings are provided for various specifications..

Table 10-39: YUV/RGB Transfer Mode Selection

REG[0240h] bits 2-0	YUV/RGB Specification
000b	Reserved
001b	Recommended for ITU-R BT.709
010b	Reserved
011b	Reserved
100b	Recommended for ITU-R BT.470-6 System M
101b (Default)	Recommended for ITU-R BT.470-6 System B, G (Recommended for ITU-R BT.601-5)
110b	SMPTE 170M
111b	SMPTE 240M(1987)

REG[0242h] YUV/RGB Converter Write Start Address 0 Register 0
Default = 0000h Read/Write

YUV/RGB Converter Write Start Address 0 bits 15-8							
15	14	13	12	11	10	9	8
YUV/RGB Converter Write Start Address 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[0244h] YUV/RGB Converter Write Start Address 0 Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a					Reserved	YUV/RGB Converter Write Start Address bits 18-16	
7	6	5	4	3	2	1	0

REG[0244h] bits 1-0
REG[0242h] bits 15-0 YUV/RGB Converter Write Start Address 0 bits [17:0]
These bits determine the start address where the YUV/RGB Converter writes data. The YUV/RGB Converter writes data to the display buffer in 32-bit blocks, therefore bits 1-0 of REG[0242h] must be set to 00b.

REG[0244h] bit 2 Reserved
The default value for this bit is 0.

REG[0246h] YUV/RGB Converter Write Start Address 1 Register 0
Default = 0000h Read/Write

YUV/RGB Converter Write Start Address 1 bits 15-8							
15	14	13	12	11	10	9	8
YUV/RGB Converter Write Start Address 1 bits 7-0							
7	6	5	4	3	2	1	0

REG[0248h] YUV/RGB Converter Write Start Address 1 Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a					Reserved	YUV/RGB Converter Write Start Address 1 bits 17-16	
7	6	5	4	3	2	1	0

REG[0248h] bits 2-0
REG[0246h] bits 15-0 YUV/RGB Converter Write Start Address 1 bits [18:0]
These bits determine the start address for data input from the camera interface and for JPEG decoded images. This register value is valid when Frame Buffer Writing Mode Select bit (REG[0240h] bit 5) is set for double buffer writing mode.

REG[0248h] bit 2 Reserved
The default value for this bit is 0.

REG[024Ah] UV Data Fix Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
U Data Fix bits 7-0							
7	6	5	4	3	2	1	0
V Data Fix bits 7-0							

bits 15-8 U Data Fix bits [7:0]
These bits only have an effect when the UV Fix Select bits are set to 01b or 11b (REG[0240h] bits 13-12 = 01b or 11b). The U Data Input of the YUV/RGB Converter data is fixed to the value of these bits.

bits 7-0 V Data Fix bits [7:0]
These bits only have an effect when the UV Fix Select bits are set to 10b or 11b (REG[0240h] bits 13-12 = 10b or 11b). The V Data Input of YUV/RGB Converter data is fixed to the value of these bits.

REG[024Ch] YRC Rectangle Pixel Width Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a					YRC Rectangular Pixel Width bits 10-8		
7	6	5	4	3	2	1	0
YRC Rectangular Pixel Width bits 7-0							

bits 10-0 YRC Rectangular Pixel Width Bits [10:0]
These bits specify the horizontal pixel size of the data being written when the YUV/RGB Converter (YRC) is configured for rectangular write mode (REG[0240h] bit 6 = 1).
For a color depth of 16 bpp, it specifies an even number of pixels (only bits 9-1 are used).

REG[024Eh] YRC Rectangular Line Address Offset Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a				YRC Rectangular Line Address Offset bits 11-8			
7	6	5	4	3	2	1	0
YRC Rectangular Line Address Offset bits 7-0							

bits 11-0 YRC Rectangular Line Address Offset Bits [11:0]
These bits specify the number of pixels from the beginning of the current display line to the beginning of the next line when the YUV/RGB Converter (YRC) is configured for rectangular write mode (REG[0240h] bit 6 = 1).
For a color depth of 16 bpp, it specifies an even number of pixels (only bits 11-1 are used).
When the YUV/RGB Converter is disabled, it specifies every pixel (all bits 11-0 are used).

REG[0268h] is Reserved

This register is Reserved and should not be written.

REG[0280h] is Reserved

This register is Reserved and should not be written.

10.4.9 GPIO Registers

REG[0300h] GPIO Status and Control Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				GPIO3 Config	GPIO2 Config	GPIO1 Config	GPIO0 Config

bits 15-4 Reserved
The default value for these bits is 0.

bits 3-0 GPIO[3:0] Pin IO Configuration
When the GPIO pins (GPIO[3:0]) are configured as inputs at RESET# (CNF1 = 1), these bits can be used to change individual GPIO pins between inputs/outputs. When the GPIO pins are configured as outputs at RESET# (CNF1 = 0), these bits are ignored and the GPIO pins are always outputs.
When a bit = 0 (default), the corresponding GPIO pin is configured as an input pin.
When a bit = 1, the corresponding GPIO pin is configured as an output pin.

REG[0304h] GPIO Status and Control Register 3
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				GPIO3 Input Enable	GPIO2 Input Enable	GPIO1 Input Enable	GPIO0 Input Enable

bits 15-4 Reserved
The default value for these bits is 0.

bits 3-0 GPIO[3:0] Pin Input Enable
These bits are used to enable the input function of each GPIO pin. They must be changed to a 1 after power-on reset to enable the input function of the corresponding GPIO pin.
When a bit = 0 (default), the input function for the corresponding GPIO pin is disabled.
When a bit = 1, the input function for the corresponding GPIO pin is enabled.

Note
When the GPIO pins are configured as outputs at RESET# (CNF1 = 0), the GPIO pins are always outputs and these bits have no effect.

REG[0308h] GPIO Pull Down Control Register 0
Default = FFFFh — Read/Write

Reserved							
15	14	13	12	11	10	9	8
Reserved				GPIO3 Pull-down Control	GPIO2 Pull-down Control	GPIO1 Pull-down Control	GPIO0 Pull-down Control
7	6	5	4	3	2	1	0

bits 15-4 Reserved
The default value for these bits is FFFh.

bits 3-0 GPIO[3:0] Pull-down Control
All GPIO pins have internal pull-down resistors. These bits individually control the state of the pull-down resistors.
When a bit = 0, the pull-down resistor for the associated GPIO pin is inactive.
When a bit = 1, the pull-down resistor for the associated GPIO pin is active (Default).

REG[030Ch] GPIO Status and Control Register 4
Default = 0000h — Read/Write

Reserved							
15	14	13	12	11	10	9	8
Reserved				GPIO3 Status	GPIO2 Status	GPIO1 Status	GPIO0 Status
7	6	5	4	3	2	1	0

bits 15-4 Reserved
The default value for these bits is 0.

bits 3-0 GPIO[3:0] Pin IO Status
When GPIOx is configured as an output (see REG[0300h]), writing a 0 to this bit drives the corresponding GPIOx low and writing a 1 to this bit drives the corresponding GPIOx high. When GPIOx is configured as an input (see REG[0300h]), a read from this bit returns the status of the corresponding GPIOx.

Note
To read the status of a GPIO pin configured as an input, the GPIO pin must first have it's input function enabled using REG[0304h].

10.4.10 Overlay Registers

REG[0310h] Average Overlay Key Color Red Data Register
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
Average Overlay Key Color Red Data bits 7-0							
7	6	5	4	3	2	1	0

bit 7-0 Average Overlay Key Color Red Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the red color component of the Average Overlay Key Color. For more information on Overlays, see Section 15.1, "Overlay Display" on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, "Bit Cover When LUT Bypassed" on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn't apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0312h] Average Overlay Key Color Green Data Register
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
Average Overlay Key Color Green Data bits 7-0							
7	6	5	4	3	2	1	0

bit 7-0 Average Overlay Key Color Green Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the green color component of the Average Overlay Key Color. For more information on Overlays, see Section 15.1, "Overlay Display" on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, "Bit Cover When LUT Bypassed" on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn't apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0314h] Average Overlay Key Color Blue Data Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Average Overlay Key Color Blue Data bits 7-0							

bit 7-0 Average Overlay Key Color Blue Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the blue color component of the Average Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0316h] AND Overlay Key Color Red Data Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
AND Overlay Key Color Red Data bits 7-0							

bit 7-0 AND Overlay Key Color Red Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the red color component of the AND Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0318h] AND Overlay Key Color Green Data Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
AND Overlay Key Color Green Data bits 7-0							
7	6	5	4	3	2	1	0

bit 7-0 AND Overlay Key Color Green Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the green color component of the AND Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[031Ah] AND Overlay Key Color Blue Data Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
AND Overlay Key Color Blue Data bits 7-0							
7	6	5	4	3	2	1	0

bit 7-0 AND Overlay Key Color Blue Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the blue color component of the AND Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. If this function doesn’t apply to a display area, it still prevents a lower priority function from taking effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[031Ch] OR Overlay Key Color Red Data Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
OR Overlay Key Color Red Data bits 7-0							
7	6	5	4	3	2	1	0

bit 7-0 OR Overlay Key Color Red Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the red color component of the OR Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[031Eh] OR Overlay Key Color Green Data Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
OR Overlay Key Color Green Data bits 7-0							
7	6	5	4	3	2	1	0

bit 7-0 OR Overlay Key Color Green Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the green color component of the OR Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0320h] OR Overlay Key Color Blue Data Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
OR Overlay Key Color Blue Data bits 7-0							
7	6	5	4	3	2	1	0

bit 7-0 OR Overlay Key Color Blue Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the blue color component of the OR Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0322h] INV Overlay Key Color Red Data Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
INV Overlay Key Color Red Data bits 7-0							
7	6	5	4	3	2	1	0

bit 7-0 INV Overlay Key Color Red Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the red color component of the INV Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0324h] INV Overlay Key Color Green Data Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
INV Overlay Key Color Green Data bits 7-0							

bit 7-0 INV Overlay Key Color Green Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the green color component of the INV Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0326h] INV Overlay Key Color Blue Data Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
INV Overlay Key Color Blue Data bits 7-0							

bit 7-0 INV Overlay Key Color Blue Data bits [7:0]
These bits only have an effect when PIP+ with Overlay is enabled (REG[0200h] bits 9-8 = 11b). These bits set the blue color component of the INV Overlay Key Color. For more information on Overlays, see Section 15.1, “Overlay Display” on page 316.

Note
If LUT bypass mode is enabled (see REG[0200h] bits 5-4), the key color bits must be expanded to a full 8 bits using the bit cover method in Section 13.3.2, “Bit Cover When LUT Bypassed” on page 298.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

REG[0328h] Overlay Miscellaneous Register
Default = 0000h Read/Write

Overlay PIP+ Window Bit Shift	n/a	Overlay Main Window Bit Shift	n/a				
15	14	13	12	11	10	9	8
n/a			INV Overlay Key Color Enable	OR Overlay Key Color Enable	AND Overlay Key Color Enable	Average Overlay Key Color Enable	Transparent Overlay Key Color Enable
7	6	5	4	3	2	1	0

bit 15 Overlay PIP$^+$ Window Bit Shift
This bit only has an effect if the Display Mode Select bits are set for PIP$^+$ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 316.
When this bit = 0, the PIP$^+$ window pixel data is normal.
When this bit = 1, the PIP$^+$ window is pixel data is bit shifted to the right by 1 bit.

bits 13 Overlay Main Window Bit Shift
This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11b) and any Overlay Key Color Enable bit is set to 1. For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 316.
When this bit = 0, the main window pixel data is normal.
When this bit = 1, the main window pixel data is bit shifted to the right by 1 bit.

bit 4 INV Overlay Key Color Enable
This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 316.
When this bit = 0, the INV overlay key color function is disabled.
When this bit = 1, the INV overlay key color function is enabled.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

bit 3 OR Overlay Key Color Enable
This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 316.
When this bit = 0, the OR overlay key color function is disabled.
When this bit = 1, the OR overlay key color function is enabled.

Note
If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

bit 2 AND Overlay Key Color Enable

This bit only has an effect if the Display Mode Select bits are set for PIP+ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 316.

When this bit = 0, the AND overlay key color function is disabled.

When this bit = 1, the AND overlay key color function is enabled.

Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

bit 1 Average Overlay Key Color Enable

This bit only has an effect if the Display Mode Select bits are set for PIP$^+$ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 316.

When this bit = 0, the average overlay key color function is disabled.

When this bit = 1, the average overlay key color function is enabled.

Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

bit 0 Transparent Overlay Key Color Enable

This bit only has an effect if the Display Mode Select bits are set for PIP$^+$ with Overlay (REG[0200h] bits 9-8 = 11b). For more information on the Overlay function, see Section 15.1, “Overlay Display” on page 316.

When this bit = 0, the transparent overlay key color function is disabled.

When this bit = 1, the transparent overlay key color function is enabled.

Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. However, if this function doesn’t apply to a display area, the next lower priority function takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color.

10.4.11 LUT1 (Main Window) Registers

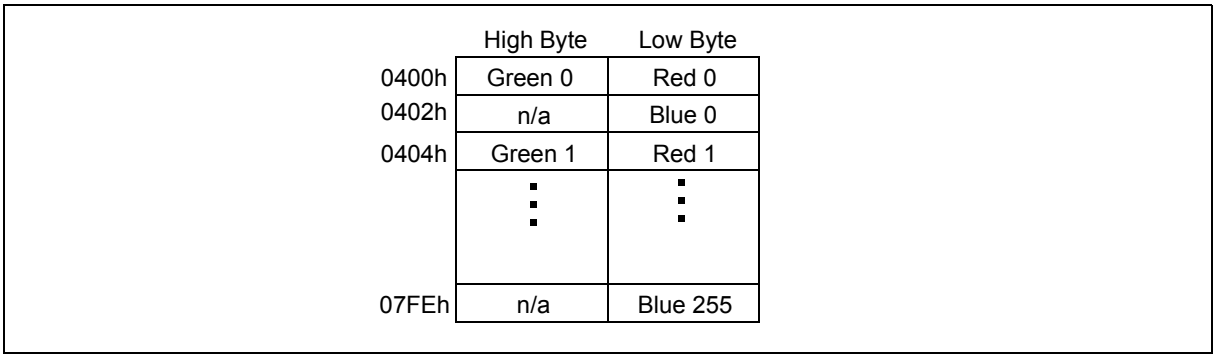


Figure 10-2: LUT1 Mapping

REG[0400 - 07FCh] LUT1 Data Register 0
Default = not applicable — Read/Write

15	14	13	12	11	10	9	8
LUT1 Green Data bits 7-0							
7	6	5	4	3	2	1	0
LUT1 Red Data bits 7-0							

bits 15-8 LUT1 (Main Window) Green Data bits [7:0]
These bits are used to set the LUT1 Green Data. There are 256 entries in LUT1 from 0400h to 07FCh. LUT1 is used for the Main Window.

bits 7-0 LUT1 (Main Window) Red Data bits [7:0]
These bits are used to set the LUT1 Red Data. There are 256 entries in LUT1 from 0400h to 07FCh. LUT1 is used for the Main Window.

REG[0402 - 07FEh] LUT1 Data Register 1
Default = not applicable — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LUT1 Blue Data bits 7-0							

bits 7-0 LUT1 (Main Window) Blue Data bits [7:0]
These bits are used to set the LUT1 Blue Data. There are 256 entries in LUT1 from 0402h to 07FEh. LUT1 is used for the Main Window.

10.4.12 LUT2 (PIP+ Window) Registers

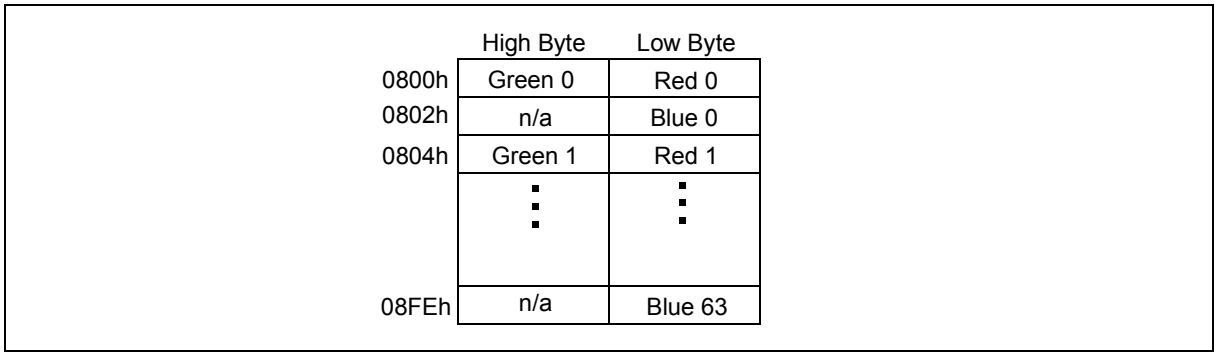


Figure 10-3: LUT2 mapping

REG[0800 - 08FCh] LUT2 Data Register 0
Default = not applicable — Read/Write

15	14	13	12	11	10	9	8
LUT2 Green Data bits 7-0							
7	6	5	4	3	2	1	0
LUT2 Red Data bits 7-0							

bits 15-8 LUT2 (PIP+ Window) Green Data bits [7:0]
These bits are used to set the LUT2 Green Data. There are 64 entries in LUT2 from 0800h to 08FCh. LUT2 is used for the PIP+ Window.

bits 7-0 LUT2 (PIP+ Window) Red Data bits [7:0]
These bits are used to set the LUT2 Red Data. There are 64 entries in LUT2 from 0800h to 08FCh. LUT2 is used for the PIP+ Window.

REG[0802 - 08FEh] LUT2 Data Register 1
Default = not applicable — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LUT2 Blue Data bits 7-0							

bits 7-0 LUT2 (PIP+ Window) Blue Data bits [7:0]
These bits are used to set the LUT2 Blue Data. There are 64 entries in LUT2 from 0802h to 08FEh. LUT2 is used for the PIP+ Window.

10.4.13 Resizer Operation Registers

Note

The resizer registers must not be changed while receiving data from the camera interface, JPEG decoder, or host interface.

REG[0930h] Global Resizer Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a					Resizer Frame Reduction	Reserved	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a			Reserved	Output Source Select	n/a	Camera Display Control bits 1-0	

bit 10 Resizer Frame Reduction
This bit controls frame reduction in the resizer block.
When this bit = 0, the resizer performs no reduction.
When this bit = 1, the resizer performs frame reduction by using only every second frame.

bit 9 Reserved
The default value for this bit is 0.

bit 8 Reserved
The default value for this bit is 0.

bit 4 Reserved
The default value for this bit is 0.

bit 3 Output Source Select

This bit selects which resizer outputs data to the YUV/RGB Converter (YRC). Typically, the view resizer is selected when data comes from the camera interface since JPEG encode dimensions may differ from display dimensions. For JPEG decode and host to S1D13717 YUV mode, the view resizer must be selected.

When this bit = 0, the view resizer outputs data to the YRC.

When this bit = 1, the capture resizer outputs data to the YRC and the view resizer logic is powered down.

Note

During JPEG encoding, this bit must be set to an active resizer, or the YRC must be disabled (REG[0240h] bit 14 = 1).

Table 10-40: Output Source Select

Output Source Select REG[0930h] bit 3	View Resizer Enable REG[0940h] bit 0	Capture Resizer Enable REG[0960h] bit 0	to YUV/RGB Converter	to JPEG Line Buffer
0	0	0	—	—
0	0	1	—	—
0	1	0	Available	—
0	1	1	Available	Available
1	0	0	—	—
1	0	1	Available	Available
1	1	0	—	—
1	1	1	Available	Available

0: View Resizer Selected
1: Capture Resizer Selected

bits 1-0 Camera Display Control bits [1:0]

These bits control how camera data is displayed when a JPEG encode operation is performed (REG[0980h] bits 3-1 = 000b) and when YUV to Host mode (JPEG Bypass) is enabled (REG[0980h] bits 3-1 = 011b or 111b).

Table 10-41: Camera Display Control Selection

REG[0930h] bits 1-0	Function
00b	**JPEG Encode:** YUV data from the camera interface is continuously written to the display buffer until a JPEG encode operation is performed. When a JPEG encode operation is started (REG[098Ah] bit 0 = 1), camera data is no longer written to the display buffer once the next frame is written. After REG[098Ah] bit 0 is set to 0, camera data is again written to the display buffer from the next frame. **JPEG Bypass:** YUV data from the camera interface is continuously written to the JPEG FIFO and converted YUV data (YUV/RGB Converter) is continuously written to the display buffer.
01b	**JPEG Encode:** When a JPEG encode operation is started, REG[098A] bit 0 = 1b, only the next frame of camera data is written to the display buffer. When a JPEG encode operation is not enabled, REG[098A] bit 0 = 0b, camera data is not written to the display buffer. **JPEG Bypass:** YUV data from the camera interface is continuously written to the JPEG FIFO. When the shutter is enabled, REG[098A] bit 0 = 1b, camera data is written to the display buffer. When the shutter is disabled, REG[098A] bit 0 = 0b, camera data is not written to the display buffer.
10b	**JPEG Encode:** Data from the camera interface is always written to the display buffer. **JPEG Bypass:** YUV data from the camera interface is continuously written to the JPEG FIFO and converted YUV data (YUV/RGB Converter) is continuously written to the display buffer.
11b	Reserved.

REG[0932h] through REG[093Eh] are Reserved

These registers are Reserved and should not be written.

REG[0940h] View Resizer Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a					Reserved	n/a	

7	6	5	4	3	2	1	0
View Resizer Software Reset (WO)	n/a				View Resizer Independent Horizontal/Vertical Scaling Enable	View Resizer Register Update VSYNC Enable	View Resizer Enable

bit 10 Reserved
The default value for this bit is 0.

bit 7 View Resizer Software Reset (Write Only)
When a 0 is written to this bit, there is no hardware effect.
When the resizers are activated by writing a 1 to REG[0940h] bit 0 or REG[0960h] bit 0 and a 1 is written to this bit, the view resizer logic is reset.

bit 2 View Resizer Independent Horizontal/Vertical Scaling Enable
When this bit = 0, the horizontal and vertical scaling rates are the same. Both horizontal and vertical scaling rates are controlled by REG[094Ch] bits 5-0.
When this bit = 1, the horizontal and vertical scaling rates can be selected independently. Horizontal scaling rate is controlled by REG[094Ch] bits 5-0 and vertical scaling rate is controlled by REG[094Ch] bits 13-8.

bit 1 View Resizer Register Update VSYNC Enable
When this bit = 0, the View Resizer use the new register value immediately.
When this bit = 1, the View Resizer uses the previous register value until the next camera VSYNC occurs.

bit 0 View Resizer Enable
This bit controls the view resizer logic.
When this bit = 0, the view resizer logic is disabled.
When this bit = 1, the view resizer logic is enabled.

Note
When this bit and the Capture Resizer Enable bit (REG[0960h] bit 0) are both set to 0, the clock to the resizer block is automatically stopped.

REG[0944h] View Resizer Start X Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a					Reserved	View Resizer Start X Position bits 9-8	
View Resizer Start X Position bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved
The default value for this bit is 0.

bits 9-0 View Resizer Start X Position bits [9:0]
These bits determine the X start position for the View Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 337.

REG[0946h] View Resizer Start Y Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a					Reserved	View Resizer Start Y Position bits 9-8	
View Resizer Start Y Position bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved
The default value for this bit is 0.

bits 9-0 View Resizer Start Y Position bits [9:0]
These bits determine the Y start position for the View Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 337.

REG[0948h] View Resizer End X Position Register
Default = 027Fh — Read/Write

n/a					Reserved	View Resizer End X Position bits 9-8	
15	14	13	12	11	10	9	8
View Resizer End X Position bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved
The default value for this bit is 0.

bits 9-0 View Resizer End X Position bits [9:0]
These bits determine the X End position for the View Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 337.

REG[094Ah] View Resizer End Y Position Register
Default = 01DFh — Read/Write

n/a					Reserved	View Resizer End Y Position bits 9-8	
15	14	13	12	11	10	9	8
View Resizer End Y Position bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved
The default value for this bit is 0.

bits 9-0 View Resizer End Y Position bits [9:0]
These bits determine the Y end position for the View Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 337.

REG[094Ch] View Resizer Operation Setting Register 0
Default = 0101h — Read/Write

n/a		View Resizer Vertical Scaling Rate bits 5-0					
15	14	13	12	11	10	9	8
n/a		View Resizer Horizontal Scaling Rate bits 5-0					
7	6	5	4	3	2	1	0

bits 13-8 View Resizer Vertical Scaling Rate bits [5:0]
These bits determine the view resizer vertical scaling rate when independent horizontal/vertical scaling is enabled (REG[0940h] bit 2 = 1). Not all scaling rates are available for all scaling modes (see REG[094Eh] bits 1-0). For a summary of the available scaling rate/mode options, see Table 10-42: “View Resizer Vertical Scaling Rate Selection,” on page 200.

Table 10-42: View Resizer Vertical Scaling Rate Selection

REG[094Ch] bits 13-8	View Resizer Vertical Scaling Rate			
	REG[094Eh] bits 1-0 = 00	REG[094Eh] bits 1-0 = 01	REG[094Eh] bits 1-0 = 10	REG[094Eh] bits 1-0 = 11
00 0000b	Reserved	Reserved	Reserved	Reserved
00 0001b	n/a	1/1	1/1	Reserved
00 0010b	n/a	1/2	1/2	Reserved
00 0011b	n/a	1/3	1/3	Reserved
00 0100b	n/a	1/4	1/4	Reserved
00 0101b	n/a	1/5	1/5	Reserved
00 0110b	n/a	1/6	1/6	Reserved
00 0111b	n/a	1/7	1/7	Reserved
00 1000b	n/a	1/8	1/8	Reserved
00 1001b	n/a	1/9	1/9	Reserved
00 1010b	n/a	1/10	1/10	Reserved
00 1011b	n/a	1/11	1/11	Reserved
00 1100b	n/a	1/12	1/12	Reserved
00 1101b	n/a	1/13	1/13	Reserved
00 1110b	n/a	1/14	1/14	Reserved
00 1111b	n/a	1/15	1/15	Reserved
01 0000b	n/a	1/16	1/16	Reserved
01 0001b	n/a	1/17	1/17	Reserved
01 0010b	n/a	1/18	1/18	Reserved
01 0011b	n/a	1/19	1/19	Reserved
01 0100b	n/a	1/20	1/20	Reserved
01 0101b	n/a	1/21	1/21	Reserved
01 0110b	n/a	1/22	1/22	Reserved
01 0111b	n/a	1/23	1/23	Reserved
01 1000b	n/a	1/24	1/24	Reserved
01 1001b	n/a	1/25	1/25	Reserved
01 1010b	n/a	1/26	1/26	Reserved
01 1011b	n/a	1/27	1/27	Reserved
01 1100b	n/a	1/28	1/28	Reserved
01 1101b	n/a	1/29	1/29	Reserved
01 1110b	n/a	1/30	1/30	Reserved
01 1111b	n/a	1/31	1/31	Reserved
10 0000b	n/a	1/32	1/32	Reserved
10 0001b - 11 1111b	Reserved	Reserved	Reserved	Reserved

bits 5-0 View Resizer Horizontal Scaling Rate bits [5:0]

When independent horizontal/vertical scaling is disabled (REG[0940h] bit 2 = 0), these bits determine the vertical and horizontal scaling rate. When independent horizontal/vertical scaling is enabled (REG[0940h] bit 2 = 1), these bits only determine the horizontal scaling rate. Not all scaling rates are available for all scaling modes (see REG[094Eh] bits 1-0). For a summary of the available scaling rate/mode options, see Table 10-43: "View Resizer Horizontal Scaling Rate Selection," on page 201.

Table 10-43: View Resizer Horizontal Scaling Rate Selection

REG[094Ch] bits 5-0	View Resizer Horizontal Scaling Rate			
	REG[094Eh] bits 1-0 = 00	**REG[094Eh] bits 1-0 = 01**	**REG[094Eh] bits 1-0 = 10**	**REG[094Eh] bits 1-0 = 11**
00 0000b	Reserved	Reserved	Reserved	Reserved
00 0001b	n/a	1/1	1/1	Reserved
00 0010b	n/a	1/2	1/2	Reserved
00 0011b	n/a	1/3	Reserved	Reserved
00 0100b	n/a	1/4	1/4	Reserved
00 0101b	n/a	1/5	Reserved	Reserved
00 0110b	n/a	1/6	Reserved	Reserved
00 0111b	n/a	1/7	Reserved	Reserved
00 1000b	n/a	1/8	1/8	Reserved
00 1001b	n/a	1/9	Reserved	Reserved
00 1010b	n/a	1/10	Reserved	Reserved
00 1011b	n/a	1/11	Reserved	Reserved
00 1100b	n/a	1/12	Reserved	Reserved
00 1101b	n/a	1/13	Reserved	Reserved
00 1110b	n/a	1/14	Reserved	Reserved
00 1111b	n/a	1/15	Reserved	Reserved
01 0000b	n/a	1/16	1/16	Reserved
01 0001b	n/a	1/17	Reserved	Reserved
01 0010b	n/a	1/18	Reserved	Reserved
01 0011b	n/a	1/19	Reserved	Reserved
01 0100b	n/a	1/20	Reserved	Reserved
01 0101b	n/a	1/21	Reserved	Reserved
01 0110b	n/a	1/22	Reserved	Reserved
01 0111b	n/a	1/23	Reserved	Reserved
01 1000b	n/a	1/24	Reserved	Reserved
01 1001b	n/a	1/25	Reserved	Reserved
01 1010b	n/a	1/26	Reserved	Reserved
01 1011b	n/a	1/27	Reserved	Reserved
01 1100b	n/a	1/28	Reserved	Reserved
01 1101b	n/a	1/29	Reserved	Reserved
01 1110b	n/a	1/30	Reserved	Reserved
01 1111b	n/a	1/31	Reserved	Reserved
10 0000b	n/a	1/32	1/32	Reserved
10 0001b - 11 1111b	Reserved	Reserved	Reserved	Reserved

REG[094Eh] View Resizer Operation Setting Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a				Reserved		View Resizer Scaling Mode bits 1-0	

bits 3-2 Reserved
The default value for these bits is 0.

bits 1-0 View Resizer Scaling Mode bits[1:0]
These bits determine the view resizer scaling mode. Not all scaling modes are available for all scaling rates. Before selecting a scaling mode, set the View Resizer Vertical Scaling Rate bits (REG[094Eh] bits 13-8) and/or the View Resizer Horizontal Scaling Rate bits (REG[094Ch] bits 5-0) to a valid scaling rate. Enabling a scaling mode with an unsupported scaling rate (reserved or n/a) may turn off the view resizer.

Table 10-44: View Resizer Scaling Mode Selection

REG[094Eh] bits 1-0	View Resizer Scaling Mode
00b	no resizer scaling
01b	V/H Reduction
10b	V: Reduction, H: Average
11b	Reserved

REG[0960h] Capture Resizer Control Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Capture Resizer Software Reset (WO)	n/a				Capture Resizer Independent Horizontal/Vertical Scaling Enable	Capture Resizer Register Update VSYNC Enable	Capture Resizer Enable

bit 7 Capture Resizer Software Reset (Write Only)
When a 0 is written to this bit, there is no hardware effect.
When the resizers are activated by writing a 1 to REG[940h] bit 0 or REG[0960h] bit 0 and a 1 is written to this bit, the capture resizer logic is reset.

bit 2 Capture Resizer Independent Horizontal/Vertical Scaling Enable
When this bit = 0, the horizontal and vertical scaling rates are the same. Both horizontal and vertical scaling rates are controlled by REG[096Ch] bits 4-0.
When this bit = 1, the horizontal and vertical scaling rates can be selected independently. Horizontal scaling rate is controlled by REG[096Ch] bits 4-0 and vertical scaling rate is controlled by REG[096Ch] bits 12-8.

bit 1 Capture Resizer Register Update VSYNC Enable
When this bit = 0, the Capture Resizer use the new register value immediately.
When this bit = 1, the Capture Resizer uses the previous register value until the next camera VSYNC occurs.

bit 0 Capture Resizer Enable
This bit controls the capture resizer logic.
When this bit = 0, the capture resizer logic is disabled.
When this bit = 1, the capture resizer logic is enabled.

Note
When this bit and the View Resizer Enable bit (REG[0940h] bit 0) are both set to 0, the clock to the resizer block is automatically stopped.

REG[0964h] Capture Resizer Start X Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a					Reserved	Capture Resizer Start X Position bits 9-0	
7	6	5	4	3	2	1	0
Capture Resizer Start X Position bits 7-0							

bit 10 Reserved
The default value for this bit is 0.

bits 9-0 Capture Resizer Start X Position bits [9:0]
These bits determine the X start position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 337.

The following image size limitations must be observed when the JPEG functions (or JPEG Bypass) are used.

Table 10-45: Capture Resizer Limitations

YUV Format	Minimum Horizontal Resolution	Minimum Vertical Resolution	Minimum Size
YUV 4:4:4	multiples of 1 pixel	multiples of 1 line	8 pixels/8 lines
YUV 4:2:2	multiples of 2 pixels	multiples of 1 line	16 pixels/8 lines
YUV 4:2:0	multiples of 2 pixels	multiples of 2 lines	16 pixels/16 lines
YUV 4:1:1	multiples of 4 pixels	multiples of 1 line	32 pixels/8 lines

REG[0966h] Capture Resizer Start Y Position Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a					Reserved	Capture Resizer Start Y Position bits 9-8	
Capture Resizer Start Y Position bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved
The default value for this bit is 0.

bits 9-0 Capture Resizer Start Y Position bits [9:0]
These bits determine the Y start position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 337.

REG[0968h] Capture Resizer End X Position Register
Default = 027Fh — Read/Write

15	14	13	12	11	10	9	8
n/a					Reserved	Capture Resizer End X Position bits 9-8	
Capture Resizer End X Position bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved
The default value for this bit is 0.

bits 9-0 Capture Resizer End X Position bits [9:0]
These bits determine the X End position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 337.

REG[096Ah] Capture Resizer End Y Position Register
Default = 01DFh — Read/Write

15	14	13	12	11	10	9	8
n/a					Reserved	Capture Resizer End Y Position bits 9-8	
Capture Resizer End Y Position bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved
The default value for this bit is 0.

bits 9-0 Capture Resizer End Y Position bits [9:0]
These bits determine the Y end position for the Capture Resizer. These bits must be programmed according to the restrictions in Section 17.3, “Resizer Restrictions” on page 337.

REG[096Ch] Capture Resizer Operation Setting Register 0
Default = 0101h Read/Write

n/a		Capture Resizer Vertical Scaling Rate bits 5-0					
15	14	13	12	11	10	9	8
n/a		Capture Resizer Horizontal Scaling Rate bits 5-0					
7	6	5	4	3	2	1	0

bits 13-8 Capture Resizer Vertical Scaling Rate bits [5:0]
These bits determine the capture resizer vertical scaling rate when independent horizontal/vertical scaling is enabled (REG[0960h] bit 2 = 1). Not all scaling rates are available for all scaling modes (see REG[096Eh] bits 1-0). For a summary of the available scaling rate/mode options, see Table 10-46: “Capture Resizer Vertical Scaling Rate Selection,” on page 206.

Table 10-46: Capture Resizer Vertical Scaling Rate Selection

REG[096Ch] bits 13-8	Capture Resizer Vertical Scaling Rate			
	REG[096Eh] bits 1-0 = 00	REG[096Eh] bits 1-0 = 01	REG[096Eh] bits 1-0 = 10	REG[096Eh] bits 1-0 = 11
00 0000b	Reserved	Reserved	Reserved	Reserved
00 0001b	n/a	1/1	1/1	Reserved
00 0010b	n/a	1/2	1/2	Reserved
00 0011b	n/a	1/3	1/3	Reserved
00 0100b	n/a	1/4	1/4	Reserved
00 0101b	n/a	1/5	1/5	Reserved
00 0110b	n/a	1/6	1/6	Reserved
00 0111b	n/a	1/7	1/7	Reserved
00 1000b	n/a	1/8	1/8	Reserved
00 1001b	n/a	1/9	1/9	Reserved
00 1010b	n/a	1/10	1/10	Reserved
00 1011b	n/a	1/11	1/11	Reserved
00 1100b	n/a	1/12	1/12	Reserved
00 1101b	n/a	1/13	1/13	Reserved
00 1110b	n/a	1/14	1/14	Reserved
00 1111b	n/a	1/15	1/15	Reserved
01 0000b	n/a	1/16	1/16	Reserved
01 0001b	n/a	1/17	1/17	Reserved
01 0010b	n/a	1/18	1/18	Reserved
01 0011b	n/a	1/19	1/19	Reserved
01 0100b	n/a	1/20	1/20	Reserved
01 0101b	n/a	1/21	1/21	Reserved
01 0110b	n/a	1/22	1/22	Reserved
01 0111b	n/a	1/23	1/23	Reserved
01 1000b	n/a	1/24	1/24	Reserved
01 1001b	n/a	1/25	1/25	Reserved
01 1010b	n/a	1/26	1/26	Reserved
01 1011b	n/a	1/27	1/27	Reserved
01 1100b	n/a	1/28	1/28	Reserved
01 1101b	n/a	1/29	1/29	Reserved
01 1110b	n/a	1/30	1/30	Reserved
01 1111b	n/a	1/31	1/31	Reserved
10 0000b	n/a	1/32	1/32	Reserved
10 0001b - 11 1111b	Reserved	Reserved	Reserved	Reserved

bits 5-0 Capture Resizer Horizontal Scaling Rate bits [5:0]

When independent horizontal/vertical scaling is disabled (REG[0960h] bit 2 = 0), these bits determine the vertical and horizontal scaling rate. When independent horizontal/vertical scaling is enabled (REG[0960h] bit 2 = 1), these bits only determine the horizontal scaling rate. Not all scaling rates are available for all scaling modes (see REG[096Eh] bits 1-0). For a summary of the available scaling rate/mode options, see Table 10-47: “Capture Resizer Horizontal Scaling Rate Selection,” on page 207.

Table 10-47: Capture Resizer Horizontal Scaling Rate Selection

REG[096Ch] bits 5-0	Capture Resizer Horizontal Scaling Rate			
	REG[096Eh] bits 1-0 = 00	REG[096Eh] bits 1-0 = 01	REG[096Eh] bits 1-0 = 10	REG[096Eh] bits 1-0 = 11
00 0000b	Reserved	Reserved	Reserved	Reserved
00 0001b	n/a	1/1	1/1	Reserved
00 0010b	n/a	1/2	1/2	Reserved
00 0011b	n/a	1/3	Reserved	Reserved
00 0100b	n/a	1/4	1/4	Reserved
00 0101b	n/a	1/5	Reserved	Reserved
00 0110b	n/a	1/6	Reserved	Reserved
00 0111b	n/a	1/7	Reserved	Reserved
00 1000b	n/a	1/8	1/8	Reserved
00 1001b	n/a	1/9	Reserved	Reserved
00 1010b	n/a	1/10	Reserved	Reserved
00 1011b	n/a	1/11	Reserved	Reserved
00 1100b	n/a	1/12	Reserved	Reserved
00 1101b	n/a	1/13	Reserved	Reserved
00 1110b	n/a	1/14	Reserved	Reserved
00 1111b	n/a	1/15	Reserved	Reserved
01 0000b	n/a	1/16	1/16	Reserved
01 0001b	n/a	1/17	Reserved	Reserved
01 0010b	n/a	1/18	Reserved	Reserved
01 0011b	n/a	1/19	Reserved	Reserved
01 0100b	n/a	1/20	Reserved	Reserved
01 0101b	n/a	1/21	Reserved	Reserved
01 0110b	n/a	1/22	Reserved	Reserved
01 0111b	n/a	1/23	Reserved	Reserved
01 1000b	n/a	1/24	Reserved	Reserved
01 1001b	n/a	1/25	Reserved	Reserved
01 1010b	n/a	1/26	Reserved	Reserved
01 1011b	n/a	1/27	Reserved	Reserved
01 1100b	n/a	1/28	Reserved	Reserved
01 1101b	n/a	1/29	Reserved	Reserved
01 1110b	n/a	1/30	Reserved	Reserved
01 1111b	n/a	1/31	Reserved	Reserved
10 0000b	n/a	1/32	1/32	Reserved
10 0001b - 11 1111b	Reserved	Reserved	Reserved	Reserved

REG[096Eh] Capture Resizer Operation Setting Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				Reserved		Capture Resizer Scaling Mode bits 1-0	
7	6	5	4	3	2	1	0

bits 3-2 Reserved
The default value for these bits is 0.

bit 1-0 Capture Resizer Scaling Mode bits[1:0]
These bits determine the capture resizer scaling mode. Not all scaling rates are available for all scaling modes. Before selecting a scaling mode, set the Capture Resizer Vertical Scaling Rate bits (REG[096Eh] bits 13-8) and/or the Capture Resizer Horizontal Scaling Rate bits (REG[096Ch] bits 5-0) to a valid scaling rate. Enabling a scaling mode with an unsupported scaling rate (reserved or n/a) may turn off the capture resizer.

Table 10-48: Capture Resizer Scaling Mode Selection

REG[096Eh] bits 1-0	Capture Resizer Scaling Mode
00b	no resizer scaling
01b	V/H Reduction
10b	V: Reduction, H: Average
11b	Reserved

10.4.14 JPEG Module Registers

REG[0980h] JPEG Control Register
Default = 0000h — Read/Write

Reserved				n/a			JPEG 180° Rotation Enable
15	14	13	12	11	10	9	8
JPEG Module SW Reset (WO)	Reserved		YUV Data No Offset Select	JPEG Data Control bits 2-0			JPEG Module Enable
7	6	5	4	3	2	1	0

bits 15-12 Reserved
The default value for these bits is 0.

bit 8 JPEG 180° Rotation Enable
This bit is only for camera data encode. This bit selects the rotation mode for JPEG encoded data. For an overview diagram, see Section 18.4, "JPEG 180° Rotate Encode Diagram" on page 344.
When this bit = 0, the JPEG encoded data is normal.
When this bit = 1, the JPEG encoded data is rotated 180°.

Note
The dimensions of the image must be in MCU size multiples.

bit 7 JPEG Module Software Reset (Write Only)
This bit initiates a software reset of the internal JPEG module circuit. The JPEG module should be reset using this bit before each JPEG encode operation.

This bit resets only the internal JPEG module circuit and has no effect on the JPEG codec registers (REG[1000h]-[17A2h], the JPEG codec or the JPEG module registers (REG[0980h]-[09E0h]), except as follows.

REG[0984] is reset except for bits 14, 5, and 1.
REG[09B4] is reset
REG[09B6] is reset
REG[09AC] is reset
REG[09AA] is reset
REG[09A8] is reset
REG[09A2] is reset

To reset the JPEG codec, set the JPEG Codec Software Reset bit (REG[1002h] bit 7) to 1.
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the JPEG module is reset.

bit 6 Reserved
The default value for this bit is 0.

bit 5 Reserved
The default value for this bit is 0.

bit 4 YUV Data No Offset Select

This bit specifies whether an offset is applied to the U and V data when in YUV Capture, YUV Display, Host Encode, and Host Decode modes, REG[0980h] bits [3:1] = 001b, 011b, 100b, 101b, or 111b. This bit is used in conjunction with REG[0110h] bit 8 to select the desired YUV output capture range for YUV Capture mode.

When this bit = 0, an offset is applied to the U and V data (MSB is inverted).
When this bit = 1, no offset is applied to the U and V data is not modified.

The YUV data range depends on the interface data range and the YUV Data No Offset Select bit. For Host Decode mode, this bit must be set to 1.

Table 10-49: YUV Output Range Selection (REG[0980h] bits 3-1 = 011b or 111b)

Camera Interface Input YUV Data	REG[0110h] bit 8	REG[0980h] bit 4	YUV Output Data Range
Straight Data	0	0	0 =< Y =< 255 -128 =< U =< 127 -128 =< V =< 127 or 16 =< Y =< 235 -112 =< Cb=< 112 -112 =< Cr=< 112
		1	0 =< Y =< 255 0 =< U =< 255 0 =< V =< 255 or 16 =< Y =< 235 16 =< Cb=< 240 16 =< Cr =< 240
	1	0	0 =< Y =< 255 0 =< U =< 255 0 =< V =< 255 or 16 =< Y =< 235 16 =< Cb =< 240 16 =< Cr =< 240
		1	0 =< Y =< 255 -128 =< U =< 127 -128 =< V =< 127 or 16 =< Y =< 235 -112 =< Cb =< 112 -112 =< Cr =< 112

Table 10-49: YUV Output Range Selection (REG[0980h] bits 3-1 = 011b or 111b) (Continued)

Camera Interface Input YUV Data	REG[0110h] bit 8	REG[0980h] bit 4	YUV Output Data Range
Offset Data	0	0	0 =< Y =< 255 0 =< U =< 255 0 =< V =< 255 or 16 =< Y =< 235 16 =< Cb =< 240 16 =< Cr =< 240
		1	0 =< Y =< 255 -128 =< U =< 127 -128 =< V =< 127 or 16 =< Y =< 235 -112 =< Cb =< 112 -112 =< Cr =< 112
	1	0	0 =< Y =< 255 -128 =< U =< 127 -128 =< V =< 127 or 16 =< Y =< 235 -112 =< Cb=< 112 -112 =< Cr=< 112
		1	0 =< Y =< 255 0 =< U =< 255 0 =< V =< 255 or 16 =< Y =< 235 16 =< Cb=< 240 16 =< Cr =< 240

Table 10-50: YUV Input Range Selection (REG[0980h] bits 3-1 = 001b, 100b or 101b)

Host Interface Input YUV Data	REG[0980h] bit 4	YUV Input Data Range
Straight Data	0	$0 \leq Y \leq 255$ $-128 \leq U \leq 127$ $-128 \leq V \leq 127$ or $16 \leq Y \leq 235$ $-112 \leq Cb \leq 112$ $-112 \leq Cr \leq 112$
	1	$0 \leq Y \leq 255$ $0 \leq U \leq 255$ $0 \leq V \leq 255$ or $16 \leq Y \leq 235$ $16 \leq Cb \leq 240$ $16 \leq Cr \leq 240$
Offset Data	0	$0 \leq Y \leq 255$ $0 \leq U \leq 255$ $0 \leq V \leq 255$ or $16 \leq Y \leq 235$ $16 \leq Cb \leq 240$ $16 \leq Cr \leq 240$
	1	$0 \leq Y \leq 255$ $-128 \leq U \leq 127$ $-128 \leq V \leq 127$ or $16 \leq Y \leq 235$ $-112 \leq Cb \leq 112$ $-112 \leq Cr \leq 112$

bits 3-1 JPEG Data Control bits [2:0]

Table 10-51: JPEG Data Mode Selection

REG[0980h] bits 3-1	JPEG Data Mode	Description
000b	JPEG Encode/Decode	In this mode the encode data paths are: • **Camera Interface** => Capture Resizer => JPEG Line Buffer => Codec Core => JPEG FIFO => Host Interface • **Display Buffer** => Capture Resizer => JPEG Line Buffer => Codec Core => JPEG FIFO => Host Interface • **Host Interface** => Capture Resizer => JPEG Line Buffer => Codec Core => JPEG FIFO => Host Interface In this mode the decode data path is: • **Host Interface** => JPEG FIFO => Codec Core => JPEG Line Buffer => View Resizer => Display Buffer
001b	YUV Data Input from Host (YUV 4:2:2)	The data by-passes the JPEG Module.
010b	Reserved	
011b	YUV Data Output to Host (YUV 4:2:2)	The data by-passes the JPEG Module.
100b	Host Input/Output JPEG Encode/Decode (YUV 4:2:0 or YUV 4:2:2)	In this mode the encode data path is: • **Host Interface** => JPEG Line Buffer => Capture Resizer => Codec Core => JPEG FIFO => Host Interface In this mode the decode data path is: • **Host Interface** => JPEG FIFO => Codec Core => JPEG Line Buffer => View Resizer => Host Interface
101b	YUV Data Input from Host (YUV 4:2:0)	The data by-passes the JPEG Module.
110b	Reserved	
111b	YUV Data Output to Host (YUV 4:2:0)	The data by-passes the JPEG Module.

bit 0 JPEG Module Enable

This bit enables/disables the JPEG module and its associated registers. **If the JPEG module is disabled, REG[1000h] - REG[17A2h] must not be accessed.**

When this bit = 0, the JPEG module is disabled and the clock source is disabled.

When this bit = 1, the JPEG module is enabled and a clock source is supplied.

Note

The JPEG module must be disabled before the View Resizer Enable bit (REG[0940h] bit 0) or the Capture Resizer Enable bit (REG[0960h] bit 0) are disabled.

REG[0982h] JPEG Status Flag Register
Default = 8080h Read/Write

15	14	13	12	11	10	9	8
Reserved	JPEG Codec File Out Status (RO)	JPEG FIFO Threshold Status bits 1-0 (RO)		Encode Size Limit Violation Flag	JPEG FIFO Threshold Trigger Flag	JPEG FIFO Full Flag	JPEG FIFO Empty Flag
7	6	5	4	3	2	1	0
Reserved		JPEG Decode Complete Flag	Decode Marker Read Flag	Reserved	JPEG Line Buffer Overflow Flag (RO)	JPEG Codec Interrupt Flag (RO)	JPEG Line Buffer Interrupt Flag (RO)

bit 15 Reserved
The default value for this bit is 1.

bit 14 JPEG Codec File Out Status (Read Only)
This bit indicates the status of the JPEG Codec output.
When this bit = 0, the JPEG Codec is not outputing encoded data.
When this bit = 1, the JPEG Codec is encoding or outputing encoded data.

bits 13-12 JPEG FIFO Threshold Status bits [1:0] (Read Only)
These bits indicate how much data is currently in the JPEG FIFO. See the JPEG FIFO Size register (REG[09A4h]) for information on setting the JPEG FIFO size.

Table 10-52: JPEG FIFO Threshold Status

REG[0982h] bits 13-12	JPEG FIFO Threshold Status
00b	no data (same as empty
01b	more than 4 bytes of data exist
10b	more than 1/4 of specified FIFO size data exists
11b	more than 1/2 of specified FIFO size data exists

bit 11 Encode Size Limit Violation Flag

This flag is asserted when the JPEG compressed data size is over the encode size limit as specified in the Encode Size Limit registers (REG[09B0h], REG[09B2h]). This flag is masked by the JPEG Encode Size Limit Violation Interrupt Enable bit and is only available when REG[0986h] bit 11 = 1.

For Reads:
When this bit = 0, no violation has occurred.
When this bit = 1, an encode size limit violation has occurred.

For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the Encode Size Limit Violation Flag is cleared.

Note
The Encode Size Limit Violation Flag can only be cleared when an Encode Size Limit Violation no longer exists. This can be done by setting the Encode Size Limit to a value greater then the Encode Size Result (REG[09B0h] - REG[09B2h] > REG[09B4h] - REG[09B6h]), or by resetting the JPEG Module (REG[0980h] bit 7 = 1).

Note
For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 347.

bit 10 JPEG FIFO Threshold Trigger Flag

This flag is asserted when the amount of data in the JPEG FIFO meets the condition specified by the JPEG FIFO Trigger Threshold bits (REG[09A0h] bits 5-4). This flag is masked by the JPEG FIFO Threshold Trigger Interrupt Enable bit and is only available when REG[0986h] bit 10 = 1.

For Reads:
When this bit = 0, the amount of data in the JPEG FIFO is less than the JPEG FIFO Trigger Threshold.
When this bit = 1, the amount of data in the JPEG FIFO has reached the JPEG FIFO Trigger Threshold.

For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the FIFO Threshold Trigger Flag is cleared.

Note
The JPEG FIFO Threshold Trigger Flag can only be cleared when a JPEG FIFO Threshold Trigger Flag condition no longer exists. This can be done by increasing the JPEG FIFO Threshold (REG[09A0h] bits 5-4), emptying the JPEG FIFO until it drops below the specified threshold, or by resetting the JPEG Module (REG[0980h] bit 7 = 1).

Note
For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 347.

bit 9 JPEG FIFO Full Flag

This flag is asserted when the JPEG FIFO is full. This flag is masked by the JPEG FIFO Full Interrupt Enable bit and is only available when REG[0986h] bit 9 = 1.

For Reads:
When this bit = 0, the JPEG FIFO is not full.
When this bit = 1, the JPEG FIFO is full.

For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the JPEG FIFO Full Flag is cleared.

Note
The JPEG FIFO Full Flag can only be cleared when the JPEG FIFO is no longer full, or after a JPEG Module Software Reset (REG[0980h] bit 7 = 1).

Note
For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 347.

bit 8 JPEG FIFO Empty Flag

This flag is asserted when the JPEG FIFO is empty. This flag is masked by the JPEG FIFO Empty Interrupt Enable bit and is only available when REG[0986h] bit 8 = 1.

For Reads:
When this bit = 0, the JPEG FIFO is not empty.
When this bit = 1, the JPEG FIFO is empty.

For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the JPEG FIFO Empty Flag is cleared.

Note
The JPEG FIFO Empty Flag can only be cleared when the JPEG FIFO is no longer empty, or after a JPEG Module Software Reset (REG[0980h] bit 7 = 1).

Note
For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 347.

bit 7 Reserved

The default value for this bit is 1.

bit 6 Reserved

The default value for this bit is 0.

bit 5 JPEG Decode Complete Flag

This flag is asserted when the JPEG decode operation is finished. This flag is masked by the JPEG Decode Complete Interrupt Enable bit and is only available when REG[0986h] bit 5 = 1.

For Reads:
When this bit = 0, the JPEG decode operation is not finished yet.
When this bit = 1, the JPEG decode operation is finished.

For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, this bit is cleared.

Note
When error detection is enabled (REG[101Ch] bits 1-0 = 01b) and an error is detected while decoding a JPEG image, this status bit is not set at the end of the decode process.

Note
For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 347.

bit 4 Decode Marker Read Flag

This flag is asserted during the JPEG decoding process when decoded marker information is read from the JPEG file. This flag is masked by the JPEG Decode Marker Read Interrupt Enable bit and is only available when REG[0986h] bit 4 = 1.
When this bit = 0, a JPEG decode marker has not been read.
When this bit = 1, a JPEG decode marker has been read.

To clear this flag, disable the Decode Marker Read Interrupt Enable bit (REG[0986h] bit 4 = 0).

Note
For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 347.

bit 3 Reserved

The default value for this bit is 0.

bit 2 JPEG Line Buffer Overflow Flag (Read Only)

This flag is asserted when a JPEG Line Buffer overflow occurs. This flag is masked by the JPEG Line Buffer Overflow Interrupt Enable bit and is only available when REG[0986h] bit 2 = 1.
When this bit = 0, a JPEG Line Buffer overflow has not occurred.
When this bit = 1, a JPEG Line Buffer overflow has occurred.

To clear this flag, perform a JPEG Software Reset (REG[0980h] bit 7 = 1).

Note
For further information on the use of this bit, see Section 19.1.2, “JPEG Codec Interrupts” on page 347.

bit 1

JPEG Codec Interrupt Flag (Read Only)
This flag is asserted when the JPEG codec generates an interrupt. This flag is masked by the JPEG Codec Interrupt Enable bit and is only available when REG[0986h] bit 1 = 1).
When this bit = 0, the JPEG codec has not generated an interrupt.
When this bit = 1, the JPEG codec has generated an interrupt.

To clear this flag, read the JPEG Operation Status bit (REG[1004h] bit 0).

Note
For further information on the use of this bit, see Section 19.1.2, "JPEG Codec Interrupts" on page 347.

bit 0

JPEG Line Buffer Interrupt Flag (Read Only)
This bit is valid only when YUV Capture/Display or Host Decode/Encode mode is selected (REG[0980h] bits 3-1 ≠ 000b). This bit is set when a JPEG Line Buffer Interrupt occurs in REG[09C0h] and is used for YUV data transfers or Host Decode/Encode operations with interrupt handling. This flag is masked by the JPEG Line Buffer Interrupt Enable bit and is only available when REG[0986h] bit 0 = 1). This bit is cleared when all JPEG Line Buffer Interrupt requests are cleared in REG[09C0h].
When this bit = 0, the JPEG Line Buffer has not generated an interrupt.
When this bit = 1, the JPEG Line Buffer has generated an interrupt.

REG[0984h] JPEG Raw Status Flag Register
Default = 8180h — Read Only

Reserved	JPEG Codec File Out Status	JPEG FIFO Threshold Status bits 1-0		Raw Encode Size Limit Violation Flag	Raw JPEG FIFO Threshold Trigger Flag	Raw JPEG FIFO Full Flag	Raw JPEG FIFO Empty Flag
15	14	13	12	11	10	9	8
Reserved		Raw JPEG Decode Complete Flag	Raw JPEG Decode Marker Read Flag	Reserved	Raw JPEG Line Buffer Overflow Flag	Raw JPEG Codec Interrupt Flag	Raw JPEG Line Buffer Interrupt Flag
7	6	5	4	3	2	1	0

bit 15

Reserved
The default value for this bit is 1.

bit 14

JPEG Codec File Out Status (Read Only)
This bit provides the status of the JPEG Codec output.
When this bit = 0, the JPEG Codec is not outputing encoded data.
When this bit = 1, the JPEG Codec is encoding or outputing encoded data.

Note
This bit has the same functionality as REG[0982h] bit 14.

bits 13-12 JPEG FIFO Threshold Status bits [1:0] (Read Only)
These bits indicate how much data is currently in the JPEG FIFO. See the JPEG FIFO Size Register (REG[09A4h) for information on setting the JPEG FIFO Size.

Table 10-53: JPEG FIFO Threshold Status

REG[0984h] bits 13-12	JPEG FIFO Threshold Status
00b	no data (same as empty
01b	more than 4 bytes of data exist
10b	more than 1/4 of specified FIFO size data exists
11b	more than 1/2 of specified FIFO size data exists

Note
These bits have the same functionality as REG[0982h] bits 13-12.

bit 11 Raw Encode Size Limit Violation Flag (Read Only)
This flag is asserted when the JPEG encoded data size is over the size limit as specified in the Encode Size Limit registers (REG[09B02h] - REG[09B2h]). This flag is not affected by the JPEG Encode Size Limit Violation Interrupt Enable bit (REG[0986h] bit 11).
When this bit = 0, no violation has occurred.
When this bit = 1, an encode size limit violation has occurred.

To clear this flag, write a 1 to the Encode Size Limit Violation Flag, REG[0982h] bit 11, when an Encode Size Limit Violation condition no longer exists. (i.e. Set the Encode Size Limit, REG[09B0h] and REG[09B2h] > Encode Size Result, REG[09B4h] and REG[09B6h], or reset the JPEG Module, REG[0980h] bit 7 = 1.)

bit 10 Raw JPEG FIFO Threshold Trigger Flag (Read Only)
This flag is asserted when the amount of data in the JPEG FIFO meets the condition specified by the JPEG FIFO Trigger Threshold bits (REG[09A0] bits 5-4). This flag is not affected by the JPEG FIFO Threshold Trigger Interrupt Enable bit (REG[0986h] bit 10).
When this bit = 0, the amount of data in the JPEG FIFO is less than the JPEG FIFO Trigger Threshold.
When this bit = 1, the amount of data in the JPEG FIFO has reached the JPEG FIFO Trigger Threshold.

To clear this flag, write a 1 to the JPEG FIFO Threshold Trigger Flag, REG[0982] bit 10, when a JPEG FIFO Threshold Trigger condition no longer exists. (i.e. Set the JPEG FIFO Threshold in REG[09A0] bits [5:4] greater, empty the JPEG FIFO until it's level is below the specified threshold, or reset the JPEG Module, REG[0980] bit 7 = 1.)

bit 9 Raw JPEG FIFO Full Flag (Read Only)
This flag is asserted when the JPEG FIFO is full. This flag is not affected by the JPEG FIFO Full Interrupt Enable bit (REG[0986h] bit 9).
When this bit = 0, the JPEG FIFO is not full.
When this bit = 1, the JPEG FIFO is full.

To clear this flag, write a 1 to the JPEG FIFO Full Flag, REG[0982h] bit 9, when the JPEG FIFO is no longer full or after a JPEG Module reset, REG[0980h] bit 7 = 1.

bit 8 Raw JPEG FIFO Empty Flag (Read Only)
This flag is asserted when the JPEG FIFO is empty. This flag is not affected by the JPEG FIFO Empty Interrupt Enable bit (REG[0986h] bit 8).
When this bit = 0, the JPEG FIFO is not empty.
When this bit = 1, the JPEG FIFO is empty.

To clear this flag, write a 1 to the JPEG FIFO Empty Flag, REG[0982h] bit 8, when the JPEG FIFO is no longer empty or after a JPEG Module reset, REG[0980h] bit 7 = 1.

Note
This bit is not affected by the JPEG FIFO Clear bit (REG[09A0h] bit 2).

bit 7 Reserved
The default value for this bit is 1.

bit 6 Reserved
The default value for this bit is 0.

bit 5 Raw JPEG Decode Complete Flag (Read Only)
This flag is asserted when the JPEG decode operation is finished. This flag is not affected by the JPEG Decode Complete Interrupt Enable bit (REG[0986h] bit 5).
When this bit = 0, the JPEG decode operation is not finished yet.
When this bit = 1, the JPEG decode operation is finished.

To clear this flag, write a 1 to the JPEG Decode Complete Flag (REG[0982h] bit 5 = 1).

Note
When error detection is enabled (REG[101Ch] bits 1-0 = 01) and an error is detected while decoding a JPEG image, this status bit is not set at the end of the decode process.

bit 4 Raw JPEG Decode Marker Read Flag (Read Only)
This flag is asserted during the JPEG decoding process when decoded marker information is read from the JPEG file and when REG[0986h] bit 4 = 1.
When this bit = 0, a JPEG decode marker has not been read.
When this bit = 1, a JPEG decode marker has been read.

To clear this flag, disable the JPEG Decode Marker Read Interrupt Enable bit (REG[0986h] bit 4 = 0).

bit 3 Reserved
The default value for this bit is 0.

bit 2 Raw JPEG Line Buffer Overflow Flag (Read Only)
This flag is asserted when a JPEG Line Buffer overflow occurs. This flag is not affected by the JPEG Line Buffer Overflow Interrupt Enable (REG[0986h] bit 2).
When this bit = 0, a JPEG Line Buffer overflow has not occurred.
When this bit = 1, a JPEG Line Buffer overflow has occurred.

To clear this flag, perform a JPEG module software reset (REG[0980h] bit 7 = 1).

bit 1 Raw JPEG Codec Interrupt Flag (Read Only)
This flag is asserted when an interrupt is generated by the JPEG codec. This flag is not affected by the JPEG Codec Interrupt Enable bit (REG[0986h] bit 1).
When this bit = 0, no interrupt has been generated.
When this bit = 1, the JPEG codec has generated an interrupt.

To clear this flag, read the JPEG Operation Status bit (REG[1004h] bit 0).

bit 0 Raw JPEG Line Buffer Interrupt Flag
This bit is valid only when YUV Capture/Display mode is selected (REG[0980h] bits 3-1 ≠ 000). This flag is not affected by the JPEG Line Buffer Interrupt Enable bit (REG[0986h] bit 0). This bit is set when a JPEG Line Buffer Interrupt occurs in REG[09C0h] and is cleared when all JPEG Line Buffer Interrupt requests are cleared in REG[09C0h].
When this bit = 0, the JPEG Line Buffer has not generated an interrupt.
When this bit = 1, the JPEG Line Buffer has generated an interrupt.

REG[0986h] JPEG Interrupt Control Register
Default = 0000h Read/Write

Reserved				Encode Size Limit Violation Interrupt Enable	JPEG FIFO Threshold Trigger Interrupt Enable	JPEG FIFO Full Interrupt Enable	JPEG FIFO Empty Interrupt Enable
15	14	13	12	11	10	9	8
Reserved		JPEG Decode Complete Interrupt Enable	Decode Marker Read Interrupt Enable	Reserved	JPEG Line Buffer Overflow Interrupt Enable	JPEG Codec Interrupt Enable	JPEG Line Buffer Interrupt Enable
7	6	5	4	3	2	1	0

bits 15-12 Reserved
The default value for these bits is 0.

bit 11 Encode Size Limit Violation Interrupt Enable
This bit controls the encode size limit violation interrupt. The status of this interrupt can be determined using the Encode Size Limit Violation Flag bit (REG[0982h] bit 11).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 10 JPEG FIFO Threshold Trigger Interrupt Enable
This bit controls the JPEG FIFO threshold trigger interrupt. The status of this interrupt can be determined using the JPEG FIFO Threshold Trigger Flag bit (REG[0982h] bit 10).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 9 JPEG FIFO Full Interrupt Enable
This bit controls the JPEG FIFO full interrupt. The status of this interrupt can be determined using the JPEG FIFO Full Flag bit (REG[0982h] bit 9).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 8 JPEG FIFO Empty Interrupt Enable
This bit controls the JPEG FIFO empty interrupt. The status of this interrupt can be determined using the JPEG FIFO Empty Flag bit (REG[0982h] bit 8).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 7 Reserved
The default value for this bit is 0.

bit 6 Reserved
The default value for this bit is 0.

bit 5 JPEG Decode Complete Interrupt Enable
This bit controls the JPEG decode complete interrupt. The status of this interrupt can be determined using the JPEG Decode Complete Flag bit (REG[0982h] bit 5).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 4 JPEG Decode Marker Read Interrupt Enable
This bit controls the JPEG decode marker read interrupt. The status of this interrupt can be determined using the JPEG Decode Complete Flag (REG[0982h] bit 4).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 3 Reserved
The default value for this bit is 0.

bit 2 JPEG Line Buffer Overflow Interrupt Enable
This bit controls the JPEG line buffer overflow interrupt. The status of this interrupt can be determined using the Line Buffer Overflow Flag (REG[0982h] bit 2).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 1 JPEG Codec Interrupt Enable
This bit controls the JPEG codec interrupt. The status of this interrupt can be determined using the JPEG Codec Interrupt Flag (REG[0982h] bit 1).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 0 JPEG Line Buffer Interrupt Enable
This bit controls the JPEG Line Buffer Interrupt. The status of this interrupt can be determined using the JPEG Line Buffer Interrupt Flag (REG[0982h] bit 0).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.
This bit should be disabled if YUV Data in not being input from host and then displayed (REG[0980h] bits 3-1 = 001b or 101b).

REG[0988h] is Reserved

This register is Reserved and should not be written.

REG[098Ah] JPEG Code Start/Stop Control Register
Default = 0000h — Write Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							JPEG Start/Stop Control

bit 0 JPEG Start/Stop Control (Write Only)
This bit controls the JPEG codec for both JPEG encode mode and YUV data capture (JPEG bypass) mode. This bit is not used for JPEG decoding.

For JPEG Encode:
When this bit is set to 0, the JPEG codec will be ready to capture from the next frame.
When this bit is set to 1, the JPEG codec starts capturing the next frame and then stops.

For YUV Data Capture (JPEG Bypass):
When this bit is set to 0, YUV data capturing stops at the end of the current frame.
When this bit is set to 1, YUV data capturing starts from the next frame.

REG[098Ch] through REG[098Eh] are Reserved

These registers are Reserved and should not be written.

10.4.15 JPEG FIFO Setting Register

REG[09A0h] JPEG FIFO Control Register
Default = 0000h — Read/Write

Reserved							
15	14	13	12	11	10	9	8
Reserved		JPEG FIFO Trigger Threshold bits 1-0		Reserved	JPEG FIFO Clear (WO)	JPEG FIFO Direction (RO)	n/a
7	6	5	4	3	2	1	0

bits 15-6 Reserved
The default value for these bits is 0.

bits 5-4 JPEG FIFO Trigger Threshold bits[1:0]
These bits set the JPEG FIFO Threshold Trigger Flag (REG[0982h] bit 10) when the specified conditions are met.

Table 10-54: JPEG FIFO Trigger Threshold Selection

REG[09A0h] bits 5-4	JPEG FIFO Trigger Threshold
00b	Never trigger
01b	Trigger when the JPEG FIFO contains 4 bytes of data or more
10b	Trigger when the JPEG FIFO contains more than 1/4 of the specified JPEG FIFO size (REG[09A4h] bits 3-0)
11b	Trigger when the JPEG FIFO contains more than 1/2 of the specified JPEG FIFO size (REG[09A4h] bits 3-0)

bit 3 Reserved
The default value for this bit is 0.

bit 2 JPEG FIFO Clear (Write Only)

This bit clears the JPEG FIFO. It is recommended that the JPEG module should also be reset (REG[0980h] bit 7 = 1) when the JPEG FIFO is cleared.
When this bit = 0, there is no hardware effect.
When this bit = 1, the JPEG FIFO, the JPEG FIFO Read/Write Pointer registers (REG[09AAh]-[09ACh]), and the JPEG FIFO Valid Data Size registers (REG[09A8h] are cleared.

The following sequence is used clear the JPEG FIFO.

1. Clear the JPEG FIFO, REG[09A0h] bit 2 = 1.
2. Reset the JPEG module, REG[0980h] bit 7 = 1.
3. Perform 2 dummy reads from REG[09A6h] to ensure that the JPEG FIFO is empty.

Note
Clearing the JPEG FIFO using this bit has no effect on the Raw JPEG FIFO Empty Flag (REG[0984h] bit 8).

Note
This bit only clears the JPEG FIFO and does not clear the JPEG Line Buffer. For details on using the JPEG FIFO, see Section 19.1.1, “JPEG FIFO” on page 346.

bit 1 JPEG FIFO Direction Bit (Read Only)

This bit indicates the configuration of the JPEG FIFO.
When this bit = 0, the JPEG FIFO is configured to receive (encode process).
When this bit = 1, the JPEG FIFO is configured to transmit (decode process).

REG[09A2h] JPEG FIFO Status Register
Default = 8001h — Read Only

Reserved	n/a						
15	14	13	12	11	10	9	8
Reserved				JPEG FIFO Threshold Status bits 1-0		JPEG FIFO Full Status	JPEG FIFO Empty Status
7	6	5	4	3	2	1	0

bit 15 Reserved

The default value for this bit is 0.

bits 3-2 JPEG FIFO Threshold Status bits [1:0] (Read Only)
These bits indicate how much data is currently in the JPEG FIFO. See the JPEG FIFO Size register (REG[09A4h]) for information on setting the JPEG FIFO size.

Table 10-55: JPEG FIFO Threshold Status

REG[09A2h] bits 3-2	JPEG FIFO Threshold Status
00b	no data (same as empty
01b	more than 4 bytes of data exist
10b	more than 1/4 of specified FIFO size data exists
11b	more than 1/2 of specified FIFO size data exists

Note
These bits have the same functionality as REG[0982h] bits 13-12.

bit 1 JPEG FIFO Full Status (Read Only)
This bit indicates whether the JPEG FIFO is full.
When this bit = 0, the JPEG FIFO is not full.
When this bit = 1, the JPEG FIFO is full.

bit 0 JPEG FIFO Empty Status (Read Only)
This bit indicates that the JPEG FIFO is empty.
When this bit = 0, the JPEG FIFO is not empty.
When this bit = 1, the JPEG FIFO is empty.

REG[09A4h] JPEG FIFO Size Register
Default = 0000h Read/Write

Reserved							
15	14	13	12	11	10	9	8
Reserved			JPEG FIFO Size bits 4-0				
7	6	5	4	3	2	1	0

bits 15-5 Reserved
The default value for these bits is 0.

bits 4-0 JPEG FIFO Size bits [4:0]
These bits determine the JPEG FIFO size in 4K byte units. The maximum size of the JPEG FIFO is 128K bytes. These bits also specify the amount of memory reserved for the JPEG FIFO.

JPEG FIFO size = (REG[09A4h] bits 4-0 + 1) x 4K bytes

Note
For further information on S1D13717 memory mapping, see Section 8, “Memory Allocation” on page 106.

REG[09A6h] JPEG FIFO Read/Write Port Register
Default = Not Applicable — Read/Write

JPEG FIFO Read/Write Port bits 15-8							
15	14	13	12	11	10	9	8
JPEG FIFO Read/Write Port bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 JPEG FIFO Read/Write Port bits[15:0]
These bits are the access port for the JPEG FIFO. The current address pointed to by the port can be determined using the JPEG FIFO Read Pointer register (REG[09AAh) and the JPEG FIFO Write Pointer register (REG[09ACh]).

When JPEG encoding is selected, these bits are used as the JPEG FIFO read data port. When JPEG decoding is selected, these bits are used as the JPEG FIFO write data port. When YUV data is output to the Host interface (REG[0980] bits 3-1 = 011b or 111b), these bits are used as the JPEG FIFO read data port.

Note
Since the JPEG FIFO is 32 bits wide and the Host CPU interface is 16 bits wide, this register must be accessed an even number of times.

REG[09A8h] JPEG FIFO Valid Data Size Register
Default = 0000h — Read Only

JPEG FIFO Valid Data Size bits 15-8							
15	14	13	12	11	10	9	8
JPEG FIFO Valid Data Size bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 JPEG FIFO Valid Data Size bits[15:0] (Read Only)
These bits indicate the valid data size in 32-bit units which can be read from the JPEG FIFO. If the JPEG file size is not aligned on 32-bit boundaries, the JPEG FIFO may contain more data (1 to 3 bytes) than the indicated size. See the Encode Size Result registers (REG[09B4h]-[09B6h]) to determine the correct data size.

REG[09AAh] JPEG FIFO Read Pointer Register
Default = 0000h — Read Only

JPEG FIFO Read Pointer bits 15-8							
15	14	13	12	11	10	9	8
JPEG FIFO Read Pointer bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 JPEG FIFO Read Pointer bits[15:0] (Read Only)
These bits are used during evaluation and are for reference only. These bits indicate the 32-bit read pointer into the JPEG FIFO. The read pointer is automatically incremented when either a read or write to/from the JPEG FIFO Read/Write Port register (REG[09A6h]) takes place. For details on the JPEG FIFO, see Section 19.1.1, “JPEG FIFO” on page 346.

REG[09ACh] JPEG FIFO Write Pointer Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
JPEG FIFO Write Pointer bits 15-8							
7	6	5	4	3	2	1	0
JPEG FIFO Write Pointer bits 7-0							

bits 15-0 JPEG FIFO Write Pointer bits[15:0] (Read Only)
These bits are used during evaluation and are for reference only. These bits indicate the 32-bit write pointer into the JPEG FIFO. The write pointer is automatically incremented when a write to the JPEG FIFO Read/Write Port register (REG[09A6h]) takes place. For details on the JPEG FIFO, see Section 19.1.1, “JPEG FIFO” on page 346.

REG[09B0h] Encode Size Limit Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Encode Size Limit bits 15-8							
7	6	5	4	3	2	1	0
Encode Size Limit bits 7-0							

REG[09B2h] Encode Size Limit Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Encode Size Limit bits 23-16							

REG[09B2h] bits 7-0
REG[09B0h] bits 15-0 Encode Size Limit bits[23:0]
These bits are required for the JPEG encode process only. These bits specify the data size limit, in bytes, for the encoded JPEG file.

Note
Setting these registers to 0 will disable the Encode Size Limit Violation function and REG[0984h] bit 11 will not be set.

REG[09B4h] Encode Size Result Register 0
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
Encode Size Result bits 15-8							
7	6	5	4	3	2	1	0
Encode Size Result bits 7-0							

REG[09B6h] Encode Size Result Register 1
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Encode Size Result bits 23-16							

REG[09B6h] bits 7-0
REG[09B4h] bits 15-0 Encode Size Result bits[23:0] (Read Only)
These bits are required for the JPEG encode process only. These bits indicate the data size result, in bytes, for the encoded JPEG file.

REG[09B8h] JPEG File Size Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
JPEG File Size bits 15-8							
7	6	5	4	3	2	1	0
JPEG File Size bits 7-0							

REG[09BAh] JPEG File Size Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
JPEG File Size bits 23-16							

REG[09BAh] bits 7-0
REG[09B8h] bits 15-0 JPEG File Size bits[23:0]
These bits are required for the JPEG decode process only. These bits specify the JPEG file size in bytes and must be set before the Host begins writing decoded data to the JPEG FIFO.

REG[09BCh] is Reserved

This register is Reserved and should not be written.

10.4.16 JPEG Line Buffer Setting Register

REG[09C0h] JPEG Line Buffer Status Flag Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a					JPEG Line Buffer Full Flag	JPEG Line Buffer Half Flag	JPEG Line Buffer Empty Flag
7	6	5	4	3	2	1	0

bit 2 JPEG Line Buffer Full Flag

This flag is asserted when the JPEG Line Buffer becomes full. This flag is masked by the JPEG Line Buffer Full Interrupt Enable bit and is only available when REG[09C6h] bit 2 = 1. This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1 ≠ 000b).
When this bit = 0, the JPEG Line Buffer is not full.
When this bit = 1, the JPEG Line Buffer is full.

To clear this flag, when the JPEG Line Buffer is not full, write a 1 to this bit.

bit 1 JPEG Line Buffer Half Full Flag

This flag is asserted when the JPEG Line Buffer has become half full. This flag is masked by the JPEG Line Buffer Half Full Interrupt Enable bit and is only available when REG[09C6h] bit 1 = 1. This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1 ≠ 000b).
When this bit = 0, the JPEG Line Buffer is not half full.
When this bit = 1, the JPEG Line Buffer is half full.

To clear this flag, when the JPEG Line Buffer is not half full, write a 1 to this bit.

bit 0 JPEG Line Buffer Empty Flag

This flag is asserted when the JPEG Line Buffer contains less than or equal to 16 bytes of YUV 4:2:2 data or 8 bytes of YUV 4:2:0 data. This flag is masked by the JPEG Line Buffer Empty Interrupt Enable bit and is only available when REG[09C6h] bit 0 = 1. This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1 ≠ 000b).
When this bit = 0, the JPEG Line Buffer is not empty.
When this bit = 1, the JPEG Line Buffer contains 16 bytes or less of YUV 4:2:2 data or 8 bytes or less of YUV 4:2:0 data.

To clear this flag, when the JPEG Line Buffer is not empty, write a 1 to this bit.

REG[09C2h] JPEG Line Buffer Raw Status Flag Register
Default = 0000h — Read Only

n/a							
15	14	13	12	11	10	9	8
n/a					Raw JPEG Line Buffer Full Flag	Raw JPEG Line Buffer Half Flag	Raw JPEG Line Buffer Empty Flag
7	6	5	4	3	2	1	0

bit 2 Raw JPEG Line Buffer Full Flag (Read Only)
This flag is asserted when the JPEG Line Buffer becomes full. This flag is not affected by the JPEG Line Buffer Full Interrupt Enable bit (REG[09C6h] bit 2). This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1 ≠ 000b).
When this bit = 0, the JPEG Line Buffer is not full.
When this bit = 1, the JPEG Line Buffer is full.

To clear this flag, when the JPEG Line Buffer is not full, write a 1 to REG[09C0h] bit 2.

bit 1 Raw JPEG Line Buffer Half Full Flag (Read Only)
This flag is asserted when the JPEG Line Buffer becomes half full. This flag is not affected by the JPEG Line Buffer Half Full Interrupt Enable bit (REG[09C6h] bit 1).
When this bit = 0, the JPEG Line Buffer is not half full.
When this bit = 1, the JPEG Line Buffer is half full. This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1 ≠ 000b).

To clear this flag, when the JPEG Line Buffer is not half full, write a 1 to REG[09C0h] bit 1.

bit 0 Raw JPEG Line Buffer Empty Flag (Read Only)
This flag is asserted when the JPEG Line Buffer contains less than or equal to 16 bytes of YUV 4:2:2 data or 8 bytes of YUV 4:2:0 data. This flag is not affected by the JPEG Line Buffer Empty Interrupt Enable bit (REG[09C6h] bit 0). This bit is only valid for YUV Capture/Display and Host Encode/Decode modes (REG[0980h] bits 3-1 ≠ 000b).
When this bit = 0, the JPEG Line Buffer is not empty.
When this bit = 1, the JPEG Line Buffer contains 16 bytes or less of YUV 4:2:2 data or 8 bytes or less of YUV 4:2:0 data.

To clear this flag, when the JPEG Line Buffer is not empty, write a 1 to REG[09C0h] bit 0.

REG[09C4h] JPEG Line Buffer Raw Current Status Register
Default = F001h — Read Only

Reserved 15	Reserved 14	Reserved 13	Reserved 12	Reserved 11	Reserved 10	Reserved 9	Reserved 8
Reserved 7	n/a 6	n/a 5	n/a 4	n/a 3	Raw JPEG Line Buffer Full Current Status 2	Raw JPEG Line Buffer Half Full Current Status 1	Raw JPEG Line Buffer Empty Current Status 0

bits 15-7 Reserved
The default value for bits 15 - 12 is 1 and the default value for bits 11 - 8 is 0.

bit 2 Raw JPEG Line Buffer Full Current Status (Read Only)
This flag indicates the current status of the JPEG Line Buffer. This flag is not affected by the JPEG Line Buffer Full Interrupt Enable bit (REG[09C6h] bit 2).
When this bit = 0, the JPEG Line Buffer is not full.
When this bit = 1, the JPEG Line Buffer is full.

bit 1 Raw JPEG Line Buffer Half Full Current Status (Read Only)
This flag indicates the current status of the JPEG Line Buffer. This flag is not affected by the JPEG Line Buffer Half Full Interrupt Enable bit (REG[09C6h] bit 1).
When this bit = 0, the JPEG Line Buffer is not half full.
When this bit = 1, the JPEG Line Buffer is half full.

bit 0 Raw Line Buffer Empty Current Status (Read Only)
This flag indicates the current status of the JPEG Line Buffer. This flag is not affected by the JPEG Line Buffer Empty Interrupt Enable bit (REG[09C6h] bit 0).
When this bit = 0, the JPEG Line Buffer is not empty.
When this bit = 1, the JPEG Line Buffer contains 16 bytes or less of YUV 4:2:2 data or 8 bytes or less of YUV 4:2:0 data.

REG[09C6h] JPEG Line Buffer Interrupt Control Register
Default = 0000h — Read/Write

n/a 15	n/a 14	n/a 13	n/a 12	n/a 11	n/a 10	n/a 9	n/a 8
n/a 7	n/a 6	n/a 5	n/a 4	n/a 3	JPEG Line Buffer Full Interrupt Enable 2	JPEG Line Buffer Half Full Interrupt Enable 1	JPEG Line Buffer Empty Interrupt Enable 0

bit 2 JPEG Line Buffer Full Interrupt Enable
This bit controls the JPEG Line Buffer Full Interrupt. The status of the interrupt can be determined using the JPEG Line Buffer Full Flag (REG[09C0h] bit 2).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 1 JPEG Line Buffer Half Full Interrupt Enable
This bit controls the JPEG Line Buffer Half Full Interrupt. The status of the interrupt can be determined using the JPEG Line Buffer Half Full Flag (REG[09C0h] bit 1).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 0 JPEG Line Buffer Empty Interrupt Enable
This bit controls the JPEG Line Buffer Empty Interrupt. The status of the interrupt can be determined using the JPEG Line Buffer Empty Flag (REG[09C0h] bit 0).
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

REG[09C8h] through REG[09CEh] are Reserved

These registers are Reserved and should not be written.

REG[09D0h] JPEG Line Buffer Configuration Register
Default = 2800h Read/Write

Reserved	JPEG Line Buffer Raw Horizontal Pixel Size bits 10-4 (RO)						
15	14	13	12	11	10	9	8
JPEG Line Buffer Raw Horizontal Pixel Size bits 3-0 (RO)				Reserved	JPEG Line Buffer Horizontal Pixel Size bits 2-0		
7	6	5	4	3	2	1	0

bit 15 Reserved
The default value for this bit is 0.

bits 14-4 JPEG Line Buffer Raw Horizontal Pixel Size bits [10:0] (Read Only
These bits provide actual number of the horizontal pixel size supported by the JPEG Line Buffer as set in REG[09D0h] bits 2-0.

bit 3 Reserved
The default value for this bit is 0.

bits 2-0 JPEG Line Buffer Horizontal Pixel Size bits [2:0]
These bits indicate the horizontal pixel size supported by the JPEG Line Buffer.

Table 10-56: Supported Horizontal Pixel Size

REG[09D0h] bits 2-0	Supported Horizontal Pixel Size	Line Buffer Size
000b	VGA (640)	30k Bytes
001b	SVGA (800)	38k Bytes
010b	XGA (1024)	48k Bytes
011b - 111b	Reserved	

REG[09D2h] JPEG Line Buffer Address Offset Register
Default = 0040h Read/Write

Reserved							
15	14	13	12	11	10	9	8
Reserved	JPEG Line Buffer Address Offset bits 6-0						
7	6	5	4	3	2	1	0

bits 15-7 Reserved
The default value for these bits is 0.

bits 6-0 JPEG Line Buffer Address Offset bits [6:0]
These bits provide the address offset of the JPEG Line Buffer, and therefore the size (default is 256 bytes), as follows.

REG[09D2h] bits 6-0 = [(96 x 1024) - (XSize x 2 x 24 x F)] / 1024
Offset Value (h) = (REG[09C2h] bits 6-0) x 400h + 20000h

Where:
XSize = Horizontal Size = 640
F (YUV format) = 1 (4:2:0 & 4:4:4) | 0.75 (4:2:2) | 0.5 (4:1:1)
>> 10 represents a 10 bit, shift right operator
<< 10 represents a 10 bit, shift left operator

Note
YUV 4:4:4 format is possible for JPEG decoding only.

Table 10-57: Line Buffer Address Offset Example

Horizontal Size (XSIZE)	K Bytes	REG[09D2h] Value	Offset Value	Area
640	30	42h	30800h	30800h - 37FFFh

REG[09D4h] through REG[09DEh] are Reserved

These registers are Reserved and should not be written.

REG[09E0h] JPEG Line Buffer Read/Write Port Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
JPEG Line Buffer Read/Write Port bits 15-8							
7	6	5	4	3	2	1	0
JPEG Line Buffer Read/Write Port bits 7-0							

bits 15-0 JPEG Line Buffer Read/Write Port bits [15:0]
If YUV data is being input from the Host, these bits are used as the JPEG Line Buffer read/write port. For all other modes, these bits have no hardware effect.

When YUV data is input from Host I/F (REG[0980] bits 3-1 = 001b or 101b), this port becomes the JPEG Line Buffer write port.
When encoded YUV data is input from Host I/F (REG[0980] bits 3-1 = 100b), this port becomes the JPEG Line Buffer write port.
When decoded YUV data is output to Host I/F (REG[0980] bits 3-1 = 100b), this port becomes the JPEG Line Buffer read port.

10.4.17 Interrupt Control Registers

REG[0A00h] Interrupt Status Register
Default = 0000h — Read Only

n/a							
15	14	13	12	11	10	9	8
n/a		SD Card Interrupt Status	Host Interrupt Status	Camera Interrupt Status	JPEG Interrupt Status	BitBLT Interrupt Status	Debug Interrupt Status
7	6	5	4	3	2	1	0

bit 5 SD Card Interrupt Status (Read Only)
This bit indicates the status of the SD Card interrupt. This flag is masked by the SD Card Interrupt Enable bit and is only available when REG[0A02h] bit 5 = 1). This bit is cleared when all SD Card Interrupt Requests are cleared.
When this bit = 0, a SD Card interrupt has not occurred.
When this bit = 1, a SD Card interrupt has occurred. Status flags must be read in REG[6100h] to determine the exact nature of the interrupt.

bit 4 Host Interrupt Status (Read Only)
This bit indicates the status of the Host interrupt.
When this bit = 0, no Host interrupt has occurred.
When this bit = 1, a Host interrupt has occurred. Status flags must be read in REG[0A0Ah] to determine the exact nature of the interrupt.

bit 3 Camera Interrupt Status (Read Only)
This bit indicates the status of the Camera Interrupt.
When this bit = 0, no Camera interrupt has occurred.
When this bit = 1, a Camera interrupt has occurred. Status flags must be read in REG[0116h] to determine the exact nature of the interrupt.

bit 2 JPEG Interrupt Status (Read Only)
This bit indicates the status of the JPEG Interrupt.
When this bit = 0, no JPEG interrupt has occurred.
When this bit = 1, a JPEG interrupt has occurred. Status flags must be read in REG[0982h] to determine the exact nature of the interrupt.

bit 1 BitBLT Interrupt Status (Read Only)
This bit indicates the status of the BitBLT Interrupt.
When this bit = 0, no BitBLT interrupt has occurred.
When this bit = 1, a BitBLT interrupt has occurred. Status flags must be read in REG[8030h] to determine the exact nature of the interrupt.

bit 0 Debug Interrupt Status (Read Only)
This bit indicates the status of the Debug Interrupt.
When this bit = 0, no Debug interrupt has occurred.
When this bit = 1, a Debug interrupt has occurred. Status flags must be read in REG[0A06h] to determine the exact nature of the interrupt.

REG[0A02h] Interrupt Control Register 0
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a		SD Card Interrupt Enable	Host Interrupt Enable	Camera Interrupt Enable	JPEG Interrupt Enable	BitBLT Interrupt Enable	Debug Interrupt Enable
7	6	5	4	3	2	1	0

bit 5 SD Card Interrupt Enable
This bit controls the SD Card interface interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 4 Host Interrupt Enable
This bit controls the Host interface interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 3 Camera Interrupt Enable
This bit controls the Camera interface interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 2 JPEG Interrupt Enable
This bit controls the JPEG codec interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 1 BitBLT Interrupt Enable
This bit controls the BitBLT interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

bit 0 Debug Interrupt Enable
This bit controls the debug interrupt.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

REG[0A04h] Interrupt Control Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a		SD Card Manual Interrupt	Host Manual Interrupt	Camera Manual Interrupt	JPEG Manual Interrupt	BitBLT Manual Interrupt	Debug Manual Interrupt
7	6	5	4	3	2	1	0

bit 5 SD Card Manual Interrupt
This bit manually sets a SD Card interface interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

bit 4 Host Manual Interrupt
This bit manually sets a Host interface interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

bit 3 Camera Manual Interrupt
This bit manually sets a Camera interface interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

bit 2 JPEG Manual Interrupt
This bit manually sets a JPEG codec interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

bit 1 BitBLT Manual Interrupt
This bit manually sets a BitBLT interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

bit 0 Debug Manual Interrupt
This bit manually sets a debug interrupt.
When this bit = 0, the interrupt is cleared.
When this bit = 1, the interrupt is asserted.

REG[0A06h] Debug Status Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a						Display FIFO Empty Flag	YUV/RGB Write Buffer Overflow Flag
7	6	5	4	3	2	1	0

bit 1 Display FIFO Empty Flag
This flag is masked by REG[0A08h] bit 1 and indicates whether the panel interface has attempted to read data from the display FIFO while it is empty. This flag can be used to generate an interrupt (INT signal) to the Host by setting both the Display FIFO Empty Interrupt Enable (REG[0A08h] bit 1 = 1) and the Debug Interrupt Enable (REG[0A02h] bit 0 = 1).
For Reads:
When this bit = 0, the panel interface has not attempted to read data from the display FIFO while it is empty.
When this bit = 1, the panel interface has attempted to read data from the display FIFO while it is empty.

For Writes:
When this bit is written as 0, there is no hardware effect.
When this bit is written as 1, the Display FIFO Empty Flag is cleared.

bit 0 YUV/RGB Write Buffer Overflow Flag
For Reads:
When this bit = 0, no write buffer overflow has occurred.
When this bit = 1, a write buffer overflow has occurred in the path from the YUV/RGB converter to the display buffer.

For Writes:
When this bit is written as 0, there is no hardware effect.
When this bit is written as 1, the YUV/RGB write buffer overflow flag is cleared.

REG[0A08h] Interrupt Control for Debug Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						Display FIFO Empty Interrupt Enable	YUV/RGB Write Buffer Overflow Interrupt Enable

bit 1 Display FIFO Empty Interrupt Enable
This bit controls the display FIFO empty interrupt. The status of this interrupt can be determined using the Display FIFO empty flag (REG[0A06h] bit 1).
When this bit = 0, the display FIFO empty interrupt is disabled.
When this bit = 1, the display FIFO empty interrupt is enabled

bit 0 YUV/RGB Write Buffer Overflow Interrupt Enable
This bit controls the YUV/RGB write buffer overflow flag interrupt output.
When this bit = 0, the YUV/RGB write buffer overflow interrupt is disabled.
When this bit = 1, the YUV/RGB write buffer overflow interrupt is enabled

REG[0A0Ah] Host Cycle Interrupt Status Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Cycle Time Out Interrupt Raw Status	n/a						
n/a		BitBLT FIFO Terminate Write Cycle Interrupt Raw Status	BitBLT FIFO Terminate Read Cycle Interrupt Raw Status	JPEG Line Buffer Terminate Write Cycle Interrupt Raw Status	JPEG Line Buffer Terminate Read Cycle Interrupt Raw Status	JPEG FIFO Terminate Write Cycle Interrupt Raw Status	Reserved
7	6	5	4	3	2	1	0

bit 15 Cycle Time Out Interrupt Raw Status

This bit indicates the raw status of the Cycle Time Out Interrupt which happens when an access cycle to/from the JPEG FIFO, JPEG Line Buffer, or BitBLT FIFO lasts longer than the specified Time Out Value (REG[0A0Eh] bits 4-0). If a Cycle Time Out Interrupt occurs and the Cycle Time Out Interrupt is enabled (REG[0A0Ch] bit 15 = 1) and the Host Interrupt Enable bit (REG[0A02h] bit 4) is set to 1, the INT pin is asserted.
When this bit = 0, a interrupt has not occurred.
When this bit = 1, a Cycle Time Out Interrupt has occurred.

To clear this bit, write a 1 to this bit.

bit 5 BitBLT FIFO Terminate Write Cycle Interrupt Raw Status

This bit indicates the status of the BitBLT FIFO Terminate Write Cycle Interrupt.
When this bit = 0, no interrupt has occurred.
When this bit = 1, a BitBLT FIFO Terminate Write Cycle Interrupt has occurred.

To clear this bit, write this bit as 1.

bit 4 BitBLT FIFO Terminate Read Cycle Interrupt Raw Status

This bit indicates the status of the BitBLT FIFO Terminate Read Cycle Interrupt.
When this bit = 0, no interrupt has occurred.
When this bit = 1, a BitBLT FIFO Terminate Read Cycle Interrupt has occurred.

To clear this bit, write this bit as 1.

bit 3 JPEG Line Buffer Terminate Write Cycle Interrupt Raw Status

This bit indicates the status of the JPEG Line Buffer Terminate Write Cycle Interrupt which happens when a write cycle attempts to write to the JPEG line buffer when it is full. When this happens, the cycle is terminated and no data is written to the JPEG line buffer. This interrupt is used to determine whether another write must be performed. If a JPEG Line Buffer Terminate Write Cycle Interrupt occurs and the JPEG Line Buffer Terminate Write Cycle Interrupt is enabled (REG[0A0Ch] bit 3 = 1). and the Host Interrupt Enable bit (REG[0A02h] bit 4) is set to 1, the INT pin is asserted.
When this bit = 0, a interrupt has not occurred.
When this bit = 1, a JPEG Line Buffer Terminate Write Cycle Interrupt has occurred.

To clear this bit, write a 1 to this bit.

bit 2 JPEG Line Buffer Terminate Read Cycle Interrupt Raw Status
This bit indicates the status of the JPEG Line Buffer Terminate Read Cycle Interrupt which happens when a read cycle attempts to read from the JPEG line buffer when it is empty. When this happens, the cycle is terminated and no data is read from the JPEG line buffer. This interrupt is used to determine whether another read must be performed. If a JPEG Line Buffer Terminate Read Cycle Interrupt occurs and the JPEG Line Buffer Terminate Read Cycle Interrupt is enabled (REG[0A0Ch] bit 2 = 1), and the Host Interrupt Enable bit (REG[0A02h] bit 4) is set to 1, the INT pin is asserted.
When this bit = 0, a interrupt has not occurred.
When this bit = 1, a JPEG Line Buffer Terminate Read Cycle Interrupt has occurred.

To clear this bit, write a 1 to this bit.

bit 1 JPEG FIFO Terminate Write Cycle Interrupt Raw Status
This bit indicates the status of the JPEG FIFO Terminate Write Cycle Interrupt which happens when a write cycle attempts to write to the JPEG FIFO when it is full. When this happens, the cycle is terminated and no data is written to the JPEG FIFO. This interrupt is used to determine whether another write must be performed. If a JPEG FIFO Terminate Write Cycle Interrupt occurs and the JPEG FIFO Terminate Write Cycle Interrupt is enabled (REG[0A0Ch] bit 1 = 1), and the Host Interrupt Enable bit (REG[0A02h] bit 4) is set to 1, the INT pin is asserted.
When this bit = 0, a interrupt has not occurred.
When this bit = 1, a JPEG FIFO Terminate Write Cycle Interrupt has occurred.

To clear this bit, write a 1 to this bit.

bit 0 Reserved
The default value for this bit is 0.

REG[0A0Ch] Host Cycle Interrupt Control Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
Cycle Time Out Interrupt Enable	n/a						
7	6	5	4	3	2	1	0
n/a		BitBLT FIFO Terminate Write Cycle Interrupt Enable	BitBLT FIFO Terminate Read Cycle Interrupt Enable	JPEG Line Buffer Terminate Write Cycle Interrupt Enable	JPEG Line Buffer Terminate Read Cycle Interrupt Enable	JPEG FIFO Terminate Write Cycle Interrupt Enable	Reserved

bit 15 Cycle Time Out Interrupt Enable
When this bit is 0, the Host Interrupt Request bit is not set.
When this bit is 1, the Host Interrupt Request bit is set.

bit 5 BitBLT FIFO Terminate Write Cycle Interrupt Enable
When this bit is 0, the interrupt is disabled.
When this bit is 1, the interrupt is enabled.

bit 4 BitBLT FIFO Terminate Read Cycle Interrupt Enable
When this bit is 0, interrupt is disabled.
When this bit is 1, interrupt is enabled.

bit 3 JPEG Line Buffer Terminate Write Cycle Interrupt Enable
When this bit is 0, the Host Interrupt Request bit is not set.
When this bit is 1, the Host Interrupt Request bit is set.

bit 2 JPEG Line Buffer Terminate Read Cycle Interrupt Enable
When this bit is 0, the Host Interrupt Request bit is not set.
When this bit is 1, the Host Interrupt Request bit is set.

bit 1 JPEG FIFO Terminate Write Cycle Interrupt Enable
When this bit is 0, the Host Interrupt Request bit is not set.
When this bit is 1, the Host Interrupt Request bit is set.

bit 0 Reserved
The default value for this bit is 0.

REG[0A0Eh] Cycle Time Out Control Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Immediate Terminate Cycle Enable	n/a		Time Out Value bits 4-0				
7	6	5	4	3	2	1	0

bit 7 Immediate Terminate Cycle Enable
Terminate cycles are used to terminate (or end) read/write cycles to the JPEG FIFO (write only), JPEG Line Buffer and BitBLT FIFO. This bit in conjunction with the Time Out Value bits (REG[0A0Eh] bits 4-0) determines when a terminate cycle is generated. The following tables summarizes the conditions that cause a terminate cycle to be generated.

Note
When the Immediate Terminate Cycle function is enabled (REG[0A0Eh] bit 7 = 1), the Time Out Value bits (REG[0A0Eh] bits 4-0) must be set to 1Fh.

Table 10-58: Terminate Cycle Generation Summary

REG[0A0Eh] bit 7	REG[0A0Eh] bits 4-0	Terminate Cycle Generation
0	= 11111b	If a write to a full JPEG FIFO/Line Buffer/BitBLT FIFO or a read from an empty JPEG Line Buffer/BitBLT FIFO is attempted, a terminate cycle is generated once the Time Out Value of 1Fh is exceeded.
	≠ 11111b	If a write to a full JPEG FIFO/Line Buffer/BitBLT FIFO or a read from an empty JPEG Line Buffer/BitBLT FIFO is attempted, a terminate cycle is generated once the Time Out Value is exceeded.
1	= 11111b	If a write to a full JPEG FIFO/Line Buffer/BitBLT FIFO or a read from an empty JPEG Line Buffer/BitBLT FIFO is attempted, a terminate cycle is generated immediately. If a write access to a full JPEG FIFO/Line Buffer/BitBLT FIFO or a read access from a JPEG Line Buffer/BitBLT FIFO exceeds the Time Out Value (REG[0A0Eh] bits 4-0) of 1Fh, a terminate cycle is generated immediately.

bits 4-0 Time Out Value bits[4:0]
These bits control the length of time (time out value) allowed for an access cycle to the JPEG FIFO, JPEG Line Buffer, or BitBLT FIFO to take place before a terminate cycle is generated. The time out value is specified as follows and should be configured to a default value of 1Fh at initialization.

REG[0A0Eh] bits 4-0 = Time Out Value in CLKs
Time Out Value = Internal System Clock ÷ 2

REG[0A10h] is Reserved

This register is Reserved and should not be written.

REG[0A40h] Interrupt Request Status Register
Default = 0000h — Read Only

n/a							
15	14	13	12	11	10	9	8
n/a		SD Card Interrupt Request Status	Host Interface Interrupt Request Status	Camera Interrupt Request Status	JPEG Interrupt Request Status	BitBLT Interrupt Request Status	Debug Interrupt Request Status
7	6	5	4	3	2	1	0

bit 5 SD Card Interrupt Request Status (Read Only)
This bit indicates a SD Card interrupt request has taken place. This bit is not masked by the corresponding interrupt enable bit in REG[0A02h].
When this bit = 0, a SD Card interrupt has not occurred.
When this bit = 1, a SD Card interrupt has occurred. Interrupt request flags must be read in REG[6100h] to determine the exact nature of the interrupt.

bit 4 Host Interface Interrupt Request Status (Read Only)
When this bit = 0, a host interface interrupt has not occurred.
When this bit = 1, a host interface interrupt request has occurred.

bit 3 Camera Interrupt Request Status (Read Only)
When this bit = 0, a camera interrupt request has not occurred.
When this bit = 1, a camera interrupt request has occurred.

bit 2 JPEG Interrupt Request Status (Read Only)
When this bit = 0, a JPEG interrupt request has not occurred.
When this bit = 1, a JPEG interrupt request has occurred.

bit 1 BitBLT Interrupt Request Status (Read Only)
When this bit = 0, a BitBLT interrupt request has not occurred.
When this bit = 1, a BitBLT interrupt request has occurred.

bit 0 Debug Interrupt Request Status (Read Only)
When this bit = 0, a debug interrupt request has not occurred.
When this bit = 1, a debug interrupt request has occurred.

10.4.18 JPEG Encode Performance Register

REG[0F00h] JPEG Encode Performance Register
Default = 0001h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							JPEG Encode High Speed Mode

bit 0 JPEG Encode High Speed Mode
When this bit = 0, the JPEG Encoding process runs in “High Speed Mode”.
When this bit = 1, the JPEG Encoding process runs in “Normal Mode” (default).

When High Speed Mode is enabled, the Huffman Tables must be programmed according to the tables specified in the ISO/IEC IS 10918-1 ANNEX K in the ITU-T recommendation T.81 book K. For recommended values see the bit descriptions for the Huffman Tables
(REG[1400h] - [17A2h].

10.4.19 JPEG Codec Registers

REG[1000h] Operation Mode Setting Register
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
Reserved	n/a		Reserved	Marker Insert Enable	JPEG Operation Select	YUV Format Select bits 1-0	
7	6	5	4	3	2	1	0

bit 7 Reserved
The default value for this bit is 0.

bit 4 Reserved
The default value for this bit is 0.

bit 3 Marker Insert Enable
This bit determines if the marker (see REG[1020h] - [1066h]) is inserted during JPEG encoding. During JPEG decoding this bit is ignored.
When this bit = 0, the marker is not inserted.
When this bit = 1, the entire marker is inserted into the JPEG file.

Note
When the marker is inserted, the entire 36 byte marker (REG[1020h] - [1066h]) is inserted into the JPEG file regardless of what value the marker length bits (REG[1024h] - [1026h]) specify.

bit 2 JPEG Operation Select
This bit selects the JPEG operation and the input source for the resizer block. This bit should be set to 0 when resizing data from the camera. This bit must be cleared before the JPEG module is disabled (REG[0980h] bit 0 = 0).

Table 10-59: JPEG Operation Selection

REG[1000h] bit 2	JPEG Operation	Resizer Source
0	Encode	Camera data / Memory image data / Host data
1	Decode	JPEG decoded data

bits 1-0 YUV Format Select bits[1:0]
These bits select the YUV format of the JPEG codec. For the JPEG encode process, these bits must be set to the desired YUV format. For the JPEG decode process, these bits are read only and indicate the YUV format of the data being decoded.

Table 10-60: YUV Format Selection

REG[1000h] bits 1-0	YUV Format
00b	4:4:4 (decode only)
01b	4:2:2 (encode/decode)
10b	4:2:0 (encode/decode)
11b	4:1:1 (encode/decode)

Note
Only YUV 4:2:0 and YUV 4:2:2 are supported for Host input JPEG decode/encode.

REG[1002h] Command Setting Register
Default = not applicable — Write Only

15	14	13	12	11	10	9	8
n/a							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JPEG Codec SW Reset	n/a						JPEG Operation Start

Note
This register is write only. Reading this register may cause the JPEG Codec to behave unexpectedly.

Note
When the JPEG codec is working, this register must not be written to, except to perform a JPEG codec software reset.

bit 7 JPEG Codec Software Reset (Write Only)
This bit initiates a software reset of the JPEG Codec. The JPEG Codec registers (REG[1000h]-[17A2h]) are not affected.
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the JPEG Codec is reset.

bit 0 JPEG Operation Start (Write Only)
This bit is used to begin a JPEG operation.
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the JPEG operation is started.

REG[1004h] JPEG Operation Status Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							JPEG Operation Status (RO)

bit 0 JPEG Operation Status (Read Only)
This bit indicates the state of the JPEG codec and clears the JPEG codec interrupt (REG[0982h] bit 1) when read.
When this bit = 0, the JPEG codec is idle.
When this bit = 1, the JPEG codec is busy (a decode or encode operation is in progress).

REG[1006h] Quantization Table Number Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a					Color 3 Table Select	Color 2 Table Select	Color 1 Table Select

bit 2 Color 3 Table Select
When this bit = 0, the Color 3 Table uses Quantization Table No. 0 (REG[1200-127Eh].
When this bit = 1, the Color 3 Table uses Quantization Table No. 1 (REG[1280-12FEh].

bit 1 Color 2 Table Select
When this bit = 0, the Color 2 Table uses Quantization Table No. 0 (REG[1200-127Eh].
When this bit = 1, the Color 2 Table uses Quantization Table No. 1 (REG[1280-12FEh].

bit 0 Color 1 Table Select
When this bit = 0, the Color 1 Table uses Quantization Table No. 0 (REG[1200-127Eh].
When this bit = 1, the Color 1 Table uses Quantization Table No. 1 (REG[1280-12FEh].

REG[1008h] Huffman Table Number Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a		AC Color 3 Table Select	DC Color 3 Table Select	AC Color 2 Table Select	DC Color 2 Table Select	AC Color 1 Table Select	DC Color 1 Table Select
7	6	5	4	3	2	1	0

bit 5 AC Color 3 Table Select
When this bit = 0, the AC Color 3 Table uses the AC Huffman Table No. 0 (REG[1440-145Eh] and REG[1460-15A2h]).
When this bit = 1, the AC Color 3 Table uses the AC Huffman Table No. 1 (REG[1640-165Eh] and REG[1660-17A2h]).

bit 4 DC Color 3 Table Select
When this bit = 0, the DC Color 3 Table uses the DC Huffman Table No. 0 (REG[1400-141Eh] and REG[1420-1436h]).
When this bit = 1, the DC Color 3 Table uses the DC Huffman Table No. 1 (REG[1600-161Eh] and REG[1620-1636h]).

bit 3 AC Color 2 Table Select
When this bit = 0, the AC Color 2 Table uses the AC Huffman Table No. 0 (REG[1440-145Eh] and REG[1460-15A2h]).
When this bit = 1, the AC Color 2 Table uses the AC Huffman Table No. 1 (REG[1640-165Eh] and REG[1660-17A2h]).

bit 2 DC Color 2 Table Select
When this bit = 0, the DC Color 2 Table uses the DC Huffman Table No. 0 (REG[1400-141Eh] and REG[1420-1436h]).
When this bit = 1, the DC Color 2 Table uses the DC Huffman Table No. 1 (REG[1600-161Eh] and REG[1620-1636h]).

bit 1 AC Color 1 Table Select
When this bit = 0, the AC Color 1 Table uses the AC Huffman Table No. 0 (REG[1440-145Eh] and REG[1460-15A2h]).
When this bit = 1, the AC Color 1 Table uses the AC Huffman Table No. 1 (REG[1640-165Eh] and REG[1660-17A2h]).

bit 0 DC Color 1 Table Select
When this bit = 0, the DC Color 1 Table uses the DC Huffman Table No. 0 (REG[1400-141Eh] and REG[1420-1436h]).
When this bit = 1, the DC Color 1 Table uses the DC Huffman Table No. 1 (REG[1600-161Eh] and REG[1620-1636h]).

REG[100Ah] DRI Setting Register 0
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
DRI Value bits 15-8							
7	6	5	4	3	2	1	0

REG[100Ch] DRI Setting Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
DRI Value bits 7-0							
7	6	5	4	3	2	1	0

REG[100Ah] bits 7-0
REG[100Ch] bits 7-0 DRI Value bits [15:0]

These bits determine the MCU number for RST marker insertion during encoding. During decoding, these bits are ignored. The DRI value bits must be set when JPEG 180° Rotation Encode is enabled (REG[0980h] bit 8 = 1). The DRI (Designated Restart Interval) value must be set as follows.

DRI = Image Width / Horizontal MCU Size

Where:

MCU Size depends on the YUV format (REG[1000h] bits 1-0) as follows

Table 10-61: MCU Size

REG[1000h] bits 1-0	YUV Format	MCU Size (Horizontal x Vertical)
00b	Reserved	Reserved
01b	4:2:2	16 x 8
10b	4:2:0	16 x 16
11b	4:1:1	32 x 8

REG[100Eh] Vertical Pixel Size Register 0
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Y Pixel Size bits 15-8							

REG[1010h] Vertical Pixel Size Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Y Pixel Size bits 7-0							

REG[100Eh] bits 7-0
REG[1010h] bits 7-0 Y Pixel Size bits[15:0]

For the JPEG encode process, these bits specify the vertical image size before encoding takes place.
For the JPEG decode process, these bits are read-only and indicate the vertical image size.

The following restrictions must be observed when setting the Vertical Pixel Size. The minimum resolution must be set based on the YUV format as follows.

Table 10-62: Vertical Pixel Size Minimum Resolution Restrictions

YUV Format	Minimum Resolution
4:4:4 (decode only)	1x1
4:2:2 (encode/decode)	2x1
4:2:0 (encode/decode)	2x2
4:1:1 (encode/decode)	4x1

Note
For all processes (JPEG encode/decode and YUV capture/display) the following formula must be valid.
Vertical Pixel Size > 1

REG[1012h] Horizontal Pixel Size Register 0
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
X Pixel Size bits 15-8							

REG[1014h] Horizontal Pixel Size Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
X Pixel Size bits 7-0							

REG[1012h] bits 7-0
REG[1014h] bits 7-0 X Pixel Size bits[15:0]

For the JPEG encode process, these bits specify the horizontal image size before encoding takes place.
For the JPEG decode process, these bits are read-only and indicate the horizontal image size.

The following restrictions must be observed when setting the Vertical Pixel Size. The minimum resolution must be set based on the YUV format as follows.

Table 10-63: Horizontal Pixel Size Minimum Resolution Restrictions

YUV Format	Minimum Resolution	Minimum Horizontal Pixel Size
4:2:2	2x1	2
4:2:0	2x2	16
4:1:1	4x1	4

REG[1016h] DNL Value Setting Register 0
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
DNL Value bits 15-8							

REG[1018h] DNL Value Setting Register 1
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
DNL Value bits 7-0							

REG[1018h] bits 7-0
REG[1016h] bits 7-0 DNL Value bits[15:0]
For the JPEG decode process, these bits are read-only and indicate the DNL (Define Number of Lines) value for the decoded JPEG file.
For the JPEG encode process, these bits are not used.

REG[101Ah] is Reserved

This register is Reserved and should not be written.

REG[101Ch] RST Marker Operation Setting Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						RST Marker Operation Select bits 1-0	

bits 1-0 RST Marker Operation Select bits[1:0]
For the JPEG decode process, these bits select the RST Marker Operation.
For the JPEG encode process, these bits are not used.

Table 10-64: RST Marker Selection

REG[101Ch] bits 1-0	RST Marker Operation
00b	**Error detection and data revise function is turned off** This option should only be used when it is certain that the JPEG file to be decoded is correct and has no errors. If there is an error in the file, no error detection will take place and the decode process will not finish correctly.
01b	**Error detection on** When an error is detected during the decode process, the decode process finishes and the JPEG interrupt is asserted (REG[0A00h] bit 2 = 1). To determine the exact nature of the operational error see REG[0982h]. To determine the JPEG decode error (file error), check the JPEG Error Status bits (REG[101Eh] bits 6-3). Because the decode process finished before normal completion, all data can not be displayed. If the JPEG file is to be decoded again with the Data Revise function on, a software reset is required (see REG[1002h] bit 7).
10b	**Data revise function on** When an error is detected during the decode process, data is skipped/added automatically and the decode process continues normally to the end of file. After the decode process finishes, a data revise interrupt is asserted. Because the decode process is finished completely, the next JPEG file can be decoded immediately.
11b	Reserved

REG[101Eh] RST Marker Operation Status Register
Default = 0000h — Read Only

n/a							
15	14	13	12	11	10	9	8
Revise Code	JPEG Error Status bits 3-0				n/a		
7	6	5	4	3	2	1	0

bit 7 Revise Code (Read Only)

This bit is valid only when the data revise function is enabled using the RST Marker Selection bits (REG[101Ch bits 1-0 = 10b).

For the JPEG decode process, this bit indicates whether a revise operation has been done.
For the JPEG encode process, this bit is not used.
When this bit = 0, a revise operation was not done.
When this bit = 1, a revise operation was done.

bits 6-3 JPEG Error Status[3:0] (Read Only)

These bits are valid only when error detection is enabled using the RST Marker Selection bits (REG[101Ch bits 1-0 = 01b).

For the JPEG decode process, these bits indicate the type of JPEG error. If these bits return 0000b, no error has occurred.
For the JPEG encode process, these bits are not used.

Table 10-65: JPEG Error Status

REG[101Eh] bits 6-3	JPEG Error Status
0000b	No error
0001b - 1010b	Reserved
1011b	Restart interval error
1100b	Image size error
1101b - 1111b	Reserved

REG[1020 - 1066h] Insertion Marker Data Register
Default = 00FFh Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Insert marker Data bits 7-0							

REG[1020h-1066h] These registers (36 bytes) store the Insertion Marker Data which gets inserted into the JPEG file. Only the even bytes are used. All unused registers (up to REG[1200h]) should be filled with FFh. The registers are defined as follows.

Table 10-66: Insertion Marker Data Register Usage

Register	Description
REG[1020h]-[1022h]	These registers set the insertion marker code type.
REG[1024h]-[1026h]	These registers set the marker length (0002h - 0022h).
REG[1028h]-[1066h]	These registers set the marker data (up to a maximum of 32 bytes). Note that all unused registers must be filled with FFh.

REG[1200 - 127Eh] Quantization Table No. 0 Register
Default = not applicable Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Quantization Table No. 0 bits 7-0							

REG[1200-127Eh] Quantization Table No. 0
These registers are used for the JPEG encode process only.

REG[1280 - 12FEh] Quantization Table No. 1 Register
Default = not applicable Write Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Quantization Table No. 1 bits 7-0							

REG[1280-12FEh] Quantization Table No. 1
These registers are used for the JPEG encode process only.

REG[1400 - 141Eh] DC Huffman Table No. 0 Register 0
Default = not applicable — Write Only

n/a							
15	14	13	12	11	10	9	8
DC Huffman Table No. 0 Register 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1400-141Eh] DC Huffman Table No. 0 (Write Only)

These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 0 must be programmed as follows.

Table 10-67: DC Huffman Table No. 0 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1400h]	00h	REG[1408h]	01h	REG[1410h]	01h	REG[1418h]	00h
REG[1402h]	01h	REG[140Ah]	01h	REG[1412h]	00h	REG[141Ah]	00h
REG[1404h]	05h	REG[140Ch]	01h	REG[1414h]	00h	REG[141Ch]	00h
REG[1406h]	01h	REG[140Eh]	01h	REG[1416h]	00h	REG[141Eh]	00h

REG[1420 - 1436h] DC Huffman Table No. 0 Register 1
Default = not applicable — Write Only

n/a							
15	14	13	12	11	10	9	8
Reserved (must be all 0)				DC Huffman Table No. 0 Register 1 bits 3-0			
7	6	5	4	3	2	1	0

REG[1420-1436h] DC Huffman Table No. 0 (Write Only)

These registers are used for the JPEG encode process only and set a group number based on the order of probability of occurrence. Only bits 3-0 are used (bits 7-4 must be set to 0). When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 0 must be programmed as follows.

Table 10-68: DC Huffman Table No. 1 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1420h]	00h	REG[1426h]	03h	REG[142Ch]	06h	REG[1432h]	09h
REG[1422h]	01h	REG[1428h]	04h	REG[142Eh]	07h	REG[1434h]	0Ah
REG[1424h]	02h	REG[142Ah]	05h	REG[1430h]	08h	REG[1436h]	0Bh

REG[1440 - 145Eh] AC Huffman Table No. 0 Register 0
Default = not applicable — Write Only

n/a							
15	14	13	12	11	10	9	8
AC Huffman Table No. 0 Register 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1440-145Eh] AC Huffman Table No. 0 (Write Only)

These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 0 must be programmed as follows.

Table 10-69: AC Huffman Table No. 0 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1440h]	00h	REG[1448h]	03h	REG[1450h]	05h	REG[1458h]	00h
REG[1442h]	02h	REG[144Ah]	02h	REG[1452h]	05h	REG[145Ah]	00h
REG[1444h]	01h	REG[144Ch]	04h	REG[1454h]	04h	REG[145Ch]	01h
REG[1446h]	03h	REG[144Eh]	03h	REG[1456h]	04h	REG[145Eh]	7Dh

REG[1460 - 15A2h] AC Huffman Table No. 0 Register 1
Default = not applicable — Write Only

n/a							
15	14	13	12	11	10	9	8
AC Huffman Table No. 0 Register 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1460-15A2h] AC Huffman Table No. 0 (Write Only)

These registers are used for the JPEG encode process only and set a zero run length / group number based on the order of probability of occurrence. When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 0 must be programmed as follows.

Table 10-70: AC Huffman Table No. 0 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1460h]	01h	REG[14B0h]	17h	REG[1500h]	6Ah	REG[1550h]	B7h
REG[1462h]	02h	REG[14B2h]	18h	REG[1502h]	73h	REG[1552h]	B8h
REG[1464h]	03h	REG[14B4h]	19h	REG[1504h]	74h	REG[1554h]	B9h
REG[1466h]	00h	REG[14B6h]	1Ah	REG[1506h]	75h	REG[1556h]	BAh
REG[1468h]	04h	REG[14B8h]	25h	REG[1508h]	76h	REG[1558h]	C2h
REG[146Ah]	11h	REG[14BAh]	26h	REG[150Ah]	77h	REG[155Ah]	C3h
REG[146Ch]	05h	REG[14BCh]	27h	REG[150Ch]	78h	REG[155Ch]	C4h
REG[146Eh]	12h	REG[14BEh]	28h	REG[150Eh]	79h	REG[155Eh]	C5h
REG[1470h]	21h	REG[14C0h]	29h	REG[1510h]	7Ah	REG[1560h]	C6h
REG[1472h]	31h	REG[14C2h]	2Ah	REG[1512h]	83h	REG[1562h]	C7h
REG[1474h]	41h	REG[14C4h]	34h	REG[1514h]	84h	REG[1564h]	C8h
REG[1476h]	06h	REG[14C6h]	35h	REG[1516h]	85h	REG[1566h]	C9h
REG[1478h]	13h	REG[14C8h]	36h	REG[1518h]	86h	REG[1568h]	CAh
REG[147Ah]	51h	REG[14CAh]	37h	REG[151Ah]	87h	REG[156Ah]	D2h
REG[147Ch]	61h	REG[14CCh]	38h	REG[151Ch]	88h	REG[156Ch]	D3h
REG[147Eh]	07h	REG[14CEh]	39h	REG[151Eh]	89h	REG[156Eh]	D4h
REG[1480h]	22h	REG[14D0h]	3Ah	REG[1520h]	8Ah	REG[1570h]	D5h
REG[1482h]	71h	REG[14D2h]	43h	REG[1522h]	92h	REG[1572h]	D6h
REG[1484h]	14h	REG[14D4h]	44h	REG[1524h]	93h	REG[1574h]	D7h
REG[1486h]	32h	REG[14D6h]	45h	REG[1526h]	94h	REG[1576h]	D8h
REG[1488h]	81h	REG[14D8h]	46h	REG[1528h]	95h	REG[1578h]	D9h
REG[148Ah]	91h	REG[14DAh]	47h	REG[152Ah]	96h	REG[157Ah]	DAh
REG[148Ch]	A1h	REG[14DCh]	48h	REG[152Ch]	97h	REG[157Ch]	E1h
REG[148Eh]	08h	REG[14DEh]	49h	REG[152Eh]	98h	REG[157Eh]	E2h
REG[1490h]	23h	REG[14E0h]	4Ah	REG[1530h]	99h	REG[1580h]	E3h
REG[1492h]	42h	REG[14E2h]	53h	REG[1532h]	9Ah	REG[1582h]	E4h
REG[1494h]	B1h	REG[14E4h]	54h	REG[1534h]	A2h	REG[1584h]	E5h
REG[1496h]	C1h	REG[14E6h]	55h	REG[1536h]	A3h	REG[1586h]	E6h
REG[1498h]	15h	REG[14E8h]	56h	REG[1538h]	A4h	REG[1588h]	E7h
REG[149Ah]	52h	REG[14EAh]	57h	REG[153Ah]	A5h	REG[158Sh]	E8h
REG[149Ch]	D1h	REG[14ECh]	58h	REG[153Ch]	A6h	REG[158Ch]	E9h
REG[149Eh]	F0h	REG[14EEh]	59h	REG[153Eh]	A7h	REG[158Eh]	EAh
REG[14A0h]	24h	REG[14F0h]	5Ah	REG[1540h]	A8h	REG[1590h]	F1h
REG[14A2h]	33h	REG[14F2h]	63h	REG[1542h]	A9h	REG[1592h]	F2h
REG[14A4h]	62h	REG[14F4h]	64h	REG[1544h]	AAh	REG[1594h]	F3h
REG[14A6h]	72h	REG[14F6h]	65h	REG[1546h]	B2h	REG[1596h]	F4h
REG[14A8h]	82h	REG[14F8h]	66h	REG[1548h]	B3h	REG[1598h]	F5h
REG[14AAh]	09h	REG[14FAh]	67h	REG[154Ah]	B4h	REG[159Ah]	F6h
REG[14ACh]	0Ah	REG[14FCh]	68h	REG[154Ch]	B5h	REG[159Ch]	F7h
REG[14AEh]	16h	REG[14FEh]	69h	REG[154Eh]	B6h	REG[159Eh]	F8h
						REG[15A0h]	F9h
						REG[15A2h]	FAh

REG[1600 - 161Eh] DC Huffman Table No. 1 Register 0
Default = not applicable — Write Only

n/a							
15	14	13	12	11	10	9	8
DC Huffman Table 1 Register No. 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1600-161Eh] DC Huffman Table No. 1 (Write Only)

These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 1 must be programmed as follows.

Table 10-71: DC Huffman Table No. 1 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1600h]	00h	REG[1608h]	01h	REG[1610h]	01h	REG[1618h]	00h
REG[1602h]	03h	REG[160Ah]	01h	REG[1612h]	01h	REG[161Ah]	00h
REG[1604h]	01h	REG[160Ch]	01h	REG[1614h]	01h	REG[161Ch]	00h
REG[1606h]	01h	REG[160Eh]	01h	REG[1616h]	00h	REG[161Eh]	00h

REG[1620 - 1636h] DC Huffman Table No. 1 Register 1
Default = not applicable — Write Only

n/a							
15	14	13	12	11	10	9	8
Reserved (must be all 0)				DC Huffman Table No. 1 Register 1 bits 3-0			
7	6	5	4	3	2	1	0

REG[1620-1636h] DC Huffman Table No. 1 (Write Only)

These registers are used for the JPEG encode process only and set a group number based on the order of probability of occurrence. Only bits 3-0 are used (bits 7-4 must be set to 0). When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the DC Huffman Table No. 1 must be programmed as follows.

Table 10-72: DC Huffman Table No. 1 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1620h]	00h	REG[1626h]	03h	REG[162Ch]	06h	REG[1632h]	09h
REG[1622h]	01h	REG[1628h]	04h	REG[162Eh]	07h	REG[1634h]	0Ah
REG[1624h]	02h	REG[162Ah]	05h	REG[1630h]	08h	REG[1636h]	0Bh

REG[1640 - 165Eh] AC Huffman Table No. 1 Register 0
Default = not applicable — Write Only

n/a							
15	14	13	12	11	10	9	8
AC Huffman Table No. 1 Register 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1640-165Eh] AC Huffman Table No. 1 (Write Only)

These registers are used for the JPEG encode process only and set the codes for code length. When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 1 must be programmed as follows.

Table 10-73: AC Huffman Table No. 1 Values for High Speed Mode

Register	Value	Register	Value	Register	Value	Register	Value
REG[1640h]	00h	REG[1648h]	04h	REG[1650h]	07h	REG[1658h]	00h
REG[1642h]	02h	REG[164Ah]	04h	REG[1652h]	05h	REG[165Ah]	01h
REG[1644h]	01h	REG[164Ch]	03h	REG[1654h]	04h	REG[165Ch]	02h
REG[1646h]	02h	REG[164Eh]	04h	REG[1656h]	04h	REG[165Eh]	77h

REG[1660 - 17A2h] AC Huffman Table No. 1 Register 1
Default = not applicable — Write Only

n/a							
15	14	13	12	11	10	9	8
AC Huffman Table No. 1 Register 0 bits 7-0							
7	6	5	4	3	2	1	0

REG[1660-17A2h] AC Huffman Table No. 1 (Write Only)

These registers are used for the JPEG encode process only and set a zero run length / group number based on the order of probability of occurrence. When JPEG Encode "High Speed Mode" is enabled (REG[0F00h] bit 0 = 0), the AC Huffman Table No. 1 must be programmed as follows.

Table 10-74: AC Huffman Table No. 1 Values for High Speed Mode

Register	Value
REG[1660h]	00h
REG[1662h]	01h
REG[1664h]	02h
REG[1666h]	03h
REG[1668h]	11h
REG[166Ah]	04h
REG[166Ch]	05h
REG[166Eh]	21h
REG[1670h]	31h
REG[1672h]	06h
REG[1674h]	12h
REG[1676h]	41h
REG[1678h]	51h
REG[167Ah]	07h
REG[167Ch]	61h
REG[167Eh]	71h
REG[1680h]	13h
REG[1682h]	22h
REG[1684h]	32h
REG[1686h]	81h
REG[1688h]	08h
REG[168Ah]	14h
REG[168Ch]	42h
REG[168Eh]	91h
REG[1690h]	A1h
REG[1692h]	B1h
REG[1694h]	C1h
REG[1696h]	09h
REG[1698h]	23h
REG[169Ah]	33h
REG[169Ch]	52h
REG[169Eh]	F0h
REG[16A0h]	15h
REG[16A2h]	62h
REG[16A4h]	72h
REG[16A6h]	D1h
REG[16A8h]	0Ah
REG[16AAh]	16h
REG[16ACh]	24h
REG[16AEh]	34h

Register	Value
REG[16B0h]	E1h
REG[16B2h]	25h
REG[16B4h]	F1h
REG[16B6h]	17h
REG[16B8h]	18h
REG[16BAh]	19h
REG[16BCh]	1Ah
REG[16BEh]	26h
REG[16C0h]	27h
REG[16C2h]	28h
REG[16C4h]	29h
REG[16C6h]	2Ah
REG[16C8h]	35h
REG[16CAh]	36h
REG[16CCh]	37h
REG[16CEh]	38h
REG[16D0h]	39h
REG[16D2h]	3Ah
REG[16D4h]	43h
REG[16D6h]	44h
REG[16D8h]	45h
REG[16DAh]	46h
REG[16DCh]	47h
REG[16DEh]	48h
REG[16E0h]	49h
REG[16E2h]	4Ah
REG[16E4h]	53h
REG[16E6h]	54h
REG[16E8h]	55h
REG[16EAh]	56h
REG[16ECh]	57h
REG[16EEh]	58h
REG[16F0h]	59h
REG[16F2h]	5Ah
REG[16F4h]	63h
REG[16F6h]	64h
REG[16F8h]	65h
REG[16FAh]	66h
REG[16FCh]	67h
REG[16FEh]	68h

Register	Value
REG[1700h]	69h
REG[1702h]	6Ah
REG[1704h]	73h
REG[1706h]	74h
REG[1708h]	75h
REG[170Ah]	76h
REG[170Ch]	77h
REG[170Eh]	78h
REG[1710h]	79h
REG[1712h]	7Ah
REG[1714h]	82h
REG[1716h]	83h
REG[1718h]	84h
REG[171Ah]	85h
REG[171Ch]	86h
REG[171Eh]	87h
REG[1720h]	88h
REG[1722h]	89h
REG[1724h]	8Ah
REG[1726h]	92h
REG[1728h]	93h
REG[172Ah]	94h
REG[172Ch]	95h
REG[172Eh]	96h
REG[1730h]	97h
REG[1732h]	98h
REG[1734h]	99h
REG[1736h]	9Ah
REG[1738h]	A2h
REG[173Ah]	A3h
REG[173Ch]	A4h
REG[173Eh]	A5h
REG[1740h]	A6h
REG[1742h]	A7h
REG[1744h]	A8h
REG[1746h]	A9h
REG[1748h]	AAh
REG[174Ah]	B2h
REG[174Ch]	B3h
REG[174Eh]	B4h

Register	Value
REG[1750h]	B5h
REG[1752h]	B6h
REG[1754h]	B7h
REG[1756h]	B8h
REG[1758h]	B9h
REG[175Ah]	BAh
REG[175Ch]	C2h
REG[175Eh]	C3h
REG[1760h]	C4h
REG[1762h]	C5h
REG[1764h]	C6h
REG[1766h]	C7h
REG[1768h]	C8h
REG[176Ah]	C9h
REG[176Ch]	CAh
REG[176Eh]	D2h
REG[1770h]	D3h
REG[1772h]	D4h
REG[1774h]	D5h
REG[1776h]	D6h
REG[1778h]	D7h
REG[177Ah]	D8h
REG[177Ch]	D9h
REG[177Eh]	DAh
REG[1780h]	E2h
REG[1782h]	E3h
REG[1784h]	E4h
REG[1786h]	E5h
REG[1788h]	E6h
REG[178Ah]	E7h
REG[178Ch]	E8h
REG[178Eh]	E9h
REG[1790h]	EAh
REG[1792h]	F2h
REG[1794h]	F3h
REG[1796h]	F4h
REG[1798h]	F5h
REG[179Ah]	F6h
REG[179Ch]	F7h
REG[179Eh]	F8h
REG[17A0h]	F9h
REG[17A2h]	FAh

10.4.20 SD Memory Card Interface Registers

REG[6000h] SD Memory Card Configuration Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							Reserved
7	6	5	4	3	2	1	0
n/a				SD Memory Card Software Reset (WO)	Reserved		SD Memory Card Interface Enable

bit 8 Reserved
The default value for this bit is 0.

bit 3 SD Memory Card Software Reset (Write Only)
This bit performs a software reset of the SD Memory Card interface and resets REG[6100h] - REG[613Eh].
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, a software reset is performed.

bits 2-1 Reserved
The default value for these bits is 0.

bit 0 SD Memory Card Interface Enable
This bit enables the SD Memory Card interface. When the interface is disabled, REG[6100h] - REG[613Eh] are inaccessible.
When this bit = 0, the SD Memory Card interface is disabled (default).
When this bit = 1, the SD Memory Card interface is enabled.

Note
When the SD Memory Card Interface is not used (REG[6000h] bit 0 = 0), the SDCARD pins must be left unconnected and the pulldown resistance must be enabled (REG[6002h] bit bits 7-0 = 1) to avoid unnecessary current draw. If the SD Memory Card Interface interface is used (REG[6000h] bit 0 = 1), the pulldown resistance must be disabled (REG[6002h] bit bits 7-0 = 0) immediately to avoid unnecessary current draw.

REG[6002h] SD Memory Card Configuration Register 1
Default = 00FFh Read/Write

n/a							
15	14	13	12	11	10	9	8
SDDAT3 Pull-down Control	SDDAT2 Pull-down Control	SDDAT1 Pull-down Control	SDDAT0 Pull-down Control	SDCMD Pull-down Control	SDCLK Pull-down Control	SDWP Pull-down Control	SDCD# Pull-down Control
7	6	5	4	3	2	1	0

bit 7 SDDAT3 Pull-down Control

This bit controls the pull-down resistance for the SDDAT3 pin.
When this bit = 0, the pull-down resistance is disabled.
When this bit = 1, the pull-down resistance is enabled (default).

Note

When the SD Memory Card Interface is not used (REG[6000h] bit 0 = 0), the SDCARD pins must be left unconnected and the pulldown resistance must be enabled (REG[6002h] bit bits 7-0 = 1) to avoid unnecessary current draw. If the SD Memory Card Interface interface is used (REG[6000h] bit 0 = 1), the pulldown resistance must be disabled (REG[6002h] bit bits 7-0 = 0) immediately to avoid unnecessary current draw.

bit 6 SDDAT2 Pull-down Control

This bit controls the pull-down resistance for the SDDAT2 pin.
When this bit = 0, the pull-down resistance is disabled.
When this bit = 1, the pull-down resistance is enabled (default).

Note

When the SD Memory Card Interface is not used (REG[6000h] bit 0 = 0), the SDCARD pins must be left unconnected and the pulldown resistance must be enabled (REG[6002h] bit bits 7-0 = 1) to avoid unnecessary current draw. If the SD Memory Card Interface interface is used (REG[6000h] bit 0 = 1), the pulldown resistance must be disabled (REG[6002h] bit bits 7-0 = 0) immediately to avoid unnecessary current draw.

bit 5 SDDAT1 Pull-down Control

This bit controls the pull-down resistance for the SDDAT1 pin.
When this bit = 0, the pull-down resistance is disabled.
When this bit = 1, the pull-down resistance is enabled (default).

Note

When the SD Memory Card Interface is not used (REG[6000h] bit 0 = 0), the SDCARD pins must be left unconnected and the pulldown resistance must be enabled (REG[6002h] bit bits 7-0 = 1) to avoid unnecessary current draw. If the SD Memory Card Interface interface is used (REG[6000h] bit 0 = 1), the pulldown resistance must be disabled (REG[6002h] bit bits 7-0 = 0) immediately to avoid unnecessary current draw.

bit 4 SDDAT0 Pull-down Control

This bit controls the pull-down resistance for the SDDAT0 pin.
When this bit = 0, the pull-down resistance is disabled.
When this bit = 1, the pull-down resistance is enabled (default).

Note

When the SD Memory Card Interface is not used (REG[6000h] bit 0 = 0), the SDCARD pins must be left unconnected and the pulldown resistance must be enabled (REG[6002h] bit bits 7-0 = 1) to avoid unnecessary current draw. If the SD Memory Card Interface interface is used (REG[6000h] bit 0 = 1), the pulldown resistance must be disabled (REG[6002h] bit bits 7-0 = 0) immediately to avoid unnecessary current draw.

bit 3 SDCMD Pull-down Control

This bit controls the pull-down resistance for the SDCMD pin.
When this bit = 0, the pull-down resistance is disabled.
When this bit = 1, the pull-down resistance is enabled (default).

Note

When the SD Memory Card Interface is not used (REG[6000h] bit 0 = 0), the SDCARD pins must be left unconnected and the pulldown resistance must be enabled (REG[6002h] bit bits 7-0 = 1) to avoid unnecessary current draw. If the SD Memory Card Interface interface is used (REG[6000h] bit 0 = 1), the pulldown resistance must be disabled (REG[6002h] bit bits 7-0 = 0) immediately to avoid unnecessary current draw.

bit 2 SDCLK Pull-down Control

This bit controls the pull-down resistance for the SDCLK pin.
When this bit = 0, the pull-down resistance is disabled.
When this bit = 1, the pull-down resistance is enabled (default).

Note

When the SD Memory Card Interface is not used (REG[6000h] bit 0 = 0), the SDCARD pins must be left unconnected and the pulldown resistance must be enabled (REG[6002h] bit bits 7-0 = 1) to avoid unnecessary current draw. If the SD Memory Card Interface interface is used (REG[6000h] bit 0 = 1), the pulldown resistance must be disabled (REG[6002h] bit bits 7-0 = 0) immediately to avoid unnecessary current draw.

bit 1 SDWP Pull-down Control

This bit controls the pull-down resistance for the SDWP pin.
When this bit = 0, the pull-down resistance is disabled.
When this bit = 1, the pull-down resistance is enabled (default).

Note

When the SD Memory Card Interface is not used (REG[6000h] bit 0 = 0), the SDCARD pins must be left unconnected and the pulldown resistance must be enabled (REG[6002h] bit bits 7-0 = 1) to avoid unnecessary current draw. If the SD Memory Card Interface interface is used (REG[6000h] bit 0 = 1), the pulldown resistance must be disabled (REG[6002h] bit bits 7-0 = 0) immediately to avoid unnecessary current draw.

bit 0 SDCD# Pull-down Control
This bit controls the pull-down resistance for the SDCD# pin.
When this bit = 0, the pull-down resistance is disabled.
When this bit = 1, the pull-down resistance is enabled (default).

Note
When the SD Memory Card Interface is not used (REG[6000h] bit 0 = 0), the SDCARD pins must be left unconnected and the pulldown resistance must be enabled (REG[6002h] bit bits 7-0 = 1) to avoid unnecessary current draw. If the SD Memory Card Interface interface is used (REG[6000h] bit 0 = 1), the pulldown resistance must be disabled (REG[6002h] bit bits 7-0 = 0) immediately to avoid unnecessary current draw.

REG[6004h] SD Memory Card Configuration Register 2
Default = xxxxh Read/Write

n/a							
15	14	13	12	11	10	9	8
SDDAT3 Status	SDDAT2 Status	SDDAT1 Status	SDDAT0 Status	SDCMD Status	SDCLK Status	SDWP Status (RO)	SDCD# Status (RO)
7	6	5	4	3	2	1	0

bit 7 SDDAT3 Status
When SDDAT3 is an input, this bit indicates the status of SDDAT3.
For Reads:
When this bit returns a 0, SDDAT3 input is low.
When this bit returns a 1, SDDAT3 input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 6 SDDAT2 Status
When SDDAT2 is an input, this bit indicates the status of SDDAT2.
For Reads:
When this bit returns a 0, SDDAT2 input is low.
When this bit returns a 1, SDDAT2 input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 5 SDDAT1 Status
When SDDAT1 is an input, this bit indicates the status of SDDAT1.
For Reads:
When this bit returns a 0, SDDAT1 input is low.
When this bit returns a 1, SDDAT1 input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 4 SDDAT0 Status
When SDDAT0 is an input, this bit indicates the status of SDDAT0.
For Reads:
When this bit returns a 0, SDDAT0 input is low.
When this bit returns a 1, SDDAT0 input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 3 SDCMD Status
When SDCMD is an input, this bit indicates the status of SDCMD.
For Reads:
When this bit returns a 0, SDCMD input is low.
When this bit returns a 1, SDCMD input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 2 SDCLK Status
When the SDCLK is an input, this bit indicates the status of SDCLK.
For Reads:
When this bit returns a 0, SDCLK input is low.
When this bit returns a 1, SDCLK input is high.
For Writes:
Writing to this bit has no hardware effect.

bit 1 SDWP Status (Read Only)
This bit indicates the status of SDWP.
When this bit returns a 0, SDWP input is low.
When this bit returns a 1, SDWP input is high.

bit 0 SDCD# Status (Read Only)
This bit indicates the status of SDCD#.
When this bit returns a 0, SDCD# input is low.
When this bit returns a 1, SDCD# input is high.

REG[6100h] SD Memory Card Control Register 0
Default = 0031h Read/Write

n/a							
15	14	13	12	11	10	9	8
SDCLK Divide Select bits 3-0				Reserved		SD Card Interrupt Enable	SD Card Interrupt Flag
7	6	5	4	3	2	1	0

bits 7-4 SDCLK Divide Select bits [3:0]

These bits select the divide ratio for the SD Memory Card clock (SDCLK signal). The clock source for the SD Memory Card clock is the system clock. When the divide ratio is changed, write a 1 to the SDCLK Change Start bit (REG[6104h] bit 7 = 1) and wait for the change to take effect (REG[6104h] bit 7 = 0) before using the SD Memory Clock interface.

Table 10-75: SD Memory Card Clock Divide Ratio Selection

REG[6100h] bits 7-4	SD Memory Card Clock Divide Ratio
0000b	Reserved
0001b	2:1 (see Note)
0010b	3:1 (see Note)
0011b (default)	4:1
0101b	62:1
0110b through 1000b	Reserved
1001b	130:1
1010b	131:1
1011b through 1101b	Reserved
1110b	255:1
1111b	256:1

Note

SD Memory Card Clock Divide Ratio must be configured such that the resulting SDCLK frequency does not exceed 13.75MHz (see Section 7.7.2, “SD Memory Card Clock Output” on page 105).

The following table provides some examples of typical SD Memory Card clock configurations.

Table 10-76: System Clock Frequency and SD Card Clock

System Clock Frequency	REG[6100h] bits 7-4	
	Identification Mode	Data Transfer Mode
~52MHz	**1010 (~396KHz)**	**0011 (~13MHz)**
~55MHz	**1110 (~215KHz)**	**0011 (~13.75MHz Max)**

bits 3-2 Reserved
The default value for these bits is 0.

bit 1 SD Card Interrupt Enable
This bit controls the SD Memory Card Interrupt (SDCD#) and masks the SD Card Interrupt Status bit (REG[0A00h] bit 7).
When this bit = 0, the interrupt is disabled (default).
When this bit = 1, the interrupt is enabled.

bit 0 SD Card Interrupt Flag
This bit indicates that a SD Card Interrupt has occurred (change in card detect, SDCD#).
This bit is not masked by the SD Card Interrupt Enable bit (REG[6100h] bit 1).
For Reads:
When this bit returns a 0, the interrupt has not occurred.
When this bit returns a 1, the interrupt has occurred (SDCD# signal has changed).
For Writes:
When a 0 is written to this bit, the flag is cleared.
When a 1 is written to this bit, there is no hardware effect.

Note
This bit is cleared on a SD card software reset (REG[6100h] bit 3 = 1).

REG[6102h] SD Memory Card Control Register 1
Default = 00x1h Read/Write

n/a							
15	14	13	12	11	10	9	8
SDWP Status (RO)	SDGPO Inverted Data	Reserved			Response Data Length	Multi Block Enable	Data Bus Width
7	6	5	4	3	2	1	0

bit 7 SDWP Status (Read Only)
This bit indicates the status of SDWP (write protect) which is sampled by the clock referred to in Table 10-75: “SD Memory Card Clock Divide Ratio Selection,” on page 266 and Table 10-76: “System Clock Frequency and SD Card Clock,” on page 266 under REG[6100h] bits 7-4.
When this bit returns a 0, SDWP is low input.
When this bit returns a 1, SDWP is high input.

bit 6 SDGPO Inverted Data
This bit determines the polarity of SDGPO.
When this bit = 0, SDGPO is forced high.
When this bit = 1, SDGPO is forced low (default).

bits 5-3 Reserved
The default value for these bits is 0.

bit 2 Response Data Length

This bit determines the length of the response from the memory card, in bits. This bit must be set for the appropriate length before initiating a Receive Response Start (REG[6104h] bit 5).
When this bit = 0, the response length is 48 bits (default) and SD Memory Card Response Registers A - F (REG[6134h] - REG[613Eh] are used.
When this bit = 1, the response length is 136 bits and SD Memory Card Response Registers 0 - F (REG[6120h] - REG[613Eh] are used.

bit 1 Multi Block Enable

This bit controls the multi block read/write function. This bit must be set for the appropriate multi block setting before initiating a Receive Data Start (REG[6104h] bit 3) or a Send Data Start (REG[6104h] bit 2).
When this bit = 0, multi block reads/writes are disabled (default).
When this bit = 1, multi block reads/writes are enabled.

bit 0 Data Bus Width

This bit specifies the SD Memory Card data bus width, in bits, and should be set according to the SD Card. This bit must be set appropriately before initiating a Receive Data Start (REG[6104h] bit 3) or a Send Data Start (REG[6104h] bit 2).
When this bit = 0, the data bus width is four bits and SDDAT[3:0] are used to transfer data.
When this bit = 1, the data bus width is one bit and SDDAT0 is used to transfer data (default).

REG[6104h] SD Memory Card Function Register
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
SDCLK Change Start	Send Command Start	Receive Response Start	Wait Busy Start	Receive Data Start	Send Data Start	Send 8 Clock Start	Synchronous Reset Start
7	6	5	4	3	2	1	0

bit 7 SDCLK Change Start

This bit controls changes to the SD Memory Card clock (SDCLK) frequency.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the change to the SD Memory Card clock frequency begins
For Reads:
When this bit returns a 0, the change to the SD Memory Card clock frequency has completed.
When this bit returns a 1, the change to the SD Memory Card clock frequency has not completed yet.

The typical sequence for changing the SD Memory Card clock is as follows.

1. Select the SDCLK Divide Ratio using REG[6100h] bits 7-4.
2. Write a 1 to the SDCLK Change Start bit.
3. Wait for the SDCLK Change Start bit to return a 0. Once this bit returns a 0, the change is effective and the interface can be enabled.

bit 6 Send Command Start
This bit controls the transmission of commands and parameters to the SD Memory Card.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the command/parameter stored in REG[610Ch], REG[6110h] - REG[6116h] is transmitted on SDCMD.
For Reads:
When this bit returns a 0, the command/parameter transmission has completed.
When this bit returns a 1, the command/parameter is still being transmitted.

bit 5 Receive Response Start
This bit controls the reception of responses from the SD Memory Card. The Response Data Length bit (REG[6102h] bit 2) must be set according to the expected response length before starting to receive the response using this bit.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the response reception begins on SDCMD and can be read from REG[6120h] - REG[613Eh].
For Reads:
When this bit returns a 0, the response reception has completed.
When this bit returns a 1, the response reception is still being received.

bit 4 Wait Busy Start
This bit controls the reception of wait busy signals from the SD Memory Card.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the wait busy reception begins.
For Reads:
When this bit returns a 0, the wait busy reception has completed.
When this bit returns a 1, the wait busy reception is still being received.

bit 3 Receive Data Start
This bit controls the reception of data from the SD Memory Card. The Response Data Length bit (REG[6102h] bit 2) and the Multi Block Enable bit (REG[6102h] bit 1) must be set according to the expected response type before starting to receive the response.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the data reception begins on the SDDAT lines and is read from REG[6118h] - REG[611Eh].
For Reads:
When this bit returns a 0, the data reception has completed.
When this bit returns a 1, the data reception is still being received.

bit 2 Send Data Start

This bit controls the transmission of data to the SD Memory card. The Multi Block Enable bit (REG[6102h] bit 1) must be set according to the type of data to be sent before starting to transmit the data.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the data written to REG[6110h] - REG[6116] is transmitted on the SDDAT lines.
For Reads:
When this bit returns a 0, the data transmission has completed.
When this bit returns a 1, the data transmission is still being sent.

bit 1 Send 8 Clock Start

This bit controls the transmission of eight clocks to the SD Memory Card.
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the transmission begins.
For Reads:
When this bit returns a 0, the transmission has completed.
When this bit returns a 1, the eight clocks are still being transmitted.

bit 0 Synchronous Reset Start

This bit performs a synchronous reset of the SD Memory Card interface. This reset has no effect on the following SD Memory Card registers (REG[6100h] - REG[6102h] and REG[6108h] - REG[613Eh]).
For Writes:
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, a synchronous reset begins.
For Reads:
When this bit returns a 0, the synchronous reset has completed.
When this bit returns a 1, the synchronous reset is still taking place.

REG[6106h] SD Memory Card Status Register
Default = 00x0h Read Only

n/a							
15	14	13	12	11	10	9	8
Reserved	SDCD# Status	Data Writable	Data Readable	Data CRC Error	Response Over Error	Response CRC Error	Time Over Error
7	6	5	4	3	2	1	0

Note
This register is read only and must not be written to at any time.

bit 7 Reserved

The default value for this bit is 0.

bit 6 SDCD# Status (Read Only)
This bit indicates the status of the SDCD# pin as taken with the sampling clock referred to in Table 10-75: “SD Memory Card Clock Divide Ratio Selection,” on page 266 and Table 10-76: “System Clock Frequency and SD Card Clock,” on page 266 under REG[6100h] bits 7-4.
When this bit returns a 0, SDCD# is low input.
When this bit returns a 1, SDCD# is high input.

bit 5 Data Writable (Read Only)
This bit indicates whether data can be written to the SD Memory Card.
When this bit returns a 0, writing data is not possible.
When this bit returns a 1, writing data is possible.

bit 4 Data Readable (Read Only)
This bit indicates whether data can be read from the SD Memory Card.
When this bit returns a 0, reading data is not possible.
When this bit returns a 1, reading data is possible.

bit 3 Data CRC Error (Read Only)
This bit indicates when a data CRC error has occurred.
When this bit returns a 0, a CRC error has not occurred.
When this bit returns a 1, a CRC error has occurred.

bit 2 Response Over Error (Read Only)
This bit indicates that the response from the SD Memory Card has exceeded more than 64 clocks.
When this bit returns a 0, the response is not more than 64 clocks.
When this bit returns a 1, the response is more than 64 clocks.

bit 1 Response CRC Error (Read Only)
This bit indicates that a CRC error has occurred in the response from the SD Memory Card.
When this bit returns a 0, a CRC error has not occurred.
When this bit returns a 1, a CRC error has occurred.

bit 0 Time Over Error (Read Only)
This bit indicates that a Time Over Error has occurred during data transmission.
When this bit returns a 0, a time over error has not occurred.
When this bit returns a 1, a time over error has occurred.

REG[6108h] SD Memory Card Data Length Register 0
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Reserved						Data Length bits 9-8	
7	6	5	4	3	2	1	0

REG[610Ah] SD Memory Card Data Length Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Data Length bits 7-0							
7	6	5	4	3	2	1	0

REG[6108h] bits 7-2 Reserved
The default value for these bits is 0.

REG[6108h] bits 1-0
REG[610Ah] bits 7-0 Data Length bits [9:0]
These bits specify the SD Memory Card data length.

The data length must be programmed such that the following formula is valid.
$1 \leq$ Data Length ≤ 512

REG[610Ch] SD Memory Card Command Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Reserved		Command bits 5-0					
7	6	5	4	3	2	1	0

bits 7-6 Reserved
The default value of these bits is 0.

bits 5-0 Command bits [5:0]
These bits specify the command to be transmitted to the SDCMD signal when data is transmitted.

REG[610Eh] SD Memory Card Timer Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Timer Value bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Timer Value bits [7:0]
These bits specify the timer value used to limit the length of data and command accesses to/from the SD Memory Card. An error occurs when the timer value is exceeded by any SD Memory Card access. To determine the nature of the error, check the status bits in the SD Memory Card Status register (REG[6106h].

Timer limit = REG[610Eh] bits 7-0 x SD Memory Card clock cycle (time)

REG[6110h] SD Memory Card Parameter Register 0
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Parameter 0 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Parameter 0 bits [7:0]
These bits specify Parameter 0 which is used when data is transmitted to the SDCMD signal. Data is transmitted as follows: Command, Parameter 0, Parameter 1, Parameter 2, and Parameter 3.

REG[6112h] SD Memory Card Parameter Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Parameter 1 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Parameter 1 bits [7:0]
These bits specify Parameter 1 which is used when data is transmitted to the SDCMD signal. Data is transmitted as follows: Command, Parameter 0, Parameter 1, Parameter 2, and Parameter 3.

REG[6114h] SD Memory Card Parameter Register 2
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Parameter 2 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Parameter 2 bits [7:0]
These bits specify Parameter 2 which is used when data is transmitted to the SDCMD signal. Data is transmitted as follows: Command, Parameter 0, Parameter 1, Parameter 2, and Parameter 3.

REG[6116h] SD Memory Card Parameter Register 3
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Parameter 3 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Parameter 3 bits [7:0]
These bits specify Parameter 3 which is used when data is transmitted to the SDCMD signal. Data is transmitted as follows: Command, Parameter 0, Parameter 1, Parameter 2, and Parameter 3.

REG[6118h~611Eh] SD Memory Card Data Register
Default = 00xxh Read/Write

n/a							
15	14	13	12	11	10	9	8
Write Data / Read Data							
7	6	5	4	3	2	1	0

REG[6118h] bits 7-0
REG[611Ah] bits 7-0
REG[611Ch] bits 7-0
REG[611Eh] bits 7-0

Write Data / Read Data
These bits specify the read/write data to be received from/transmitted to the SD Memory Card. When the Data Writable bit returns a 0 (REG[6106h] bit 5 = 0), writing data to the SD Memory Card is not possible. When the Data Readable bit returns a 0 (REG[6106h] bit 4 = 0), reading data from the SD Memory Card is not possible.

Note
These registers are Write Only unless data has been received from the SDCARD.

REG[6120h] SD Memory Card Response Register 0
Default = 00FFh Read Only

n/a							
15	14	13	12	11	10	9	8
Response 0 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 0 bits [7:0]
These bits contain the Response 0 data received from the SD Memory Card at the SDCMD signal.

REG[6122h] SD Memory Card Response Register 1
Default = 00FFh Read Only

n/a							
15	14	13	12	11	10	9	8
Response 1 bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response 1 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 1 data received from the SD Memory Card at the SDCMD signal.

REG[6124h] SD Memory Card Response Register 2
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response 2 bits 7-0							

bits 7-0 Response 2 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 2 data received from the SD Memory Card at the SDCMD signal.

REG[6126h] SD Memory Card Response Register 3
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response 3 bits 7-0							

bits 7-0 Response 3 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 3 data received from the SD Memory Card at the SDCMD signal.

REG[6128h] SD Memory Card Response Register 4
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response 4 bits 7-0							

bits 7-0 Response 4 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 4 data received from the SD Memory Card at the SDCMD signal.

REG[612Ah] SD Memory Card Response Register 5
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response 5 bits 7-0							

bits 7-0 Response 5 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 5 data received from the SD Memory Card at the SDCMD signal.

REG[612Ch] SD Memory Card Response Register 6
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response 6 bits 7-0							

bits 7-0 Response 6 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 6 data received from the SD Memory Card at the SDCMD signal.

REG[612Eh] SD Memory Card Response Register 7
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response 7 bits 7-0							

bits 7-0 Response 7 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 7 data received from the SD Memory Card at the SDCMD signal.

REG[6130h] SD Memory Card Response Register 8
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response 8 bits 7-0							

bits 7-0 Response 8 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 8 data received from the SD Memory Card at the SDCMD signal.

REG[6132h] SD Memory Card Response Register 9
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response 9 bits 7-0							

bits 7-0 Response 9 bits [7:0]
These bits are used only when the Response Data Length is 136 bits (REG[6102h] bit 2 = 1). These bits contain the Response 9 data received from the SD Memory Card at the SDCMD signal.

REG[6134h] SD Memory Card Response Register A
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response A bits 7-0							

bits 7-0 Response A bits [7:0]
These bits contain the Response A data received from the SD Memory Card at the SDCMD signal.

REG[6136h] SD Memory Card Response Register B
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response B bits 7-0							

bits 7-0 Response B bits [7:0]
These bits contain the Response B data received from the SD Memory Card at the SDCMD signal.

REG[6138h] SD Memory Card Response Register C
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response C bits 7-0							

its 7-0 Response C bits [7:0]
These bits contain the Response C data received from the SD Memory Card at the SDCMD signal.

REG[613Ah] SD Memory Card Response Register D
Default = 00FFh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Response D bits 7-0							

bits 7-0 Response D bits [7:0]
These bits contain the Response D data received from the SD Memory Card at the SDCMD signal.

REG[613Ch] SD Memory Card Response Register E
Default = 00FFh — Read Only

n/a							
15	14	13	12	11	10	9	8
Response E bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response E bits [7:0]
These bits contain the Response E data received from the SD Memory Card at the SDCMD signal.

REG[613Eh] SD Memory Card Response Register F
Default = 00FFh — Read Only

n/a							
15	14	13	12	11	10	9	8
Response F bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Response F bits [7:0]
These bits contain the Response F data received from the SD Memory Card at the SDCMD signal.

10.4.21 2D BitBLT Registers

REG[8000h] BitBLT Control Register 0
Default = 0000h — Write Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
BitBLT Reset	n/a						BitBLT Enable

bit 7 BitBLT Reset (Write Only)
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the 2D BitBLT engine is reset.

bit 0 BitBLT Enable (Write Only)
When a 0 is written to this bit, the 2D BitBLT operation is terminated.
When a 1 is written to this bit, the 2D BitBLT operation is started.

REG[8002h] BitBLT Control Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
n/a					Color Format Select	Dest Linear Select	Source Linear Select

bits 15-8 Reserved
The default value for these bits is 0.

bit 2 BitBLT Color Format Select
This bit selects the color format that the 2D operation is applied to.
When this bit = 0, 8 bpp (256 color) format is selected.
When this bit = 1, 16 bpp (64K color) format is selected.

bit 1 BitBLT Destination Linear Select
When this bit = 0, the Destination BitBLT is stored as a rectangular region of memory. The BitBLT Memory Address Offset register (REG[8014h]) determines the address offset from the start of one line to the next line.
When this bit = 1, the Destination BitBLT is stored as a contiguous linear block of memory.

bit 0 BitBLT Source Linear Select
When this bit = 0, the Source BitBLT is stored as a rectangular region of memory. The BitBLT Memory Address Offset register (REG[8014h]) determines the address offset from the start of one line to the next line.
When this bit = 1, the Source BitBLT is stored as a contiguous linear block of memory.

REG[8004h] BitBLT Status Register 0
Default = 0000h — Read Only

n/a			Reserved				
15	14	13	12	11	10	9	8
Reserved	FIFO Not Empty	FIFO Half Full	FIFO Full Status	n/a			BitBLT Busy Status
7	6	5	4	3	2	1	0

bits 12-7 Reserved
The default value for these bits is 0.

bit 6 BitBLT FIFO Not-Empty Status (Read Only)
This bit indicates if the BitBLT FIFO is empty or not.
When this bit = 0, the BitBLT FIFO is empty.
When this bit = 1, the BitBLT FIFO has at least one entry.
To reduce system memory read latency, software can monitor this bit prior to a BitBLT read burst operation.

The following table shows the number of words available in the BitBLT FIFO under different status conditions.

Table 10-77: Possible BitBLT FIFO Writes

BitBLT Status Register (REG[8004h])			Word Writes Available
FIFO Not Empty Status	FIFO Half Full Status	FIFO Full Status	
0	0	0	16
1	0	0	8
1	1	0	up to 8
1	1	1	0 (do not write)

bit 5 BitBLT FIFO Half Full Status (Read Only)
This bit indicates whether the BitBLT FIFO is more or less than half full.
When this bit = 0, the BitBLT FIFO is less than half full.
When this bit = 1, the BitBLT FIFO is half full or greater than half full.

bit 4 BitBLT FIFO Full Status (Read Only)
This bit indicates whether the BitBLT FIFO is full or not. **This bit must be confirmed as not full (0) before writing to the BitBLT FIFO.**
When this bit = 0, the BitBLT FIFO is not full.
When this bit = 1, the BitBLT FIFO is full.

bit 0 BitBLT Busy Status (Read Only)
This bit indicates the state of the current BitBLT operation.
When this bit = 0, the BitBLT operation is complete.
When this bit = 1, the BitBLT operation is in progress.

REG[8006h] is Reserved

This register is Reserved and should not be written.

REG[8008h] BitBLT Command Register 0
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				BitBLT Operation bits 3-0			
7	6	5	4	3	2	1	0

bits 3-0 BitBLT Operation bits [3:0]
These bits specify the 2D Operation to be performed.

Table 10-78: BitBLT Operation Selection

BitBLT Operation bits [3:0]	BitBLT Operation
0000b	Reserved
0001b	Read BitBLT
0010b	Move BitBLT in positive direction with ROP
0011b	Move BitBLT in negative direction with ROP
0100b	Reserved
0101b	Transparent Move BitBLT in positive direction
0110b	Pattern Fill with ROP
0111b	Pattern Fill with transparency
1000b	Reserved
1001b	Reserved
1010b	Move BitBLT with Color Expansion
1011b	Move BitBLT with Color Expansion and transparency
1100b	Solid Fill
Other combinations	Reserved

REG[800Ah] BitBLT Command Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a				BitBLT ROP Code bits 3-0			

bits 3-0 BitBLT Raster Operation Code/Color Expansion bits [3:0]
These bits determine the ROP Code for Write BitBLT and Move BitBLT. Bits 2-0 also specify the start bit position for Color Expansion.

Table 10-79: BitBLT ROP Code/Color Expansion Function Selection

BitBLT ROP Code bits [3:0]	Boolean Function for Write BitBLT and Move BitBLT	Boolean Function for Pattern Fill	Start Bit Position for Color Expansion
0000b	0 (Blackness)	0 (Blackness)	bit 0
0001b	~S . ~D or ~(S + D)	~P . ~D or ~(P + D)	bit 1
0010b	~S . D	~P . D	bit 2
0011b	~S	~P	bit 3
0100b	S . ~D	P . ~D	bit 4
0101b	~D	~D	bit 5
0110b	S ^ D	P ^ D	bit 6
0111b	~S + ~D or ~(S . D)	~P + ~D or ~(P . D)	bit 7
1000b	S . D	P . D	bit 0
1001b	~(S ^ D)	~(P ^ D)	bit 1
1010b	D	D	bit 2
1011b	~S + D	~P + D	bit 3
1100b	S	P	bit 4
1101b	S + ~D	P + ~D	bit 5
1110b	S + D	P + D	bit 6
1111b	1 (Whiteness)	1 (Whiteness)	bit 7

Note
S = Source, D = Destination, P = Pattern.

REG[800Ch] BitBLT Source Start Address Register 0
Default = 0000h — Read/Write

BitBLT Source Start Address bits 15-8							
15	14	13	12	11	10	9	8
BitBLT Source Start Address bits 7-0							
7	6	5	4	3	2	1	0

REG[800Eh] BitBLT Source Start Address Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
			Reserved		BitBLT Source Start Address bits 18-16		
7	6	5	4	3	2	1	0

REG[800Eh] bits 2-0
REG[800Ch] bits 15-0 BitBLT Source Start Address bits [18:0]
These bits specify the source start address for the BitBLT operation.
If data is sourced from the CPU, then bit 0 is used for byte alignment within a 16-bit word and the other address bits are ignored. In pattern fill operation, the BitBLT Source Start Address is defined by the following equation.

Value programmed to the Source Start Address Register =
Pattern Base Address + Pattern Line Offset + Pixel Offset.

The following table shows how Source Start Address Register is defined for 8 and 16 bpp color depths.

Table 10-80: BitBLT Source Start Address Selection

Color Format	Pattern Base Address[18:0]	Pattern Line Offset[2:0]	Pixel Offset[3:0]
8 bpp	BitBLT Source Start Address[18:6]	BitBLT Source Start Address[5:3]	BitBLT Source Start Address[2:0]
16 bpp	BitBLT Source Start Address[18:7]	BitBLT Source Start Address[6:4]	BitBLT Source Start Address[3:0]

REG[800Eh] bits 4-3 Reserved
The default value for these bits is 0.

REG[8010h] BitBLT Destination Start Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
BitBLT Destination Start Address bits 15-8							
7	6	5	4	3	2	1	0
BitBLT Destination Start Address bits 7-0							

REG[8012h] BitBLT Destination Start Address Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a			Reserved		BitBLT Destination Start Address bits 18-16		

REG[8012h] bits 4-0
REG[8010h] bits 15-0 BitBLT Destination Start Address bits [18:0]
These bits specify the destination start address for the BitBLT operation.

REG[8012h] bits 4-3 Reserved
The default value for these bits is 0.

REG[8014h] BitBLT Memory Address Offset Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a					BitBLT Memory Address Offset bits 10-8		
7	6	5	4	3	2	1	0
BitBLT Memory Address Offset bits 7-0							

bits 10-0 BitBLT Memory Address Offset bits [10:0]
These bits are the display's 11-bit address offset from the starting word of line *n* to the starting word of line *n + 1*. They are used only for address calculation when the BitBLT is configured as a rectangular region of memory. They are not used for the displays.

REG[8018h] BitBLT Width Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						BitBLT Width bits 9-8	
7	6	5	4	3	2	1	0
BitBLT Width bits 7-0							

bits 9-0 BitBLT Width bits [9:0]
These bits determine the BitBLT width in pixels.
BitBLT width in pixels = (REG[8018h] bits 9-0) + 1

REG[801Ch] BitBLT Height Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						BitBLT Height bits 9-8	
7	6	5	4	3	2	1	0
BitBLT Height bits 7-0							

bits 9-0 BitBLT Height bits [9:0]
These bits determine the BitBLT height in lines.
BitBLT height in lines = (REG[801Ch] bits 9-0) + 1

REG[8020h] BitBLT Background Color Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
BitBLT Background Color bits 15-8							
7	6	5	4	3	2	1	0
BitBLT Background Color bits 7-0							

bits 15-0 BitBLT Background Color bits [15:0]
These bits specify the BitBLT background color for Color Expansion or key color for Transparent BitBLT. For 16 bpp color depths (REG[8000h] bit 18 = 1), bits 15-0 are used. For 8 bpp color depths (REG[8000h] bit 18 = 0), bits 7-0 are used.

REG[8024h] BitBLT Foreground Color Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
BitBLT Foreground Color bits 15-8							
7	6	5	4	3	2	1	0
BitBLT Foreground Color bits 7-0							

bits 15-0 BitBLT Foreground Color bits [15:0]
These bits specify the BitBLT foreground color for Color Expansion or Solid Fill. For 16 bpp color depths (REG[8000h] bit 18 = 1), bits 15-0 are used. For 8 bpp color depths (REG[8000h] bit 18 = 0), bits 7-0 are used.

REG[8030h] BitBLT Interrupt Status Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							BitBLT Operation Complete Flag

bit 0 BitBLT Operation Complete Flag
This bit is set when the BitBLT operation is finished. This bit is masked by REG[8032h] bit 0.
When a 0 is written to this bit, there is no hardware effect.
When a 1 is written to this bit, the flag is cleared.

REG[8032h] BitBLT Interrupt Control Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							BitBLT Operation Complete Interrupt Enable

bit 0 BitBLT Operation Complete Interrupt Enable
This bit determines whether an interrupt is generated when the current BitBLT operation finishes.
When this bit = 0, the interrupt is disabled.
When this bit = 1, the interrupt is enabled.

REG[10000h] 2D BitBLT Data Memory Mapped Region Register
Default = not applicable Read/Write

15	14	13	12	11	10	9	8
BitBLT Data bits 15-8							
7	6	5	4	3	2	1	0
BitBLT Data bits 7-0							

bits 15-0 BitBLT Data bits [15:0]
This register specifies the BitBLT data when a Direct Interface is selected (CNF[4:2]). When an Indirect Interface is selected, BitBLT data must be specified using the Indirect Interface 2D BitBLT Data Read/Write Port register (REG[002Ah]).

11 Power Save Modes

11.1 Power-On/Power-Off Sequence

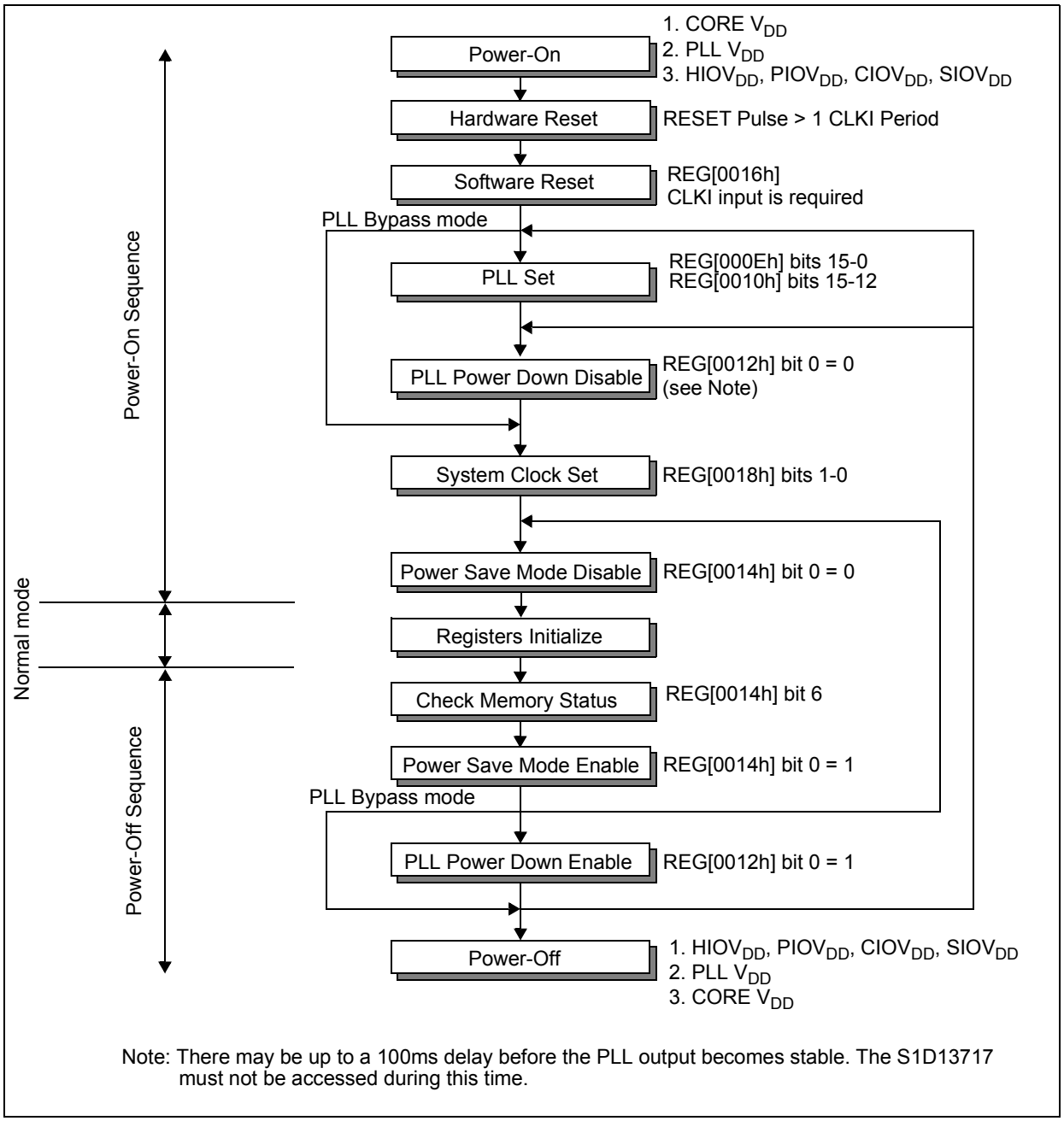


Figure 11-1: Power-On/Power-Off Sequence

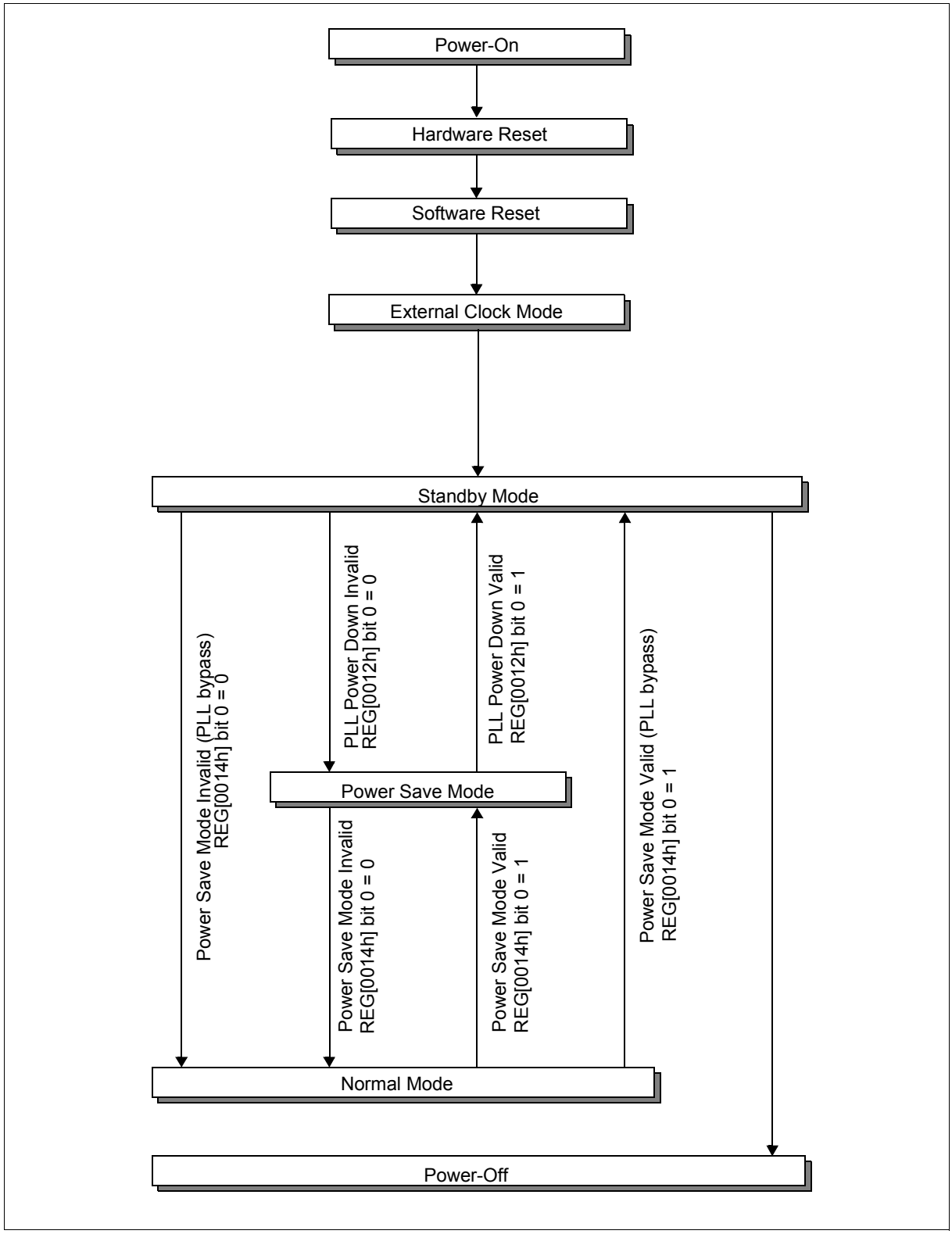


Figure 11-2: Power Modes

11.1.1 Power-On

When powering-on the S1D13717, the following sequence must be used unless all power is active within 10 ms.

1. $COREV_{DD}$ On
2. $PLLV_{DD}$ On
3. $HIOV_{DD}$, $PIOV_{DD}$, $SIOV_{DD}$, $CIOV_{DD}$ On

11.1.2 Reset

After power-on, an active low hardware reset pulse, which is one external clock cycle (CLKI) in length, must be input to the S1D13715 RESET# pin. All registers, including the Clock Setting registers (REG[000Eh]-[0018h]) are reset by a hardware reset. After releasing the RESET# signal, the Clock Setting registers are immediately accessible.

A software reset is enabled by writing to REG[0016h]. All registers above REG[0018h] are reset to the default values by a software reset (REG[0000h] - [0018h] are not reset). The following conditions apply to software reset.

- After initialization, and before the software reset (REG[0016h]), Power Save Mode should be enabled (REG[0014h] bit 0 = 1).
- After the software reset, Power Save Mode can be disabled (REG[0016h] bit 0 = 0) after waiting 100ms. All registers, synchronous and asynchronous, may now be accessed.

11.1.3 Standby Mode

Standby Mode offers the lowest power consumption because all internal clock supplies are stopped and the PLL is disabled. This mode must be entered before turning off the power supplies or setting the PLL registers.

In order to switch to the Standby Mode, a PLL power down should be executed (REG[0012h] bit 0 = 1). After power down, the CLKI input should be continued for a minimum 100us to allow the PLL power down to complete.

11.1.4 Power Save Mode

Power Save Mode stops all internal clock supplies. This mode must be entered before setting the System Clock Setting register (REG[0018h]). Also, there may be up to a 100ms delay before the PLL output becomes stable after it is enabled. The S1D1717 should be in Power Save Mode during this time.

11.1.5 Normal Mode

All functions are available in Normal Mode. However, clocks to modules that are not in use are dynamically stopped. Before enabling Power Save Mode (REG[0014] bit 0 = 1) from Normal Mode, confirm that the memory controller is idle (REG[0014h] bit 6 = 1).

11.1.6 Power-Off

When powering-off the S1D13717, the following sequence must be used.

1. $HIOV_{DD}$, $PIOV_{DD}$, $SIOV_{DD}$, $CIOV_{DD}$ Off
2. $PLLV_{DD}$ Off
3. $COREV_{DD}$ Off

11.2 Power Save Mode Function

Table 11-1: Power Save Mode Function Selection

Item		Reset State	Power Save Mode	Normal Mode
IO (Register) Access Possible?	REG[0000h-0018h], REG[0300h-030Eh]	Yes	Yes	Yes
	All other registers	No	No	Yes
Memory Access Possible?		No	No	Yes
Look-Up Table Registers Access Possible?		No	No	Yes
Display Active?		No	No	Yes
LCD1, LCD2 Interface Outputs and GPIO Pins configured for Panel Support	FPCS1#	Inactive	Inactive	Active
	All other pins	Forced Low	Forced Low	Active
GPIO Pins configured as GPIOs	CNF2 = 1	Input	GPIO State	GPIO State
	CNF2 = 0	Forced Low	GPO State	GPO State
Camera Interface Pins		Forced Low	Forced Low	Active
System Clock		Forced Low	Active	Active
Pixel Clock		Forced Low	Forced Low	Active
Serial Clock	For the LCD2 Serial Panel I/F setting (REG[0032h] bits 1-0 = 00b or 10b)	Inactive	Active	Active
	For all other settings	Forced Low	Forced Low	Active
Camera Clock		Forced Low	Forced Low	Active
JPEG Module	REG[0980] bit 0 = 0	Inactive	Inactive	Inactive
	REG[0980] bit 0 = 1	Inactive	Inactive	Active
BitBLT Module		Inactive	Inactive	Active
SD Card Interface	REG[6000] bit 0 = 0	Inactive	Inactive	Inactive
	REG[6000] bit 0 = 1	Inactive	Inactive	Active

12 LUT Architecture

12.1 LUT1 (Main Window) for 8 bpp

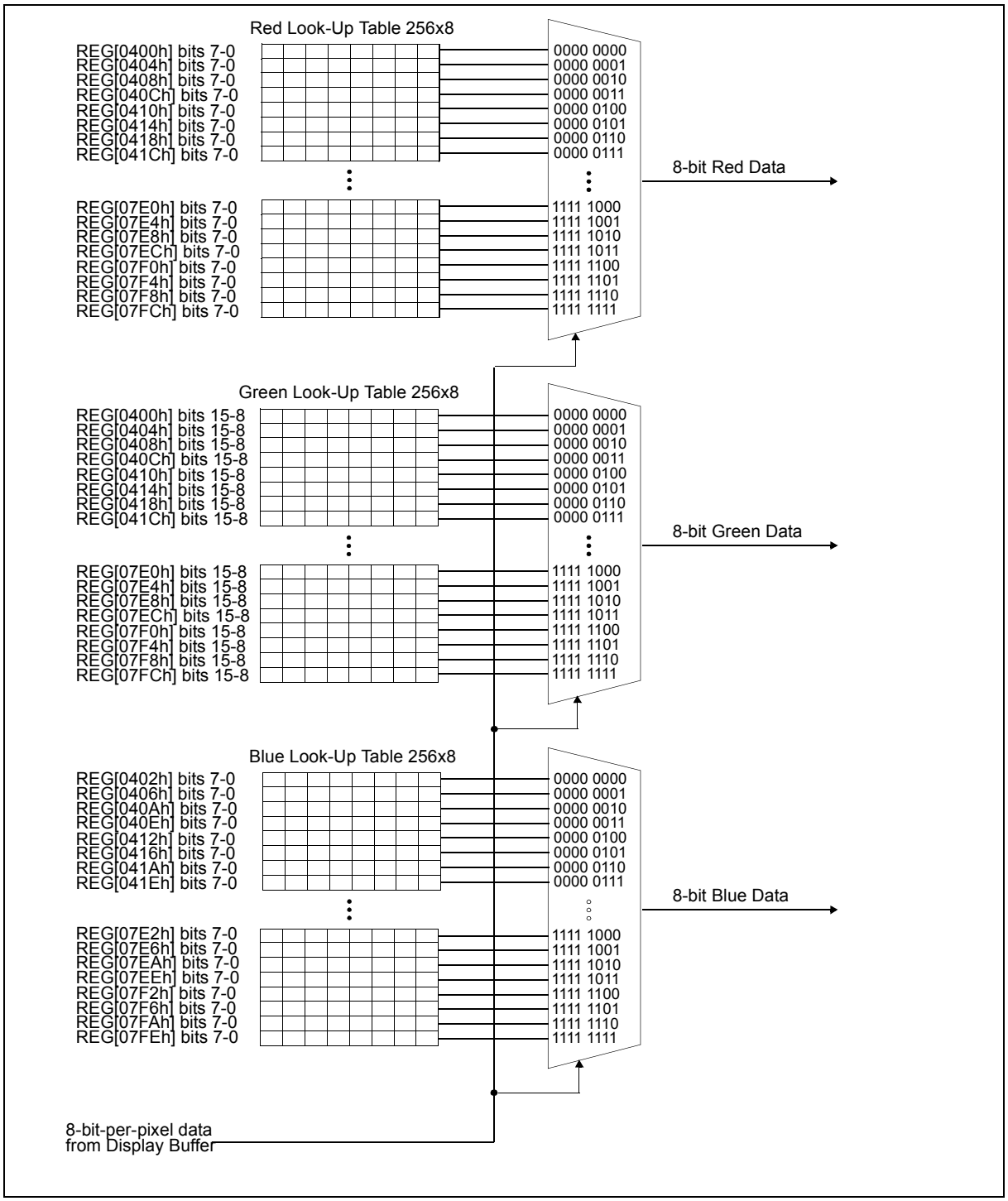


Figure 12-1: LUT1 (Main Window) for 8 Bpp Architecture

12.2 LUT2 (PIP+ Window) for 8 Bpp Architecture

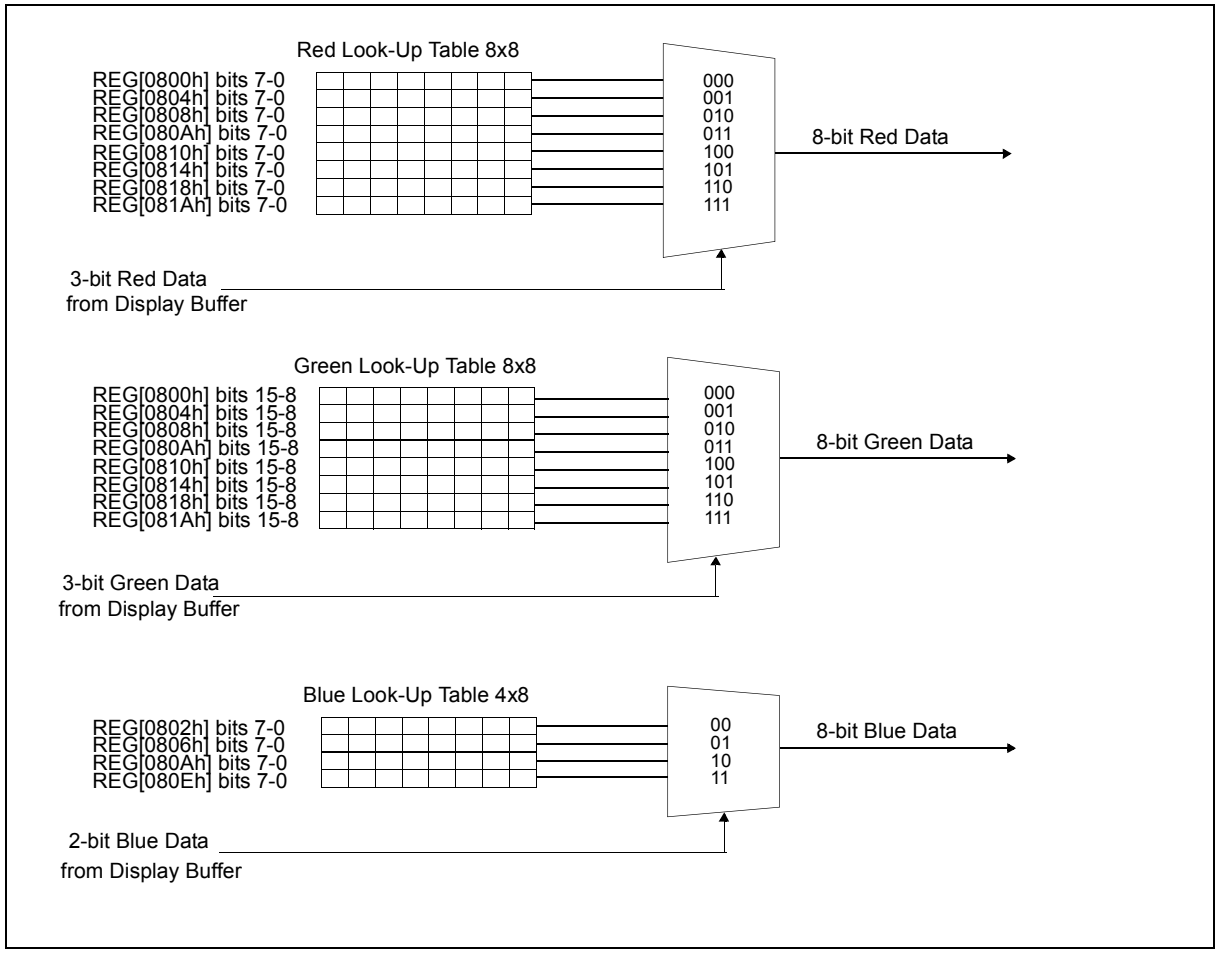


Figure 12-2: LUT2 (PIP+ Window) for 8 Bpp Architecture

12.3 LUT1 (Main Window) for 16 Bpp Architecture

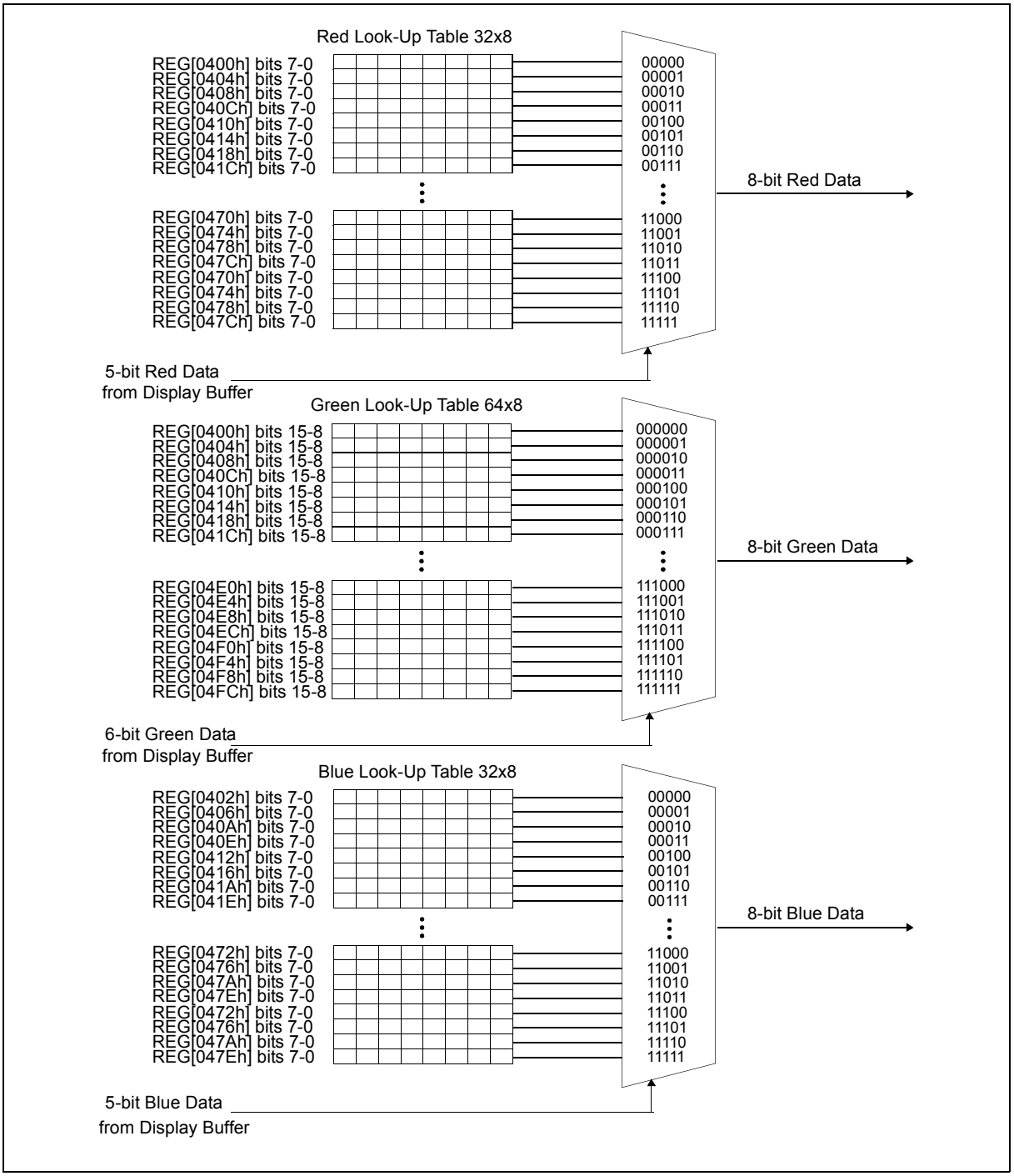


Figure 12-3: LUT1 (Main Window) for 16 Bpp Architecture

12.4 LUT2 (PIP+ Window) for 16 Bpp Architecture

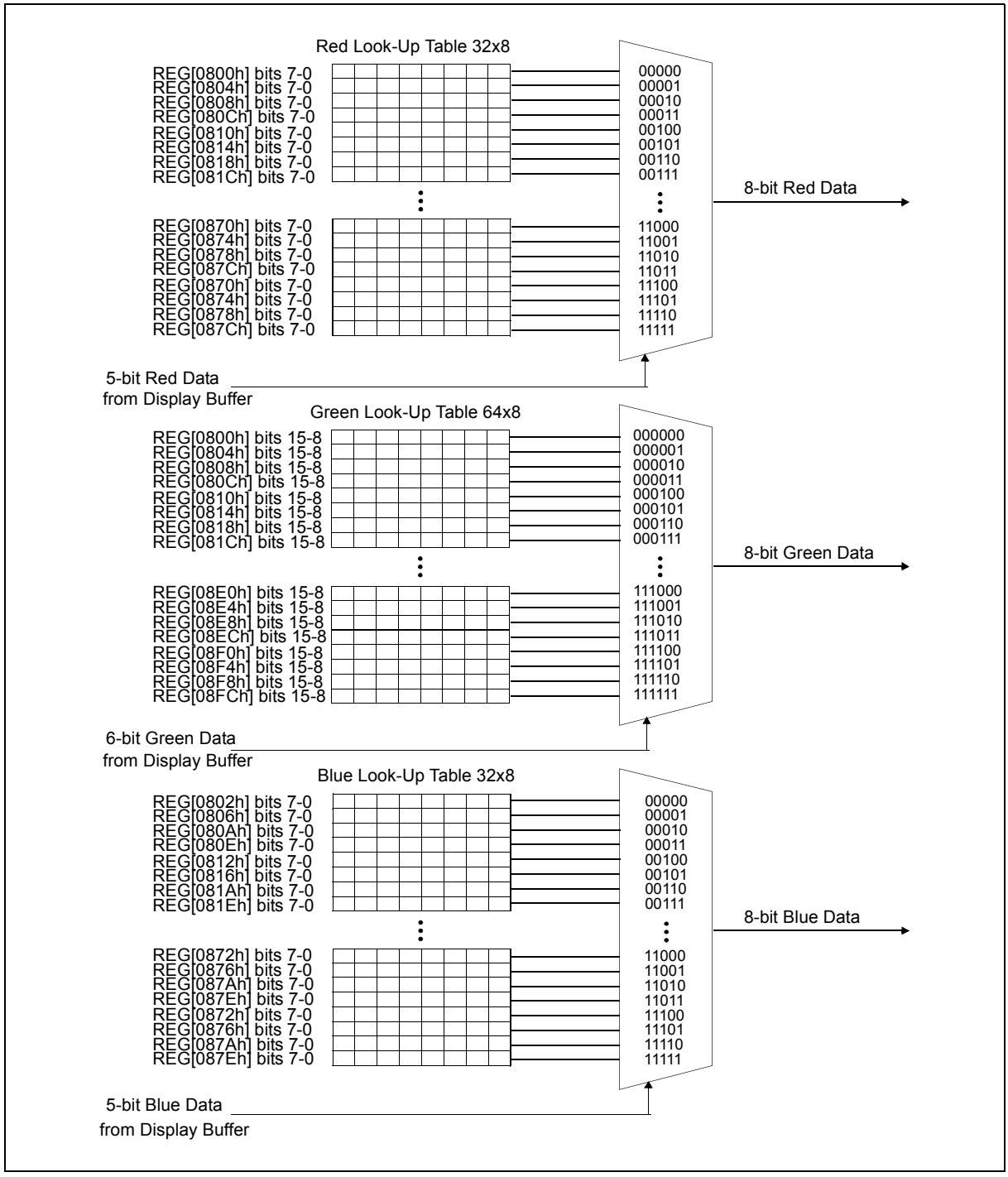


Figure 12-4: LUT2 (PIP+ Window) for 16 Bpp Architecture

13 Display Data Formats

13.1 Display Data for LUT Mode

13.1.1 8 Bpp Mode

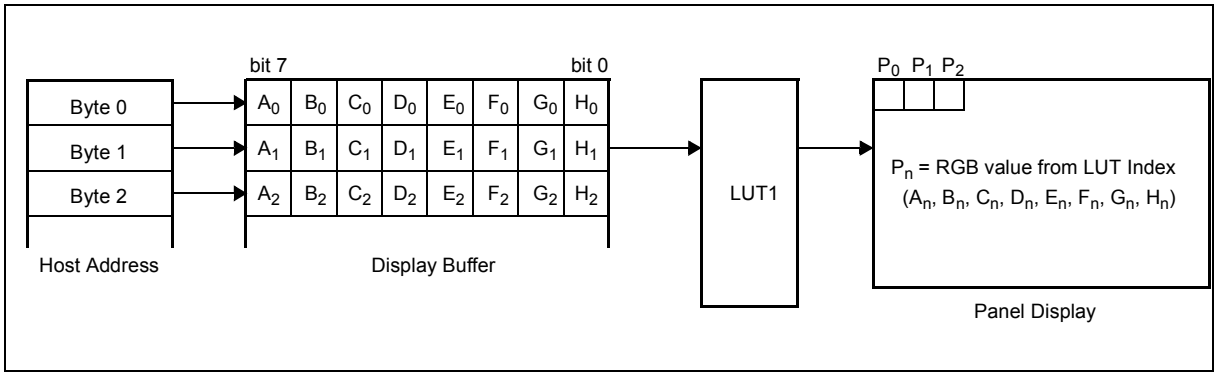


Figure 13-1: LUT1 for 8 Bpp Mode

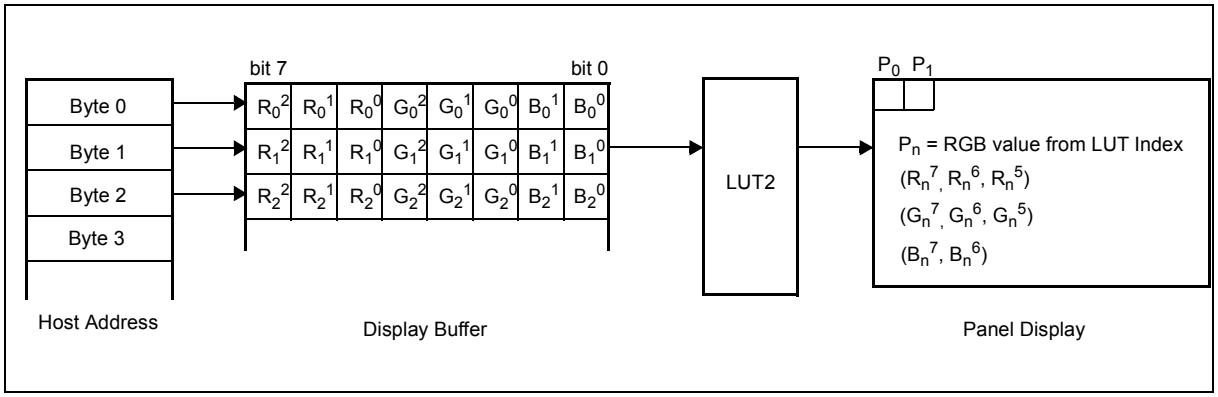


Figure 13-2: LUT2 for 8 Bpp Mode

13.1.2 16 Bpp Mode

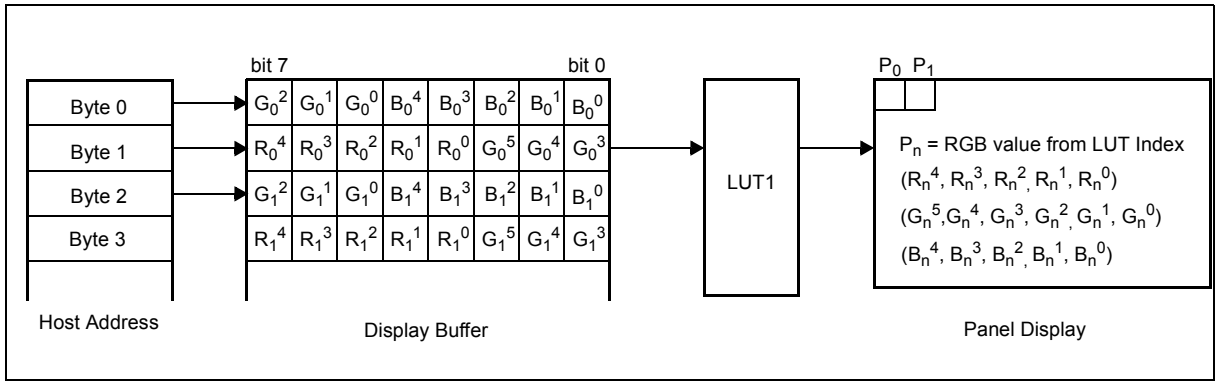


Figure 13-3: LUT1 for 16 Bpp Mode

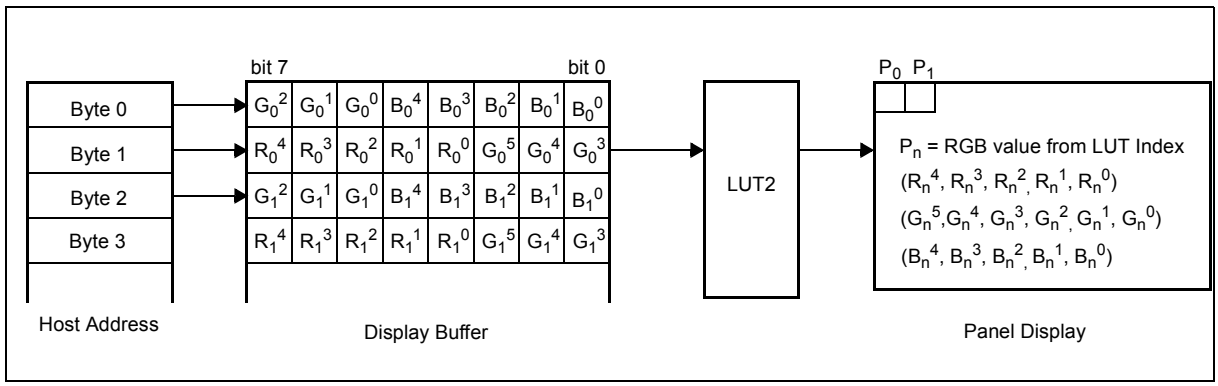


Figure 13-4: LUT2 for 16 Bpp Mode

13.2 Display Data for LUT Bypass Mode

13.2.1 8 Bpp Mode

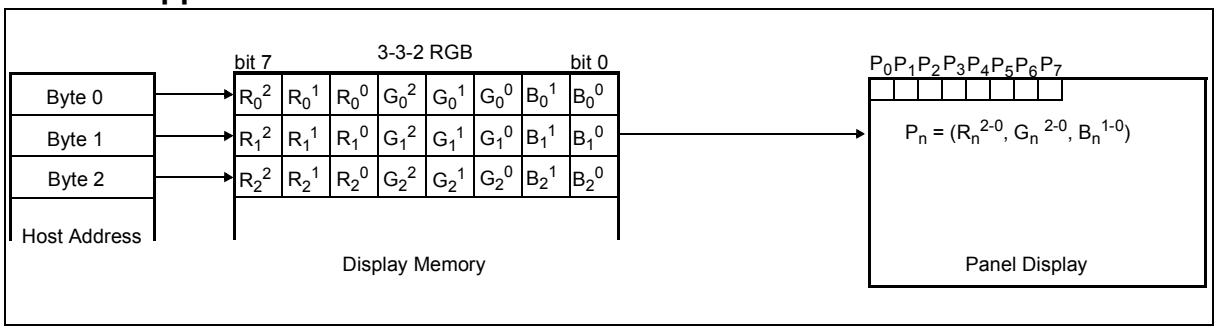


Figure 13-5: LUT Bypass for 8 Bpp mode

13.2.2 16 Bpp Mode

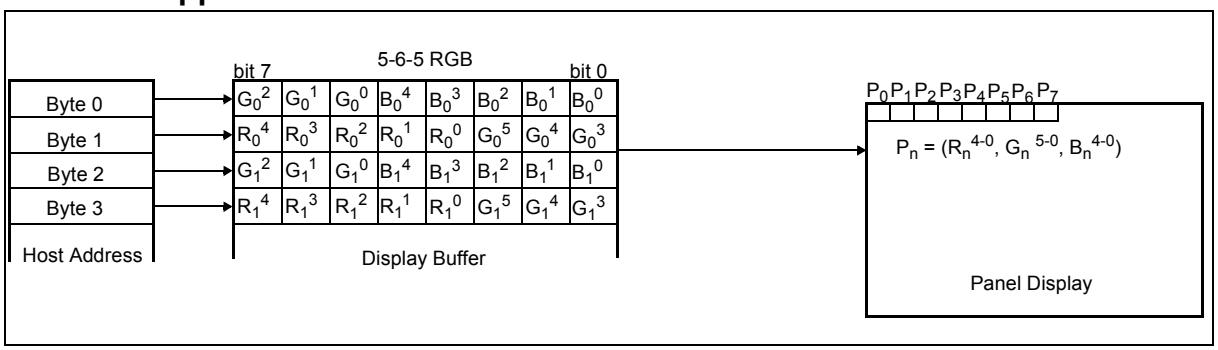


Figure 13-6: LUT Bypass for 16 Bpp mode

13.3 Display Data Flow

The 8 bpp or 16 bpp data in the display buffer is expanded to 24 bpp (RGB=8:8:8) either by the internal LUT or by bit cover (see Section 13.3.2, "Bit Cover When LUT Bypassed" on page 298). Before being output, the LCD data is altered depending on the specified LCD panel data format. For more information, see Section 5.5, "LCD Interface Pin Mapping" on page 46, Section 13.4, "Parallel Data Format" on page 299 and Section 13.5, "Serial Data Format" on page 305.

13.3.1 Display Buffer Data

Display data can be stored in the display buffer as either 8 bpp or 16 bpp. Data from the camera interface or JPEG decoder must be stored as 16 bpp only. The data format for each color depth differs based on whether the LUT is used or the LUT is bypassed.

13.3.2 Bit Cover When LUT Bypassed

When the LUT is bypassed, 8 bpp and 16 bpp data are not indexed using the LUT. The data is expanded to 24 bpp (or bit covered) by copying the MSB to the LSBs as follows.

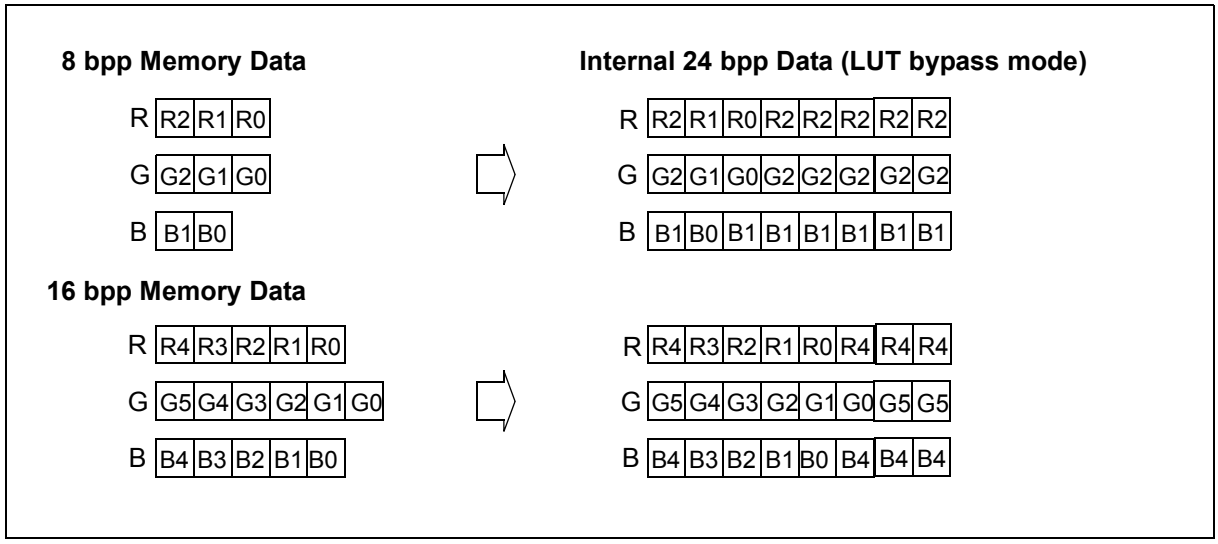


Figure 13-7: Data Bit Cover When the LUT is Bypassed

13.3.3 Overlay

The overlay function compares 24-bit data after the LUT. If the 24-bit data is the same as the Overlay key color (see REG[0204h] - REG[0208h], REG[0304h] - REG[0326h]), the data that will be output is the PIP+ window data instead of the main window data. For more information on the overlay function, see Section 15.1, "Overlay Display" on page 316.

13.4 Parallel Data Format

When the Panel Interface bits are set for a parallel panel(s) (REG[0032h] bits 1-0 = 01b or 10b or 11b), a parallel data format must be selected. REG[0056h] bits 2-0 select the data format for LCD1 and REG[005Eh] bits 2-0 select the data format for LCD2.

Note

When REG[0032h] bits 1-0 = 10b, Mode 2 is enabled and only LCD1 is configured as a parallel panel. When REG[0032h] bits 1-0 = 11b, Mode 3 is enabled and both LCD1 and LCD2 are configured as parallel panels. When REG[0032h] bits 1-0 = 01b, Mode 4 is enabled and only LCD2 is configured as a parallel panel. For more information on possible panel combinations, see REG[0032h] bits 1-0 in Section 10.4.4, "LCD Panel Interface Generic Setting Registers" on page 134.

13.4.1 8-Bit Parallel, RGB=3:3:2

When REG[0056h] bits 2-0 = 000b, the LCD1 data format is specified as this format. When REG[005Eh] bits 2-0 = 000b, the LCD2 data format is specified as this format.

Table 13-1: 8-Bit Parallel, RGB=3:2:2 Data Format Selection

	Cycle Count				
	1	**2**	**3**	**...**	**n+1**
D7	R_0^5	R_1^5	R_2^5	...	R_n^5
D6	R_0^4	R_1^4	R_2^4	...	R_n^4
D5	R_0^3	R_1^3	R_2^3	...	R_n^3
D4	G_0^5	G_1^5	G_2^5	...	G_n^5
D3	G_0^4	G_1^4	G_2^4	...	G_n^4
D2	G_0^3	G_1^3	G_2^3	...	G_n^3
D1	B_0^5	B_1^5	B_2^5	...	B_n^5
D0	B_0^4	B_1^4	B_2^4	...	B_n^4

13.4.2 8-Bit Parallel, RGB=4:4:4

When REG[0056h] bits 2-0 = 001b, the LCD1 data format is specified as this format.
When REG[005Eh] bits 2-0 = 001b, the LCD2 data format is specified as this format.

Table 13-2: 8-Bit Parallel, RGB=4:4:4 Data Format Selection

	Cycle Count						
	1	**2**	**3**	**...**	**3n+1**	**3n+2**	**3n+3**
D7	R_0^5	B_0^5	G_1^5	...	R_n^5	B_n^5	G_{n+1}^5
D6	R_0^4	B_0^4	G_1^4	...	R_n^4	B_n^4	G_{n+1}^4
D5	R_0^3	B_0^3	G_1^3	...	R_n^3	B_n^3	G_{n+1}^3
D4	R_0^2	B_0^2	G_1^2	...	R_n^2	B_n^2	G_{n+1}^2
D3	G_0^5	R_1^5	B_1^5	...	G_n^5	R_{n+1}^5	B_{n+1}^5
D2	G_0^4	R_1^4	B_1^4	...	G_n^4	R_{n+1}^4	B_{n+1}^4
D1	G_0^3	R_1^3	B_1^3	...	G_n^3	R_{n+1}^3	B_{n+1}^3
D0	G_0^2	R_1^2	B_1^2	...	G_n^2	R_{n+1}^2	B_{n+1}^2

13.4.3 8-Bit Parallel, RGB=8:8:8

When REG[0056h] bits 2-0 = 011b, the LCD1 data format is specified as this format.
When REG[005Eh] bits 2-0 = 011b, the LCD2 data format is specified as this format.

Table 13-3: 8-Bit Parallel, RGB=8:8:8 Data Format Selection

	Cycle Count						
	1	**2**	**3**	**...**	**3n+1**	**3n+2**	**3n+3**
D7	R_0^7	G_0^7	B_0^7	...	R_n^7	G_n^7	B_n^7
D6	R_0^6	G_0^6	B_0^6	...	R_n^6	G_n^6	B_n^6
D5	R_0^5	G_0^5	B_0^5	...	R_n^5	G_n^5	B_n^5
D4	R_0^4	G_0^4	B_0^4	...	R_n^4	G_n^4	B_n^4
D3	R_0^3	G_0^3	B_0^3	...	R_n^3	G_n^3	B_n^3
D2	R_0^2	G_0^2	B_0^2	...	R_n^2	G_n^2	B_n^2
D1	R_0^1	G_0^1	B_0^1	...	R_n^1	G_n^1	B_n^1
D0	R_0^0	G_0^0	B_0^0	...	R_n^0	G_n^0	B_n^0

13.4.4 16-Bit Parallel, RGB=4:4:4

When REG[0056h] bits 2-0 = 101b, the LCD1 data format is specified as this format.
When REG[005Eh] bits 2-0 = 101b, the LCD2 data format is specified as this format.

Table 13-4: 16-Bit Parallel, RGB=4:4:4 Data Format Selection

	Cycle Count				
	1	**2**	**3**	**...**	**n+1**
D15	R_0^5	R_1^5	R_2^5	...	R_n^5
D14	R_0^4	R_1^4	R_2^4	...	R_n^4
D13	R_0^3	R_1^3	R_2^3	...	R_n^3
D12	R_0^2	R_1^2	R_2^2	...	R_n^2
D11	G_0^5	G_1^5	G_2^5	...	G_n^5
D10	G_0^4	G_1^4	G_2^4	...	G_n^4
D9	G_0^3	G_1^3	G_2^3	...	G_n^3
D8	G_0^2	G_1^2	G_2^2	...	G_n^2
D7	B_0^5	B_1^5	B_2^5	...	B_n^5
D6	B_0^4	B_1^4	B_2^4	...	B_n^4
D5	B_0^3	B_1^3	B_2^3	...	B_n^3
D4	B_0^2	B_1^2	B_2^2	...	B_n^2
D3				...	
D2				...	
D1				...	
D0				...	

13.4.5 16-Bit Parallel, RGB=5:6:5

When REG[0056h] bits 2-0 = 110b, the LCD1 data format is specified as this format.
When REG[005Eh] bits 2-0 = 110b, the LCD2 data format is specified as this format.

Table 13-5: 16-Bit Parallel, RGB=5:6:5 Data Format Selection

Cycle Count	1	2	3	...	n+1
D15	R_0^5	R_1^5	R_2^5	...	R_n^5
D14	R_0^4	R_1^4	R_2^4	...	R_n^4
D13	R_0^3	R_1^3	R_2^3	...	R_n^3
D12	R_0^2	R_1^2	R_2^2	...	R_n^2
D11	R_0^1	R_1^1	R_2^1	...	R_n^1
D10	G_0^5	G_1^5	G_2^5	...	G_n^5
D9	G_0^4	G_1^4	G_2^4	...	G_n^4
D8	G_0^3	G_1^3	G_2^3	...	G_n^3
D7	G_0^2	G_1^2	G_2^2	...	G_n^2
D6	G_0^1	G_1^1	G_2^1	...	G_n^1
D5	G_0^0	G_1^0	G_2^0	...	G_n^0
D4	B_0^5	B_1^5	B_2^5	...	B_n^5
D3	B_0^4	B_1^4	B_2^4	...	B_n^4
D2	B_0^3	B_1^3	B_2^3	...	B_n^3
D1	B_0^2	B_1^2	B_2^2	...	B_n^2
D0	B_0^1	B_1^1	B_2^1	...	B_n^1

13.4.6 18-Bit Parallel, RGB=6:6:6

When REG[0056h] bits 2-0 = 111b, the LCD1 data format is specified as this format.
When REG[005Eh] bits 2-0 = 111b, the LCD2 data format is specified as this format.

Table 13-6: 18-Bit Parallel, RGB=6:6:6 Data Format Selection

Cycle Count	1	2	3	...	n+1
D17	R_0^5	R_1^5	R_2^5	...	R_n^5
D16	R_0^4	R_1^4	R_2^4	...	R_n^4
D15	R_0^3	R_1^3	R_2^3	...	R_n^3
D14	R_0^2	R_1^2	R_2^2	...	R_n^2
D13	R_0^1	R_1^1	R_2^1	...	R_n^1
D12	R_0^0	R_1^0	R_2^0	...	R_n^0
D11	G_0^5	G_1^5	G_2^5	...	G_n^5
D10	G_0^4	G_1^4	G_2^4	...	G_n^4
D9	G_0^3	G_1^3	G_2^3	...	G_n^3
D8	G_0^2	G_1^2	G_2^2	...	G_n^2
D7	G_0^1	G_1^1	G_2^1	...	G_n^1
D6	G_0^0	G_1^0	G_2^0	...	G_n^0
D5	B_0^5	B_1^5	B_2^5	...	B_n^5
D4	B_0^4	B_1^4	B_2^4	...	B_n^4
D3	B_0^3	B_1^3	B_2^3	...	B_n^3
D2	B_0^2	B_1^2	B_2^2	...	B_n^2
D1	B_0^1	B_1^1	B_2^1	...	B_n^1
D0	B_0^0	B_1^0	B_2^0	...	B_n^0

13.4.7 16-Bit Parallel, RGB=8:8:8

When REG[0056h] bits 2-0 = 010b, the LCD1 data format is specified as this format.
When REG[005Eh] bits 2-0 = 010b, the LCD2 data format is specified as this format.

Table 13-7: 16-Bit Parallel, RGB=8:8:8 Data Format Selection

	Cycle Count				
	1	**2**	**3**	**...**	**n+1**
D15	R_0^7	B_0^7	G_1^7	...	R_n^7
D14	R_0^6	B_0^6	G_1^6	...	R_n^6
D13	R_0^5	B_0^5	G_1^5	...	R_n^5
D12	R_0^4	B_0^4	G_1^4	...	R_n^4
D11	R_0^3	B_0^3	G_1^3	...	R_n^3
D10	R_0^2	B_0^2	G_1^2	...	R_n^2
D9	R_0^1	B_0^1	G_1^1	...	R_n^1
D8	R_0^0	B_0^0	G_1^0	...	R_n^0
D7	G_0^7	R_1^7	B_1^7	...	G_n^7
D6	G_0^6	R_1^6	B_1^6	...	G_n^6
D5	G_0^5	R_1^5	B_1^5	...	G_n^5
D4	G_0^4	R_1^4	B_1^4	...	G_n^4
D3	G_0^3	R_1^3	B_1^3	...	G_n^3
D2	G_0^2	R_1^2	B_1^2	...	G_n^2
D1	G_0^1	R_1^1	B_1^1	...	G_n^1
D0	G_0^0	R_1^0	B_1^0	...	G_n^0

13.5 Serial Data Format

When the Panel Interface bits are set for a serial panel (REG[0032h] bits 1-0 = 00b or 10b), a serial data format must be selected. REG[005Ch] bits 3-2 select the data format for LCD2. A data direction which sets either the MSB or the LSB first can also be specified using REG[005Ch] bit 4.

Note

When REG[0032h] bits 1-0 = 00b, Mode 1 is enabled and LCD2 is configured as a serial panel. When REG[0032h] bits 1-0 = 10b, Mode 2 is enabled and LCD2 is configured as a serial panel. For more information on possible panel combinations, see REG[0032h] bits 1-0 in Section 10.4.4, "LCD Panel Interface Generic Setting Registers" on page 134.

13.5.1 8-Bit Serial, RGB=3:3:2

When REG[005Ch] bits 1-0 = 00b, the LCD2 data format is specified as this format.

Table 13-8: 8-Bit Serial, RGB=3:2:2 Data Format Selection

	Cycle Count				
	1	**2**	**3**	**...**	**n+1**
D7	R_0^5	R_1^5	R_2^5	...	R_n^5
D6	R_0^4	R_1^4	R_2^4	...	R_n^4
D5	R_0^3	R_1^3	R_2^3	...	R_n^3
D4	G_0^5	G_1^5	G_2^5	...	G_n^5
D3	G_0^4	G_1^4	G_2^4	...	G_n^4
D2	G_0^3	G_1^3	G_2^3	...	G_n^3
D1	B_0^5	B_1^5	B_2^5	...	B_n^5
D0	B_0^4	B_1^4	B_2^4	...	B_n^4

13.5.2 8-Bit Serial, RGB=4:4:4

When REG[005Ch] bits 1-0 = 01b, the LCD2 data format is specified as this format.

Table 13-9: 8-Bit Serial, RGB=4:4:4 Data Format Selection

	Cycle Count						
	1	**2**	**3**	**...**	**3n+1**	**3n+2**	**3n+3**
D7	R_0^5	B_0^5	G_1^5	...	R_n^5	B_n^5	G_{n+1}^5
D6	R_0^4	B_0^4	G_1^4	...	R_n^4	B_n^4	G_{n+1}^4
D5	R_0^3	B_0^3	G_1^3	...	R_n^3	B_n^3	G_{n+1}^3
D4	R_0^2	B_0^2	G_1^2	...	R_n^2	B_n^2	G_{n+1}^2
D3	G_0^5	R_1^5	B_1^5	...	G_n^5	R_{n+1}^5	B_{n+1}^5
D2	G_0^4	R_1^4	B_1^4	...	G_n^4	R_{n+1}^4	B_{n+1}^4
D1	G_0^3	R_1^3	B_1^3	...	G_n^3	R_{n+1}^3	B_{n+1}^3
D0	G_0^2	R_1^2	B_1^2	...	G_n^2	R_{n+1}^2	B_{n+1}^2

13.6 YUV Input / Output Data Format

13.6.1 YUV 4:2:2 Data Input / Output Format

YUV 4:2:2 output format is selected when REG[0980h] bits 3-1 = 011b and YUV 4:2:2 input format is selected when REG[0980h] bits 3-1 = 001b.

Table 13-10: YUV 4:2:2 Data Format

	Cycle Count						
	1	**2**	**3**	**4**	**...**	**2n+1**	**2n+2**
D15	Y_0^7	Y_1^7	Y_2^7	Y_3^7	...	Y_{2n}^7	Y_{2n+1}^7
D14	Y_0^6	Y_1^6	Y_2^6	Y_3^6	...	Y_{2n}^6	Y_{2n+1}^6
D13	Y_0^5	Y_1^5	Y_2^5	Y_3^5	...	Y_{2n}^5	Y_{2n+1}^5
D12	Y_0^4	Y_1^4	Y_2^4	Y_3^4	...	Y_{2n}^4	Y_{2n+1}^4
D11	Y_0^3	Y_1^3	Y_2^3	Y_3^3	...	Y_{2n}^3	Y_{2n+1}^3
D10	Y_0^2	Y_1^2	Y_2^2	Y_3^2	...	Y_{2n}^2	Y_{2n+1}^2
D9	Y_0^1	Y_1^1	Y_2^1	Y_3^1	...	Y_{2n}^1	Y_{2n+1}^1
D8	Y_0^0	Y_1^0	Y_2^0	Y_3^0	...	Y_{2n}^0	Y_{2n+1}^0
D7	U_0^7	V_0^7	U_2^7	V_2^7	...	U_{2n}^7	V_{2n+1}^7
D6	U_0^6	V_0^6	U_2^6	V_2^6	...	U_{2n}^6	V_{2n+1}^6
D5	U_0^5	V_0^5	U_2^5	V_2^5	...	U_{2n}^5	V_{2n+1}^5
D4	U_0^4	V_0^4	U_2^4	V_2^4	...	U_{2n}^4	V_{2n+1}^4
D3	U_0^3	V_0^3	U_2^3	V_2^3	...	U_{2n}^3	V_{2n+1}^3
D2	U_0^2	V_0^2	U_2^2	V_2^2	...	U_{2n}^2	V_{2n+1}^2
D1	U_0^1	V_0^1	U_2^1	V_2^1	...	U_{2n}^1	V_{2n+1}^1
D0	U_0^0	V_0^0	U_2^0	V_2^0	...	U_{2n}^0	V_{2n+1}^0

13.6.2 YUV 4:2:0 Data Input / Output Format

YUV 4:2:0 format is selected when REG[0980h] bits 3-1 = 111b and YUV 4:2:2 input format is selected when REG[0980h] bits 3-1 = 101b. This data format differs between even and odd lines. The line number count starts at 0.

Table 13-11: YUV 4:2:0 Data Format (Even Line)

	Cycle Count						
	1	**2**	**3**	**4**	**...**	**2n**	**2n+1**
D15	Y_0^7	Y_1^7	Y_2^7	Y_3^7	...	Y_{2n}^7	Y_{2n+1}^7
D14	Y_0^6	Y_1^6	Y_2^6	Y_3^6	...	Y_{2n}^6	Y_{2n+1}^6
D13	Y_0^5	Y_1^5	Y_2^5	Y_3^5	...	Y_{2n}^5	Y_{2n+1}^5
D12	Y_0^4	Y_1^4	Y_2^4	Y_3^4	...	Y_{2n}^4	Y_{2n+1}^4
D11	Y_0^3	Y_1^3	Y_2^3	Y_3^3	...	Y_{2n}^3	Y_{2n+1}^3
D10	Y_0^2	Y_1^2	Y_2^2	Y_3^2	...	Y_{2n}^2	Y_{2n+1}^2
D9	Y_0^1	Y_1^1	Y_2^1	Y_3^1	...	Y_{2n}^1	Y_{2n+1}^1
D8	Y_0^0	Y_1^0	Y_2^0	Y_3^0	...	Y_{2n}^0	Y_{2n+1}^0
D7	U_0^7	V_0^7	U_2^7	V_2^7	...	U_{2n}^7	V_{2n+1}^7
D6	U_0^6	V_0^6	U_2^6	V_2^6	...	U_{2n}^6	V_{2n+1}^6
D5	U_0^5	V_0^5	U_2^5	V_2^5	...	U_{2n}^5	V_{2n+1}^5
D4	U_0^4	V_0^4	U_2^4	V_2^4	...	U_{2n}^4	V_{2n+1}^4
D3	U_0^3	V_0^3	U_2^3	V_2^3	...	U_{2n}^3	V_{2n+1}^3
D2	U_0^2	V_0^2	U_2^2	V_2^2	...	U_{2n}^2	V_{2n+1}^2
D1	U_0^1	V_0^1	U_2^1	V_2^1	...	U_{2n}^1	V_{2n+1}^1
D0	U_0^0	V_0^0	U_2^0	V_2^0	...	U_{2n}^0	V_{2n+1}^0

Table 13-12: YUV 4:2:0 Data Format (Odd Line)

	Cycle Count			
	1	**2**	**...**	**n+1**
D15	Y_1^7	Y_3^7	...	Y_{2n+1}^7
D14	Y_1^6	Y_3^6	...	Y_{2n+1}^6
D13	Y_1^5	Y_3^5	...	Y_{2n+1}^5
D12	Y_1^4	Y_3^4	...	Y_{2n+1}^4
D11	Y_1^3	Y_3^3	...	Y_{2n+1}^3
D10	Y_1^2	Y_3^2	...	Y_{2n+1}^2
D9	Y_1^1	Y_3^1	...	Y_{2n+1}^1
D8	Y_1^0	Y_3^0	...	Y_{2n+1}^0
D7	Y_0^7	Y_2^7	...	Y_{2n}^7
D6	Y_0^6	Y_2^6	...	Y_{2n}^6
D5	Y_0^5	Y_2^5	...	Y_{2n}^5
D4	Y_0^4	Y_2^4	...	Y_{2n}^4
D3	Y_0^3	Y_2^3	...	Y_{2n}^3
D2	Y_0^2	Y_2^2	...	Y_{2n}^2
D1	Y_0^1	Y_2^1	...	Y_{2n}^1
D0	Y_0^0	Y_2^0	...	Y_{2n}^0

13.7 YUV/RGB Conversion

The YUV/RGB Converter (YRC) converts YUV image data from the Camera interface (YUV 4:2:2), from the JPEG decoder (YUV 4:4:4, YUV 4:2:2, YUV 4:2:0, YUV 4:1:1), or from the Host (YUV 4:2:2, 4:2:0) to RGB data (RGB 5:6:5, RGB 8:8:8). The YUV data range input can be selected using the YRC Input Data Type Select bit (REG[0240h] bit 4) and the transfer mode can be selected using the YUV/RGB Transfer mode bits (REG[0240h] bits 2-0).

The YUV/RGB Converter uses the following parameters and equations.

$$0 \le Y \le 255$$
$$-128 \le U \le 127$$
$$-128 \le V \le 127$$

Table 13-13: YUV/RGB Conversion Parameter Table

Transfer Mode	REG[0240h] bit 2-0	Color	Ey	Epb	Epr
Recommendation ITU-R BT.709	001b	E_R	1.000	0.000	1.575
		E_G	1.000	-0.187	-0.468
		E_B	1.002	1.855	0.000
Recommendation ITU-R BT.470-6 System M	100b	E_R	1.000	0.001	1.400
		E_G	1.000	-0.333	-0.712
		E_B	1.000	1.780	0.002
Recommendation ITU-R BT.470-6 System B, G	101b	E_R	1.000	0.000	1.402
		E_G	1.000	-0.344	-0.714
		E_B	1.000	1.772	0.000
SMPTE 170M	110b	E_R	1.000	0.000	1.402
		E_G	1.000	-0.344	-0.714
		E_B	1.000	1.772	0.000
SMPTE 240M(1987)	111b	E_R	1.000	0.000	1.576
		E_G	1.000	-0.226	-0.477
		E_B	1.000	1.826	0.000

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} E_R E_y & E_R E_{pb} & E_R E_{pr} \\ E_G E_y & E_G E_{pb} & E_G E_{pr} \\ E_B E_y & E_B E_{pb} & E_B E_{pr} \end{bmatrix} \cdot \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

Figure 13-8: YUV/RGB Conversion Equation

14 SwivelView™

Most computer displays are refreshed in landscape orientation – from left to right and top to bottom. Computer images are stored in the same manner. SwivelView™ is designed to rotate the displayed image on an LCD by 90°, 180°, or 270° in a counter-clockwise direction. The rotation is done in hardware and is transparent to the user for all display buffer reads and writes. By processing the rotation in hardware, SwivelView™ offers a performance advantage over software rotation of the displayed image.

The image is not actually rotated in the display buffer since there is no address translation during CPU read/write. The image is rotated during display refresh.

14.1 SwivelView Modes

14.1.1 90° SwivelView

The following figure shows how the programmer sees a portrait image and how the image is being displayed. The application image is written to the S1D13717 in the following sense: A–B–C–D. The display is refreshed by the S1D13717 in the following sense: B-D-A-C.

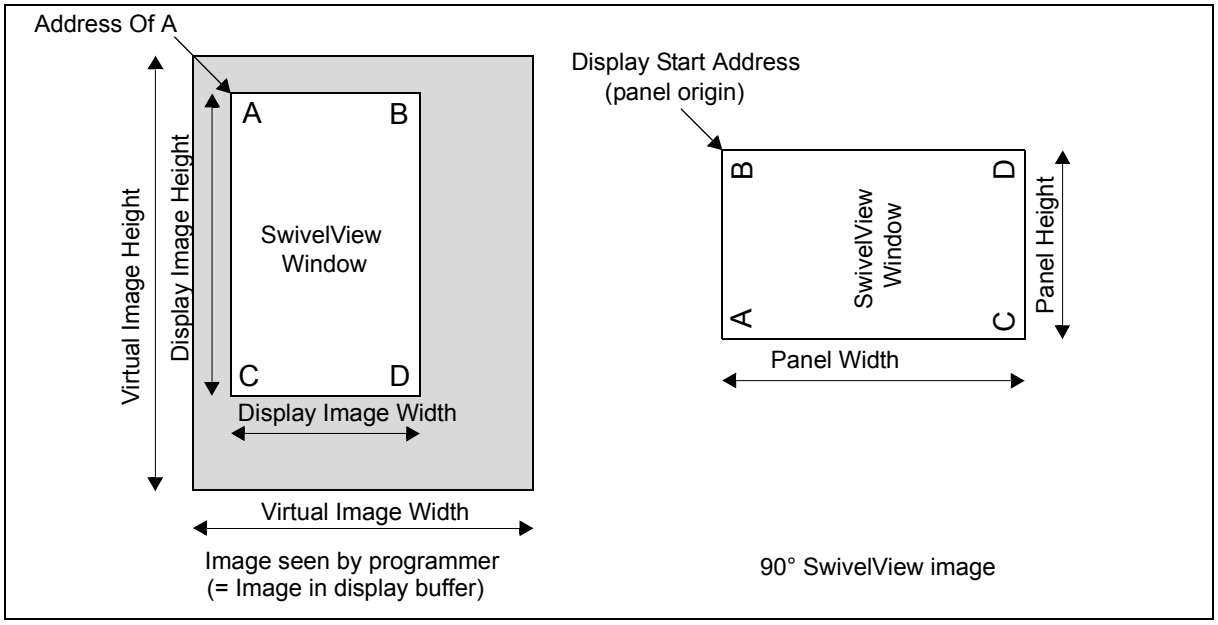


Figure 14-1: Relationship Between The Screen Image and the Image Refreshed in 90° SwivelView.

Display Start Address

The display refresh circuitry starts at pixel "B", therefore the Display Start Address register must be programmed with the address of pixel "B".

Display Start Address = Address of A + Line Address Offset - (bpp ÷ 8)

Line Address Offset

Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset = Virtual Image Width x bpp ÷ 8

Memory Address of a Given Pixel

To calculate the address of pixel at any given position for the Main Window or PIP+ window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) x Virtual Image Width] x bpp ÷ 8

14.1.2 180° SwivelView

The following figure shows how the programmer sees a landscape image and how the image is being displayed. The application image is written to the S1D13717 in the following sense: A–B–C–D. The display is refreshed by the S1D13717 in the following sense: D-C-B-A.

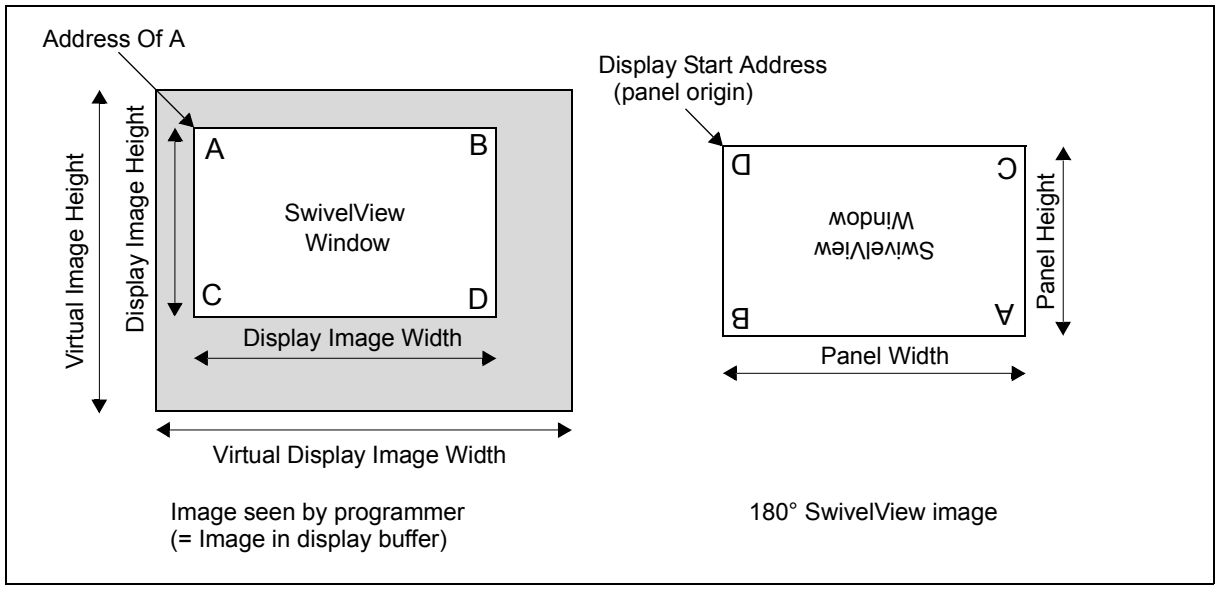


Figure 14-2: Relationship Between The Screen Image and the Image Refreshed in 180° SwivelView.

Display Start Address

The display refresh circuitry starts at pixel "D", therefore the Display Start Address register must be programmed with the address of pixel "D".

Display Start Address = Address of A + Line Address Offset x Display Image Height - (bpp ÷ 8)

Line Address Offset

Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset = Virtual Image Width x bpp ÷ 8

Memory Address of a Given Pixel

To calculate the address of pixel at any given position for the Main Window or PIP+ window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) x Virtual Image Height] x bpp ÷ 8

14.1.3 270° SwivelView

The following figure shows how the programmer sees a portrait image and how the image is being displayed. The application image is written to the S1D13717 in the following sense: A–B–C–D. The display is refreshed by the S1D13717 in the following sense: C-A-D-B.

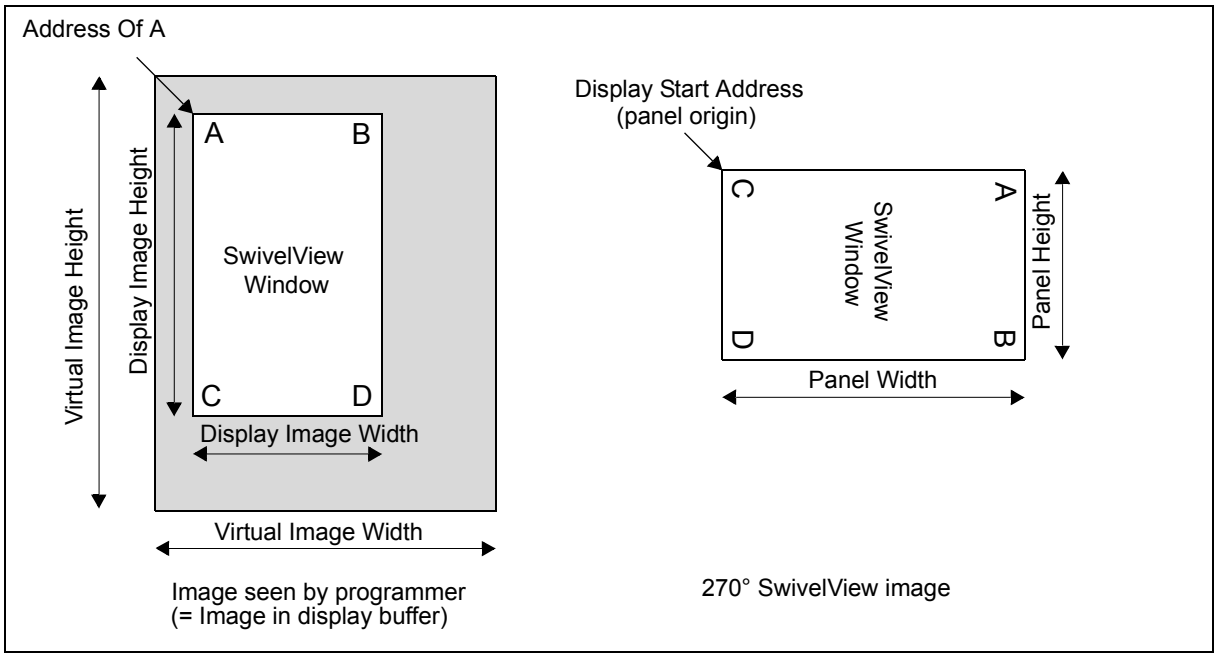


Figure 14-3: Relationship Between The Screen Image and the Image Refreshed in 270° SwivelView.

Display Start Address

The display refresh circuitry starts at pixel "C", therefore the Display Start Address register must be programmed with the address of pixel "C".

Display Start Address
= Address of A + Line Address Offset × (Display Image Width - 1)

Line Address Offset

Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset = Virtual Image Width x bpp ÷ 8

Memory Address of a Given Pixel

To calculate the address of pixel at any given position for the Main Window or PIP+ window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) x Virtual Image Width] x bpp ÷ 8

15 Picture-in-Picture Plus (PIP+)

Picture-in-Picture Plus (PIP+) enables a secondary window (or PIP+ window) within the main display window. The PIP+ window may be positioned anywhere within the main window display and is controlled using the PIP+ Window control registers (REG[0218h]-[0228h]). The PIP+ window color depth (REG[0200h] bits 3-2) and SwivelView orientation (REG[0202h] bits 5-4) are independent from the Main window.

The following diagrams show examples of a PIP+ window within a main window and the registers used to position it.

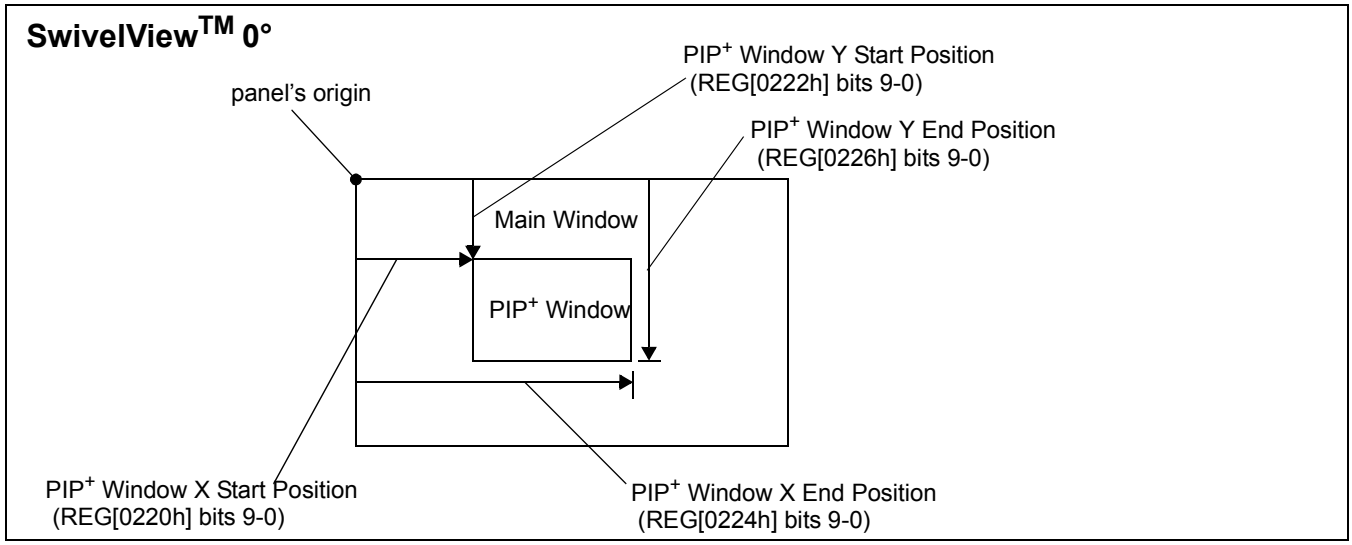


Figure 15-1: PIP+ with SwivelView Disabled (SwivelView 0°)

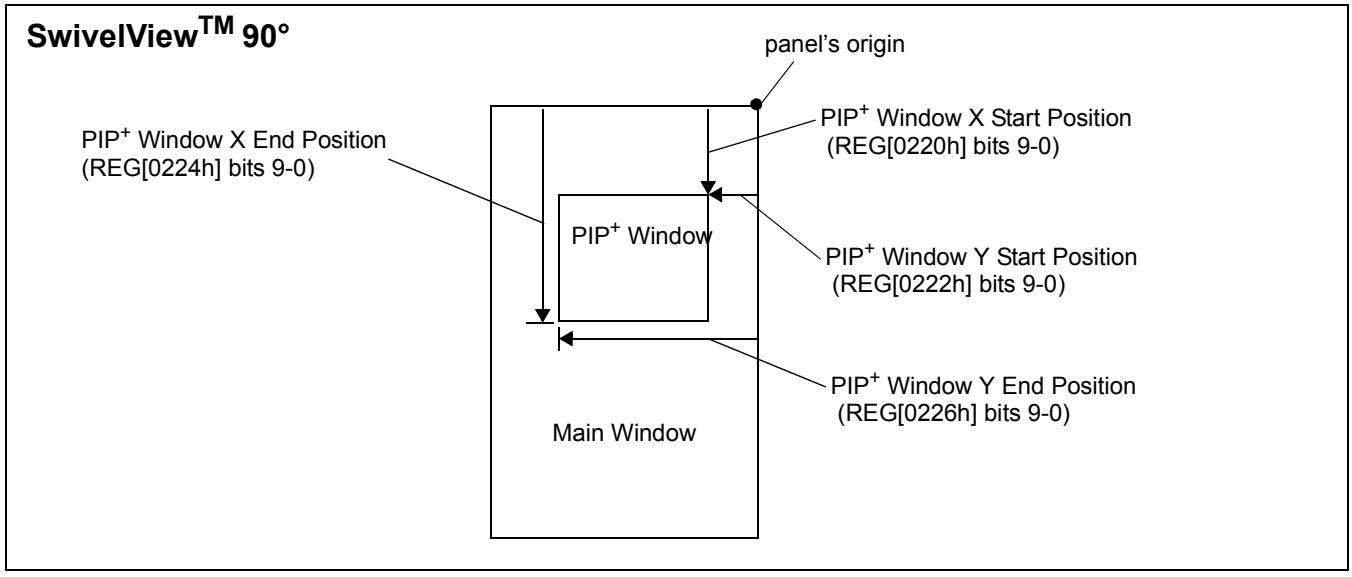


Figure 15-2: PIP+ with SwivelView 90° Enabled

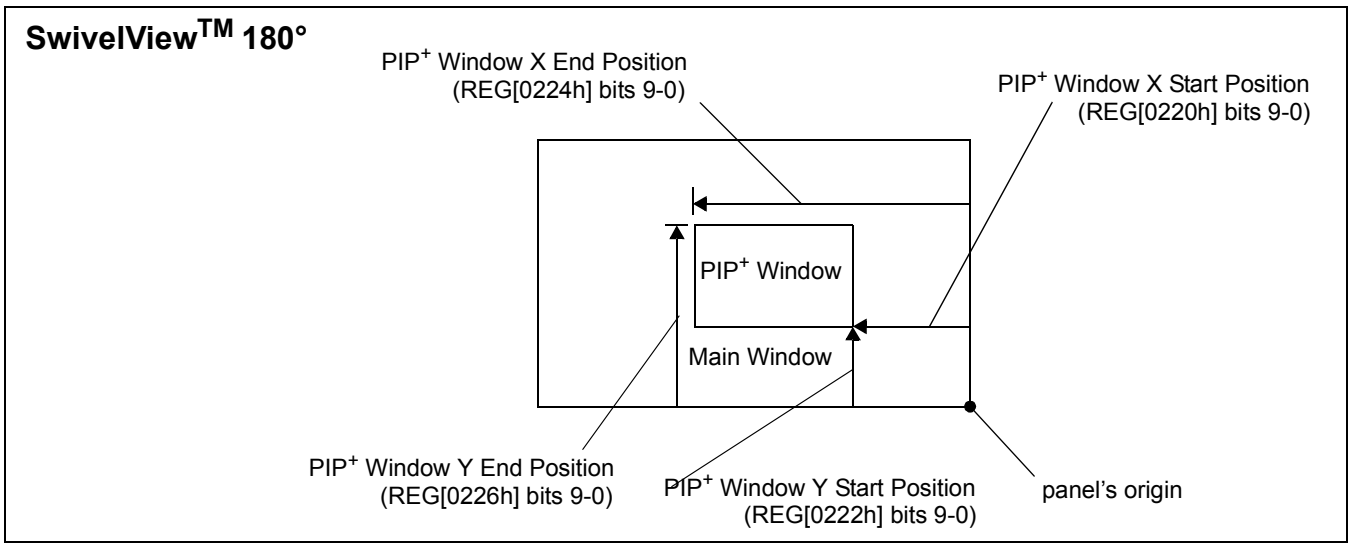


Figure 15-3: PIP+ with SwivelView 180° Enabled

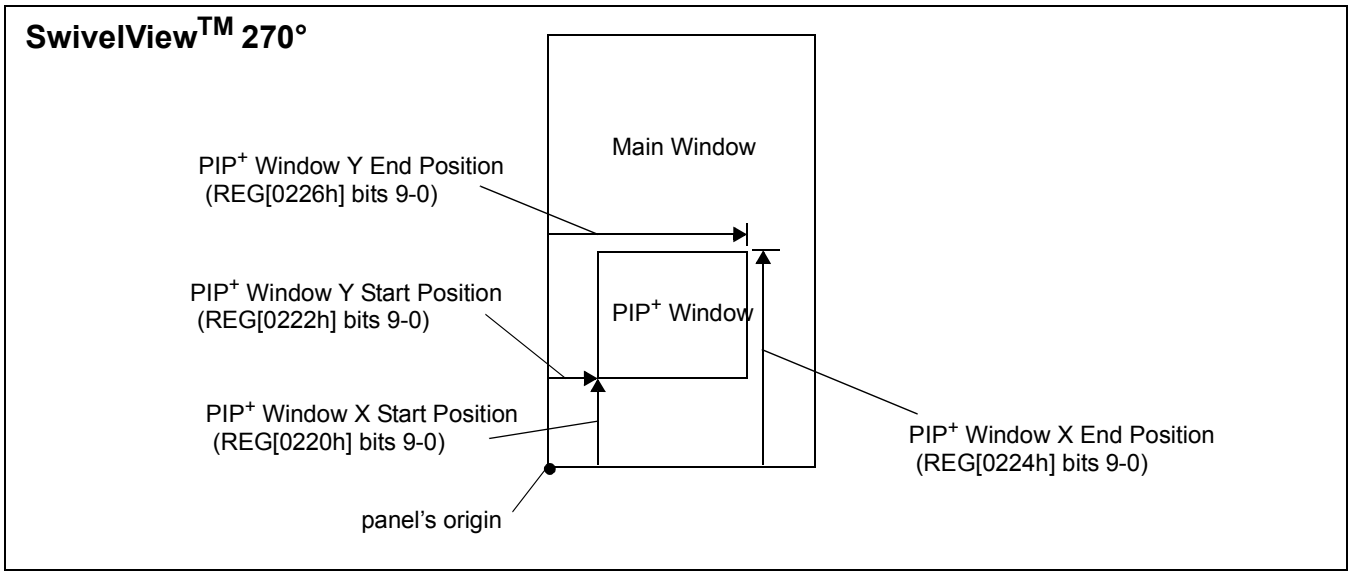


Figure 15-4: PIP+ with SwivelView 270° Enabled

15.1 Overlay Display

When Picture-in-Picture Plus (PIP+) is enabled, the S1D13717 supports an overlay with the following functions: Transparent, Average, AND, OR, and INV. Each RGB component of the overlay function key colors are set using REG[0204h]-[0208h] and REG[0304h]-[0326h].

The overlay settings are specified using the Overlay Key Color registers for each RGB color and individual Overlay Key Color Enable bits (see REG[0328h]) as follows.

Table 15-1: Overlay Mode Selection

Register	Overlay PIP+ Window Bit Shift (REG[0328h] bit 15)	Overlay Main Window Bit Shift (REG[0328h] bit 13)	Display Image
Transparent Overlay Key Color REG[0204h] REG[0206h] REG[0208h]	0	*	PIP+ window data
	1		(PIP+ window data)/2
Average Overlay Key Color REG[0310h] REG[0312h] REG[0314h]	0	0	((PIP+ window data) + (Key Color data))/2
		1	((PIP+ window data) + (Key Color data)/2)/2
	1	0	((PIP+ window data)/2 + (Key Color data))/2
		1	((PIP+ window data)/2 + (Key Color data)/2)/2
AND Overlay Key Color REG[0316h] REG[0318h] REG[031Ah]	0	0	(PIP+ window data) AND (Key Color data)
		1	(PIP+ window data) AND (Key Color data)/2
	1	0	(PIP+ window data)/2 AND (Key Color data)
		1	(PIP+ window data)/2 AND (Key Color data)/2
OR Overlay Key Color REG[031Ch] REG[031Eh] REG[0320h]	0	0	(PIP+ window data) OR (Key Color data)
		1	(PIP+ window data) OR (Key Color data)/2
	1	0	(PIP+ window data)/2 OR (Key Color data)
		1	(PIP+ window data)/2 OR (Key Color data)/2
INV Overlay Key Color REG[0322h] REG[0324h] REG[0326h]	0	*	Negative image of (PIP+ window data)
	1		Negative image of (PIP+ window data)/2

The following table shows the resulting PIP+ window color when overlay is combined with the PIP+ Window Bit Shift and the Main Window Bit Shift functions.

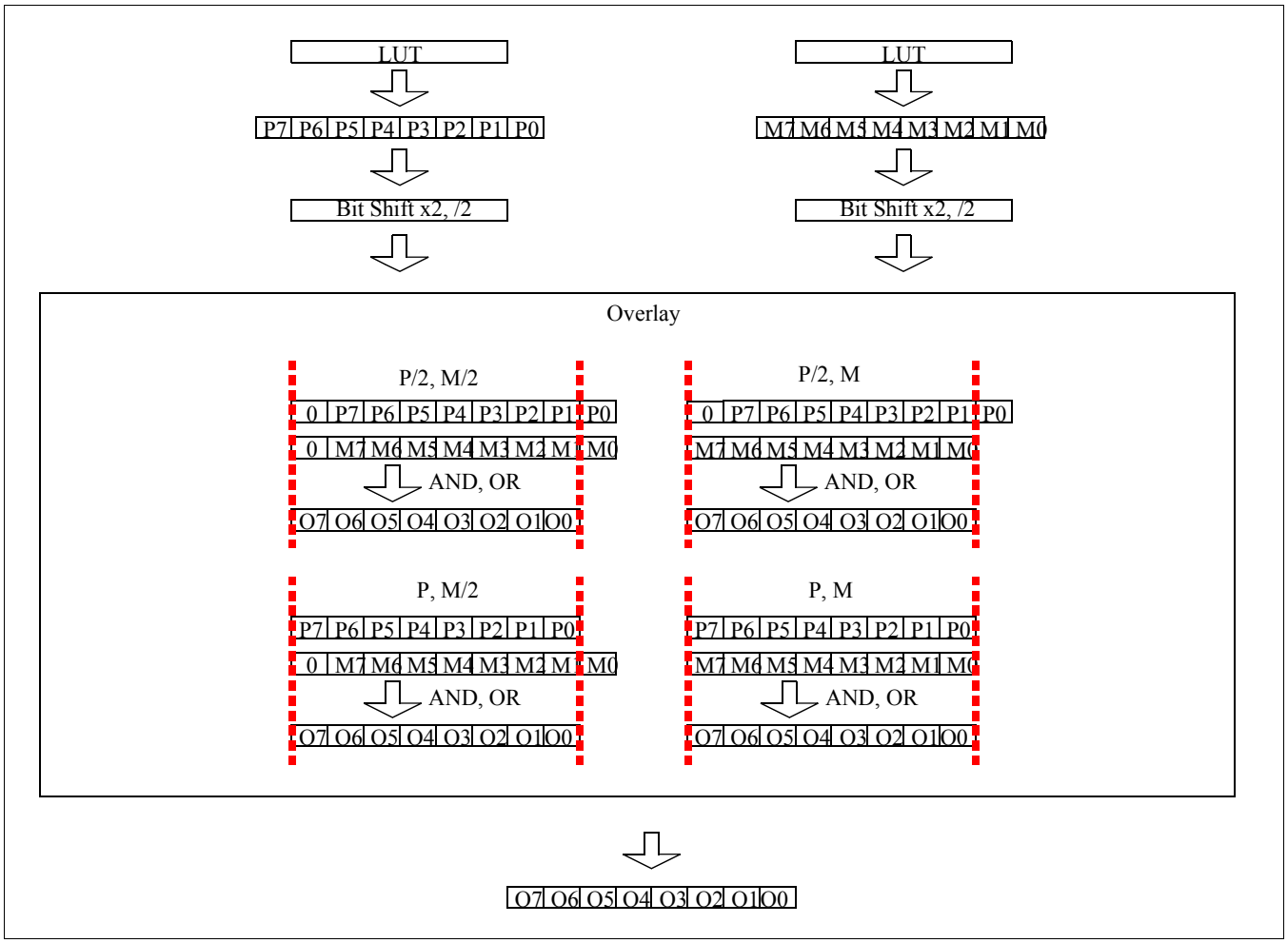


Figure 15-5: Data Flow for Bit Shift Function

15.1.1 Overlay Display Effects

When PIP+ is disabled (REG[0200h] bits 9-8 = 00)b

- Only the Main window is displayed and the PIP+ Window is ignored.

When PIP+ is enabled (REG[0200h] bits 9-8 = 01b)

- The PIP+ window area "overlays" the Main window area. The Overlay Key Color settings are ignored.

When PIP+ with overlay is enabled (REG[0200h] bits 9-8 = 11b)

- The PIP+ window area "overlays" the Main window area only on areas of the Main window where the color matches the overlay key color. For the Main window area, only the Main window is displayed.

- For the PIP+ Window area, if the Main window data is same as the Overlay Key color, then the PIP+ window data is mixed with the Main window data as specified for each overlay function (see Figure 15-6: “Overlay Display Effects 1,” on page 318). If the Main window data differs from the Overlay Key color, then the Main window data is displayed. If two or more Overlays are active, they have the following priority: Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color. A lower priority overlay function is ignored and only the highest priority overlay function is displayed.

Figure 15-6: Overlay Display Effects 1

Figure 15-7: Overlay Display Effects 2

Note

If more than one overlay function is enabled, only the function with the highest priority takes effect. Function priority is as follows (from highest to lowest) Transparent Key Color > Average Key Color > AND Key Color > OR Key Color > INV Key Color. In the case where Transparent and INV overlay are enabled, the INV function is ignored.

16 2D BitBLT Engine

16.1 Overview

The purpose of the BitBLT Engine is to off-load the work of the CPU for moving pixel data to and from the CPU and display memory and also for moving pixel data from one location to another in display memory.

There are 5 BitBLTs (Bit Block Transfer) which are used to move pixel data from one location to another.

- **Read BitBLT:** Move pixel data from Display Memory to CPU
- **Move BitBLT**: Move pixel data from one location in Display Memory to another
- **Pattern Fill BitBLT**: Move a Pixel Pattern in Display Memory and duplicate several times to produce a larger image
- **Solid Fill BitBLT**: Move a Single Color to a location in Memory

The BitBLT Engine can perform several Data Functions in combination with some of the BitBLT functions on the pixel data.

- **ROP**: Perform a Boolean function on the pixel data
- **Transparency**: Only write pixel data of which the color does not match the Transparent Color.

The BitBLT Engine supports pixel data color depths of 8 bpp and16 bpp and CPU data transfers of 16-bits or 8-bits.

The destination and source BitBLTs can be set to be either contiguous linear blocks of memory (Linear) or as a rectangular region of memory (Rectangular).

16.2 BitBLTs

16.2.1 Read BitBLT

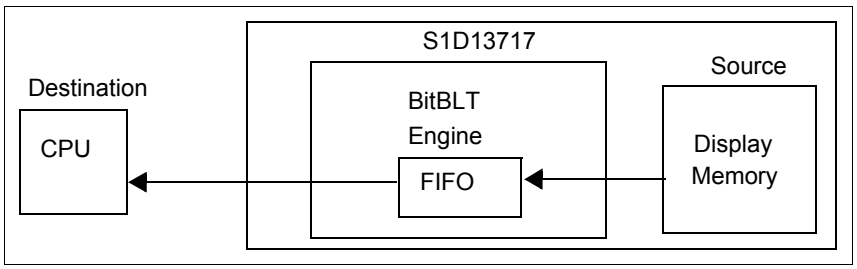


Figure 16-1: Read BitBLT Data Flow

Data can be read from memory by the Host CPU using the BitBLT Engine. The source of the data is the S1D13717 internal memory (stored as either Linear or Rectangular data format). The destination of the data to the Host CPU can also be configured to either Linear or Rectangular data format. No data functions like ROP, Transparency or Color Expansion are supported for Read BitBLTs. If these features are enabled, they are ignored. The Read Phase can also be set for the either the first data read at the start of the BitBLT for Linear or at the start of each line for Rectangular. The Read Phase allows the user to set which byte in the data read is the first byte read from memory.

16.2.2 Move BitBLT

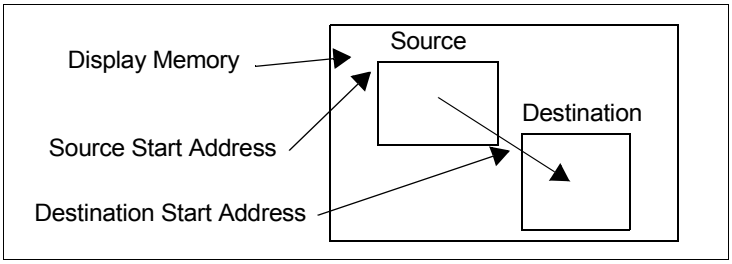


Figure 16-2: Move BitBLT data flow

The Move BitBLT copies data from the source area in memory to the destination area. The source data can also be ROP'ed with the destination data and then written back to the destination. The source data can also be Color Expanded using the Color Expansion data function and then stored to the destination. Transparency can also be applied to the source data. The source and the destination can be in either Linear or Rectangular data format. The top left hand corner of the BitBLT Window is always specified as the start address for the source and destination.

16.2.3 Pattern Fill BitBLT

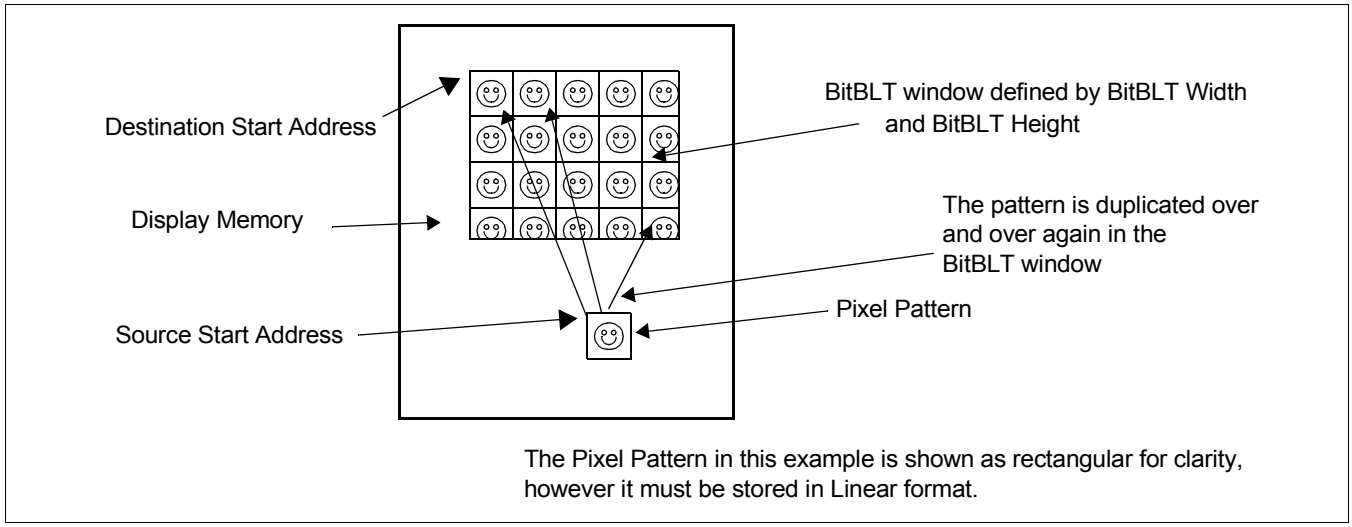


Figure 16-3: Pattern Fill Drawing

The Pattern Fill BitBLT allows an 8 x 8 pixel pattern to be duplicated multiple times to a larger area in memory as shown in the example above. The Pixel Pattern is stored at one location and it is read and drawn multiple times to the BitBLT window. For Pattern Fill BitBLTs, the Pixel Pattern, which is the source data, must be Linear and the destination, which is the BitBLT window, must be Rectangular. The source data can also be ROP'ed with the destination data and then written back to the destination.

The start of the Pixel Pattern must be aligned to a 16-bit address. The Pixel Pattern can be drawn to a BitBLT window area of 1 x 1 pixel to a max of the BitBLT Width x BitBLT Height.

16.2.4 Solid Fill BitBLT

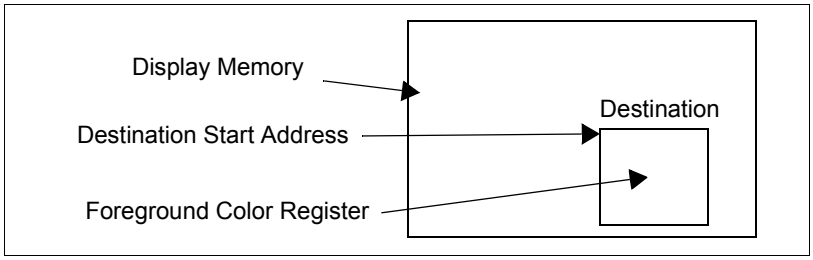


Figure 16-4: Solid Fill BitBLT Data Flow

For Solid Fill BitBLTs, the foreground color is written to the destination. The foreground color can be ROP'ed with the destination. The destination can also be Linear or Rectangular data format.

For 8 bpp, the foreground color is specified by REG[8024h] bits 7-0.
For 16 bpp, the foreground color is specified by REG[8024h] bits 15-0.

16.2.5 BitBLT Terms

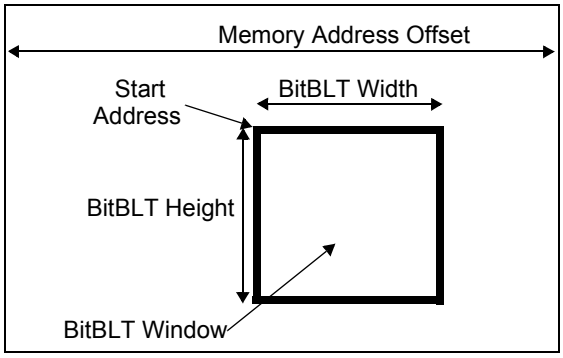


Figure 16-5: BitBLT Terms

Memory Address Offset	Width of the display (i.e. Main Window width or PIP+ Window width) in 16-bit words. The source and destination share the memory address offsets.
Start Address	Top left corner of the BitBLT window specified in bytes.
BitBLT Width	Width of the BitBLT in pixels.
BitBLT Height	Height of the BitBLT in pixels.
BitBLT Window	The area of the display memory to work with.

For each bitBLT there is a source of data and a destination for the result data. The source is the location where the data for the data function (i.e. color expansion, ROP, and transparency) is read from. The destination is where the data for the data function (i.e. ROP) is read from and also the location where the result is written to.

16.2.6 Source and Destination

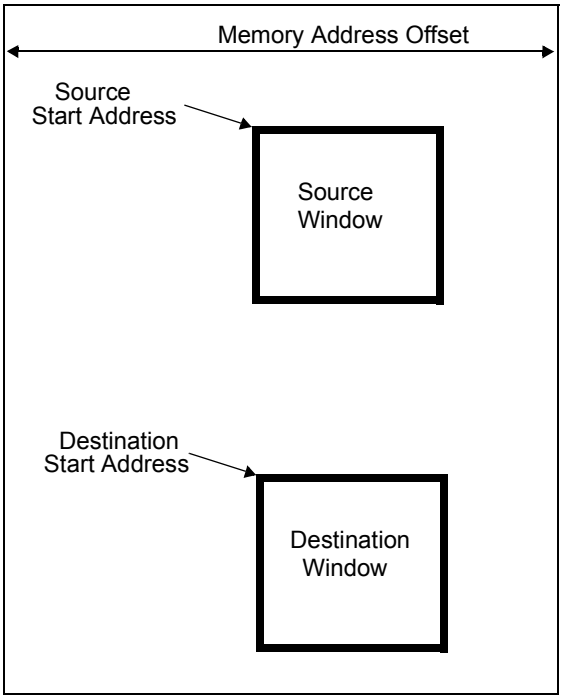


Figure 16-6: Source and Destination

16.3 Data Functions

The following data functions are supported by the BitBLT Engine. For some BitBLTs these functions can be combined together for some BitBLTs.

- Color Expansion
- ROP
- Transparency

16.3.1 ROP

ROPs allow for a boolean function to be applied to the source and destination data. The boolean function is selected using the BitBLT ROP Code bits (REG[800Ah] bits 3-0). Functions such as AND, OR, XOR, NAND, NOR, and others can be selected. The following example shows the results for 3 different ROPs with the same source and destination input.

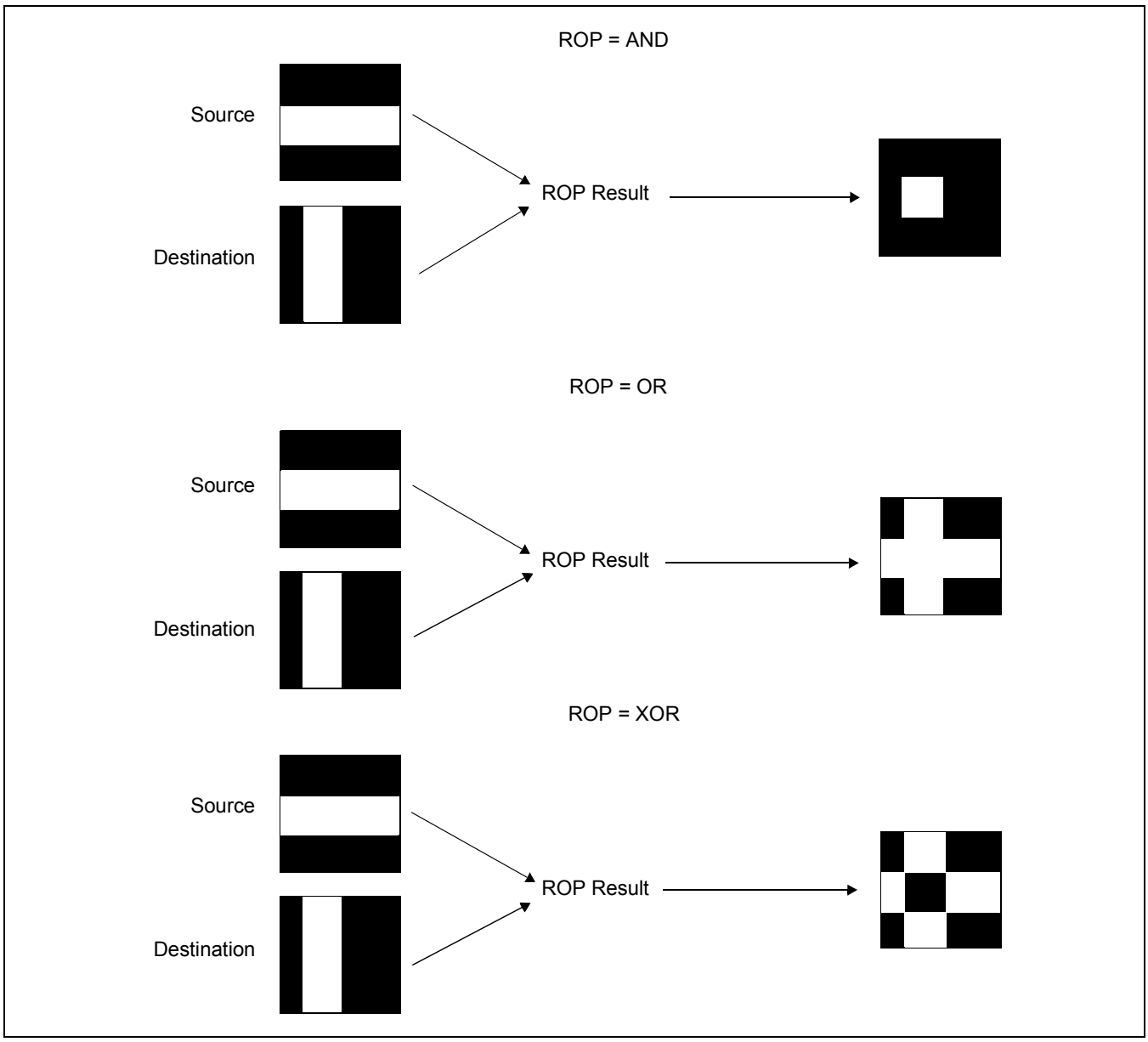


Figure 16-7: ROP Example

16.3.2 Transparency

Transparency allows for colors which do not match the background color to be written to the destination. This is useful when a non-square image contained in the BitBLT window is to be written over another image. For example, a mouse pointer is stored in memory as a block, but when the pointer is written to the display only the color of the pointer is written and the colors around it are not. The following example shows how the source image of a mouse pointer with its color set to black and color around it set to white would appear over the destination image using Transparency. The white color (which matches the background color) around the mouse pointer is not written over the destination image, yet the black mouse pointer is.

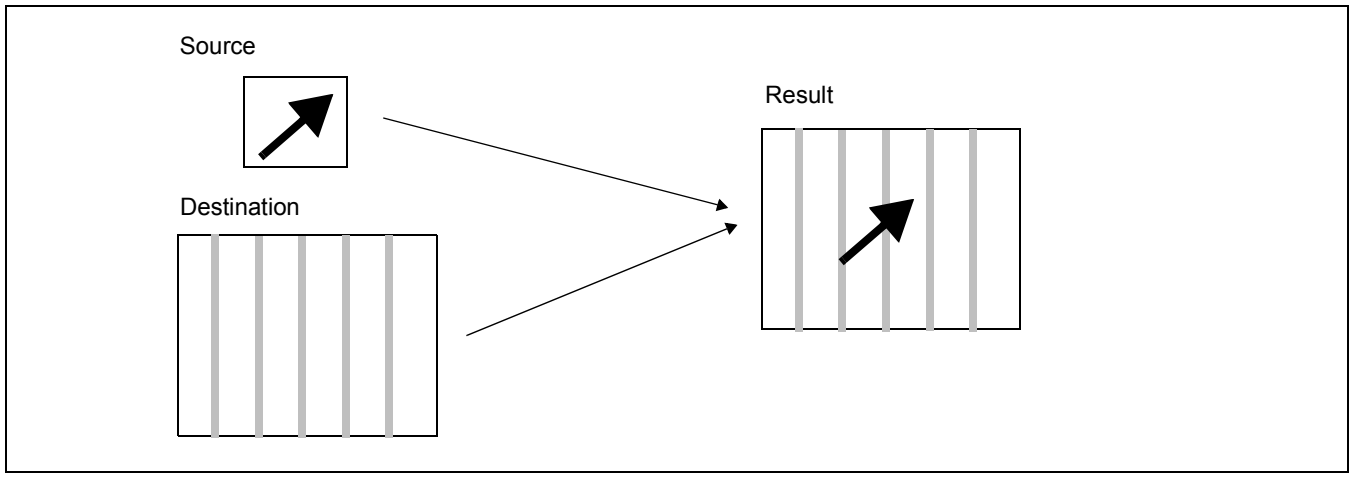


Figure 16-8: Transparency Example

16.4 Linear / Rectangular

Most BitBLTs support linear or rectangular data formats for the source and destination.

Linear means that the data in memory or to be written by the Host CPU is in a continuous format with no gaps between the EOL (End of Line) and SOL (Start of Line). The line offset is ignored for the linear data format. The following example shows how each line of linear data is stored in display memory for a BitBLT with a height of 5. Note that the SOL of Line 2 starts right after the EOL of Line 1. For 8 bpp, the next SOL starts in the byte after the previous lines EOL. For 16 bpp, it is the word after the previous line's EOL.

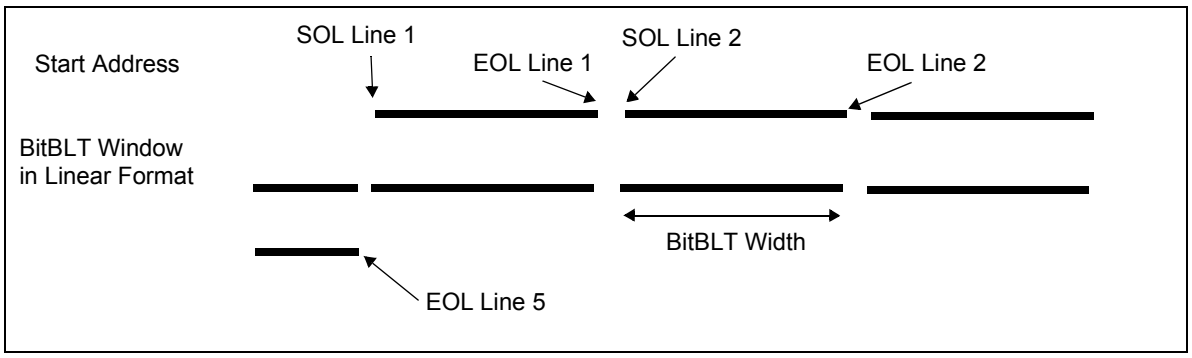


Figure 16-9: Memory Linear Example

The following example shows how linear Host CPU data is written for 16-bit writes. The SOL of the next line starts in the same 16-bit data as the EOL of the previous line.

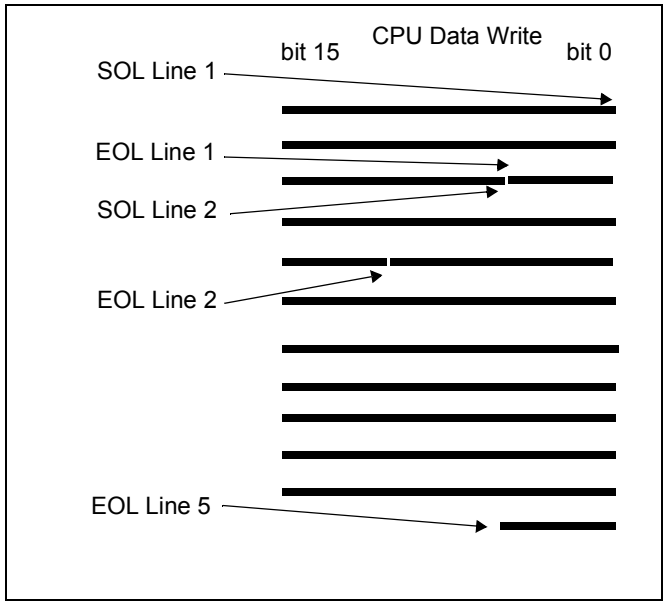


Figure 16-10: Memory Linear Example

Rectangular means that after each EOL, the SOL of the next line is the SOL of the current line plus the line offset for memory accesses. For Host CPU accesses, the SOL of the next line is always in the data written after the data with the EOL.

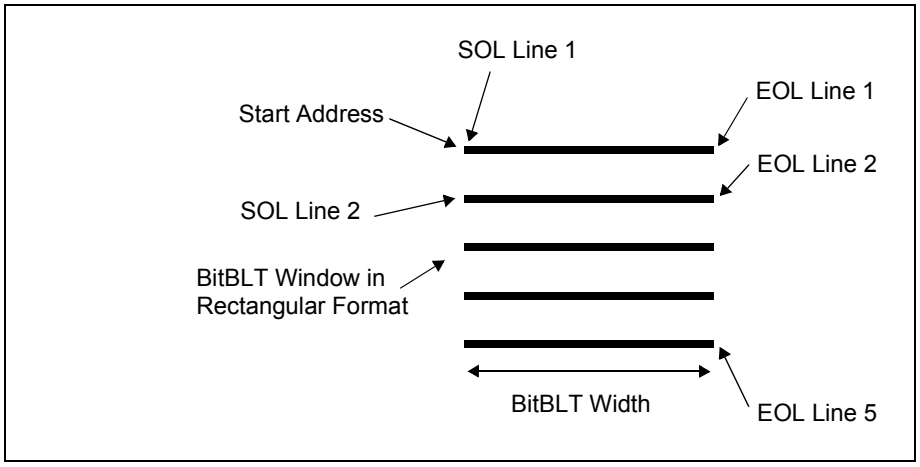


Figure 16-11: Memory Rectangular Example

The following example shows how rectangular Host CPU data is written for 16-bit writes. The SOL of the next line starts in the next 16-bit data after the EOL of the previous line.

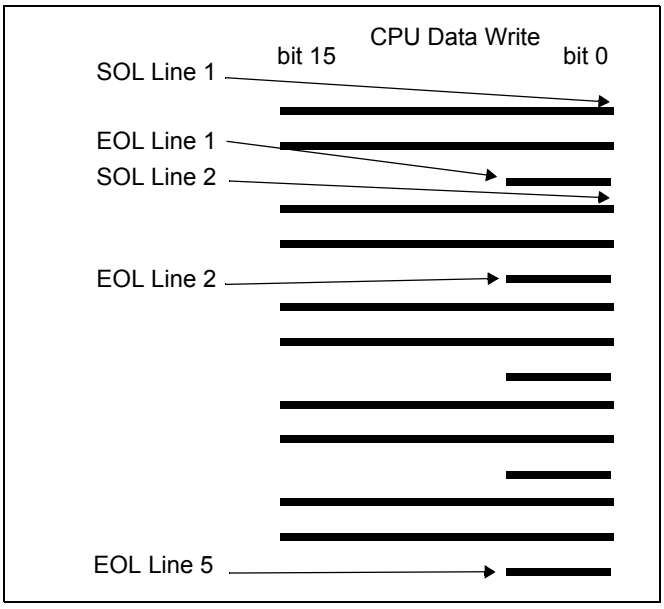


Figure 16-12: Memory Linear Example

17 Resizers

Resizers perform the trimming and scaling functions that can be used to "resize" image data from the camera interface and/or the JPEG decoder. There are two resizers, one for viewing image data and one for viewing/capturing image data.

Image data from the camera interface (always YUV 4:2:2 format) can use either the View resizer or the Capture resizer before being stored in the display memory. If image data from the camera interface is being sent to the JPEG Codec for JPEG encoding, it must use the Capture resizer. View and Capture resizer functions are configured independently.

Image data from the JPEG decoder (YUV 4:4:4, YUV 4:2:2, YUV 4:2:0, YUV 4:1:1 formats) or from the Host CPU can only use the View resizer before being stored in the display buffer.

The resize function is a two stage process - trimming then scaling.

17.1 Trimming Function

The trimming function is similar to cropping an image and "trims" the unwanted portion of the image. The trimming is controlled using the Resizer X/Y Start/End Position registers (REG[0944h]-[094Ah] or REG[0964h]-[096Ah]). The Start and End addresses programmed in these registers are limited by the size of the actual camera image or the actual size of the decoded JPEG image and must not be set to a value greater than these actual sizes. The Start and End Position registers are set in 1 pixel increments.

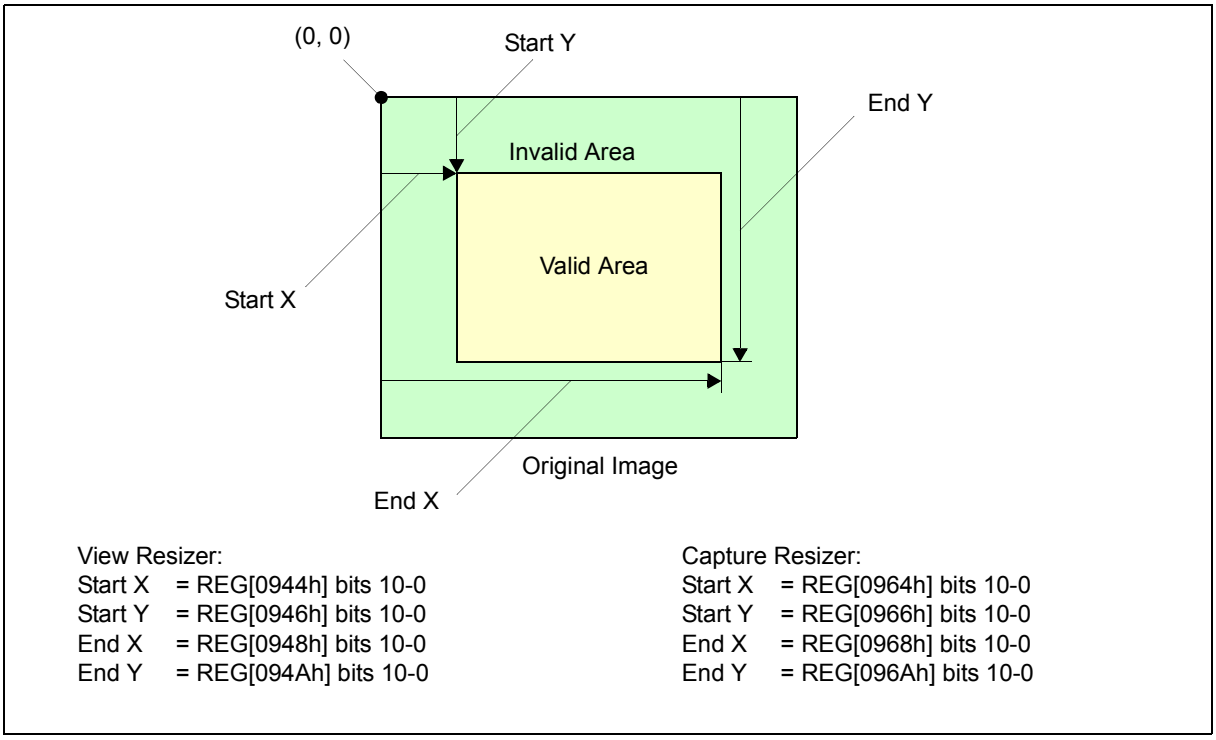


Figure 17-1: Trimming Function

17.2 Scaling Function

The scaling function takes place after the trimming stage and it specifies the desired compression ratio to be applied to the image. When image data is scaled by the capture resizer for JPEG Encoding, the JPEG Codec size registers must be set for the image size **after** scaling.

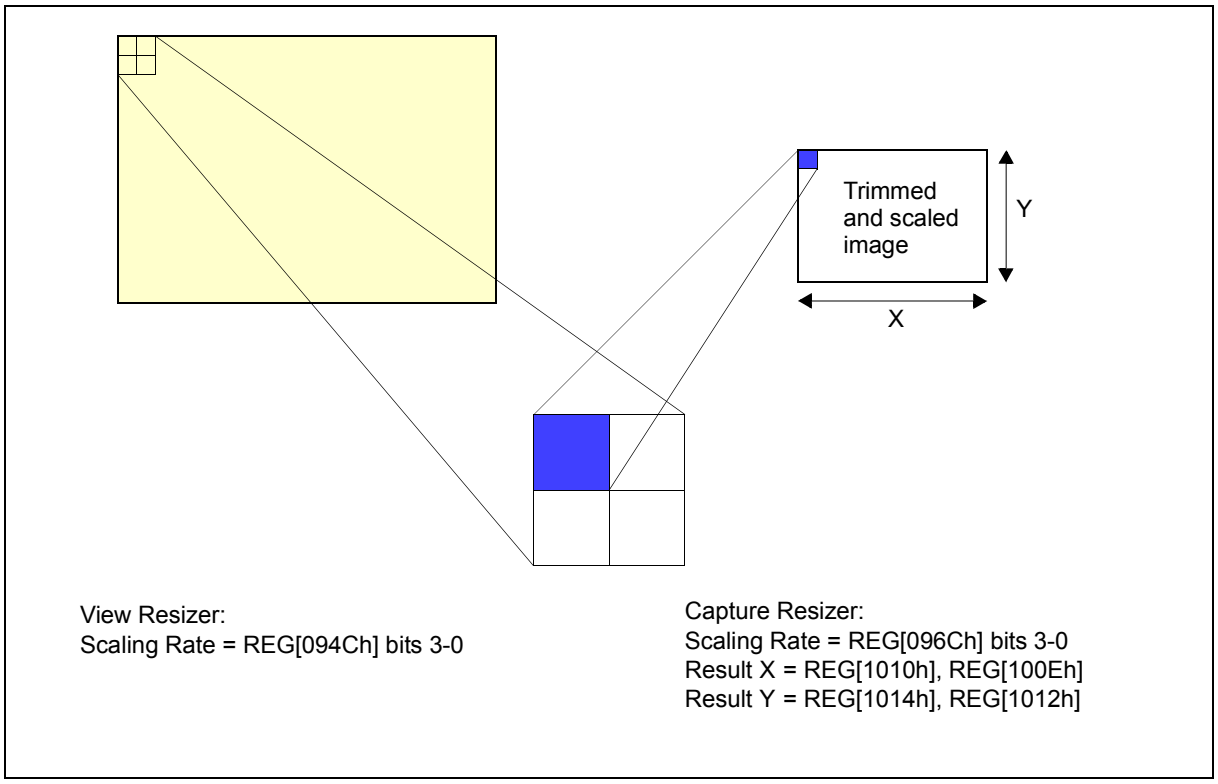


Figure 17-2: Scaling Example (1/2 Scaling)

17.2.1 1/2 Scaling

For 1/2 scaling, each 2x2 pixel block is scaled to 1 pixel. For the horizontal dimension, the scaling method can be either average or reduction (see REG[094Eh] or REG[096Eh]). For the vertical dimension, the scaling method is always reduction.

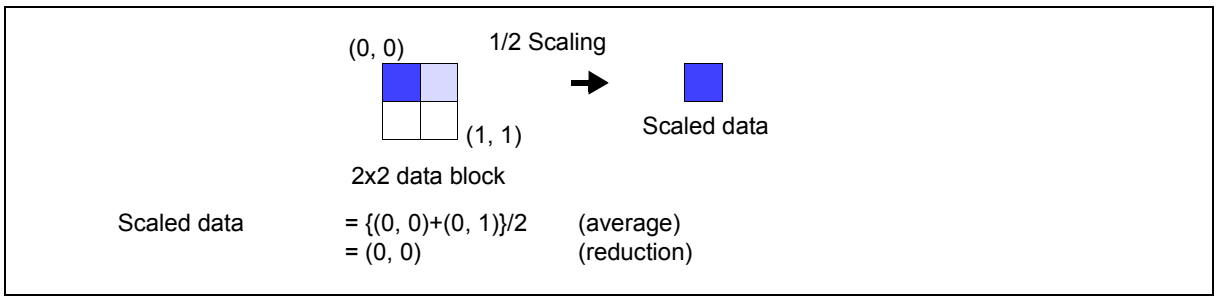


Figure 17-3: 1/2 Compression

17.2.2 1/3 Scaling

For 1/3 scaling, each 3x3 pixel block is scaled to 1 pixel. For both the horizontal and vertical dimensions, the scaling method is always reduction.

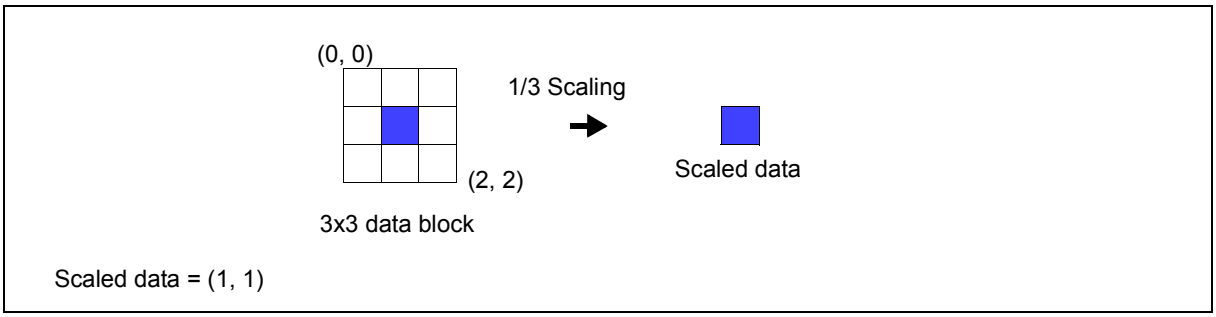


Figure 17-4: 1/3 Scaling

17.2.3 1/4 Scaling

For 1/4 scaling, each 4x4 pixel block is scaled to 1 pixel. For the horizontal dimension, the scaling method can be either average or reduction (see REG[094Eh] or REG[096Eh]). For the vertical dimension, the scaling method is always reduction.

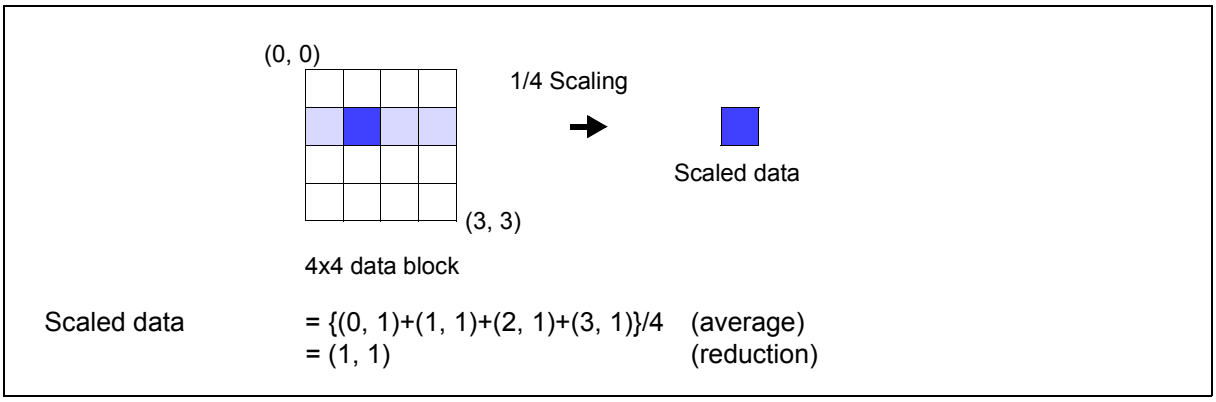


Figure 17-5: 1/4 Scaling

17.2.4 1/5 Scaling

For 1/5 Scaling, each 5x5 pixel block is scaled to 1 pixel. For both the horizontal and vertical dimensions, the scaling method is always reduction.

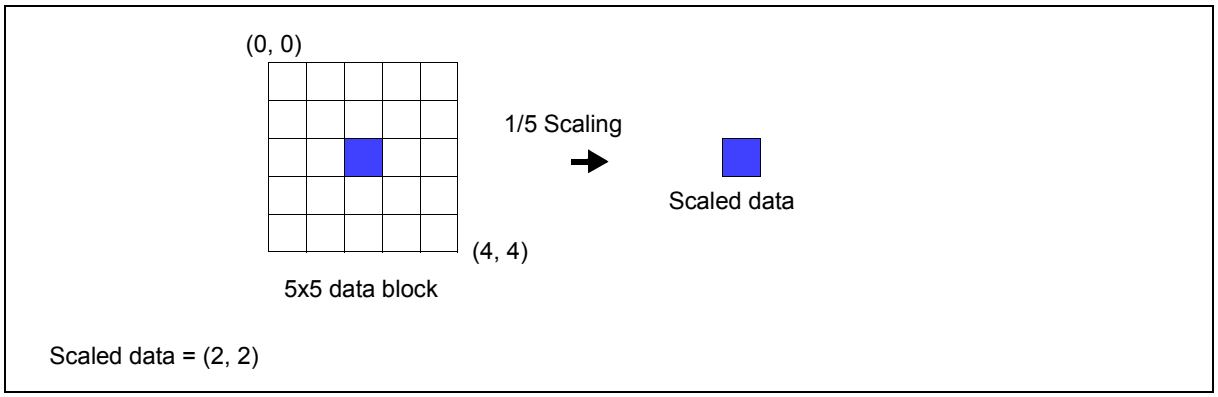


Figure 17-6: 1/5 Scaling

17.2.5 1/6 Scaling

For 1/6 scaling, each 6x6 pixel block is scaled to 1 pixel. For both the horizontal and vertical dimensions, the scaling method is always reduction.

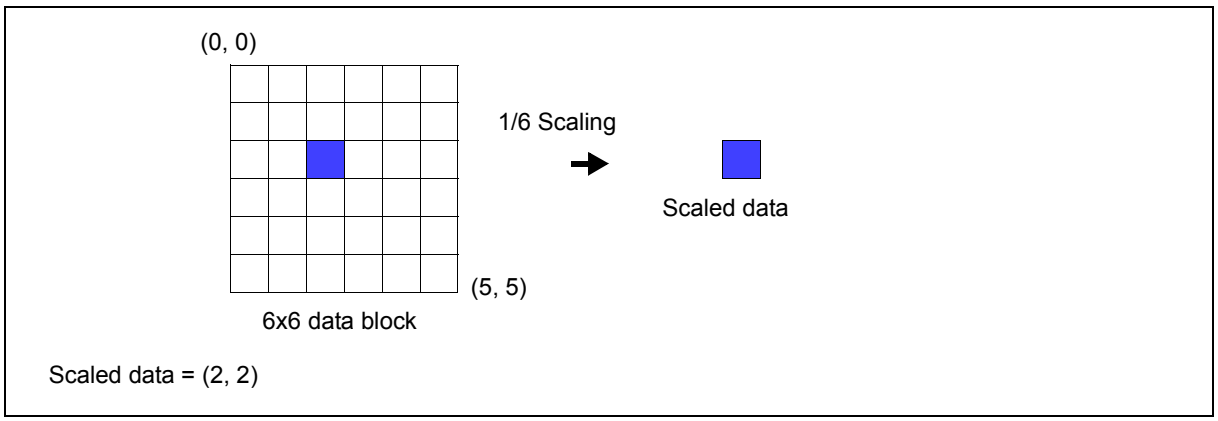


Figure 17-7: 1/6 Scaling

17.2.6 1/7 Scaling

For 1/7 scaling, each 7x7 pixel block is scaled to 1 pixel. For both the horizontal and vertical dimensions, the scaling method is always reduction.

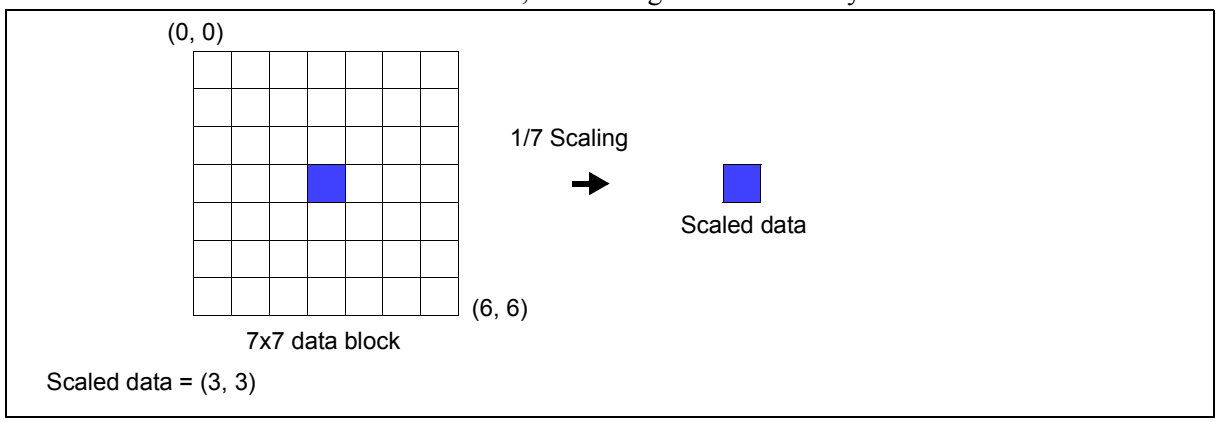


Figure 17-8: 1/7 Scaling

17.2.7 1/8 Scaling

For 1/8 scaling, each 8x8 pixel block is scaled to 1 pixel. For the horizontal dimension, the scaling method can be either average or reduction (see REG[094Eh] or REG[096Eh]). For the vertical dimension, the scaling method is always reduction.

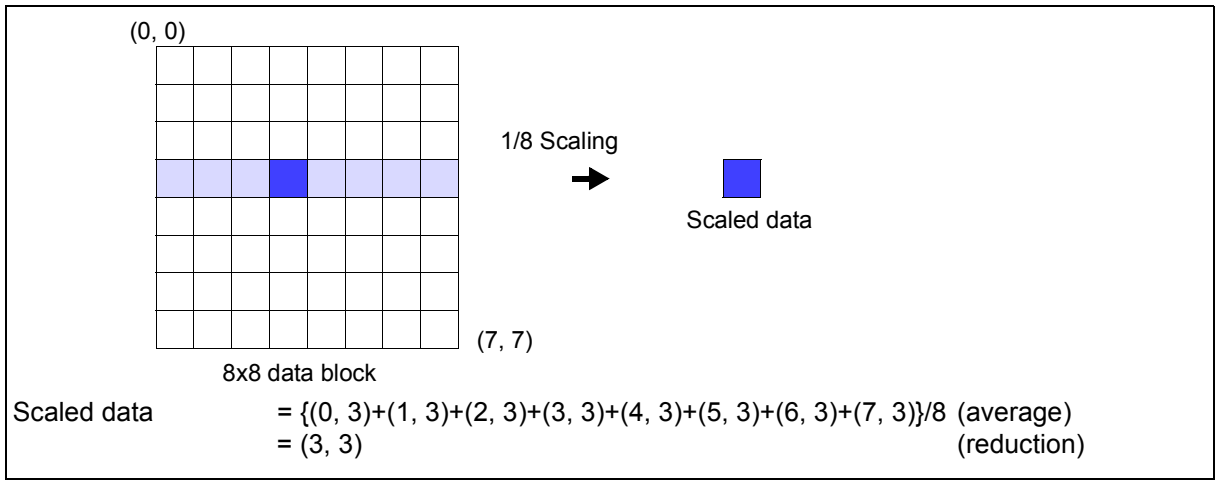


Figure 17-9: 1/8 Scaling

17.3 Resizer Restrictions

If any of the resizer registers must be changed while data is being received (from the camera interface, from the JPEG Decoder, or from the Host CPU), the View Resizer Register Update VSYNC Enable bit (REG[0940h] bit 1) or the Capture Resizer Update VSYNC Enable bit (REG[0960h] bit 1) must be set to 1 before changing any resizer register values.

The resizer X/Y Start/End Position registers must not be set larger than the incoming image size.

The dimensions specified by the View Resizer X/Y Start/End Position registers (REG[0944h] - REG[094Ah]) must be divisible by the View Resizer Scaling Rate (REG[094Ch] bits 5-0). The dimensions specified by the Capture Resizer X/Y Start/End Position registers (REG[0964h] - REG[096Ah]) must be divisible by the Capture Resizer Scaling Rate (REG[096Ch] bits 5-0).

Refer to the following table for a summary of the resizer horizontal restrictions.

Table 17-1: Resizer Horizontal Restrictions Summary

YUV Format	Scaling Rate	Start Position	Resolution	YUV Format	Scaling Rate	Start Position	Resolution	YUV Format	Scaling Rate	Start Position	Resolution
4:4:4	1/1	1 pixel	1 pixel	4:2:2 4:2:0	1/1	2 pixel	2 pixels	YUV 4:1:1	1/1	4 pixel	4 pixels
	1/2		2 pixels		1/2		2 pixels		1/2		4 pixels
	1/3		3 pixels		1/3		6 pixels		1/3		12 pixels
	1/4		4 pixels		1/4		4 pixels		1/4		4 pixels
	1/5		5 pixels		1/5		10 pixels		1/5		20 pixels
	1/6		6 pixels		1/6		6 pixels		1/6		12 pixels
	1/7		7 pixels		1/7		14 pixels		1/7		28 pixels
	1/8		8 pixels		1/8		8 pixels		1/8		8 pixels
	1/9		9 pixels		1/9		18 pixels		1/9		36 pixels
	1/10		10 pixels		1/10		10 pixels		1/10		20 pixels
	1/11		11 pixels		1/11		22 pixels		1/11		44 pixels
	1/12		12 pixels		1/12		12 pixels		1/12		12 pixels
	1/13		13 pixels		1/13		26 pixels		1/13		52 pixels
	1/14		14 pixels		1/14		14 pixels		1/14		28 pixels
	1/15		15 pixels		1/15		30 pixels		1/15		60 pixels
	1/16		16 pixels		1/16		16 pixels		1/16		16 pixels
	1/17		17 pixels		1/17		34 pixels		1/17		68 pixels
	1/18		18 pixels		1/18		18 pixels		1/18		36 pixels
	1/19		19 pixels		1/19		38 pixels		1/19		76 pixels
	1/20		20 pixels		1/20		20 pixels		1/20		20 pixels
	1/21		21 pixels		1/21		42 pixels		1/21		84 pixels
	1/22		22 pixels		1/22		22 pixels		1/22		44 pixels
	1/23		23 pixels		1/23		46 pixels		1/23		92 pixels
	1/24		24 pixels		1/24		24 pixels		1/24		24 pixels
	1/25		25 pixels		1/25		50 pixels		1/25		100 pixels
	1/26		26 pixels		1/26		26 pixels		1/26		52 pixels
	1/27		27 pixels		1/27		54 pixels		1/27		108 pixels
	1/28		28 pixels		1/28		28 pixels		1/28		28 pixels
	1/29		29 pixels		1/29		58 pixels		1/29		116 pixels
	1/30		30 pixels		1/30		30 pixels		1/30		60 pixels
	1/31		31 pixels		1/31		62 pixels		1/31		124 pixels
	1/32		32 pixels		1/32		32 pixels		1/32		32 pixels

Refer to the following table for a summary of the resizer vertical restrictions.

Table 17-2: Resizer Vertical Restrictions Summary

YUV Format	Scaling Rate	Start Position	Resolution	YUV Format	Scaling Rate	Start Position	Resolution
4:4:4 4:2:2 4:1:1	1/1	1 line	1 pixel	4:2:0	1/1	2 lines	2 pixels
	1/2		2 pixels		1/2		2 pixels
	1/3		3 pixels		1/3		6 pixels
	1/4		4 pixels		1/4		4 pixels
	1/5		5 pixels		1/5		10 pixels
	1/6		6 pixels		1/6		6 pixels
	1/7		7 pixels		1/7		14 pixels
	1/8		8 pixels		1/8		8 pixels
	1/9		9 pixels		1/9		18 pixels
	1/10		10 pixels		1/10		10 pixels
	1/11		11 pixels		1/11		22 pixels
	1/12		12 pixels		1/12		12 pixels
	1/13		13 pixels		1/13		26 pixels
	1/14		14 pixels		1/14		14 pixels
	1/15		15 pixels		1/15		30 pixels
	1/16		16 pixels		1/16		16 pixels
	1/17		17 pixels		1/17		34 pixels
	1/18		18 pixels		1/18		18 pixels
	1/19		19 pixels		1/19		38 pixels
	1/20		20 pixels		1/20		20 pixels
	1/21		21 pixels		1/21		42 pixels
	1/22		22 pixels		1/22		22 pixels
	1/23		23 pixels		1/23		46 pixels
	1/24		24 pixels		1/24		24 pixels
	1/25		25 pixels		1/25		50 pixels
	1/26		26 pixels		1/26		26 pixels
	1/27		27 pixels		1/27		54 pixels
	1/28		28 pixels		1/28		28 pixels
	1/29		29 pixels		1/29		58 pixels
	1/30		30 pixels		1/30		30 pixels
	1/31		31 pixels		1/31		62 pixels
	1/32		32 pixels		1/32		32 pixels

18 Digital Video Functions

The following is an overview block diagram of how the digital video functions interact.

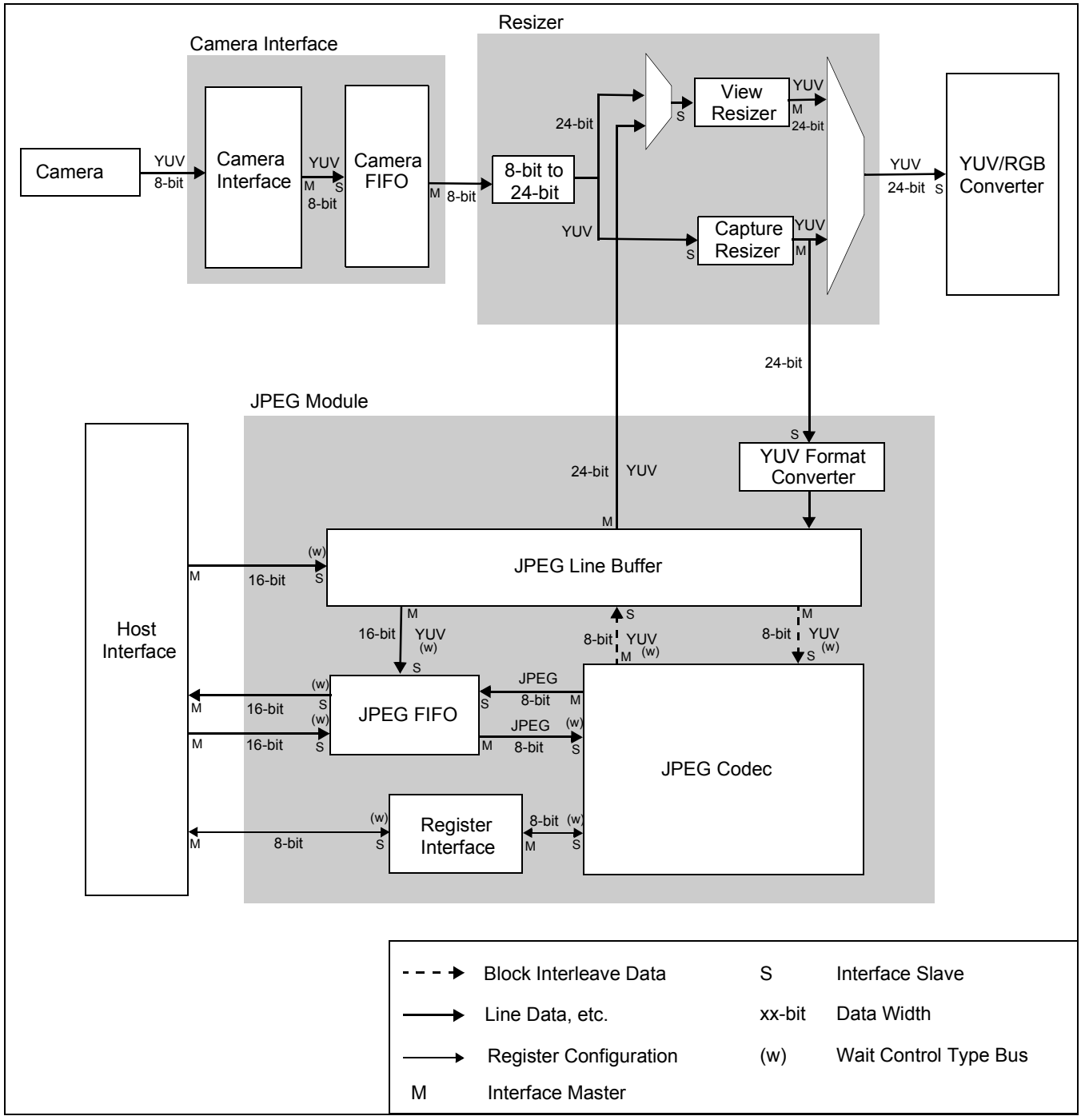


Figure 18-1: Digital Video Functions

18.1 Display Image Data from the Camera Interface

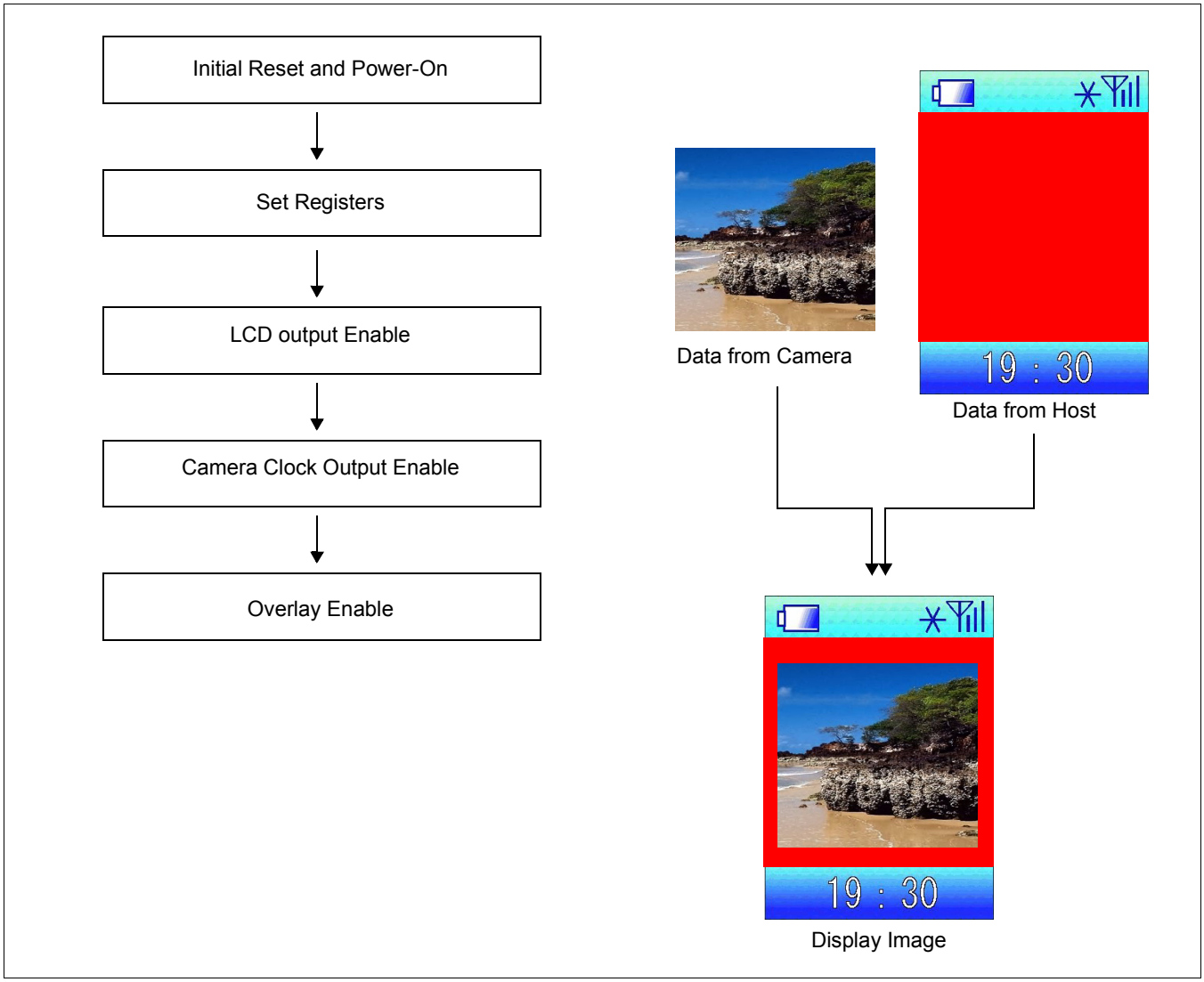


Figure 18-2: Display Image Data from the Camera Interface

18.2 JPEG Encode and Camera Data to the Host

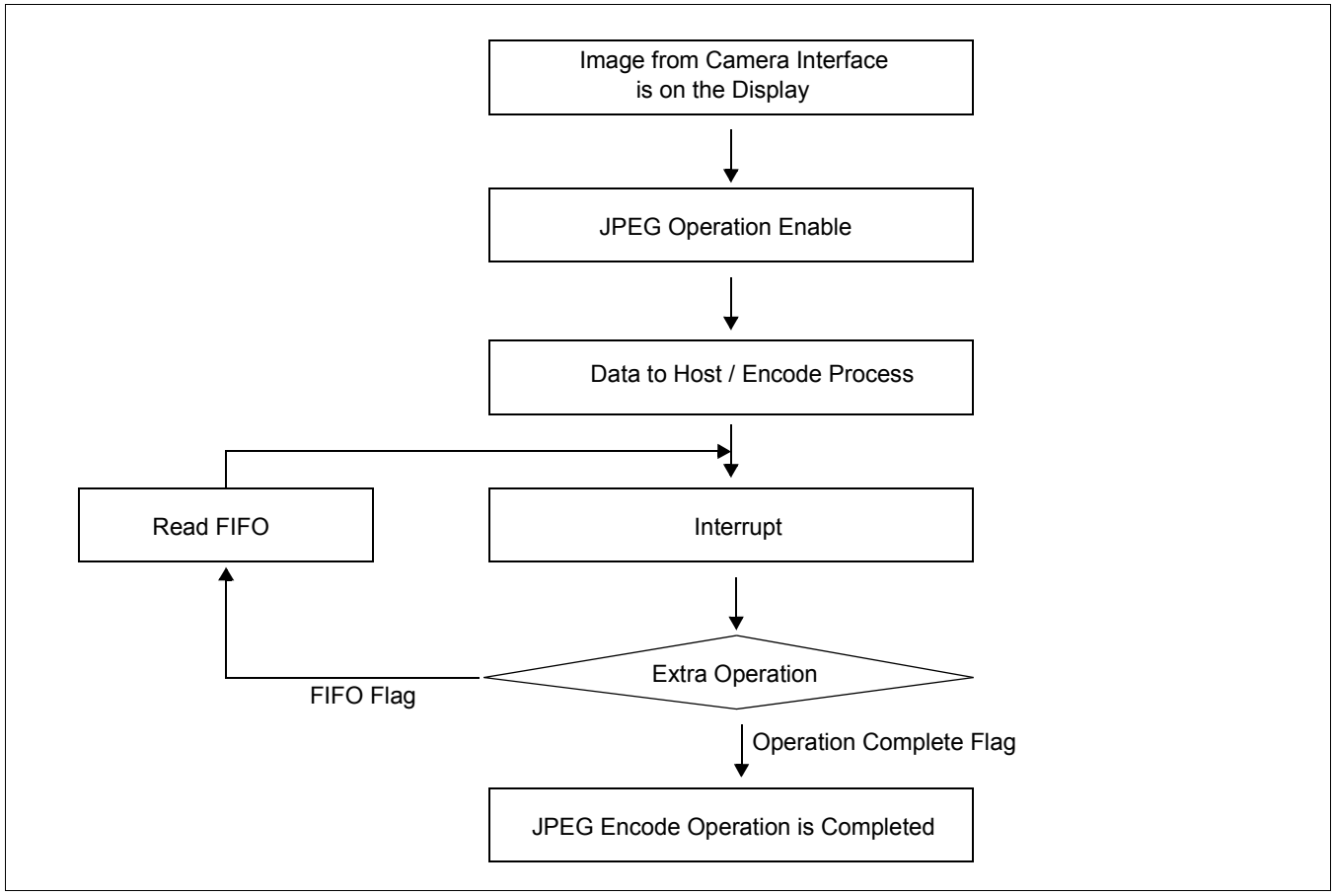


Figure 18-3: JPEG Encode Data from the Camera Interface

18.3 JPEG Decode and Display Data from the Host

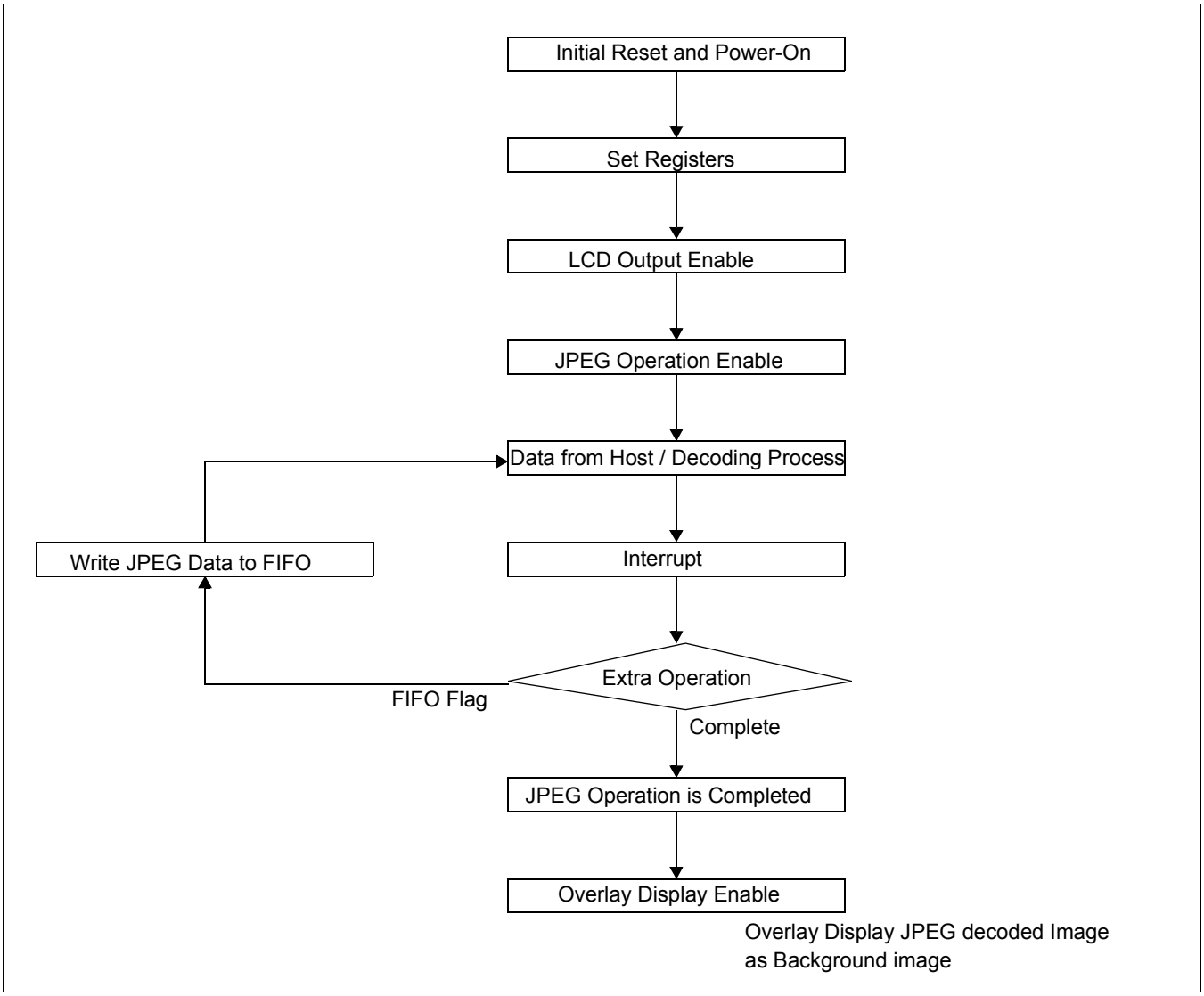


Figure 18-4: JPEG Decode and Display Data from the Host

18.4 JPEG 180° Rotate Encode Diagram

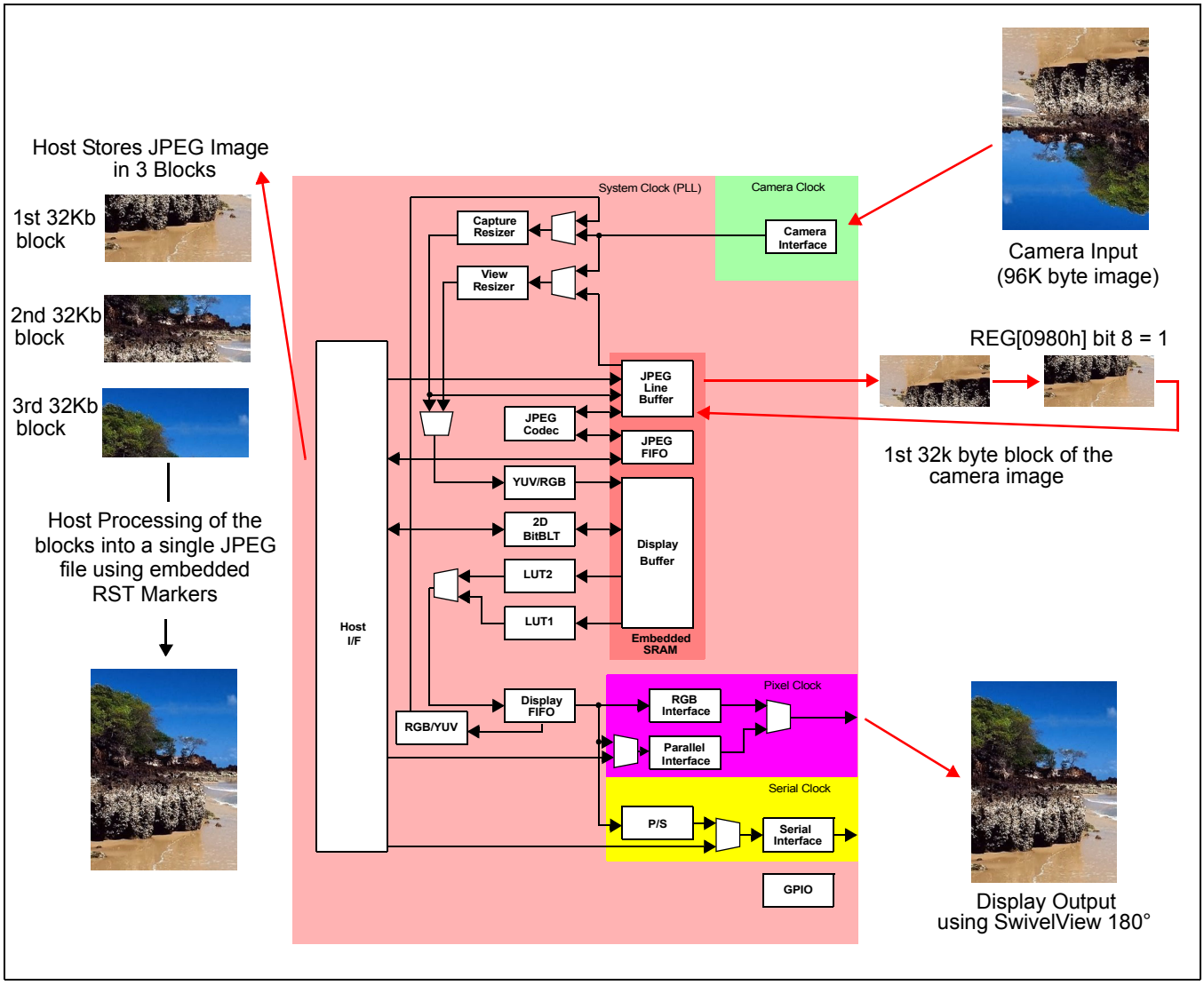


Figure 18-5: JPEG 180° Rotate Encode Diagram

19 JPEG Encode/Decode Operation

The S1D13717 JPEG Codec is based on the JPEG baseline standard and the arithmetic accuracy satisfies the requirement of the compatibility test of JPEG Part-2 (ISO/IEC10918-2). The maximum image size is 1600 x 1200 and the image to be compressed/decompressed must be YUV format with a minimum resolution as shown in Table 19-1: “Minimum Resolution Restrictions”.

The following image restrictions must be observed for JPEG encode/decode, YUV data input from the Host (only YUV 4:2:2, 4:2:0), and YUV data to the Host (only YUV 4:2:2, 4:2:0). The image must be in YUV format and the minimum image resolution must be set based on the YUV format as follows.

Table 19-1: Minimum Resolution Restrictions

YUV Format	Minimum Resolution
4:4:4 (decode only)	1x1
4:2:2 (encode/decode)	2x1
4:2:0 (encode/decode)	2x2
4:1:1 (encode/decode)	4x1

The quantization table accommodates two compression tables and four decompression tables. The Huffman table accommodates two tables for each AC and DC. It is possible to insert markers (up to a 36 byte maximum size) during the encoding process. Markers which can be processed and automatically translated during the decoding process are SOI, SOF0, SOS, DQT, DHT, DRI, RSTm and EOI. The decoding process supports YUV 4:4:4, YUV 4:2:2, YUV 4:1:1 and YUV 4:2:0, and the encoding process supports YUV 4:2:2, 4:1:1 and 4:2:0 format. RGB format is not supported. The image data processing ratio is almost less than 1/15 second at 640x480 resolution. However, the image data processing ratio is not guaranteed since it depends on the image data, the Huffman table and the quantization table.

19.1 JPEG Features

19.1.1 JPEG FIFO

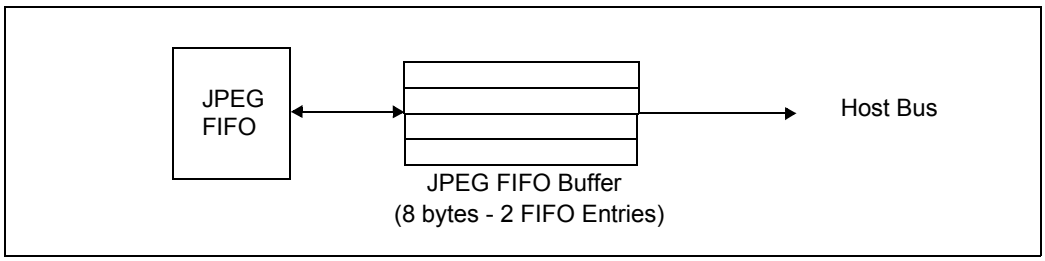


Figure 19-1: JPEG FIFO Overview

The JPEG FIFO is mapped at the beginning of the display buffer and is programmable to a maximum size of 128K bytes using REG[09A4h]. The JPEG file size and Host CPU performance should be considered when determining the JPEG FIFO size.

The status of the JPEG FIFO can be checked using the JPEG FIFO Status register (REG[09A2h]). It is also possible to indicate the JPEG FIFO status using interrupts via the JPEG Interrupt Control register (REG[0986h]).

The JPEG FIFO must be read by the Host CPU during the JPEG encode process. There are two methods.

1. High Performance - Before reading the JPEG FIFO, check how much data is available in the FIFO using the status bits in the JPEG FIFO Status register (REG[09A2h]). Next, read the FIFO through REG[09A6h] based on the available amount of data. Note that the FIFO must be read twice for each entry in the FIFO (32-bit FIFO but only 16-bit read/write port). Continue to check and read the FIFO until it is empty. This method offers the best performance because it is possible to transfer the block of data in the FIFO without a FIFO status check for each entry. If the JPEG FIFO is read while no data is in the FIFO, a terminate cycle will occur and no data will be read from the FIFO.

2. Low Performance - Before reading the JPEG FIFO, confirm that the FIFO is not empty using the JPEG FIFO Empty Status bit (REG[09A2h] bit 0) and JPEG FIFO Threshold Status bits (REG[09A2h] bits 3-2). After confirmation, read one entry from the FIFO. Note that the FIFO must be read twice for each entry in the FIFO (32-bit FIFO but only 16-bit read/write port).

The JPEG FIFO must be written by the Host CPU during the JPEG decode process. Much like the methods for reading the JPEG FIFO, writing to the JPEG FIFO can be done entry by entry or as a block of data once it has been determined how many entries are available in the JPEG FIFO.If the JPEG FIFO is full and data is written to it by the Host CPU, a terminate cycle will occur and no data will be read from the FIFO.

19.1.2 JPEG Codec Interrupts

The JPEG codec can generate the following interrupts to avoid continuously poling the JPEG status bits. Using interrupts decreases the CPU load for a JPEG process. For information on the JPEG Interrupt register bits, see the register descriptions in Section 10.4.14, "JPEG Module Registers" on page 209.

1. **JPEG Codec Interrupt Flag (REG[0982h] bit 1)**
   This flag is asserted when all JPEG processes have finished without errors, or during the decode process when a RST marker process error is detected. This interrupt flag should be enabled when RST marker error detection is enabled.

   However, if the RST marker is not required during the decode process, confirm that the operation has finished using the JPEG Decode Complete Flag (REG[0982h] bit 5). For the encoding process, confirm that the operation has finished using the JPEG FIFO Empty Flag (REG[0982h] bit 8) and the JPEG Operation Status bit (REG[1004h] bit 0).

2. **JPEG Line Buffer Overflow Flag (REG[0982h] bit 2)**
   If the JPEG FIFO is read slower than the JPEG Line Buffer is written to during the encoding process, this flag is asserted when the JPEG Line Buffer overflows. This flag should be enabled for JPEG encoding.

3. **JPEG Decode Marker Read Flag (REG[0982h] bit 4)**
   During JPEG decoding, this flag is asserted when marker information is read from the JPEG file. Marker information may include resize settings or LCD settings. JPEG decoding is stopping while this flag is asserted and does not restart until after this flag is cleared (REG[0986h] bit 4 = 0).

4. **JPEG Decode Complete Flag (REG[0982h] bit 5)**
   This flag is asserted after the JPEG decode process is finished and the decompressed image data is stored in memory. This flag is useful as a trigger for enabling the overlay or display of the image.

5. **JPEG FIFO Empty Flag (REG[0982h] bit 8)**
   This flag is asserted when the JPEG FIFO is empty. For the decode process, this flag is useful for timing JPEG data writes to the FIFO and to identify when the JPEG decode process is finished completely. For the encode process, this flag indicates that the entire JPEG file has been read by the host.

6. **JPEG FIFO Full Flag (REG[0982h] bit 9)**
   This flag is asserted when the JPEG FIFO is full. For the encode process, this flag is used as a trigger for increasing the priority of host reads to the FIFO. For the decode process, this flag indicates if it is possible to write data to the FIFO.

7. **JPEG FIFO Threshold Trigger Flag (REG[0982h] bit 10)**
   This flag is asserted when the amount of data in the JPEG FIFO meets the condition programmed into the JPEG FIFO Trigger Threshold bits (REG[09A0h] bits 5-4). This flag is useful for timing when the host will start to read JPEG compressed data in the FIFO.

8. **Encode Size Limit Violation Flag (REG[0982h] bit 11)**
   This flag is asserted when the compressed JPEG data size is greater than the programmed size in the JPEG Encode Size Limit registers (see REG[09B0h] - REG[09B2h]).

19.1.3 JPEG Bypass Modes

The S1D13717 can bypass the JPEG Codec in order for the Host CPU to capture raw YUV data from the camera interface (YUV Data Capture Mode). The S1D13717 can also bypass the JPEG Codec in order for the Host CPU to send raw YUV data to be displayed (YUV Data Display Mode). For YUV Data Capture Mode, YUV data is still sent to the Host CPU through the JPEG FIFO which is accessed through REG[09A6h]. For YUV Data Display Mode, the JPEG FIFO is bypassed and the Host CPU writes YUV data directly to the JPEG Line Buffer using the JPEG Line Buffer Write Port (REG[09E0h]).

The raw YUV data can be in either of the two YUV format as follows (YUV 4:2:2 = 2x1, YUV 4:2:0 = 2x2).

	YUV 4:2:2	**YUV 4:2:0**
Nth line	UYVYUYVY	UYVYUYVY
N+1th line	UYVYUYVY	YYYYYYYY

19.2 Example Sequences

19.2.1 JPEG Encoding Process

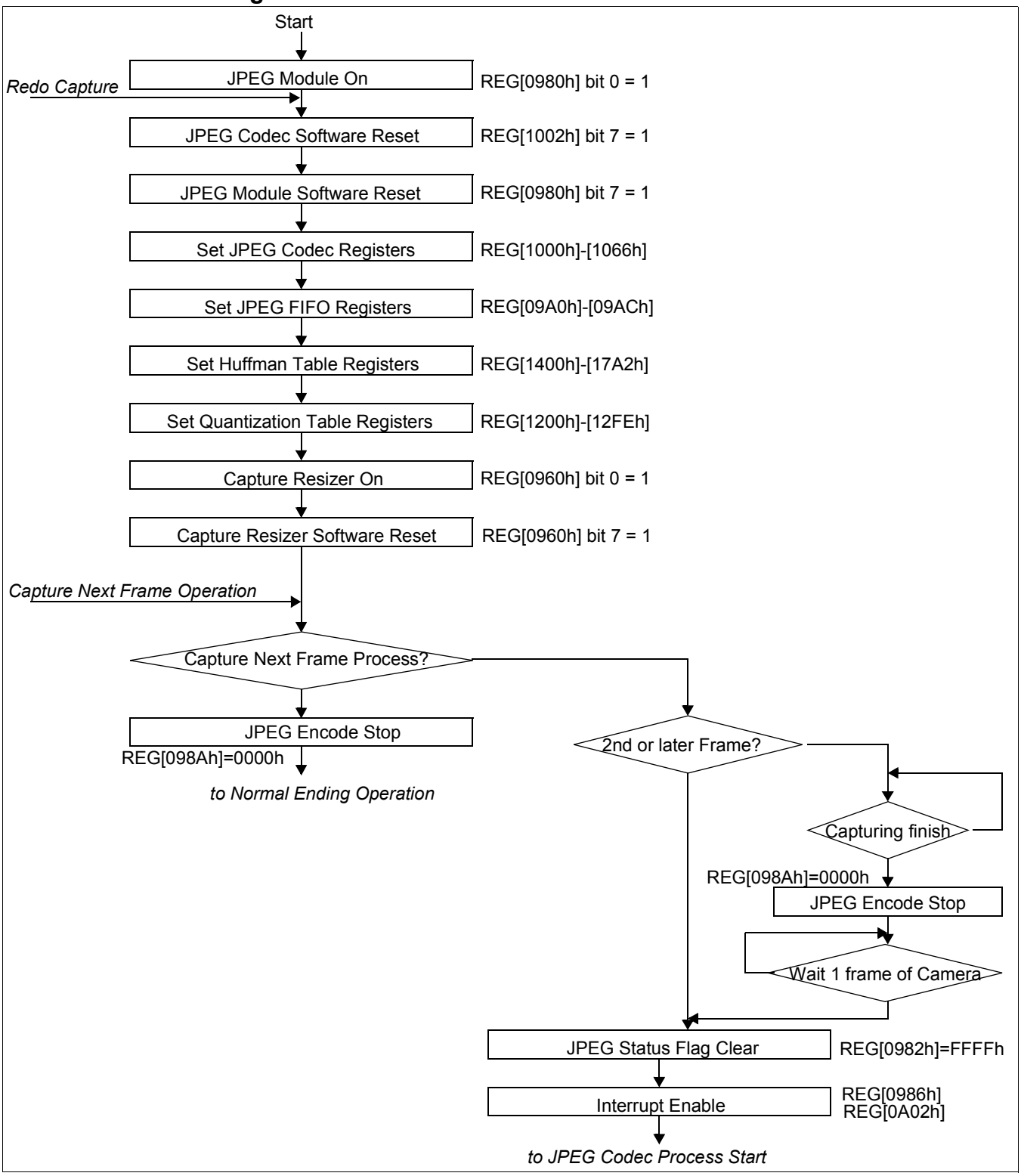


Figure 19-2: JPEG Encoding Process (1 of 4)

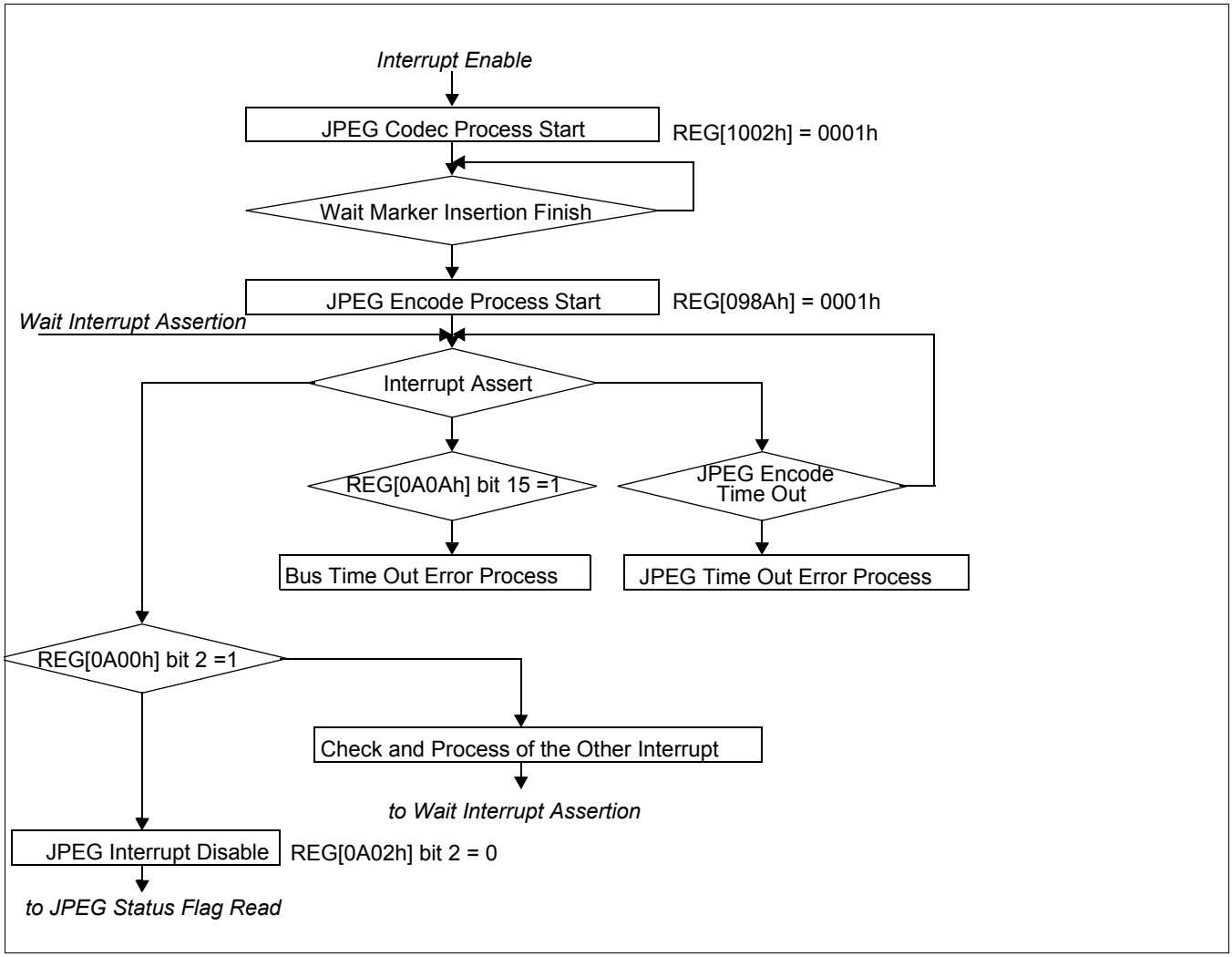


Figure 19-3: JPEG Encoding Process (2 of 4)

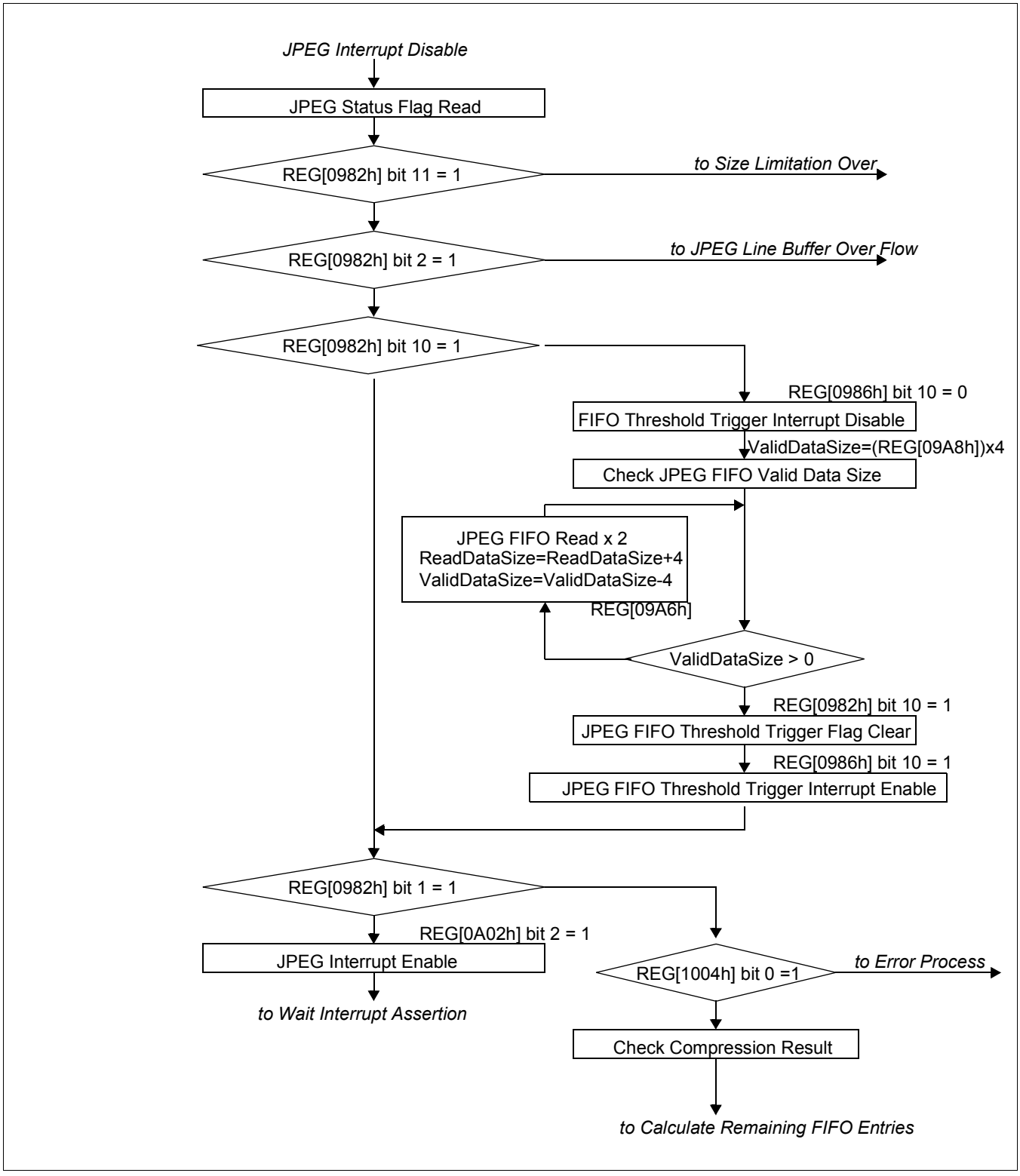


Figure 19-4: JPEG Encoding Process (3 of 4)

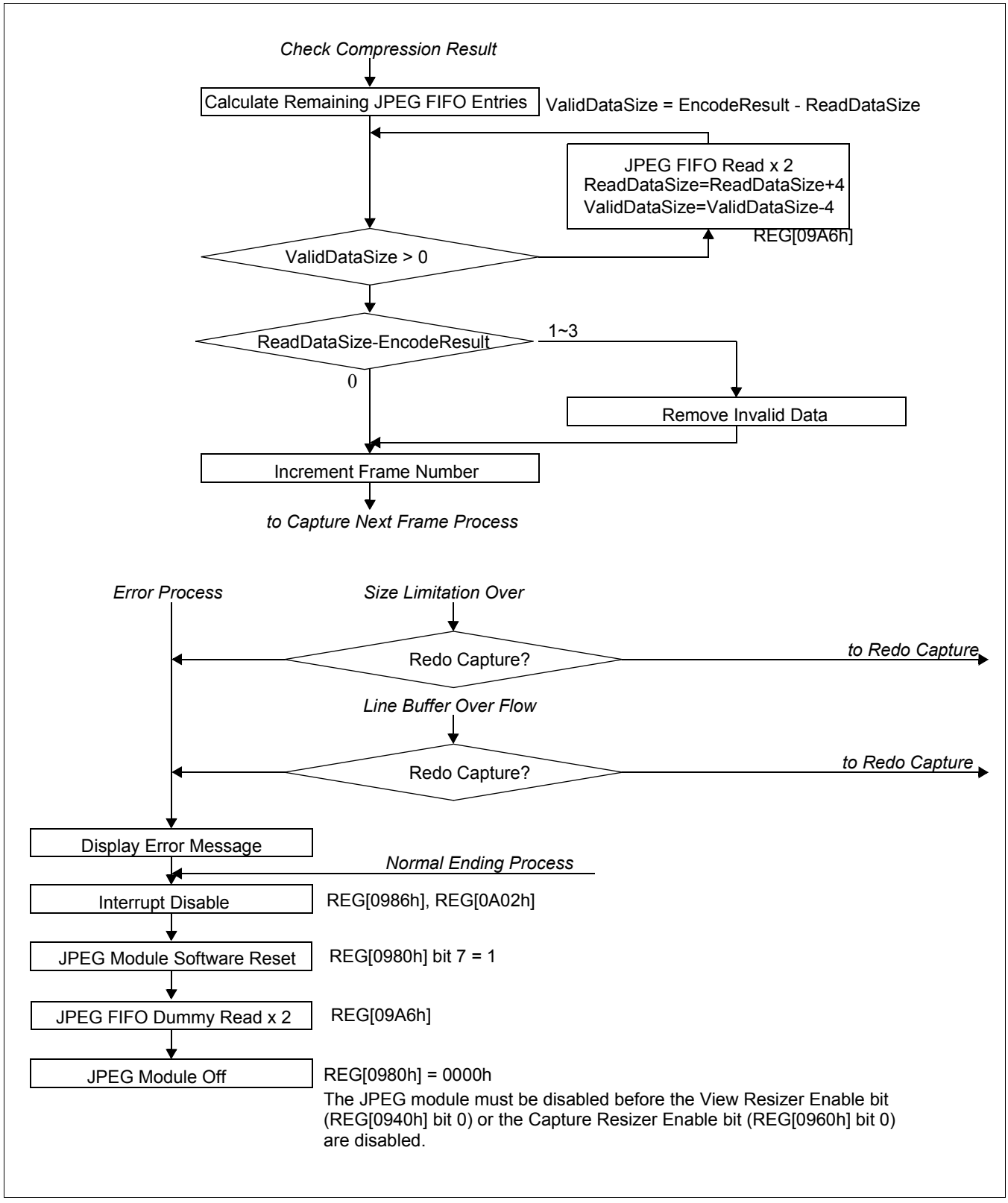


Figure 19-5: JPEG Encoding Process (4 of 4)

1. Initialize the camera interface registers (REG[0100h]-[0124h]).
2. Enable the JPEG module, set REG[0980h] bits 3-0 = 0001b.
3. Initialize the JPEG Codec registers.
    a. Software reset the JPEG codec, set REG[1002h] bit 7 = 1.
    b. Select the operation mode for encoding, set REG[1000h] bit 2 = 0.
    c. Set the desired quantization table number (REG[1006h]) and the huffman table number (REG[1008h]).
    d. Select the DRI setting (REG[100Ah]-[100Ch]).
    e. Configure the vertical pixel size (REG[100Eh]-[1010h]) and the horizontal pixel size (REG[1012h]-[1014h]).
    f. Set the Insertion Marker Data in REG[1020h]-[1066h]. When REG[1000h] bit 3 = 1, the data in these registers is written to the JPEG file. Unused bits must be written as FFh.
    g. Initialize Quantization Table No. 0 (REG[1200h]-[127Eh]) and Quantization Table No. 1 (REG[1280h]-[12FEh]) with the following sequence.

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64

h. Set DC Huffman Tables and the AC Huffman Tables according to ISO/IEC 10918 attachment K, each numerical formula is specified as follows:

DC Huffman Table No. 0 Register 0 (REG[1400h-141Eh]) is set as A
DC Huffman Table No. 0 Register 1 (REG[1420h-1436h]) is set as B
AC Huffman Table No. 0 Register 0 (REG[1440h-145Eh]) is set as C
AC Huffman Table No. 0 Register 1 (REG[1460h-15A2h]) is set as D
DC Huffman Table No. 1 Register 0 (REG[1600h-161Eh]) is set as E
DC Huffman Table No. 1 Register 1 (REG[1620h-1636h]) is set as F
AC Huffman Table No. 1 Register 0 (REG[1640h-165Eh]) is set as G
AC Huffman Table No. 1 Register 1 (REG[1660h-17A2h]) is set as H

A:	00h, 01h, 05h, ..., 00h, 00h	16 byte
B:	00h, 01h, 02h, ..., 0Ah, 0Bh	12 byte
C:	00h, 02h, 01h, 03h, ...01h, 7Dh	16 byte
D:	01h, 02h, 03h, ..., F9h, FAh	162 byte
E:	00h, 03h, 01h, ..., 00h, 00h	16 byte
F:	00h, 01h, 02h, ..., 0Ah, 0Bh	12 byte
G:	00h, 02h, 01h, 02h, ..., 02h, 77h	16 byte
H:	00h, 01h, 02h, ..., F9h, FAh	162 byte

4. Set the JPEG module registers.

   a. Enable the JPEG module and perform a JPEG software reset (REG[0980h] = 81h).

   b. Specify the JPEG FIFO size (REG[09A4h]). The FIFO size is determined using the following formula:

      JPEG FIFO size = ((REG[09A4h] bits 3-0) + 1) x 4K bytes.

      Example: for a JPEG FIFO size of 12K bytes, REG[09A4h] = 2
      (2 + 1) x 4KB = 12K bytes

   c. Set the Encode Size Limit (REG[09B0h]-[09B2h]) in bytes. To generate an interrupt when the encode size limit is exceeded use the Encode Size Limit Violation Flag (REG[0982h] bit 11).

   d. Clear the JPEG FIFO (REG[09A0h] bit 2 = 1).

   e. Set the JPEG FIFO Threshold Trigger (REG[09A0h] bits 5-4).

5. Set the capture resizer registers. The vertical and horizontal dimensions must be the same as the JPEG vertical and horizontal sizes as programmed in step 3e.

6. Start the encode process.
    a. Clear all status bits by writing REG[0982h] as FFFFh
    b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0E07h.
    c. Start the JPEG operation (REG[1002h] bit 0 = 1)
    d. Start capturing (REG[098Ah] bit 0 = 1)

    After setting REG[1002h] bit 0 = 1, 2ms (internal system clock = 50Mhz) is required to generate the Markers. If REG[098Ah] bit 0 is set to 1 before 2ms, capturing will start only after generating the Markers (after 2 ms has passed).

Host CPU Process

7. Wait for the JPEG FIFO Threshold condition to be met. This can be done using the JPEG FIFO Threshold Interrupt (see REG[0986h]) or by polling the JPEG FIFO Threshold Status bits (REG[0982h] bits 13-12). If the interrupt method is used, the interrupt should be disabled after it is asserted.
8. Confirm the FIFO Valid Data Size (REG[09A8h]).
9. Read the JPEG FIFO Read/Write register twice (REG[09A6h]). Two reads from the 16-bit FIFO read/write register are required to get the entire 32-bit FIFO entry.
10. If using the interrupt method, the interrupt should be re-enabled again.
11. Loop steps 7 through 9 continuously until the FIFO Valid Data Size reaches 0 (REG[09A8h] = 0) and the JPEG Operation Status is idle (REG[1004h] bit 0 = 0).
12. When the encode process finishes, check the actual file size with the Encode Size Result registers (REG[09B4h]-[09B6h]).
13. Confirm the process is complete with the JPEG Codec Interrupt Flag (REG[0982h] bit 1).
14. Stop the JPEG codec using the JPEG Start/Stop Control bit (REG[098Ah] bit 0 = 0).

19.2.2 JPEG Decoding Process

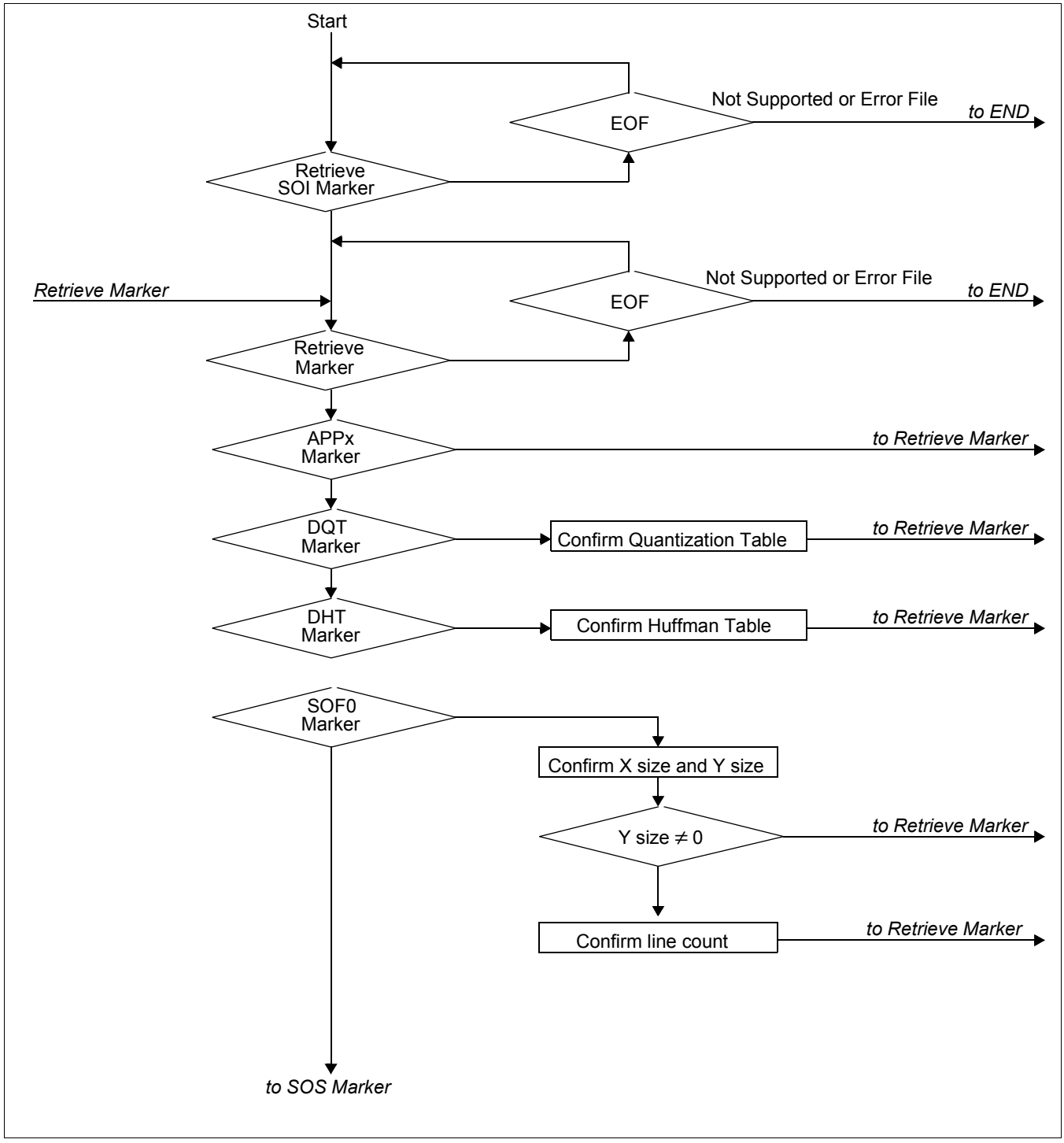


Figure 19-6: JPEG Decoding Process (1 of 6)

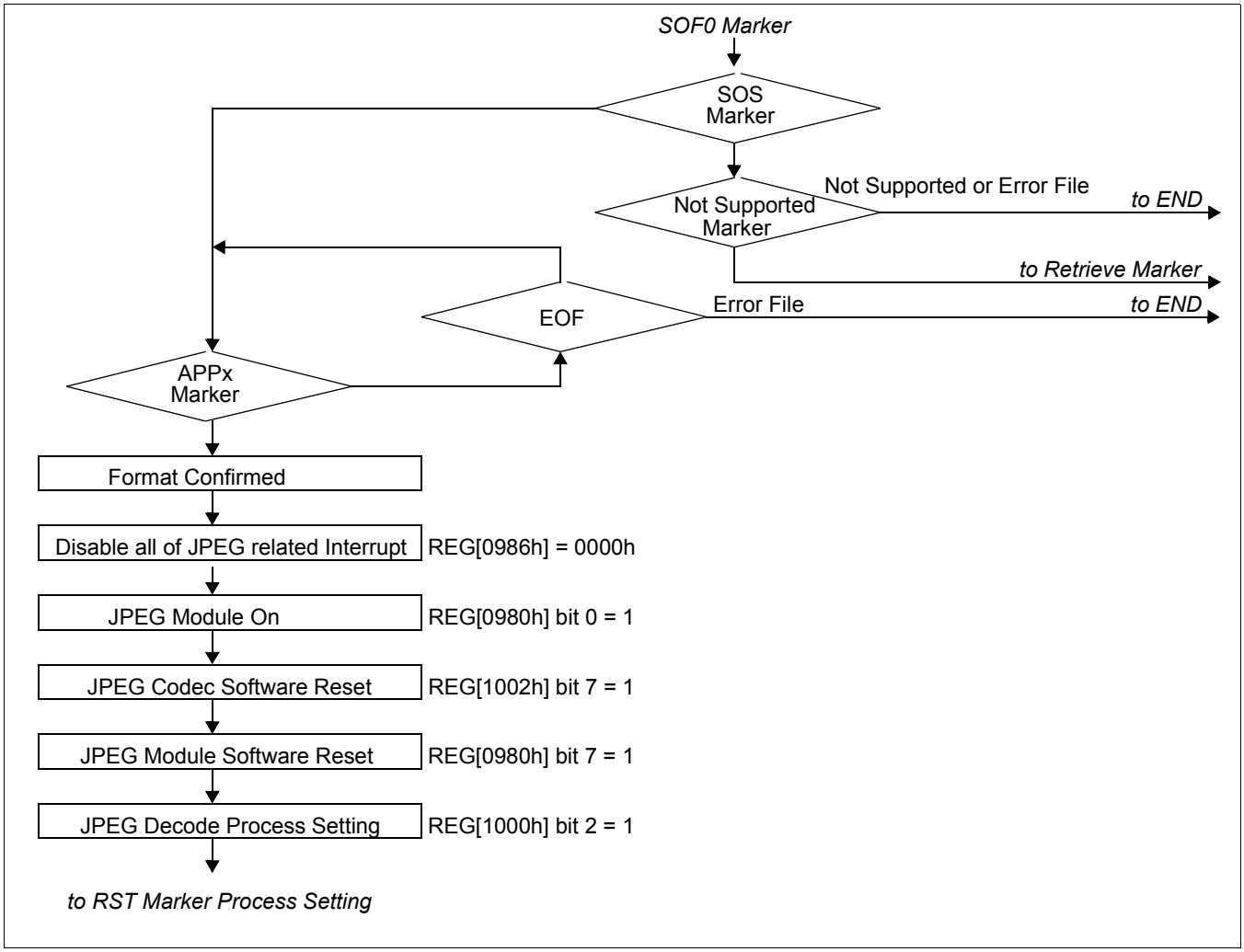


Figure 19-7: JPEG Decoding Process (2 of 6)

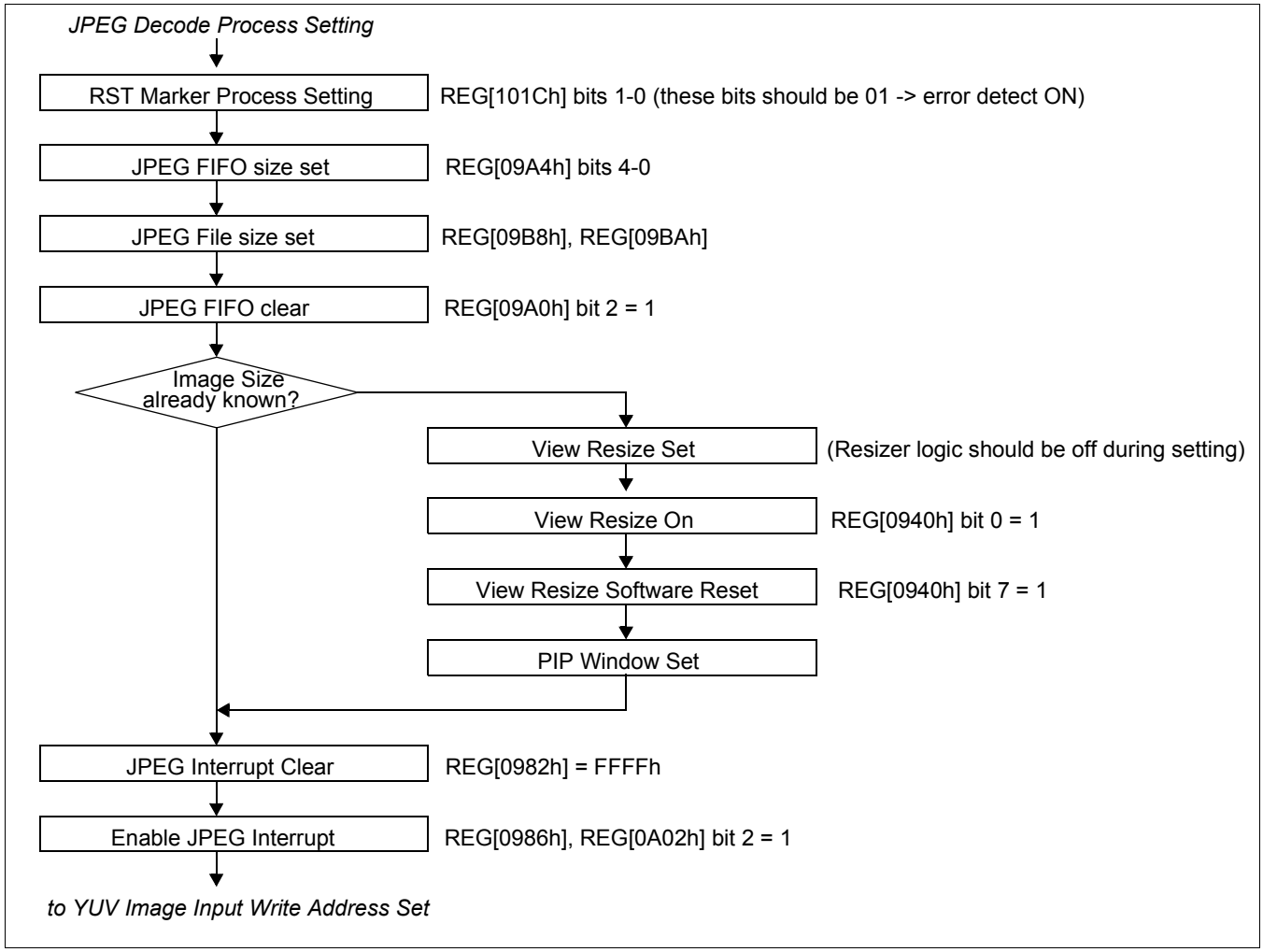


Figure 19-8: JPEG Decoding Process (3 of 6)

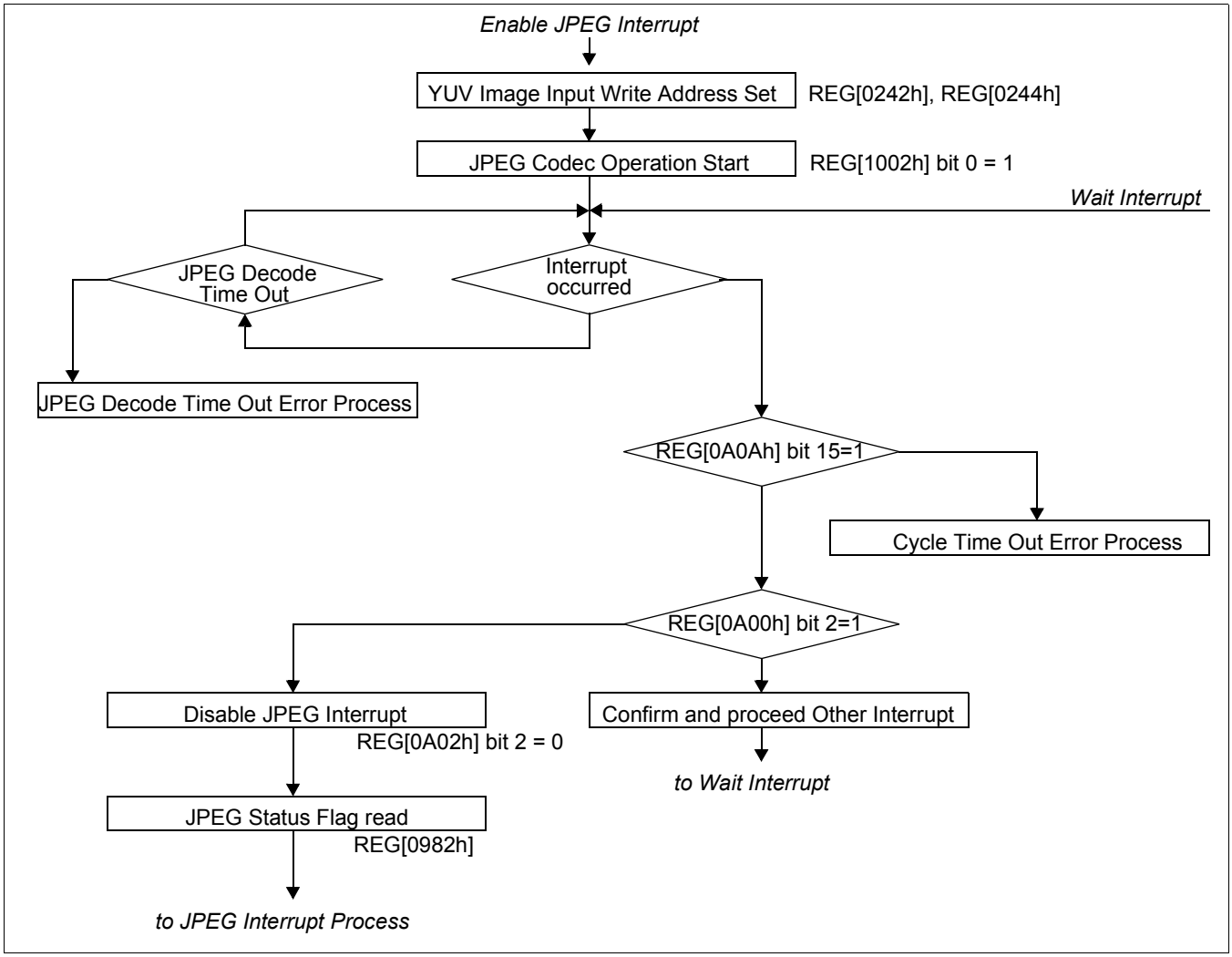


Figure 19-9: JPEG Decoding Process (4 of 6)

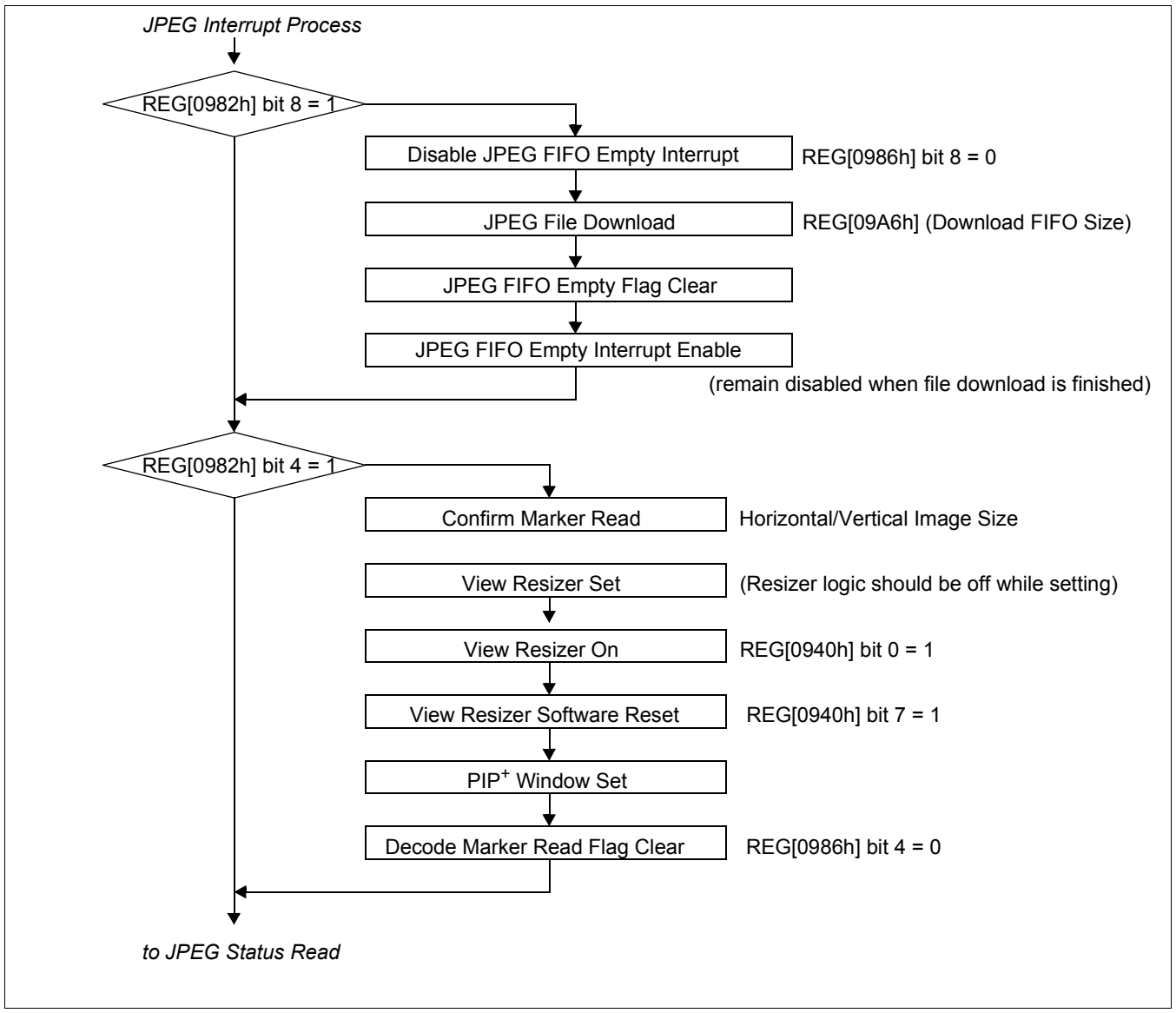


Figure 19-10: JPEG Decoding Process (5 of 6)

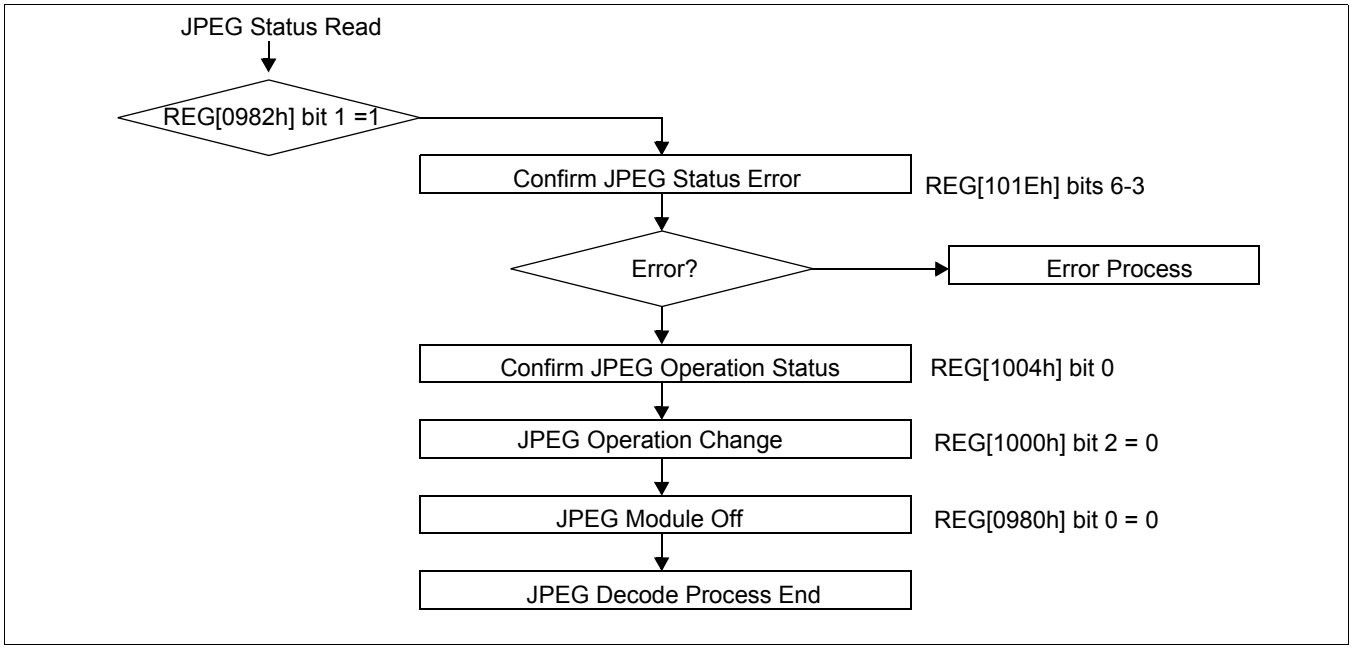


Figure 19-11: JPEG Decoding Process (6 of 6)

1. Enable the JPEG codec, set REG[0980h] bits 3-0 to 0001.
2. Initialize the JPEG Codec registers.
    a. Software reset the JPEG codec, set REG[1002h] bit 7 to 1.
    b. Select the operation mode for JPEG decoding, set REG[1000h] bit 2 = 1.
    c. Set the RST Marker Operation Setting, set REG[101Ah].
3. Set the JPEG module registers.
    a. Enable the JPEG module and perform a JPEG software reset (REG[0980h] = 81h).
    b. Specify the JPEG FIFO size (REG[09A4h]). The FIFO size is determined using the following formula:

       JPEG FIFO size = ((REG[09A4h] bits 3-0) + 1) x 4K bytes.

       Example: for a JPEG FIFO size of 12K bytes, REG[09A4h] = 2
       (2 + 1) x 4KB = 12K bytes
    c. specify the JPEG file size, set REG[09B8h]-[09BAh].
    d. Clear the JPEG FIFO (REG[09A0h] bit 2 = 1).

4. If the image size and the YUV format are already known, set the registers for the view resizer. If they are not known, read the data after stopping the JPEG decode process using the Decode Marker Read Interrupt (REG[0986h] bit 4).

5. Start decoding process.

    a. Clear all status bits, set REG[0982h] to FFFFh

    b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0133h.

    c. Start the JPEG operation (REG[1002h] bit 0 = 1).

Host CPU Process

6. After confirming FIFO valid data size (REG[09A8h]), write data to the JPEG FIFO.

7. Wait for FIFO Empty by interrupt or polling.
   If the Decode Marker Read Interrupt is enabled, there is an interrupt between steps 6 and 7. After reading data from the registers, disable the interrupt enable and clear the interrupt. Then set the registers for the view resizer.

8. Repeat steps 6 and 7 until the end of the JPEG file is detected.

9. If the JPEG Decode Complete Interrupt is enabled, there is an interrupt when the end of file marker is written to the JPEG FIFO.

10. Verify that the JPEG decode operation is complete (REG[1004h] bit 0 = 0).

Note

When accessing the JPEG FIFO, an even number of accesses is needed for both encoding and decoding.
For the encoding process, there will be up to 3 bytes of data that is not needed. Discard this data and compare the data read to the final compressed file size in the Encode size result register (REG[09B4h]-[09B6h]).
For the decoding process, 32-bit unit data should always be written to the JPEG FIFO. Pad the end of the JPEG data stream with 00s to create 32-bits of data for the last JPEG FIFO entry.

Note

If the JPEG FIFO is accessed after the JPEG process has completed or before the JPEG process has started, any data is considered invalid and ignored.

19.2.3 YUV Data Capture

1. Set the JPEG module registers.
    a. Select the YUV data format, for YUV 4:2:2 set REG[0980h] bits 3-1 = 011, for YUV 4:2:0 set REG[0980h] bits 3-1 = 111b.
    b. Enable the JPEG module and perform a JPEG software reset (REG[0980h] bit 7 = 1 and bit 0 = 1).
    c. Specify the JPEG FIFO size (REG[09A4h]). The FIFO size is determined using the following formula:

       JPEG FIFO size = ((REG[09A4h] bits 3-0) + 1) x 4K bytes.

       Example: for a JPEG FIFO size of 12K bytes, REG[09A4h] = 2
       (2 + 1) x 4KB = 12K bytes
    d. Clear the JPEG FIFO (REG[09A0h] bit 2 = 1).
    e. Set the JPEG FIFO Threshold Trigger (REG[09A0h] bits 5-4).
2. Set the YUV capture size.
    a. Configure the vertical pixel size (REG[100Eh]-[1010h]) and the horizontal pixel size (REG[1012h]-[1014h]). These registers are used for both the JPEG codec and YUV capture.
3. Set the Capture resizer registers (REG[0960h - 096Eh]) and reset the Capture Resizer. The vertical and horizontal dimensions must be the same as the JPEG vertical and horizontal sizes as programmed in step 2a.
4. Start capturing YUV data.
    a. Clear all status bits by writing REG[0982h] to FFFFh.
    b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0605h.
    c. To enable the JPEG FIFO for YUV Capture Mode, set REG[1002h] bit 0 as 1. The JPEG FIFO is now ready to receive YUV data.
    d. Start capturing (REG[098Ah] bit 0 = 1).

    At this stage, it is the Host CPU's task to access the JPEG FIFO in the same way as for a JPEG Encode process. YUV data capture continues until a 0 is written to REG[098Ah] bit 0.

19.2.4 YUV Data Display

1. Set the JPEG module registers.
    a. Select the YUV data format, for YUV 4:2:2 set REG[0980h] bits 3-1 = 001, for YUV 4:2:0 set REG[0980h] bits 3-1 = 101b.
    b. Enable the JPEG module and perform a JPEG software reset (REG[0980h] = 81h).
2. Set the YUV data display size.
    a. Configure the vertical pixel size (REG[100Eh]-[1010h]) and the horizontal pixel size (REG[1012h]-[1014h]). These registers are used for both the JPEG codec and YUV capture.
3. Set the Capture resizer registers (REG[0960h - 096Eh]) and reset the Capture Resizer. The vertical and horizontal dimensions must be the same as the JPEG vertical and horizontal sizes as programmed in step 2a.
4. Set the JPEG Line Buffer registers (If the JPEG Line Buffer empty interrupt is used).
    a. Set REG[09C6h] bit 0 =1 and set REG[0986h] bit 0 = 1.
    b. Clear the JPEG Line Buffer status bits (REG[09C0h] = FFFFh).
5. Start YUV data input.
    a. Clear all JPEG status bits (REG[0982h] = FFFFh).
    b. Enable the appropriate interrupts in the JPEG Interrupt Control register. For example, set REG[0986h] = 0001h.
    c. Write YUV data to the JPEG Line Buffer Write Port (REG[09E0h]) when the JPEG Line Buffer is empty. The following table shows the maximum data size which can be sent at one time. The minimum line unit for YUV 4:2:2 is 1, for YUV 4:2:0 it is 2. After writing the YUV data to the JPEG Line Buffer, clear the JPEG Line Buffer Empty Flag (REG[09C0h] bit 0 = 1).

Line Size	The maximum data size
> 256	Line Data Size x 16
≤ 256	Line Data Size x 32
≤ 128	Line Data Size x 64
≤ 64	Line Data Size x 128
≤ 32	Line Data Size x 256

    d. Continue writing YUV data until all the data is sent to the JPEG Line Buffer.

19.2.5 Exit Sequence

The exit sequence is the same for all cases: JPEG Decode, JPEG Encode, YUV Data Capture, and YUV Data Display.

1. Check the JPEG Operation Status bit (REG[1004h] bit 0).
2. For JPEG decode only, check the JPEG Error Status bits (REG[101Eh] bits 6-3).
3. Disable all interrupts, set REG[0986h] to 0000h.
4. Clear all status bits, set REG[0982h] to FFFFh.
5. Clear the JPEG Operation Select bit, write a 0 to REG[1000h] bit 2.
6. Perform a JPEG Software Reset, write a 1 to REG[0980h] bit 7.
7. Disable the JPEG codec, write a 0 to REG[0980h] bit 0.

20 Camera Interface

The S1D13717 is designed with a 8-bit Type 1 Camera interface. Type 1 cameras are defined as cameras that supply horizontal and vertical sync information and typically are programmed through an I^2C interface.

20.1 Type 1 Camera

The Type 1 external camera module connected to either of the camera ports must satisfy the following conditions:

- The camera module must work synchronously with the S1D13717 camera clock output.
- The camera module must output VSYNC and HSYNC to the S1D13717 unless ITU-R BT 656 mode is used. ITU-R BT 656 mode uses embedded VSYNC/HSYNC signals in the YUV data stream. The S1D13717 fully satisfies the ITU-R BT656-4 requirements.
- The camera data must be 8-bit YUV 4:2:2. The following YUV 4:2:2 data formats are supported: UYVY, VYUY, YUYV, and YUYV

  The following ranges for the camera YUV input data are supported.

Table 20-1: YUV Input Data Ranges

YUV Straight	YUV Offset	YCbCr Straight	YCbCr Offset
$0 \le Y \le 255$	$0 \le Y \le 255$	$16 \le Y \le 235$	$16 \le Y \le 235$
$0 \le U \le 255$	$-128 \le U \le 127$	$16 \le U \le 240$	$-113 \le U \le 112$
$0 \le V \le 255$	$-128 \le V \le 127$	$16 \le V \le 240$	$-113 \le V \le 112$

- The input data rate is determined by the camera module pixel clock output and must be a maximum of 1/3 of the system clock. For example, when the system clock is 54MHz, the camera module can have a maximum pixel clock output of 18MHz.

20.2 Strobe Control Signal

When the camera interface is enabled, a strobe feature is available. The strobe output is controlled using REG[0120h]-[0124h]. The strobe control signal output pin is CMSTROUT and must be enabled using the Strobe Port Enable bit (REG[0124h] bit 3).

20.2.1 Generating a Strobe Pulse

To generate a strobe pulse (CMSTROUT):

1. Enable the camera interface and ensure that the CMVREF and CMHREF signals are present. ITU-R BT656 data format must not be enabled (REG[0110h] bit 5 = 0).
2. Set the JPEG Operation Mode bits (REG[0980h] bits 3-1 to 111b (JPEG Encode/Decode is bypassed).
3. Enable the JPEG Module (REG[0980h] bit 0 = 1).
4. Configure the Strobe Line Delay (REG[0120h]), Strobe Pulse Width (REG[0122h], and Strobe Pulse Polarity (REG[0124h] bit 1).
5. Enable the strobe control signal output port by setting the Strobe Port Enable bit (REG[0124h] bit 3 = 1).
6. Enable the strobe signal (CMSTROUT) by setting the Strobe Enable bit (REG[0124] bit 0 = 1). This bit must remain enabled for the entire duration of the delay value (REG[0124h] bits 7-4), otherwise the strobe will be disabled immediately when the Strobe Enable bit is set to 0.
7. Generate a strobe signal (CMSTROUT) by setting the JPEG Start/Stop Control bit to 1 (REG[098A] bit 0 = 1).

Before generating another strobe signal, the strobe must be disabled (REG[0124h] bit 0 = 0) and then enabled again (REG[0124h] bit 0 = 1). Then generate the strobe pulse again by setting the JPEG Start/Stop Control bit to 1 (REG[098A] bit 0 = 1).

20.2.2 Strobe Timing

The strobe pulse (CMSTROUT) begins on the falling edge of CMHREF after CMVREF as specified by the Strobe Line Delay Timing bits (REG[0120h] bits 15-0). A zero delay (REG[0120h] bits 15-0 = 0h) starts the strobe pulse (CMSTROUT) on the first falling edge of CMHREF after CMVREF.

Note
Both the Line Delay and Pulse Width signals are specified by counting HREFs which leads to an inherent timing delay if the HREF signal stops. This inherent delay must be considered when programming the Line Delay (REG[0120h]) and Pulse Width (REG[0122h]) registers.

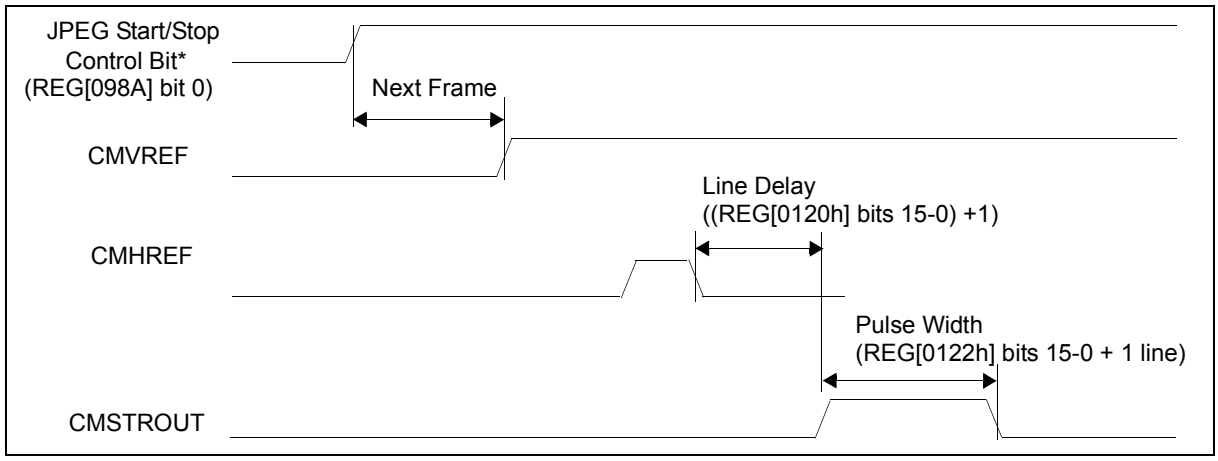


Figure 20-1: Strobe Signal Output Timing

Note
The line delay (REG[0120h] bits 15-0) may be set greater than the period of the CMVREF signal.

21 SD Memory Card Interface

The S1D13717 SD Memory Card interface is compatible with the SD Memory Card Physical Layer Specification Version 1.0. Either a 1-bit or 4-bit interface can be selected. This implementation of the SD Memory Card interface does not support SPI mode or hardware security functions.

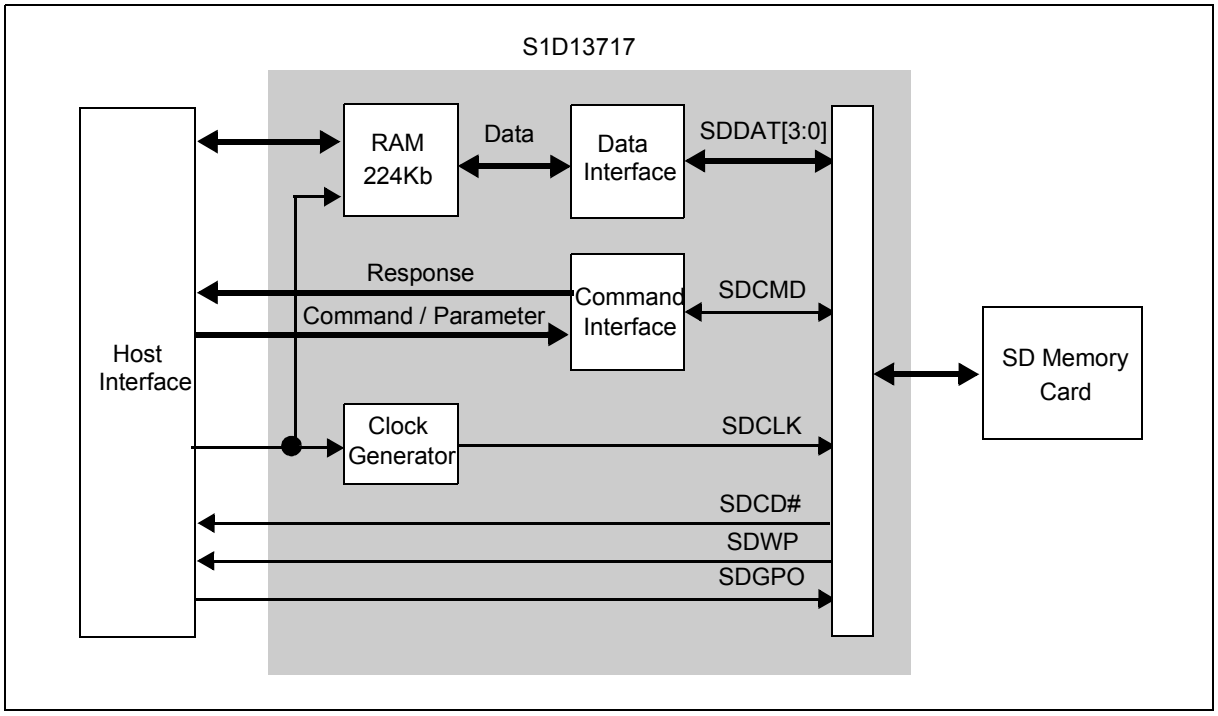


Figure 21-1: SD Memory Card Interface Block Diagram

21.1 Interface Commands

The SD memory card interface supports eight different commands.

Send Command

The send command transmits the command stream to the SDCMD pin. The command stream is composed of the contents of the command register (REG[610Ch] and the parameter registers (REG[6110h] - REG[6116h]).

Receive Response

The receive response command starts receiving the response stream from the SDCMD pin. There are two lengths of response streams (48 bits and 136 bits). The response data is written to the appropriate response registers for the length of the response stream (REG[6120h] - REG[613Eh]).

Wait Busy

This command waits for the data pins (SDDAT[3:0] to be ready.

Receive Data

The receive data command receives the data stream from the SDDAT[3:0] pins. When data is received, it is written to memory. The data length for received data can be configured between 1-512 using the SD Memory Card Data Length registers (REG[6108h] - REG[610Ah]).

Send Data

The send data command transmits the data stream from memory to the SDDAT[3:0] pins. The data length for sent data can be configured between 1-512 using the SD Memory Card Data Length registers (REG[6108h] - REG[610Ah]).

SDCLK Change

This command initiates a new clock frequency for the SDCLK pin (see REG[6104h] bit 7).

Send 8 Clock

About eight clocks are transmitted from the SDCLK pin.

Synchronous Reset

This command performs a synchronous reset of the SD memory card interface. For details on this function, see the register description for REG[6104h] bit 0.

21.2 Pin Functions

There are three pins used by the SD memory card interface.

Card Detect

The SDCD# pin detects whether a SD memory card is inserted or not. The state of this pin can be determined using the SD Memory Card Interrupt.

Write Protect

The SDWP pin detect whether the SD memory card is write-protected or not.

General Output

The SDGPO pin can be used to turn on/off the external pull-ups (SDCD# or SDWP) or for an LED.

22 Indirect Interface

The S1D13717 supports four indirect host interfaces which can be selected using CNF[4:2] (see Table 5-10: "Summary of Power-On/Reset Options," on page 42). For an overview of the indirect host interface, see Section 1.4.2, "Indirect Addressing Host Interfaces" on page 14. For timing details, see Section 7.3, "Host Interface Timing" on page 56.

22.1 Using the Indirect Interface

Accessing the S1D13717 through the indirect interface is a two step process. See Section 22.2, "Example Sequences" on page 372 for example sequences of register read/writes, memory writes, and memory reads.

First, a "Command Write" (or register address) is written to the Indirect Interface Memory Access Port register (REG[0028h] where it is stored until the next Command Write. For Command Writes, the data bus width must be 16-bit.

Next, a "Data Read/Write" is done that specifies the data to be stored or read from the register specified in the "Command Write" cycle. "Data Read/Write" accesses to registers must be 16-bit accesses.

To access the internal memory, the memory address must be written to the Indirect Interface Memory Access registers (REG[0022h]-[0024h]) by "Command Write" and "Data Read/Write" accesses. Once the memory address is stored in these registers, a "Command Write" to the Memory Access Port Register REG[0028] must be done to enable memory accesses. Then "Data Read/Write" accesses to memory can be performed and they can be either 8-bit or 16-bit accesses. Once the memory "Data Read/Write" is complete, the address stored in REG[0022h] - 0024h] is incremented based on the Auto Increment bits (REG[0026h] bits 1-0).

If the auto increment feature is enabled (REG[0026h] bits 1-0 = 00b or 01b), the S1D13717 can support a memory burst transfer where the host can "Data Read/Write" memory data continuously without issuing a "Command Write" each time. For the first access the host must set the memory address registers (REG[0022h] - REG[0024h]), but after that, the host can read/write data continuously without issuing a "Command Write".

Note
When the indirect interface is enabled, the S1D13717 uses REG[002Ah], instead of the 2D BitBLT Data Memory Mapped Region Register (REG[10000h]).

22.2 Example Sequences

Note
All example sequences are shown using the Indirect 80 Type 3 host interface (CNF[4:2] = 011).

22.2.1 Register Read/Write Example Sequence

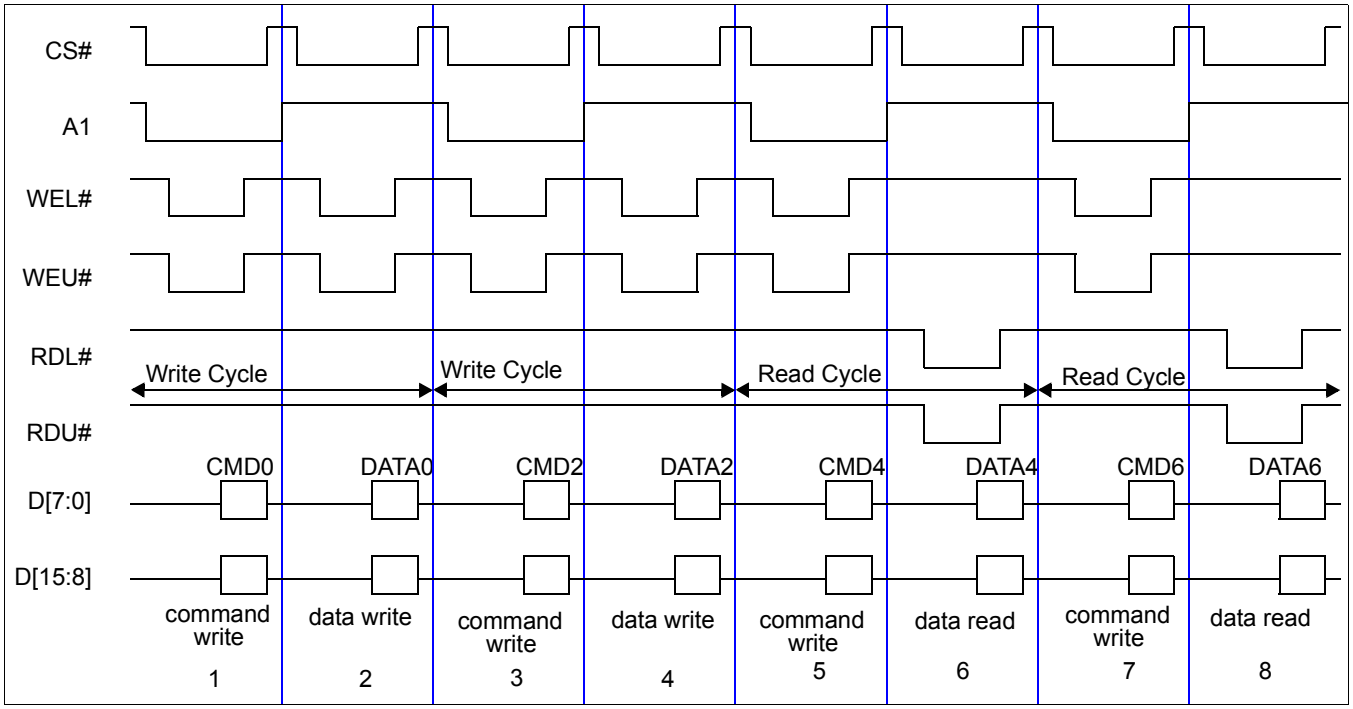


Figure 22-1: Register Read/Write" Example Sequence

1. Write the desired register number.
2. Write the data to be placed in the register.
3. Write the next register number.
4. Write the data to be placed in the register.
5. Write the desired register number.
6. Read the data from the register.
7. Write the desired register number.
8. Read the data from the register.
9. .....

Note
The data bus width for all register accesses must be 16-bit.

22.2.2 Memory Write Example Sequence

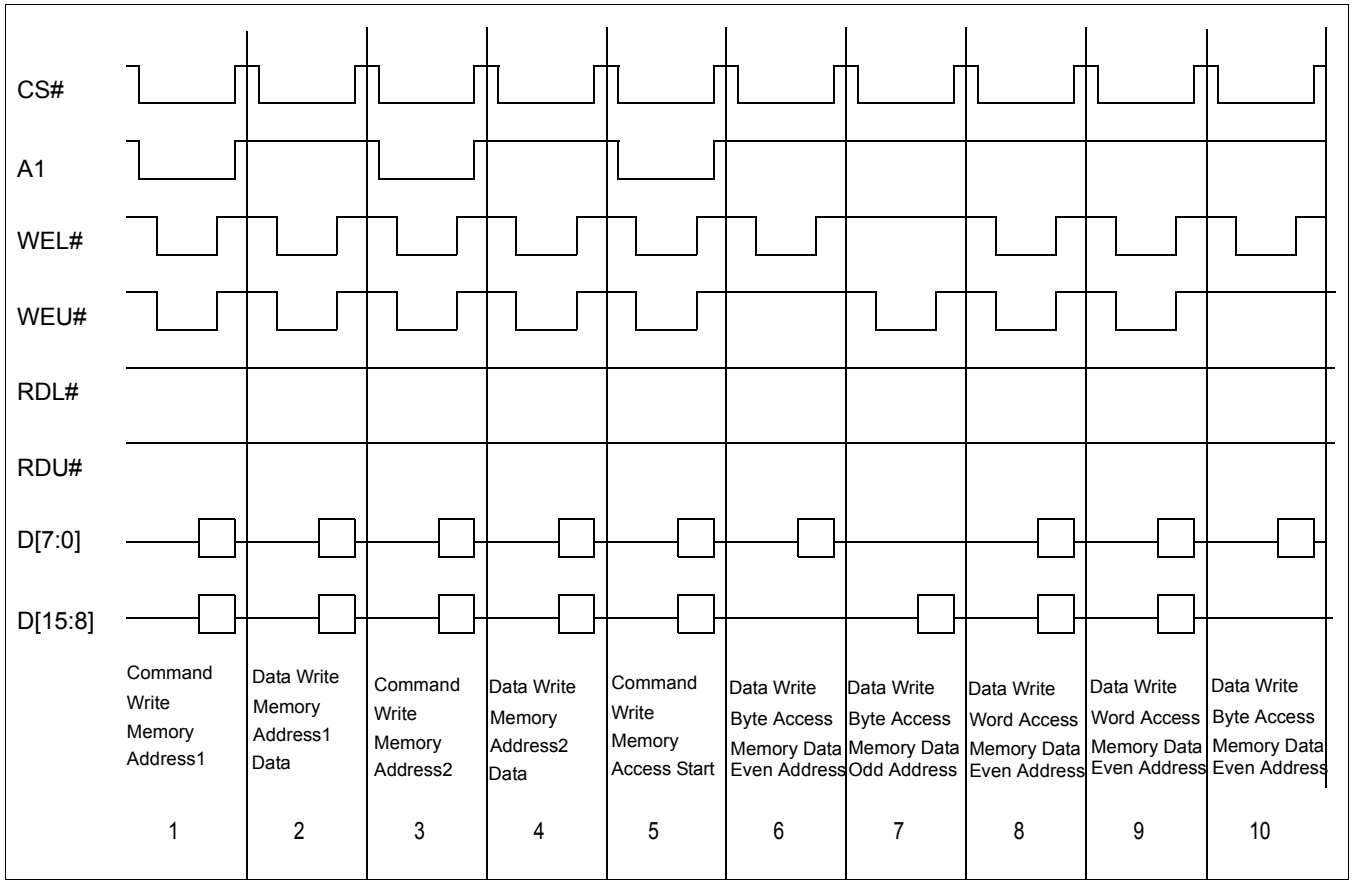


Figure 22-2: Memory Write Example Sequence

1. Write the register number of the Indirect Interface Memory Address Register 1 (REG[0022h]). The data bus width must be 16-bit.
2. Write the lower memory address (MA[15:0]) as data to REG[0022h]. The data bus width must be 16-bit.
3. Write the register number of the Indirect Interface Memory Address Register 2 (REG[0024h]). The data bus width must be 16-bit.
4. Write the upper memory address (MA[17:16]) as data to REG[0024h]. The data bus width must be 16-bit.
5. Write the register number of the Indirect Interface Memory Access Port register (REG[0028h]). This write triggers burst memory access beginning with the next access.
6. Write the memory data. Memory accesses may be either 8-bit or 16-bit. The data location (higher or lower byte) depends on the memory address (odd or even number). In this case, the memory address is an even address and is in the lower byte. After the memory data is written the Indirect Interface Memory Address registers are incremented as follows:

- if REG[0026h] bits 1-0 = 00b, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a low byte access.
- if REG[0026h] bits 1-0 = 01b, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a byte access.
- if REG[0026h] bits 1-0 = 10b, Memory Address registers (REG[0022h] - [0024h]) are not incremented.

7. Write the memory data. Memory accesses may be either 8-bit or 16-bit. The data location (higher or lower byte) depends on the memory address (odd or even number). In this case, the memory address is an odd address and is in the higher byte. After the memory data is written the Indirect Interface Memory Address registers are incremented as follows:
   - if REG[0026h] bits 1-0 = 00b, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a high byte access.
   - if REG[0026h] bits 1-0 = 01b, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a byte access.
   - if REG[0026h] bits 1-0 = 10b, Memory Address registers (REG[0022h] - [0024h]) are not incremented.
8. Write the memory data. After the memory data is written the Indirect Interface Memory Address registers are incremented as follows:
   - if REG[0026h] bits 1-0 = 00b, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
   - if REG[0026h] bits 1-0 = 01b, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
   - if REG[0026h] bits 1-0 = 10b, Memory Address registers (REG[0022h] - [0024h]) are not incremented.
9. Write the memory data. After the memory data is written the Indirect Interface Memory Address registers are incremented as follows:
   - if REG[0026h] bits 1-0 = 00b, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
   - if REG[0026h] bits 1-0 = 01b, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
   - if REG[0026h] bits 1-0 = 10b, Memory Address registers (REG[0022h] - [0024h]) are not incremented.
10. .....
11. If another Command Write is made, burst memory access mode (or auto increment) is stopped and a register access takes place. Note that the Indirect Interface Memory Address registers (REG[0022h] -[0024h]) store the last incremented memory address until it is changed.

Note

To begin (or trigger) memory accesses, a Command Write to the Indirect Interface Memory Access Port register (REG[0028h]) is required, however, a data write to the register is not required. A Command Write to REG[0028h] indicates that burst memory accesses will start from the next data write.

22.2.3 Memory Read Example Sequence

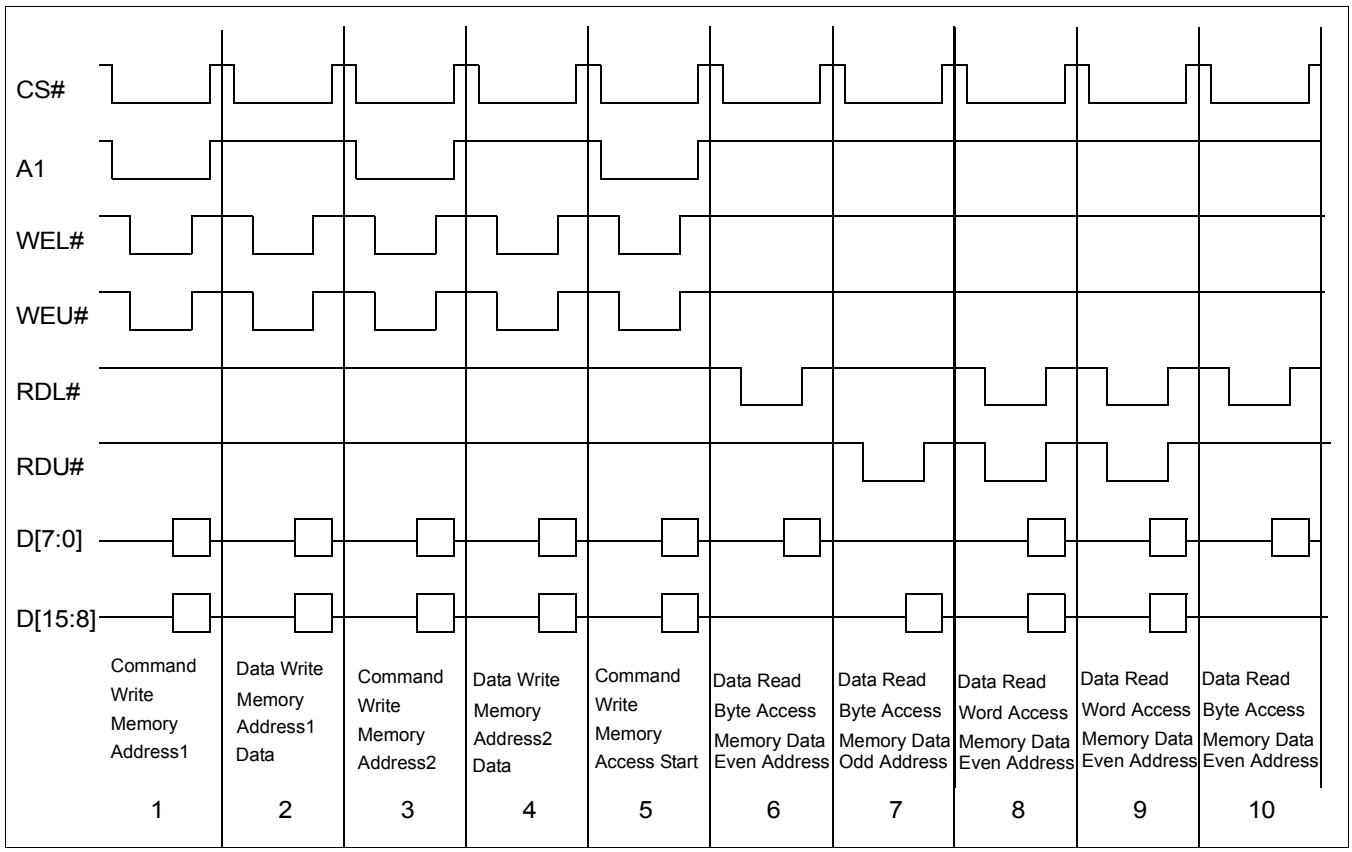


Figure 22-3: Memory Read Example Sequence

1. Write the register number of the Indirect Interface Memory Address Register 1 (REG[0022h]). The data bus width must be 16-bit.
2. Write the lower memory address (MA[15:0]) as data to REG[0022h]. The data bus width must be 16-bit.
3. Write the register number of the Indirect Interface Memory Address Register 2 (REG[0024h]). The data bus width must be 16-bit.
4. Write the upper memory address (MA[17:16]) as data to REG[0024h]. The data bus width must be 16-bit.

5. Write the register number of the Indirect Interface Memory Access Port register (REG[0028h]). This write triggers burst memory access beginning with the next access.

6. Read the memory data. Memory accesses may be either 8-bit or 16-bit. The data location (higher or lower byte) depends on the memory address (odd or even number). In this case, the memory address is an even address and is in the lower byte. After the memory data is read the Indirect Interface Memory Address registers are incremented as follows:
    - if REG[0026h] bits 1-0 = 00b, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a low byte access.
    - if REG[0026h] bits 1-0 = 01b, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a byte access.
    - if REG[0026h] bits 1-0 = 10b, Memory Address registers (REG[0022h] - [0024h]) are not incremented.

7. Read the memory data. Memory accesses may be either 8-bit or 16-bit. The data location (higher or lower byte) depends on the memory address (odd or even number). In this case, the memory address is an odd address and is in the higher byte. After the memory data is read the Indirect Interface Memory Address registers are incremented as follows:
    - if REG[0026h] bits 1-0 = 00b, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a high byte access.
    - if REG[0026h] bits 1-0 = 01b, the memory address registers (REG[0022h] - [0024h]) are not incremented because it was a byte access.
    - if REG[0026h] bits 1-0 = 10b, Memory Address registers (REG[0022h] - [0024h]) are not incremented.

8. Read the memory data. After the memory data is read the Indirect Interface Memory Address registers are incremented as follows:
    - if REG[0026h] bits 1-0 = 00b, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
    - if REG[0026h] bits 1-0 = 01b, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
    - if REG[0026h] bits 1-0 = 10b, Memory Address registers (REG[0022h] - [0024h]) are not incremented.

9. Read the memory data. After the memory data is read the Indirect Interface Memory Address registers are incremented as follows:
    - if REG[0026h] bits 1-0 = 00b, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.
    - if REG[0026h] bits 1-0 = 01b, the memory address registers (REG[0022h] - [0024h]) are incremented, +2 because it was a word access.

- if REG[0026h] bits 1-0 = 10b, Memory Address registers (REG[0022h] - [0024h]) are not incremented.

10. .....

11. If another Command Write is made, burst memory access mode (or auto increment) is stopped and a register access takes place. Note that the Indirect Interface Memory Address registers (REG[0022h] -[0024h]) store the last incremented memory address until it is changed.

Note

It is possible to perform a memory data write after a data read and vice versa without issuing another Command Write.

23 Mechanical Data

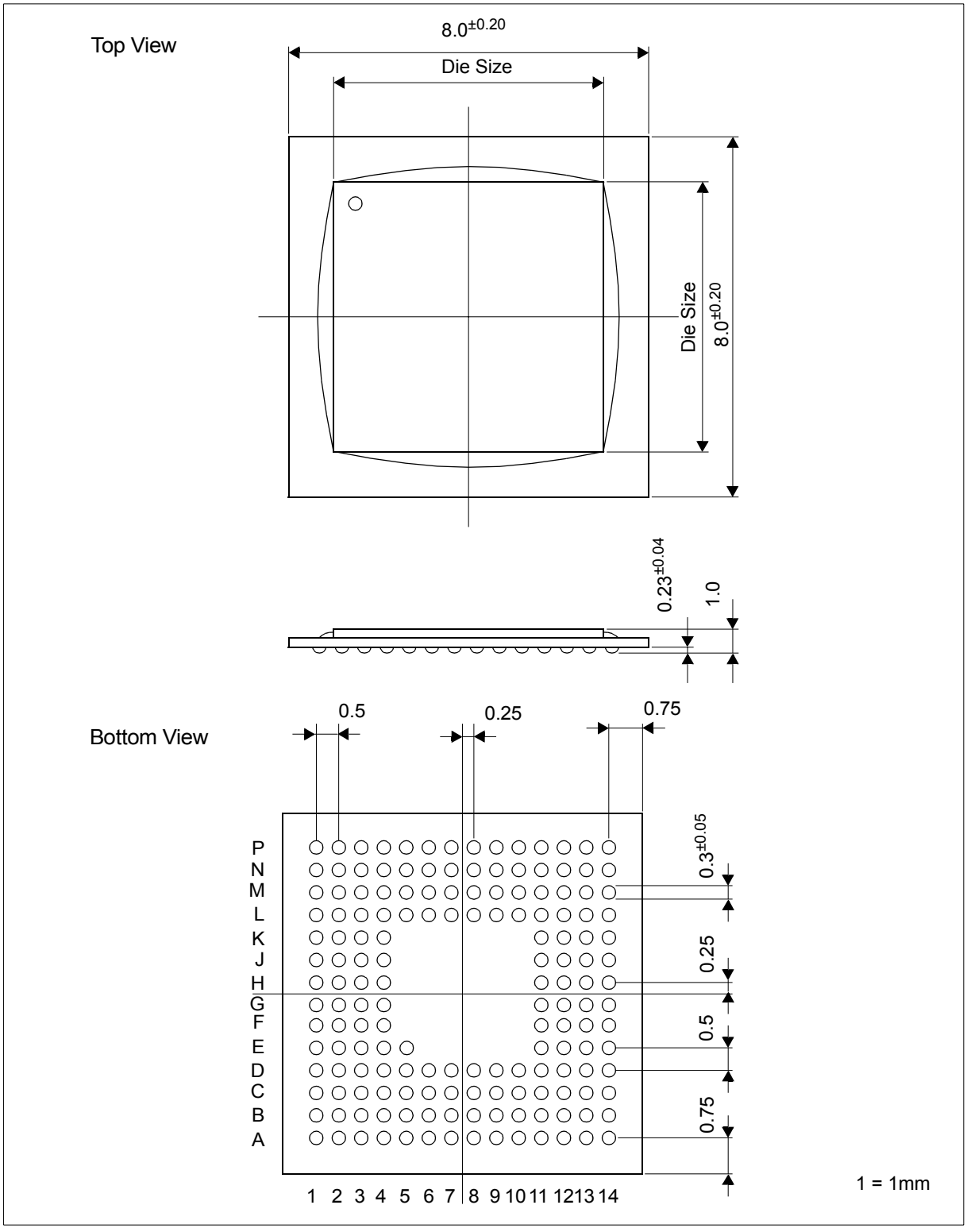


Figure 23-1: S1D13717 FCBGA-161 Pin Package

24 References

The following documents contain additional information related to the S1D13717. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

- S1D13717 Product Brief (X57A-C-001-xx)

25 Sales and Technical Support

AMERICA

EPSON ELECTRONICS AMERICA, INC.
HEADQUARTERS
2580 Orchard Parkway
San Jose, CA 95131,USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

SALES OFFICES
Northeast
301 Edgewater Place, Suite 210
Wakefield, MA 01880, U.S.A.
Phone: +1-800-922-7667 FAX: +1-781-246-5443

EUROPE

EPSON EUROPE ELECTRONICS GmbH
HEADQUARTERS
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
23F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON Electronic Technology Development (Shenzhen) LTD.
12/F, Dawning Mansion, Keji South 12th Road,
Hi- Tech Park, Shenzhen
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

GUMI OFFICE
2F, Grand B/D, 457-4 Songjeong-dong,
Gumi-City, KOREA
Phone: +82-54-454-6027 FAX: +82-54-454-6093

SEIKO EPSON CORPORATION
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

25.1 Ordering Information

To order the S1D13717 Mobile Graphics Engine, contact the Epson sales representative in your area.

Change Record

X57A-A-001-03 Revision 3.02 - Issued: September 18, 2007

- updated Epson tagline and copyright
- added Product Brief to References section
- updated Sales and Technical Support addresses

X57A-A-001-03 Revision 3.01

- REG[1660h] - REG[17A2h], fixed typo in table that referred to REG[17xxh] as REG[15xxh]
- REG[6100h] bits 7-4, updated divide ratio table to include 2:1 and 3:1, also added System Clock Frequency table

X57A-A-001-03 Revision 3.0

- released as revision 3.0 (2004/06/07)
- section 5.1 S1D13717 Pinout Diagram (FCBGA-161) - correct typo for CNF5 and CNF4 - change pins CNF5=M11 and CNF4=N12
- section 5.2.7 Miscellaneous - correct typo for CNF5 and CNF4 - change pins CNF5=M11 and CNF4=N12

X57A-A-001-02 Revision 2.0

- released as revision 2.0 (2004/04/20)
- section 5.2.2 Host Interface - in table 5-3 split AB[17:1] into AB[17:2] and AB1
- section 5.2.2 Host Interface - delete all references to “parallel bypass mode” as the S1D13717 does not support this mode
- section 5.4 Host Interface Pin Mapping - delete “Parallel” columns from both tables
- REG[0902h] bits 6-0 - correct the equations in bit description

X57A-A-001-01 Revision 1.0

- released as revision 1.0 (2004/04/14)

X57A-A-001-00 Revision 0.06

- section 6 D.C. Characteristics - Table 6-2 Recommended Operating Conditions, change T_{OPR} to “min -20, typ 25, max 70”
- REG[0056h] bit 13 - reserve this bit
- REG[0056h] bit 12 - reserve this bit
- REG[0110h] bit 10 - add this bit
- REG[0124h] - change default value to 0009h
- REG[0124h] bit 3 - make this bit Strobe Enable and rewrite description

- REG[0124h] bit 2 - make this bit Strobe Port Data and rewrite description
- REG[0124h] bit 0 - make this bit Strobe Port Select and rewrite description
- REG[0200h] bit 10 - correct typo in register bit table - mark as reserved
- REG[0200h] bit 6 - correct typo in register bit table - mark as reserved
- REG[0200h] bits 3-2 - reserve bits 3-2 = 11b in table
- REG[0200h] bits 1-0 - reserve bits 1-0 = 11b in table
- REG[022Ch] bit 2 - reserve this bit
- REG[0240h] bits 11-10 - reserve bits 11-00 = 11b in table
- REG[0300h] bits 15-4 - correct typo in register bit table - mark as reserved
- REG[0304h] bits 15-4 - correct typo in register bit table - mark as reserved
- REG[0308h] bits 15-4 - correct typo in register bit table - mark as reserved and change register default to FFFFh
- REG[030Ch] bits 15-4 - correct typo in register bit table - mark as reserved
- REG[6100h] bits 7-4 - correct typo for sampling clock frequency for ~52MHz system clock, change “~(52/1.5)MHz” to” ~(52/2)MHz”
- section 13.1.3 32 Bpp Mode - remove section
- section 13.2.3 32 Bpp Mode - remove section
- section 19.2.2 Memory Image JPEG Encoding Process - remove
- section 19.2.3 Memory Image JPEG Encoding Process from Host I/F (RGB format) - remove
- section 19.2.2 JPEG Decoding Process - figure 19-9 JPEG Decoding Process (6 of 6) - change “JPEG Process is finished - REG[1002h] bit 0 = 0” to “JPEG Operation Change - REG[1000h] bit 2 = 0”

X57A-A-001-00 Revision 0.05

- add section 5.2.1 Unused Pins - bump all other 5.2.x sections up by 1
- section 5.3 Pin Descriptions, re-arrange pin numbering order in tables
- section 5.3.3 Camera Interface - add note for CMSTROUT RESET# State in table
- add section 7.1.2 PLL Clock
- REG[000Eh] bits 1-0, updated V-Divider bit description to clarify its effect on PLL jitter and power consumption
- REG[0010h] bits 15-12, updated VCO Kv Set bit description to clarify its effect on PLL jitter and power consumption
- REG[0014h] bit 9 - unreserve this bit and name it LCD2 Serial Bypass Mode Select
- REG[0032h] bit 8 - add text “To enable the Serial Port Bypass...” and add note “The LCD Output Port Select bits...”

- REG[0056h] bit 13 - replace “tristated” with “pulled low”
- REG[0056h] bit 12 - rewrite bit description
- REG[0116h] bit 4 - correct typos in figure 10-1, change “REG[0114h] bit 4” to “REG[0116h] bit 4” and “REG[0114h] bit 5” to “REG[0116h] bit 6”
- REG[0124h] bits 7-4 - rewrite bit description
- REG[0124h] bit 3 - reserve this bit
- REG[0124h] bit 2 - unreserve this bit and name it CMSTROUT GPO Control
- REG[0124h] bit 0 - rewrite bit description “When this bit = 0...”
- REG[0268h] - add this reserved register
- REG[0280h] - add this reserved register
- REG[0310h] through REG[0326h] - rewrite note “...However, if this function doesn’t apply...”
- REG[0328h] bits 4-0 - rewrite note “...However, if this function doesn’t apply...”
- REG[0328h] bit 13 - rewrite bit description
- REG[0940h] bit 2 - correct typo in bit description change “vertical scaling rate is controlled by REG[094Eh]...” to “vertical scaling rate is controlled by REG[094Ch]...”
- REG[0980h] bits 3-1 - update description in table for 000b - remove references to RGB/YUV Converter
- REG[09A0h] bit 2 - update description for sequence to clear the JPEG FIFO
- REG[09A2h] bits 6-0 - update equation in description
- REG[0A00h] bit 5 - update bit description to correct typo
- REG[0A06h] bit 1 - update bit description read “This flag is masked by REG[0A08h]...”
- REG[0A08h] bit 1 - update bit description - “The status of this interrupt...”
- REG[1016h - 1018h] - remove note “Vertical resolutions in...”
- REG[6002h] bits 7-0 - rewrite note for each bit
- REG[6100h] bit 0 - add note “This bit is cleared on a SD card software reset...”
- REG[6102h] bit 7 - rewrite bit description
- REG[6102h] bit 7 - change default register value to 00x1
- REG[6106h] bit 6 - rewrite bit description
- REG[6118h - 611Eh] - add note “These registers are Write Only...”
- section 11.1 Power-On/Power-Off Sequence - add “Software Reset” to Figure 11-1: Power On/Power-Off Sequence after “Hardware Reset” and remove the “Clock Source Select” block as per
- section 11.1.2 Reset - rewrite software reset description

- section 11.1.3 Standby Mode - rewrite standby mode description
- section 20.1 Type 1 Camera - rewrite bulleted text “The input data rate is determined by...” for a max 1/3 system clock

X57A-A-001-00 Revision 0.04

- section 1.5.3 Serial LCD Interface - delete “... except that the LCD Module VSYNC Input is not supported for serial interface panels” from end of section
- section 1.6 Display Features - add Mirror to section
- section 1.9.1 Encoder - add “..., or to encode YUV data sent by the Host CPU” to the third paragraph
- section 1.9.2 Decoder - add “..., or to send the resulting YUV decoded data back to the Host CPU” to the first paragraph
- section 2.2 Host CPU Interface- add bullet “M/R# and CS# inputs select between memory and register address space in 2 CS# mode” and bullet “CPU parallel port for direct control of a parallel LCD”
- section 2.4 Display Modes- add bullet “Decoded by the internal JPEG decoder, resized, scaled, and downloaded to the Host CPU via the JPEG FIFO”
- section 2.8 Picture Input/Output Functions - add bullets “Host CPU can directly control parallel interface panels on LCD1 or LCD2” and “Encoded by the internal JPEG encoder, resized, scaled, and downloaded to the Host CPU via the JPEG FIFO”
- section 5.2.1 Host Interface - rewrite descriptions for SCS#, SCLK, SA0 and SI
- section 5.2.2 LCD Interface - rewrite descriptions
- section 8 Memory Allocation - re[place entire section
- section 10.1 Register Mapping - add “...(for 1 CS# mode), or CS# = 1 and M/R# = 0 (for 2 CS# mode)...” to first paragraph
- REG[0028h] - change Command Write to Index Write in bit description
- REG[0054h] - add “... for RGB displays requiring initialization through a serial interface” to all bit descriptions
- REG[0056h] bit 13 - rewrite bit description “When this bit = 1...”
- REG[0056h] bit 12 - rewrite bit description “When this bit = 1...”
- REG[0056h] bit 7 - add “When a manual transfer has been initiated...” to bit description
- REG[005Eh] bit 13 - rewrite bit description “When this bit = 1...”
- REG[005Eh] bit 12 - rewrite bit description “When this bit = 1...”
- REG[005Eh] bit 7 - add “When a manual transfer has been initiated...” to bit description
- REG[0110h] bit 8 - rename bit and add note to bit description
- REG[0114h] bit 8 - delete note in bit description

- REG[0116h] bit 1 - add “This bit is masked by the Camera Frame Capture Interrupt Enable...” to bit description
- REG[0120h] - change description to read “... the first HSYNC input of a camera frame...”
- REG[0200h] bits 10 and 6 - mark these bits as n/a
- REG[0202h] bit 12 - mark this bit as n/a
- REG[0212h] bit 2 - reserve this bit
- REG[0248h] bit 2 - reserve this bit
- REG[0124h] bits 7-4 - rewrite bit description
- REG[0124h] bit 0 - rewrite bit description
- REG[0200h] bit 12 - rewrite bit description
- REG[0200h] bit 7 - rewrite bit description
- REG[021Eh] bits 11-0 - add note to bit description
- REG[0220h] - add note to bit description
- REG[0222h] - add note to bit description
- REG[0224h] - add note to bit description
- REG[0226h] - add note to bit description
- REG[0240h] bit 5 - rewrite bit description
- REG[0240h] bit 4 - rename bit and rewrite bit description
- REG[0260h - 0280h] - remove these reserved registers
- REG[0930h] bit 3 - add note to bit description
- REG[0930h] bits 1-0 - rewrite description for bits 1-0 = 01 in table
- REG[0944h] bit 10 - reserve this bit
- REG[094Ch] bits 13-8 - rewrite bit description
- REG[094Ch] bits 5-0 - rewrite bit description
- REG[096Ch] bits 13-8 - rewrite bit description
- REG[096Ch] bits 5-0 - rewrite bit description
- REG[0980h] bit 4 - add “The YUV data range depends on the interface...” to bit description
- REG[0982h] bit 11 - add note “The Encode Size Limit Violation Flag can only be cleared...” to bit description
- REG[0982h] bit 10 - add note “The JPEG FIFO Threshold Trigger Flag can only be cleared...” to bit description

- REG[0982h] bit 9 - add note “The JPEG FIFO Full Flag can only be cleared...” to bit description
- REG[0982h] bit 8 - add note “The JPEG FIFO Empty Flag can only be cleared...” to bit description
- REG[0982h] bit 0 - add “or Host Decode/Encode...” to bit description
- REG[0984h] bit 14 - add note to bit description
- REG[0984h] bits 13-12 - add note to bit description
- REG[09A2h] - remove reserved bits 14 - 8 and mark them n/a
- REG[09A2h] bits 3-2 - changes to table
- REG[09C0h] bit 2 - add “This bit is only valid for YUV Capture/Display...” to bit description
- REG[09C0h] bit 1 - add “This bit is only valid for YUV Capture/Display...” to bit description
- REG[09C0h] bit 0 - rewrite bit description
- REG[09C2h] bit 2 - add “This bit is only valid for YUV Capture/Display...” to bit description
- REG[09C2h] bit 1 - add “This bit is only valid for YUV Capture/Display...” to bit description
- REG[09C2h] bit 0 - rewrite bit description
- REG[09C4h] bit 0 - changes to “When this bit = 1...” in bit description
- REG[8012h] bits 4-3 - reserve these bits
- section 12.2, removed separate lines about FPCS2#, FPSO, FPSCLK
- section 19.1.1, added information about terminate cycles when read from an empty FIFO or write to a full FIFO takes place

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- REG[6100h] bits 7-4 - table 10-85 System Clock Frequency and SD Card Clock - for system clock of ~40MHz change Data Transfer Mode to “0011 (~10MHz)”, for system clock of ~52MHz change Data Transfer Mode to “0011 (~13MHz)”, for system clock of ~55MHz change Data Transfer Mode to “0011 (~13.75MHz)” and change Sampling Clock Frequency to “~(52/2)MHz”
- REG[8004h] bits 12-7 - reserve these bits
- REG[8006h] - reserve this register
- REG[800Eh] bits 4-3 - reserve these bits
- figure 11-1 Power-On/Power-Off Sequence - change NIOVDD to SIOVDD
- section 11.1.1 Power-On - add SIOVDD to step 3
- section 11.1.6 Power-On - add SIOVDD to step 1

- section 13.8 RGB/YUV Conversion - remove section

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- Section 5.2 S1D13717 Pinout (FDBGA-160) - corrected typo for ball G3 - changed “FPDAT19” to “FPDAT9”
- Section 5.2 S1D13717 Pinout (FDBGA-160) - corrected typo for ball D12 - changed “DB1” to “DB10”
- section 5.3 Pin Descriptions - multiple changes throughout section to cell and RESET# State of multiple pins
- section 7.3.1 Direct 80 Type 1 - delete 1.8V in tables, change timings throughout
- section 7.3.2 Direct 80 Type 2 - delete 1.8V in tables, change timings throughout
- section 7.3.3 Direct 80 Type 3 - delete 1.8V in tables, change timings throughout
- section 7.3.4 Direct 68 - delete 1.8V in tables, change timings throughout
- section 7.3.5 Indirect 80 Type 1 - delete 1.8V in tables, change timings throughout
- section 7.3.6 Indirect 80 Type 2 - delete 1.8V in tables, change timings throughout
- section 7.3.7 Indirect 80 Type 3 - delete 1.8V in tables, change timings throughout
- section 7.3.8 Indirect 68 - delete 1.8V in tables, change timings throughout
- section 7.5.2 CMCLKOUT Characteristics - add section
- section 7.5.3 Strobe Timing - add section
- section 10.3 Register Restrictions - in first bullet change “REG[030Eh]” to “REG[030Ch]”
- section 10.3 Register Restrictions - in third bullet change “REG[0A0Eh]” to “REG[0F00h]”
- section 10.3 Register Restrictions - add bullet change “When the SD Card Interface is disabled...”
- REG[0034h] - remove reference to TFT type 5 from Note
- REG[0036h] - remove reference to TFT type 5 from Note
- REG[0102h] bits 4-3 - remove “YUV Data Format (16-bit format)” column from table
- REG[0270h] bits 14-12 - remove second reference to 000b from first bullet
- REG[0302h] - remove register
- REG[0306h] - remove register
- REG[030Ah] - remove register
- REG[030Eh] - remove register
- section 11.2 Power Save Mode Functions - add SD Card Interface to table
- change all FCBGA-160 to FCBGA-161

- REG[005Eh] bit 13 - reserve this bit
- REG[005Eh] bit 12 - reserve this bit
- REG[0110h] bit 13 - reserve this bit
- REG[0200h] bit 10 - reserve this bit
- REG[0200h] bit 6 - reserve this bit
- REG[021Ah] bit 2 - reserve this bit
- REG[0244h] bit 2 - reserve this bit
- REG[0260h] through REG[0278h] - reserve these registers
- REG[0930h] bit 4 - reserve this bit
- REG[0940h] bit 10 - add this reserved bit
- REG[0946h] bit 10 - reserve this bit
- REG[0948h] bit 10 - reserve this bit
- REG[094Ah] bit 10 - reserve this bit
- REG[0964h] bit 10 - reserve this bit
- REG[0966h] bit 10 - reserve this bit
- REG[0968h] bit 10 - reserve this bit
- REG[096Ah] bit 10 - reserve this bit
- REG[09D0h] bits 2-0 - reserve 011b, 100b in table
- REG[09D2h] bits 6-0 - remove all reference to horizontal sizes other than 640
- REG[0A00h] - move bit 7 to bit 5, make bit 7 n/a
- REG[0A02h] - move bit 7 to bit 5, make bit 7 n/a
- REG[0A04h] - move bit 7 to bit 5, make bit 7 n/a
- REG[0A40h] - move bit 7 to bit 5, make bit 7 n/a
- REG[1016h] through REG[1018h] - add to spec
- REG[6100h] bits 7-4 - reserve 0010b in table
- add section 7.5 Output Buffer Rise/Fall Time v.s. Capacitance (CL)

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- spec created from S1D13717 spec X52A-A-001-01 (Rev 1.0)
- changed memory size from 320Kb to 224Kb
- updated FCBGA and QFP pin diagrams and all pin# references in the pin description tables
- removed all references to AB18

- removed all references to GPIO[21:4] except in panel descriptions (need to know what to do with panel sections that use these GPIOs)
- removed all Camera2 and 16-bit camera information
- added SD Card timing
- added SD Card registers at REG[6000h]
- added SD Card section at section 21
- removed section 7.6, MPEG Codec Interface (no camera2 interface)
- removed section 7.7, YUV Digital Output (no camera2 interface)
- removed camera2 references in register section (or engineering text until confirmed)
- removed camera2 references in section 20
- section 5.6, updated LCD Pin mapping and LCD Bypass Mode Pin Mapping
- section 7, removed all “Extended TFT” timing
- section 10, reserved all “Extended TFT” registers and removed Type-H/Type-D references in all other registers
- REG[0014h] bits 12-8, reserved all Parallel Bypass Mode bits
- REG[0032h] bits 15-10, reserved the RGB panel type bits
- REG[0102h] bit 6, reserved
- REG[0110h] bits 6-4 and 3-1, updated these bits according to the 13731 bit descriptions