Preliminary Information[1] *(See Last Page)*

Six-Channel Supply Voltage Marginer and Active DC Output Controller (ADOC™)

FEATURES & APPLICATION

- **Extremely accurate (0.2%, typ.) Active DC Output Control**
- **Six-channel control of DC/DC converters**
- **ADOC Automatically adjusts supply output voltage level under all DC load conditions**
- **Capable of margining supplies with trim inputs using either positive or negative trim pin control**
- **Wide Margin/ADOC range from 0.35V to VDD**
- **Uses either an internal or external VREF**
- **Operates from any intermediate bus supply from 6V to 14V and VDD from 2.7V to 5.5V**
- **Programmable START and READY pins**
- **General Purpose 4k EEPROM with Write Protect**
- **I²C 2-wire serial bus for programming configuration and monitoring status.**
- **48-lead TQFP package**

Applications

- **Monitor/Control Distributed and POL Supplies**
- **Multi-voltage Processors, DSPs, ASICs used in Telecom, CompactPCI or server systems**

INTRODUCTION

The SMM605 actively controls the output voltage level of up to six DC/DC converters that use a 'Trim' or 'VADJ/FB' pin to adjust the output. An Active DC Output Control (ADOC™) feature is used during normal operation to maintain extremely accurate settings of supply voltages and, during system test, to control margining of the supplies using the industry standard I²C 2-wire data bus commands. Total accuracy with a ±0.1% external reference is ±0.2%, and ±0.5% using the internal reference. The device can margin supplies with either positive or negative trim pin control within a range of 0.35V to VDD. The SMM605 supply can range from 2.7V to 5.5V or 6V to 14V to accommodate any intermediate bus supply.

The voltage settings (margin high/low and nominal) are programmed into nonvolatile memory. The I²C bus is used to enable margin high, margin low, ADOC or normal operation. When margining, the SMM605 will check the voltage output of the converter and make adjustments to the trim pin via a feedback loop to bring the voltage to the margin setting. A margining status register is set to indicate that the system is ready for test.

SIMPLIFIED APPLICATIONS DRAWING

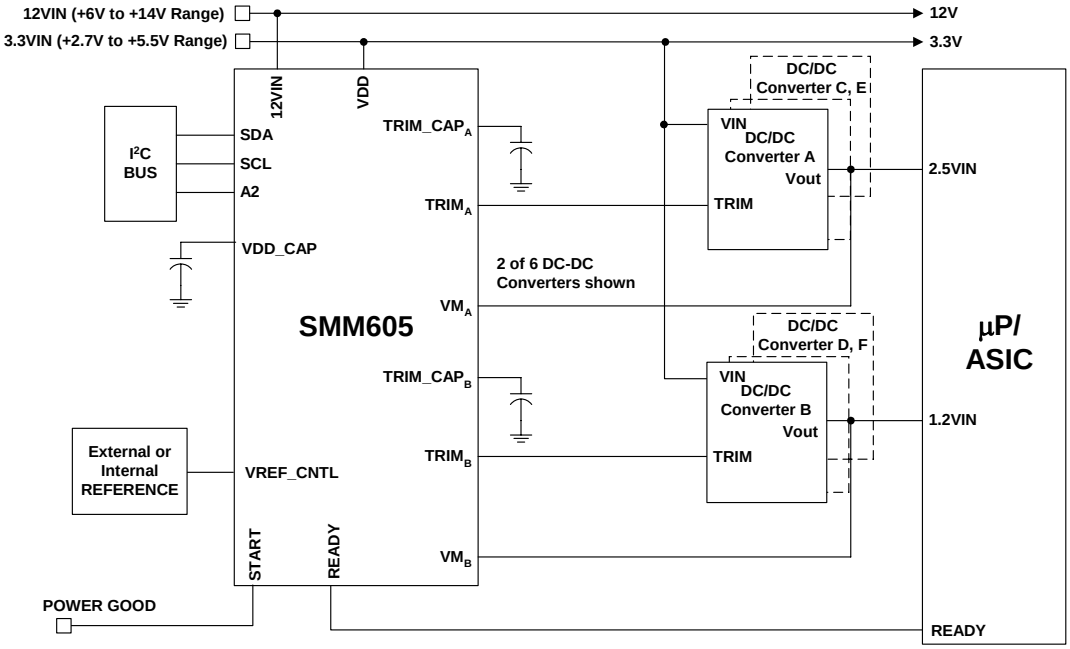


Figure 1 – Applications Schematic using the SMM605 Controller to actively control and margin the output levels of up to six DC/DC Converters.

Note: This is an applications example only. Some pins, components and values are not shown.

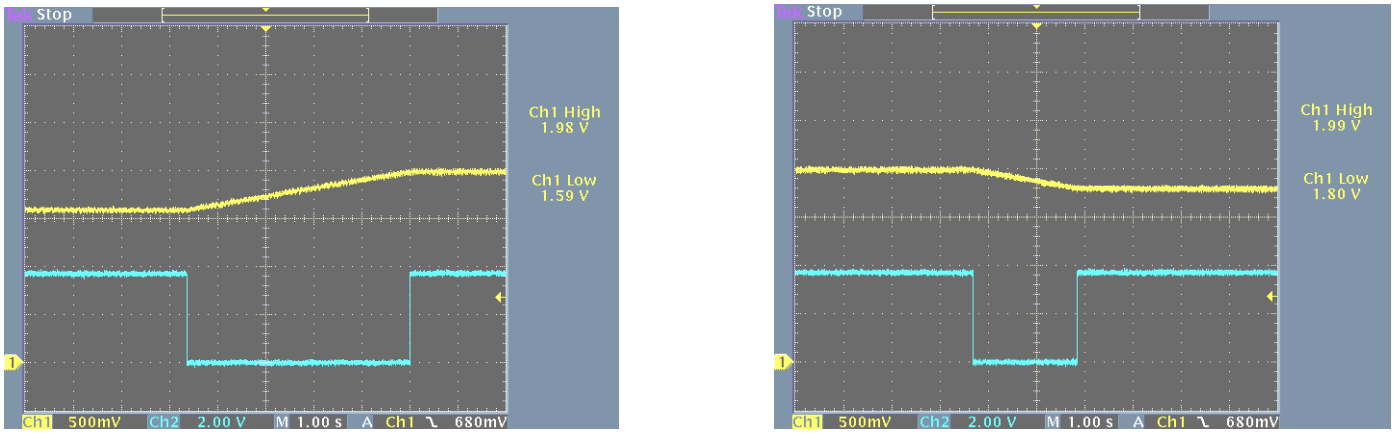


Figure 2 – Example Power Supply Margining using the SMM605. The waveform on the left is margin low to high from 1.6V to 2.0V and the waveform on the right is margin high to nominal from 2.0V to 1.8V. The ADOC function guarantees the output level to be within ±0.2% maximum with a ±0.1% external reference. The bottom waveform is the READY signal indicating margin is complete.

GENERAL DESCRIPTION

The SMM605 is capable of controlling the DC output of up to six DC/DC Modules, switching regulators or LDOs that use a trim/adjust pin and automatically change the level using a unique Active DC Output Control (ADOC™). The ADOC function is programmable over a standard 2-wire I^2C serial data interface and can be used to set the nominal DC output voltage as well as the margin high and low settings. The part actively controls the programmed set levels to maintain tight control over load variations and voltage drops at the point of load. The margin range will vary depending on the supply manufacturer and model but the normal range is 10% adjustment around the nominal output setting. However, the SMM605 has the capability to margin from 0.35V to VDD. The user can set the desired voltage settings (nominal, margin high and margin low) into the EE memory array for the device. Then, volatile registers are used to select one of these settings. These registers are accessed over the I^2C bus.

In normal operation, Active DC Output Control is set to adjust the nominal output voltage of the converter. Typical converter accuracy ratings range from ±2% to ±5% of their output voltage. Using the Active DC Output Control feature of the SMM605 can increase the accuracy to ±0.1% (±0.2% Max.). This high accuracy control of the converter output voltage is extremely important in low voltage applications where deviations in power supply voltage can result in lower system performance. Active DC Output Control can also be used for margining a supply during system test or may be turned off by de-selecting the function in the Control Register.

The margin high and margin low voltage settings can range from 0.35V to VDD around the converters' nominal output voltage setting depending on the specified margin range of the DC-DC converter. When the SMM605 receives the command to margin, the Active DC Output Control will adjust the supply to the selected margin voltage. Once the supply has reached its margined set point, the Ready bit in the status register will set and the READY pin will go active. If Active DC Control is disabled, a margined supply can return to its nominal voltage by writing to the margin command register.

In order to obtain maximum accuracy, the SMM605 requires an external voltage reference. An external reference with ±0.1% accuracy will enable an overall ±0.2% accuracy for the device. A configuration option also exists so that an internal voltage reference can be used, but with less accuracy. Total accuracy using the internal reference is ±0.5%.

The SMM605 has additional filter pins to filter unwanted switching regulator noise. They are VDD_CAP and FILT_CAP.

The SMM605 can be powered from either the 12VIN supply pin (6V to 14V range) via an internal regulator or the VDD supply pin (+2.7 to 5.5V range), see Figure 3.

Programming of the SMM605 is performed over the industry standard I^2C 2-wire serial data interface. A status register is available to read the state of the part and a Write Protect bit is available to prevent writing to the configuration registers and EE memory.

INTERNAL FUNCTIONAL BLOCK DIAGRAM

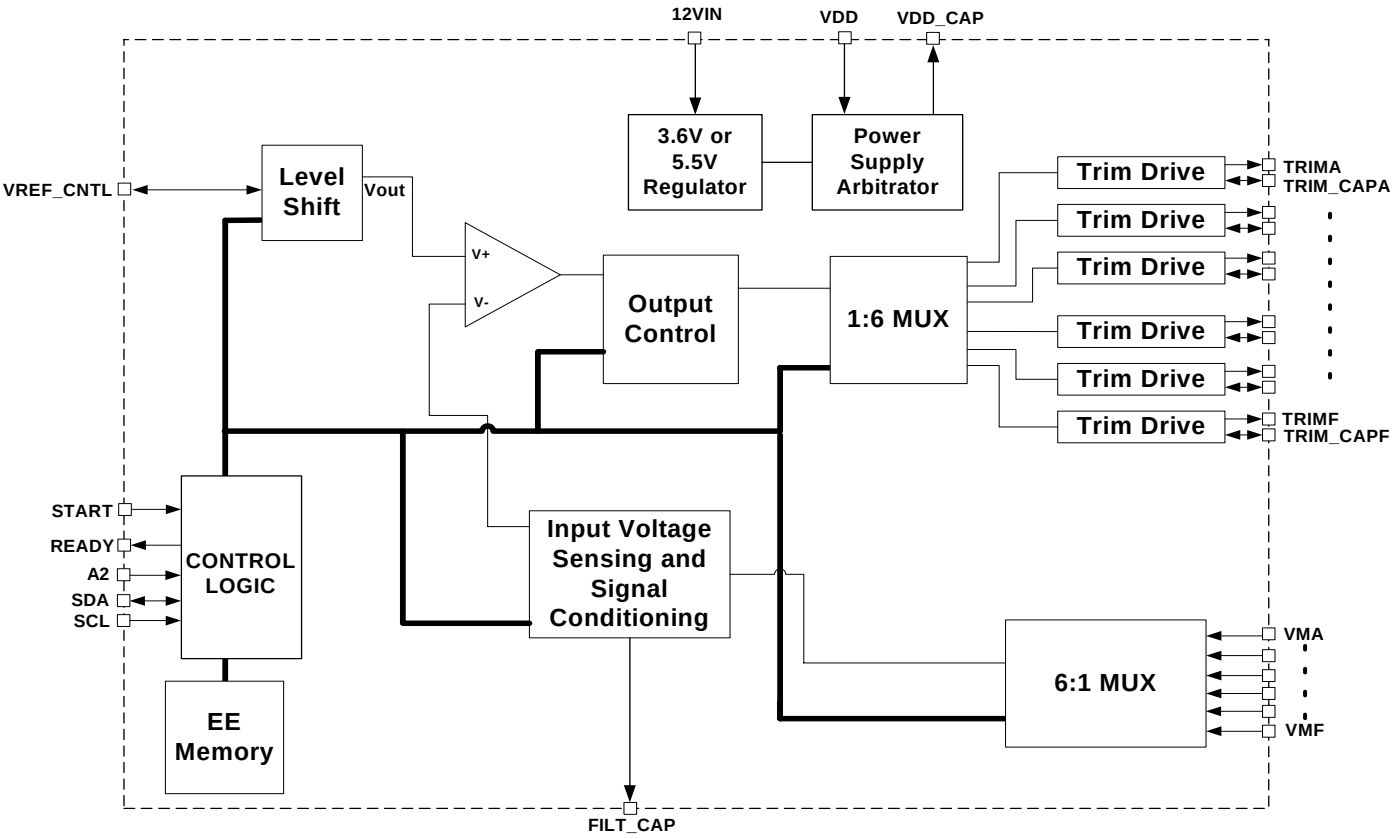


Figure 3 –SMM605 Internal Functional Block Diagram.

PIN DESCRIPTIONS

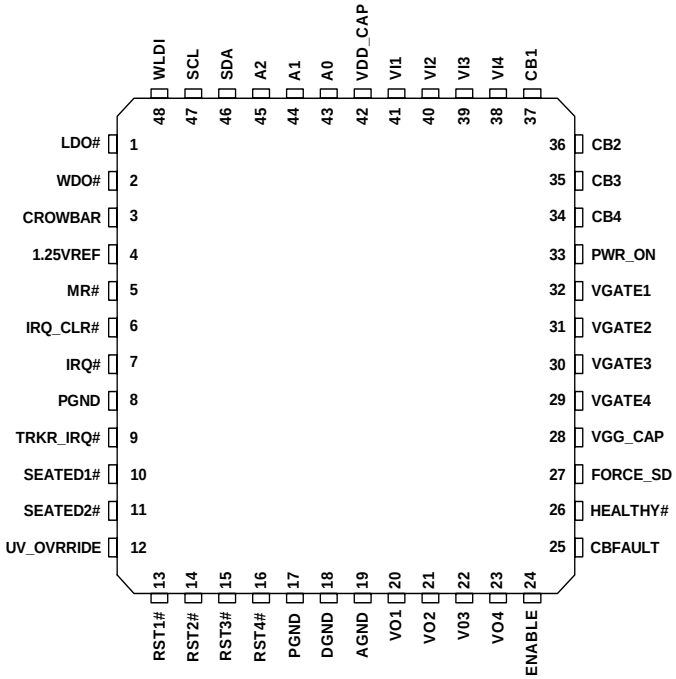
Pin Number[1]	Pin Type	Pin Name	Pin Description
41	IN	**VM_A**	Voltage monitor pin. Connect to the DC-DC converter + sense line or + Vout pin.
36		**VM_B**	
31		**VM_C**	
26		**VM_D**	
21		**VM_E**	
16		**VM_F**	
44	OUT	**$TRIM_A$**	Output voltage used to margin and/or trim converter voltages. Connect to the converter Trim input or to the VADJ or FB pin of an adjustable output switching regulator or LDO through a resistor. If the ADOC/margining functionality is not used on a channel, the associated TRIMx pin should be floating.
39		**$TRIM_B$**	
34		**$TRIM_C$**	
29		**$TRIM_D$**	
24		**$TRIM_E$**	
19		**$TRIM_F$**	
45	I/O	**$TRIM\_CAP_A$**	External sample and hold capacitor input used to set the voltage on the TRIM pins.
40		**$TRIM\_CAP_B$**	
35		**$TRIM\_CAP_C$**	
30		**$TRIM\_CAP_D$**	
25		**$TRIM\_CAP_E$**	
20		**$TRIM\_CAP_F$**	
48	IN	**VDD_CAP**	External capacitor input used to filter the internal supply rail.
47	PWR	**12VIN**	12V power supply input internally regulated to 3.6 or 5.5V. Input range is 6V to 14V using the 3.6V internal regulator setting and 10V to 14V using the 5.5V internal regulator setting.
46	PWR	**VDD**	2.7V to 5.5V Power supply of the part.
5, 6, 12, 13	GND	**GND**	Ground of the part.

PIN DESCRIPTIONS (Cont.)

Pin Number	Pin Type	Pin Name	Pin Description
15	IN	**FILT_CAP**	External capacitor input used to filter VM_X inputs. This provides an RC filter where R = 1kΩ.
14	IN	**VREF_CNTL**	Voltage reference input used for DC output control and margining.
1	I/O	**SDA**	Bi-directional I^2C data line.
2	IN	**SCL**	I^2C clock line.
3	IN	**A2**	The address pin is biased either to VDD_CAP or GND. When communicating with the SMM605 over the 2-wire bus A2 provides a mechanism for assigning a unique bus address.
4	IN	**START**	Programmable active high/low input. The START input is used solely for enabling Active Control and/or margining.
7	OUT	**READY**	Programmable active high/low open drain output signals indicating when all programmed power supplies have reached their preprogrammed setpoints.
	NC	**No Connect**	Leave the NC pins floating.

PACKAGE AND PIN CONFIGURATION

48 LEAD TQFP



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to 125°C
Storage Temperature..... -65°C to 150°C
Terminal Voltage with Respect to GND:
VDD Supply Voltage .....-0.3V to 6.0V
12VIN Supply Voltage.....-0.3V to 15.0V
All Others .....-0.3V to V_{DD} + 0.7V
Output Short Circuit Current 100mA
Lead Solder Temperature (10 secs). ……300°C
Junction Temperature.....……...…..150°C
ESD Rating per JEDEC…… ……..…..2000V
Latch-Up testing per JEDEC……..……...…±100mA

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Industrial).....–40°C to +85°C
(Commercial).....–5°C to +70°C
VDD Supply Voltage .....2.7V to 5.5V
12VIN Supply Voltage[1] .....6.0V to 14.0V
VIN ..... GND to VDD
VOUT ..... GND to 14.0V
Package Thermal Resistance (θ_{JA})
48-Lead TQFP……..…80°C/W

Moisture Classification Level 1 (MSL 1) per J-STD- 020. MSL 3 for 100% Sn, ROHS compliant, see Ordering Information.

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
VDD	Supply Voltage		2.7		5.5	V
12VIN	Supply Voltage	Internally regulated to 5.5V	10		14	V
		Internally regulated to 3.6V	6		14	V
I_{DD}	Power Supply Current from VDD	All TRIM pins floating, 12VIN floating		3	5	mA
I_{12VIN}	Power Supply Current from 12VIN	All TRIM pins floating, VDD floating		3	5	mA
TRIM Characteristics						
I_{TRIM}	TRIM output current through 100Ω to 1.0V	TRIM Sourcing Maximum Current	1.5			mA
		TRIM Sinking Maximum Current	1.5			mA
V_{TRIM}	Margin Control and ADOC Range	Depends on Trim range of DC-DC Converter	VREF_CNTL/4		VDD	V
All other Input and Output Characteristics						
V_{DD_CAP}	VDD_CAP voltage	Internally regulated to 3.6V	3.4	3.6	3.8	V
		Internally regulated to 5.5V	5.3	5.5	5.7	V
		No voltage on 12VIN	VDD – 0.1	VDD	VDD + 0.1	V
V_{IH}	Input High Voltage (FS, SDA, SCL, PWR_ON/OFF)[2]	VDD = 2.7V	0.7 x VDD_CAP			V
		VDD = 5.0V	0.7 x VDD_CAP			V
V_{IL}	Input Low Voltage (FS, SDA, SCL, PWR_ON/OFF)[2]	VDD = 2.7V			0.3 x VDD_CAP	V
		VDD = 5.0V			0.3 x VDD_CAP	V

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min	Typ.	Max	Unit
V_{IH}	Input High Voltage (FS, SDA, SCL, PWR_ON/OFF)[2]	Internally regulated to 3.6V	0.7 x VDD_CAP			V
		Internally regulated to 5.5V	0.7 x VDD_CAP			V
V_{IH}	Input High Voltage (FS, SDA, SCL, PWR_ON/OFF)[2]	Internally regulated to 3.6V			0.3 x VDD_CAP	V
		Internally regulated to 5.5V			0.3 x VDD_CAP	V
I_{OL}	Output Low Current[3]	Note – Total I_{SINK} from all PUPx pins should not exceed 6mA or $ADOC_{ACC}$ specification will be affected	0		1.0	mA
I_{OLSDA}	Output low current for SDA	VOL=0.4V	3			mA
I_S	Leakage current on SDA and SCL	SDA or SCL are at 3.6V			1.0	µA
V_{SENSE}	Positive Sense Voltage	VM pins	+0.35		VDD_CAP	V
$V_{Monitor}$	Monitor Threshold Step Size	VM pins		5		mV
V_{REF}	Internal 1.25V_{REF} Output Voltage Accuracy	T = +25°C	-0.4		+0.4	%
		T = -40°C to +85°C	-0.8		+0.8	%
External V_{REF}	External V_{REF} Voltage Range		0.5		VDD_CAP	V
$ADOC_{ACC}$	ADOC/Margin Accuracy	External V_{REF}=1.25V, ±0.1%, Total PUPx I_{SINK} = 6ma, V_{SENSE} ≤ 3.5V, T = 0°C to +50°C	-0.20	±0.1	+0.20	%
		External V_{REF}=1.25V, ±0.1%, Total PUPx I_{SINK} = 6ma, V_{SENSE} ≤ 3.5V, T = 0°C to +70°C	-0.35	±0.1	+0.35	%
		External V_{REF}=1.25V, ±0.1%, Total PUPx I_{SINK} = 6ma, V_{SENSE} ≥ 3.5V, T = 0°C to +50°C	-0.50	±0.3	+0.50	%
		Internal V_{REF}=1.25V, Total PUPx I_{SINK} = 6ma, T = 0°C to +50°C	-0.50	±0.3	+0.50	%
UVLO	Under Voltage Lockout Threshold[4]	VDD_CAP Rising		2.6		V
		VDD_CAP Falling		2.5		V
$I_{VDD-CAP}$	VDD_CAP Maximum Output Current	VDD = 2.7V to 5.5V, Internal Reg = 3.6V or 5.5V			5	mA

Note 1 – Range depends on internal regulator set to 3.6V or 5.5V see 12VIN specification.
Note 2 – All logic levels are derived with respect to the voltage present on VDD_CAP, when supplied from the VDD input VDD_CAP is equal to VDD, under no load.
Note 3 – SDA not included (separate electrical specification)
Note 4 – (100mV typ Hysteresis)

AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{DC\_CONTROL}$	Active DC Control sampling period	Update period for Active DC Control of channels A – F		1.7		ms
$T_{settling}$	Settling Time	± 10% change in voltage with 0.1% ripple		100		ms
T_{MARGIN}	Margin Time from Nominal to ±5%	Slow Margin, ±10% change in voltage with 0.1% ripple, TRIM_CAP=1µF		850		ms
		Fast Margin, ±10% change in voltage with 0.1% ripple, TRIM_CAP=1µF		85		ms

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS – 100/400kHz

Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND. See Figure 4 Timing Diagram.

Symbol	Description	Conditions	100kHz			400kHz			
			Min	Typ	Max	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency		0		100	0		400	KHz
t_{LOW}	Clock Low Period		4.7			1.3			µs
t_{HIGH}	Clock High Period		4.0			0.6			µs
t_{BUF}	Bus Free Time	Before New Transmission[5]	4.7			1.3			µs
$t_{SU:STA}$	Start Condition Setup Time		4.7			0.6			µs
$t_{HD:STA}$	Start Condition Hold Time		4.0			0.6			µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7			0.6			µs
t_{AA}	Clock Edge to Data Valid	SCL low to valid SDA (cycle n)	0.2		3.5	0.2		0.9	µs
t_{DH}	Data Output Hold Time	SCL low (cycle n+1) to SDA change	0.2			0.2			µs
t_R	SCL and SDA Rise Time	Note 5			1000			1000	ns
t_F	SCL and SDA Fall Time	Note 5			300			300	ns
$t_{SU:DAT}$	Data In Setup Time		250			150			ns
$t_{HD:DAT}$	Data In Hold Time		0			0			ns
TI	Noise Filter SCL and SDA	Noise suppression		100			100		ns
t_{WR}	Write Cycle Time				5			5	ms

Note 5 - Guaranteed by Design.

TIMING DIAGRAMS

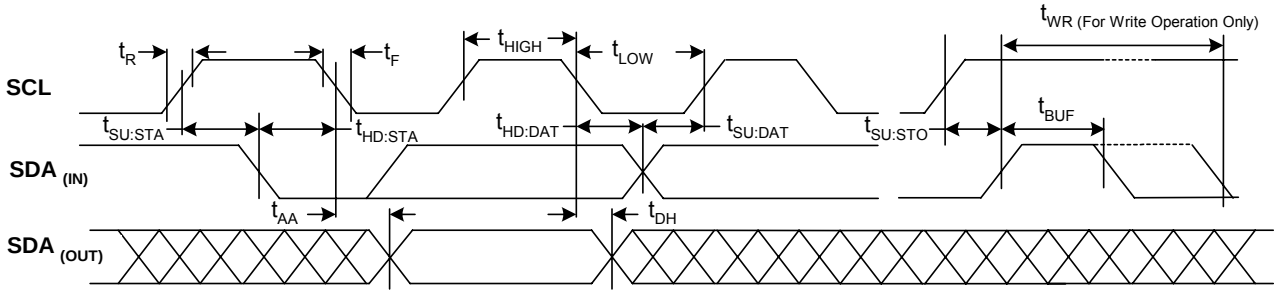


Figure 4 - Basic I²C Serial Interface Timing

APPLICATIONS INFORMATION

DEVICE OPERATION

POWER SUPPLY

The SMM605 can be powered by either a 6V to 14V input through the 12VIN pin or by a 2.7V to 5.5V input through the VDD pin (Figure 3). The 12VIN pin feeds an internal programmable regulator that internally generates either 5.5V or 3.6V. The internal regulator must be set to 3.6V if using an 8V supply. A voltage arbitration circuit allows the device to be powered by the highest voltage from either the regulator output or the VDD input. This voltage arbitration circuit continuously checks for these voltages to determine which will power the SMM605. The resultant internal power supply rail is connected to the VDD_CAP pin that allows both filtering and hold-up of the internal power supply.

VOLTAGE REFERENCE

The SMM605 can operate using either an internal or external voltage reference, VREF. The internal VREF is set to 1.25V. Total accuracy with a ±0.1% external reference is ±0.2% and ±0.5% using the internal reference.

MODES OF OPERATION

The SMM605 has two basic modes of operation: supply margining mode and Active DC Output Control (ADOC™). A detailed description of each mode and feature follows.

ACTIVE DC OUTPUT CONTROL (ADOC)

The SMM605 can actively control the DC output voltage of bricks or DC/DC converters that have a trim pin during monitoring and margining mode. The converter may be an off-the shelf compact device, or may be a “roll your own” circuit on the application board. In either case, the SMM605 dramatically improves voltage accuracy (down to ±0.2%) by implementing closed-loop ADOC active control. This utilizes the DC-DC’s “trim” pin as shown in Figure 7, or an equivalent output voltage feedback adjustment “VADJ” or “FB” node in a user’s custom circuit, Figure 8. Each of the $TRIM_X$ pins on the SMM605 is connected to the trim input pins on the power supply converters.

A sense line from the channel’s point-of-load connects to the corresponding VM_X input. The ADOC function cycles through all six channels (A-F) every 1.7ms making slight adjustments to the voltage on the associated $TRIM_X$ output pins based on the voltage inputs on the VM_X pins. These voltage adjustments allow the SMM605 to control the output voltage of power supply converters to within ±0.2% when using a ±0.1% external voltage reference.

The voltage on the $TRIM\_CAP_X$ pins is buffered and applied to the $TRIM_X$ pin. The voltage adjustments on the $TRIM_X$ pins cause a slight ripple of less than 1mV on the power supply voltage. The amplitude of this ripple is a function of the $TRIM\_CAP_X$ capacitor and the trim gain of the converter. Calculation of the $TRIM\_CAP_X$ capacitor to achieve a desired minimum ripple is detailed in Application Note 37.

The pulse of current can be increased to a 10X pulse of current until the power supply voltages are at their nominal settings by selecting the programmable Fast Convergence option. As the name implies, this option decreases the time required to bring a supply voltage from the converter’s nominal output voltage to the Active DC Output Control nominal voltage setting.

The device can be programmed to either enable or disable the Active DC Control function. When disabled or not active, the $TRIM_X$ pins on the SMM605 are high impedance inputs. The voltage on the $TRIM_X$ pins are buffered and applied to the $TRIM\_CAP_X$ pins charging the capacitor. This allows a smooth transition from the converter’s nominal voltage to the SMM605 controlling that voltage to the Active DC Control nominal setting.

MONITORING

The SMM605 monitors the VM_X pins. The READY pin is programmable active high/low open drain output indicates that all VM_X pins are at their set point.

APPLICATIONS INFORMATION (CONTINUED)

MARGINING

The SMM605 has two additional Active DC Output Control voltage settings: margin high and margin low. The margin high and margin low settings can be as much as ±10% of the nominal setting depending on the manufacturer. The SMM605 range can be as large as 0.35V to VDD. These settings are stored in the configuration registers and are loaded into the Active DC Output Control voltage setting by margin commands issued via the I^2C bus. The device must be enabled for Active DC Output Control in order to enable margining.

The margin command registers contain two bits that decode the commands to margin high, margin low, or control to the nominal setting. Once the SMM605 receives the command to margin the supply voltage, it begins adjusting the supply voltage to move toward the desired setting. When this voltage setting is reached, a bit is set in the margin status registers and the READY signal becomes active. (Figure 2, 5 and 6)

Note: Configuration writes or reads of registers 00_{HEX} to 03_{HEX} should not be performed while the SMM605 is margining.

WRITE PROTECTION

Write protection for the SMM605 is located in a volatile register where the power-on state is defaulted to write protect. There are separate write protect modes for the configuration registers and memory. In order to remove write protection, the code 55_{HEX} is written to the write protection register. Other codes will enable write protection. For example, writing 59_{HEX} will allow writes to the configuration register but not to the memory, while writing 35_{HEX} will allow writes to the memory but not to the configuration registers. In addition, there is a configuration register lock bit, which, once programmed, does not allow the configuration registers to be changed.

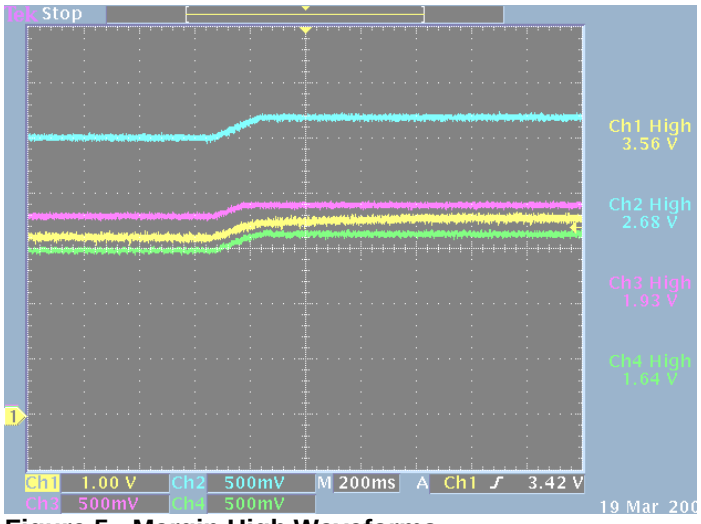


Figure 5 - Margin High Waveforms

Time/Horizontal division = 200ms

Ch 1 (1V/Div) = 3.3V DC-DC converter output (Yellow trace)
Ch 2 (500mV/Div) = 2.5VDC-DC converter output (Blue trace)
Ch 3 (500mV/Div) = 1.8V DC-DC converter output (Purple trace)
Ch 4 (500mV/Div) = 1.5V DC-DC converter output (Green trace)

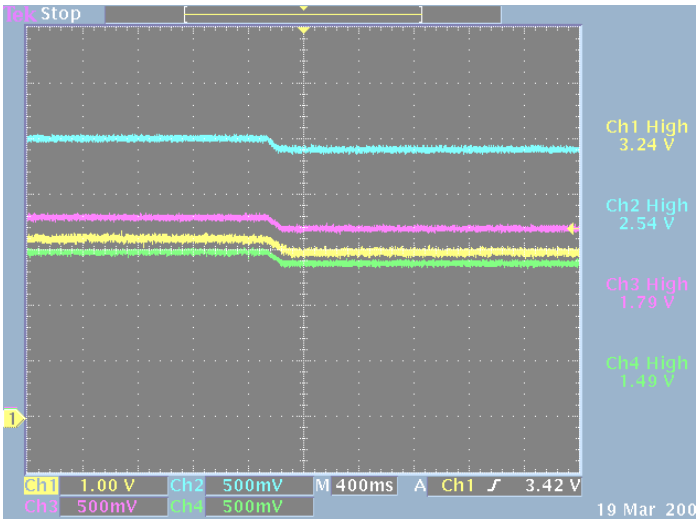


Figure 6 - Margin Low Waveforms

Time/Horizontal division = 400ms

Ch 1 (1V/Div) = 3.3V DC-DC converter output (Yellow trace)
Ch 2 (500mV/Div) = 2.5V DC-DC converter output (Blue trace)
Ch 3 (500mV/Div) = 1.8V DC-DC converter output (Purple trace)
Ch 4 (500mV/Div) = 1.5V DC-DC converter output (Green trace)

APPLICATIONS INFORMATION (CONTINUED)

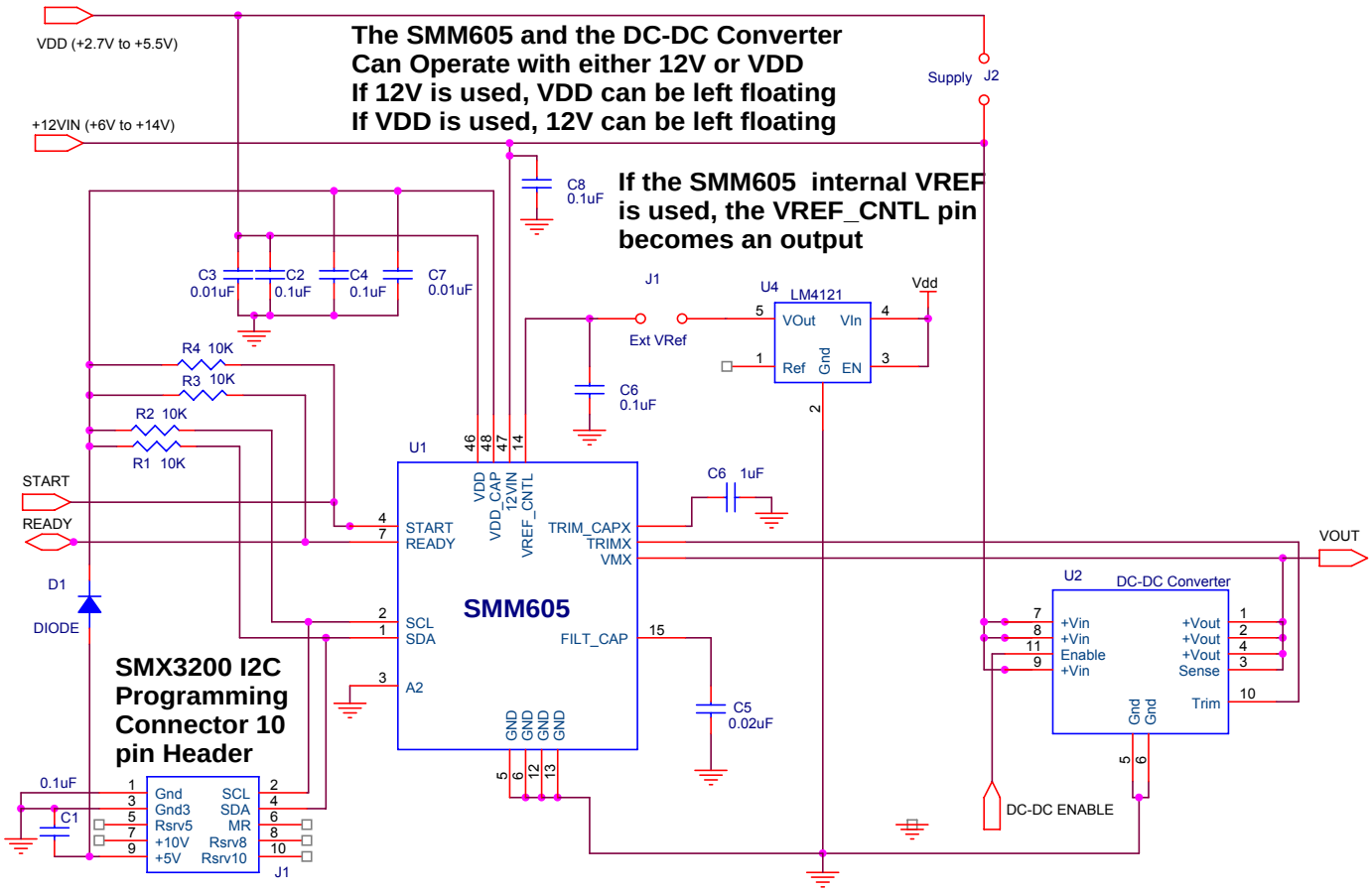


Figure 7 – SMM605 Applications schematic. The accuracy of the external (U4) or internal reference sets the accuracy of the ADOC function. Total accuracy with a ±0.1% external reference is ±0.2% and ±0.5% with the internal reference. The 12V supply can go as low as 6V if the internal regulator is set to 3.6V.

APPLICATIONS INFORMATION (CONTINUED)

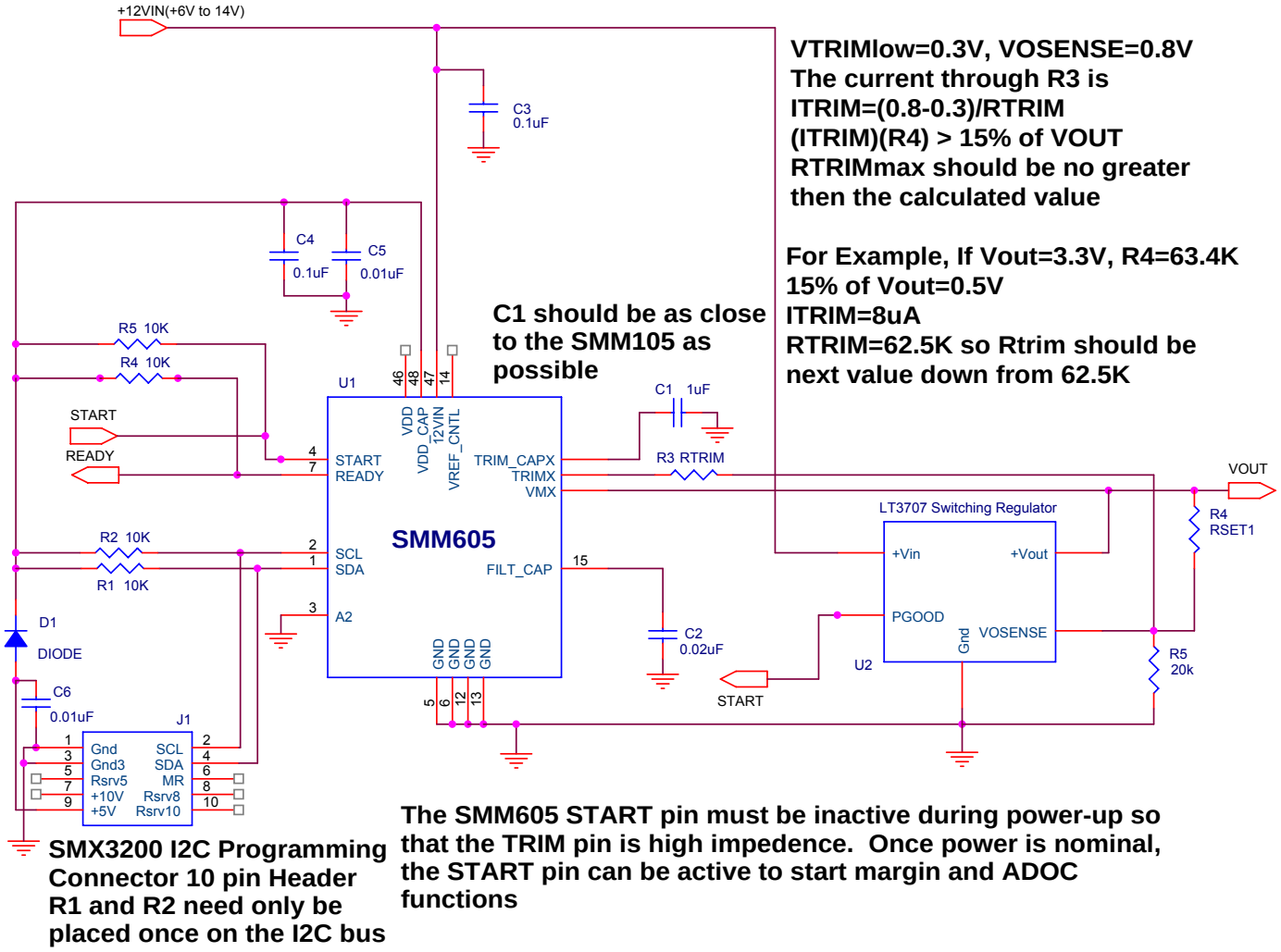


Figure 8 – SMM605 Applications schematic for an adjustable switching regulator (Full regulator circuit not shown).

APPLICATIONS INFORMATION (CONTINUED)

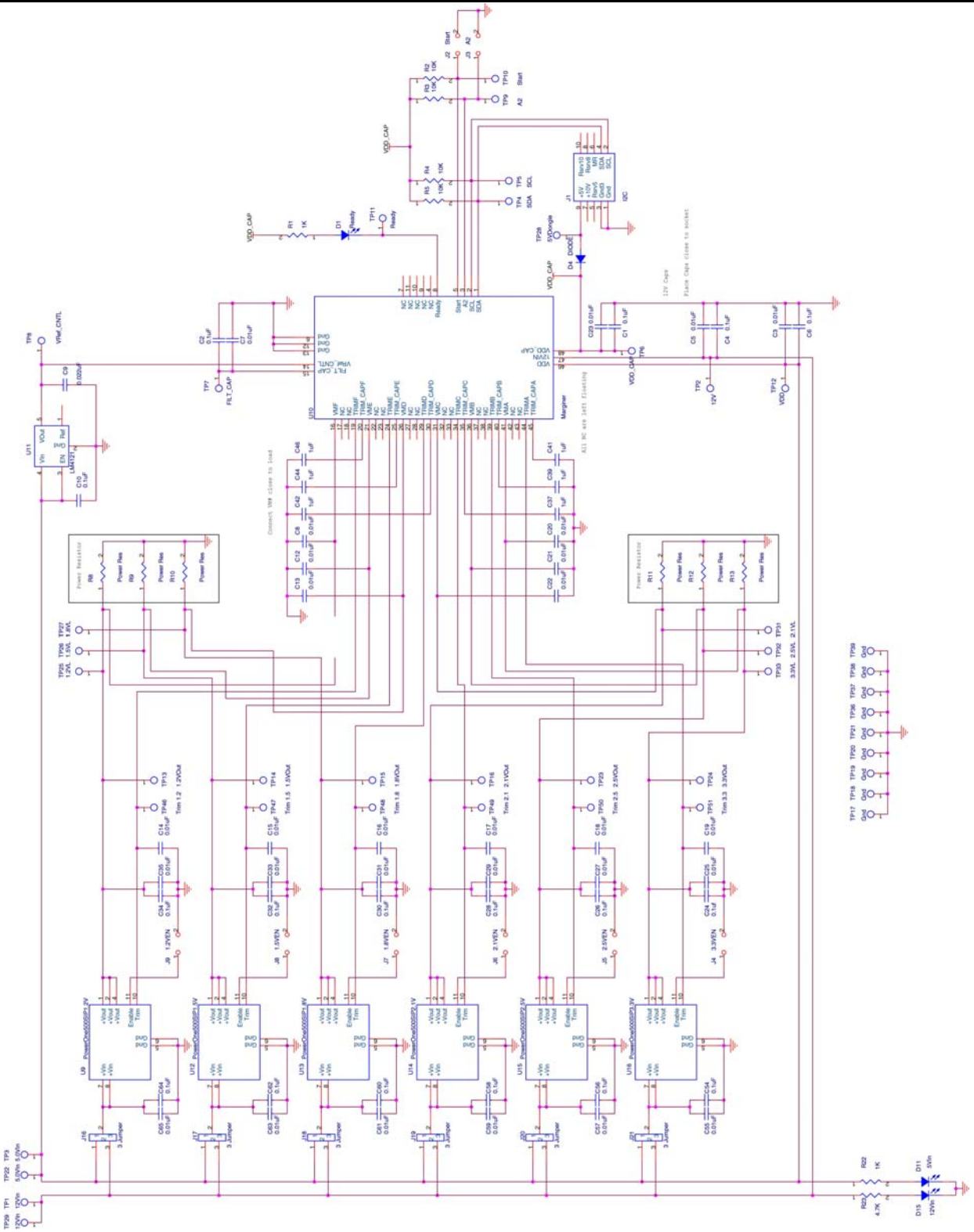


Figure 9 – SMM605 Applications schematic.

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 is available from the website (www.summitmicro.com).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I^2C serial bus format so that it can be directly downloaded to the SMM605 via the programming Dongle and cable. An example of the connection interface is shown in Figure 10.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

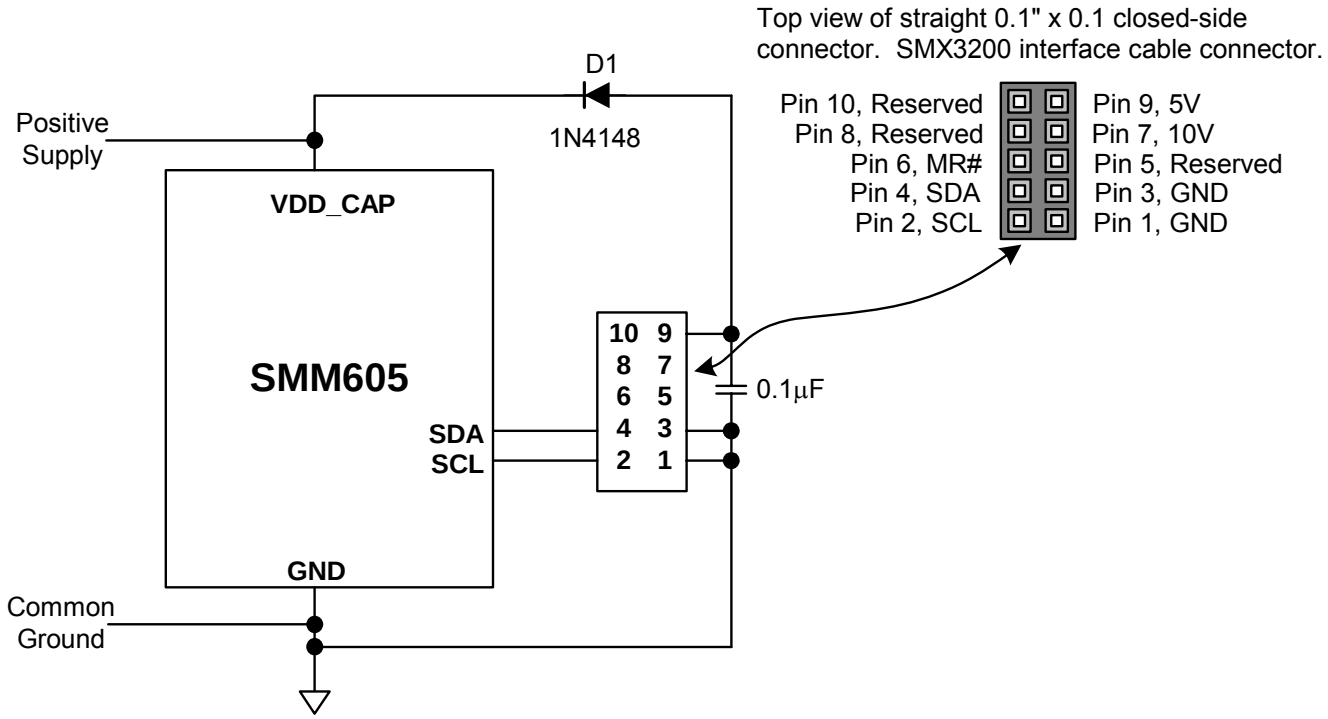


Figure 10– SMX3200 Programmer I^2C serial bus connections to program the SMM605. The SMM605 has a Write Protect pin (WP# input) which when, asserted, prevents writing to the configuration registers and EE memory. In addition, there is a configuration register lock bit which, once programmed, does not allow the configuration registers to be changed.

I²C PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers, general-purpose memory and command and status registers is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an Acknowledge is provided by the device receiving data. The SCL high period (t_{HIGH}) is used for generating Start and Stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a Start condition while a low-to-high transition of SDA while SCL is high is considered a Stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 4-bit device type identifier (slave address) and a 3-bit bus address. The remaining bit indicates either a read or a write operation. Refer to Table 1 for a description of the address bytes used by the SMM605.

The device type identifier for the memory array is generally set to 1010_{BIN} following the industry standard for a typical nonvolatile memory. There is an option to change the identifier to 1011_{BIN} allowing it to be used on a bus that may be occupied by other memory devices. The configuration registers are grouped with the memory array and thus use 1010_{BIN} or 1011_{BIN} as the device type identifier. The command and status registers are accessible with the separate device type identifier of 1001_{BIN}.

The bus address bits A[1:0] are programmed into the configuration registers. Bus address bit A[2] can be programmed as either 0 or biased by the A2 pin. The bus address accessed in the address byte of the serial data stream must match the setting in the SMM605 and on the A2 pin.

Any access to the SMM605 on the I^2C bus will temporarily halt the monitoring function. The SMM605 halts the monitor function from when it acknowledges the address byte until a valid stop is received.

WRITE

Writing to the memory or a configuration register is illustrated in Figures 11, 12, 13, 17 and 18. A Start condition followed by the address byte is provided by the host; the SMM605 responds with an Acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMM605 responds with an acknowledge; the host then clocks in on byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page. After the last byte is clocked in and the host receives an Acknowledge, a Stop condition must be issued to initiate the nonvolatile write operation.

READ

The address pointer for the configuration registers, memory, command and status registers must be set before data can be read from the SMM605. This is accomplished by issuing a dummy write command, which is simply a write command that is not followed by a Stop condition. The dummy write command sets the address from which data is read. After the dummy write command is issued, a Start command followed by the address byte is sent from the host. The host then waits for an Acknowledge and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command. Additional bytes can be clocked out of consecutive addresses with the host providing an Acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the Acknowledge clock cycle and then issuing a Stop condition. Refer to Figures 14, 16, 19 and 21 for an illustration of the read sequence.

I²C PROGRAMMING INFORMATION (CONTINUED)

WRITE PROTECTION

The SMM605 powers up into a write protected mode. Writing a code to the volatile write protection register can disable the write protection. The write protection register is located at address 87_{HEX} of slave address 1001_{BIN}.

Writing 0101_{BIN} to bits [7:4] of the write protection register allow writes to the general-purpose memory while writing 0101_{BIN} to bits [3:0] allow writes to the configuration registers. The write protection can re-enable by writing other codes (not 0101_{BIN}) to the write protection register. Writing to the write protection register is shown in Figure 11.

CONFIGURATION REGISTERS

The majority of the configuration registers are grouped with the general-purpose memory located at either slave address 1010_{BIN} or 1011_{BIN}. The bus address bits, A[1:0], used to differentiate the general-purpose memory from the configuration registers are set to 11_{BIN}. Bus address bit A[2] can be programmed as either 0 or biased by the A2 pin.

Two additional configuration registers are located at addresses 83_{HEX} and 84_{HEX} of slave address 1001_{BIN}.

Writing and reading the configuration registers is shown in Figures 14 and 16.

Note: Configuration writes or reads of registers 00_{HEX} to $0F_{HEX}$ should not be performed while the SMM605 is margining.

GENERAL-PURPOSE MEMORY

The 4k-bit general-purpose memory is located at either slave address 1010_{BIN} or 1011_{BIN}. The bus address bits, A[1:0], used to differentiate the general-purpose memory from the configuration registers are set to 00_{BIN} for the first 2k-bits and 01_{BIN} for the second 2k-bits. Bus address bit A[2] can be programmed as either 0 or biased by the A2 pin.

The word address must be set each time the memory is accessed. Memory writes and reads are shown in Figures 17, 18 and 19.

COMMAND AND STATUS REGISTERS

The command and status registers are located at slave address 1001_{BIN}. Writes and reads of the command and status registers are shown in Figures 20 and 21.

GRAPHICAL USER INTERFACE (GUI)

Device configuration utilizing the Windows based SMM605 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (www.summitmicro.com). Using the GUI in conjunction with this datasheet and application note 40 simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMM605. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I²C bus protocol.

Slave Address	Bus Address	Register Type
1001_{BIN}	A2 A1 A0	Write Protection Register, Command and Status Registers, Two Configuration Registers
1010_{BIN} or 1011_{BIN}	A2 0 0	1st 2-k Bits of General-Purpose Memory
	A2 0 1	2nd 2-k Bits of General-Purpose Memory
	A2 1 1	Configuration Registers

Table 1 - Address bytes used by the SMM605.

I²C PROGRAMMING INFORMATION (CONTINUED)

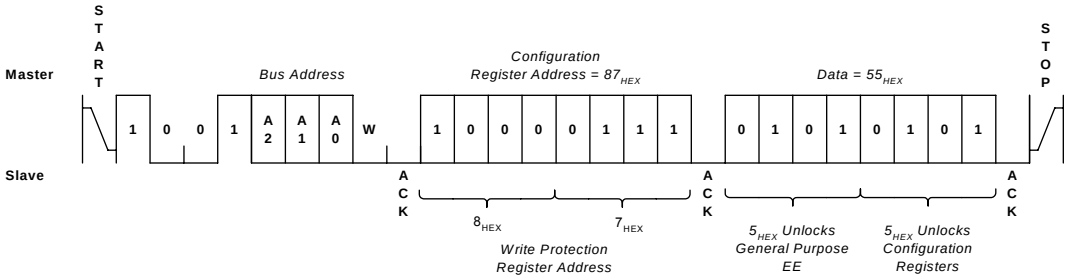


Figure 11 – Write Protection Register Write

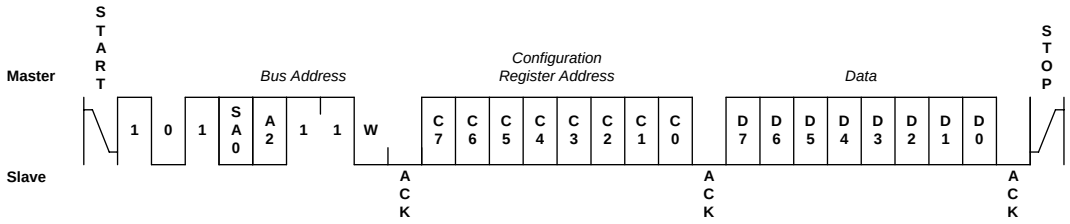


Figure 12 – Configuration Register Byte Write

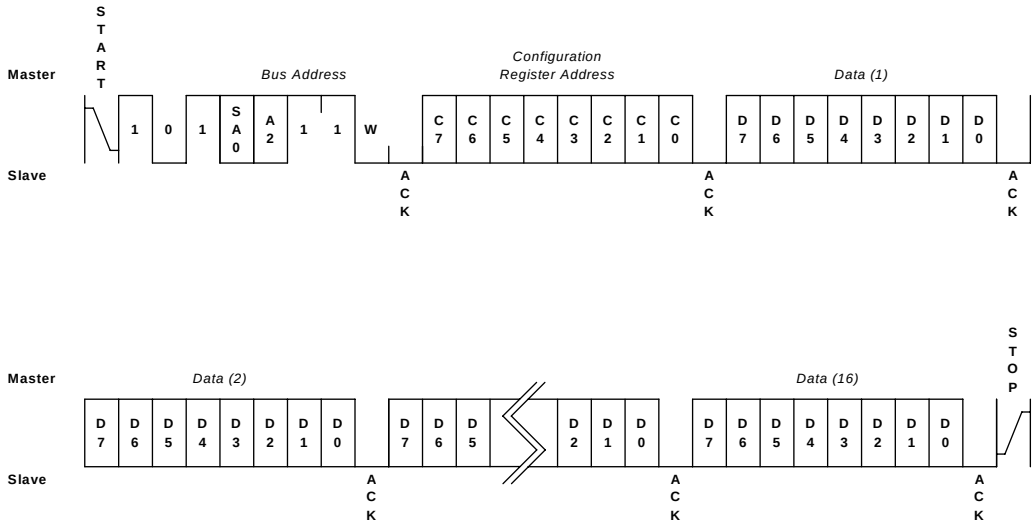


Figure 13 – Configuration Register Page Write

I²C PROGRAMMING INFORMATION (CONTINUED)

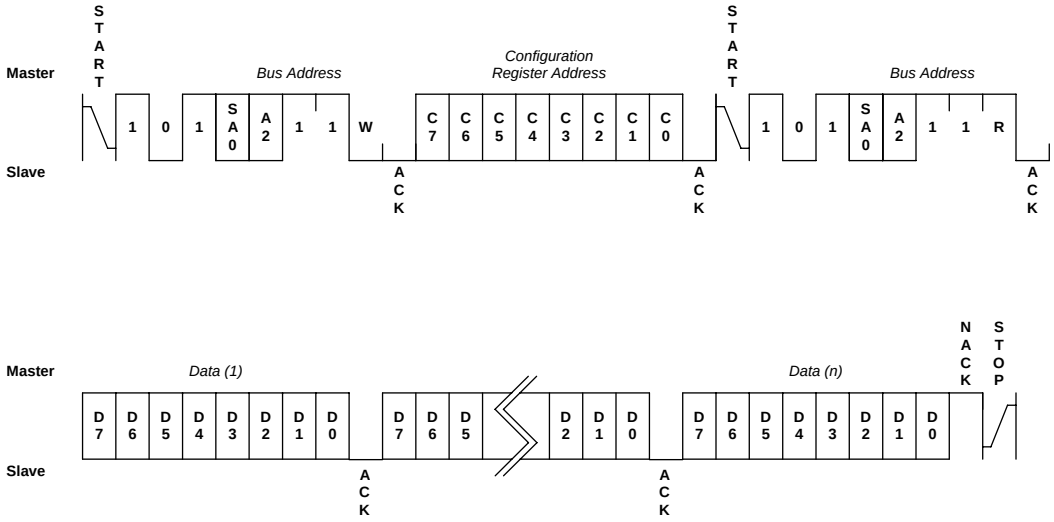


Figure 14 - Configuration Register Read

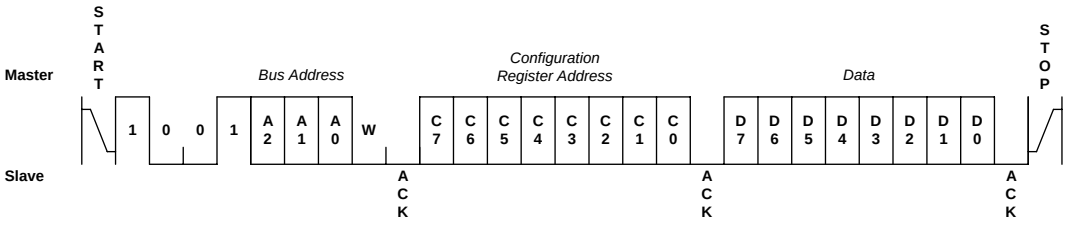


Figure 15 - Configuration Register with Slave Address 1001_{BIN} Write

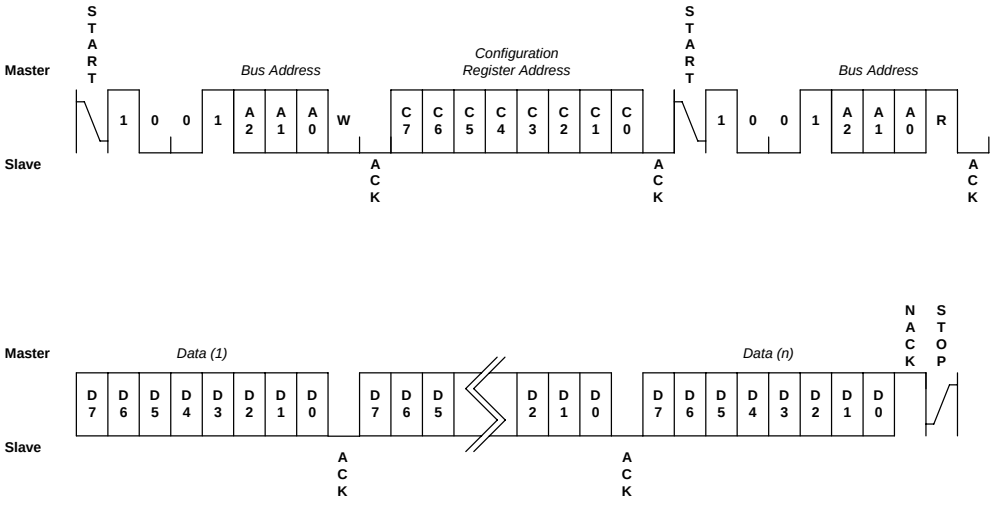


Figure 16 - Configuration Register with Slave Address 1001_{BIN} Read

I²C PROGRAMMING INFORMATION (CONTINUED)

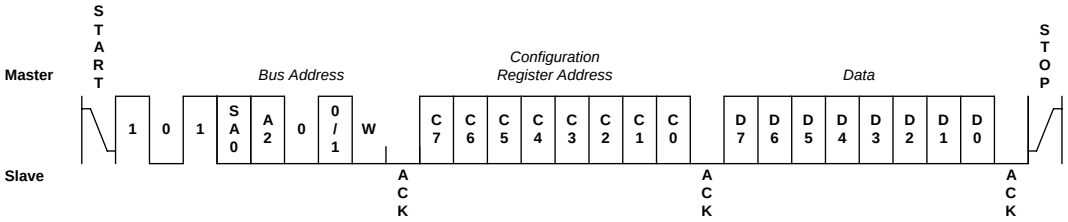


Figure 17 – General Purpose Memory Byte Write

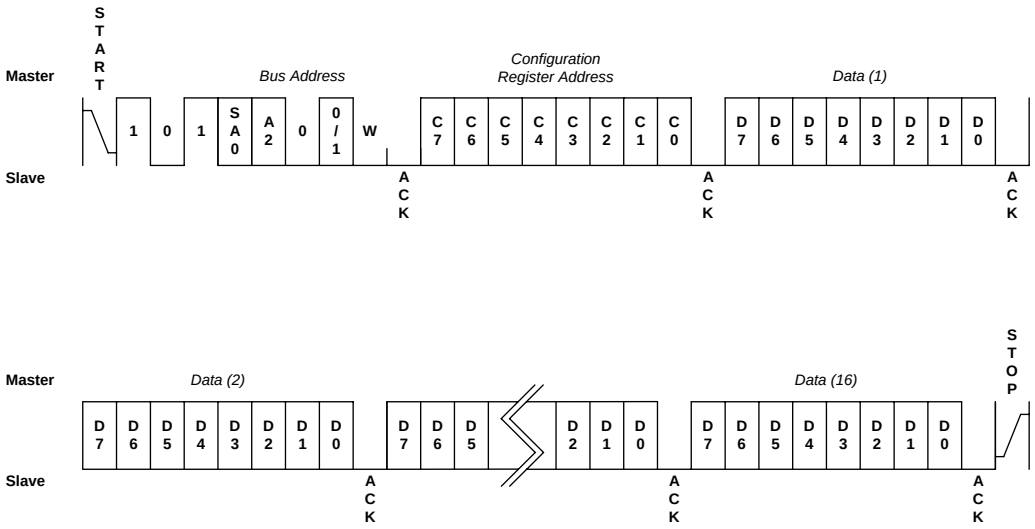


Figure 18 - General Purpose Memory Page Write

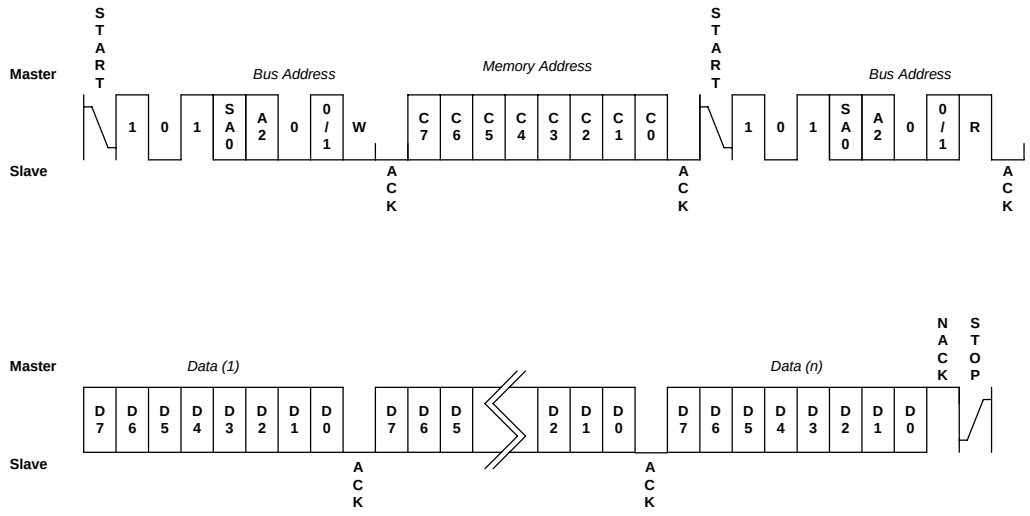


Figure 19 - General Purpose Memory Read

I²C PROGRAMMING INFORMATION (CONTINUED)

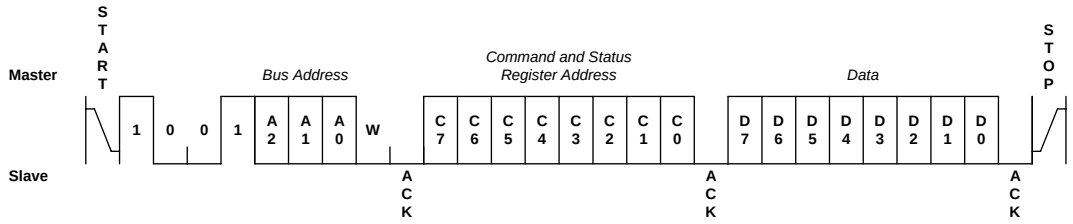
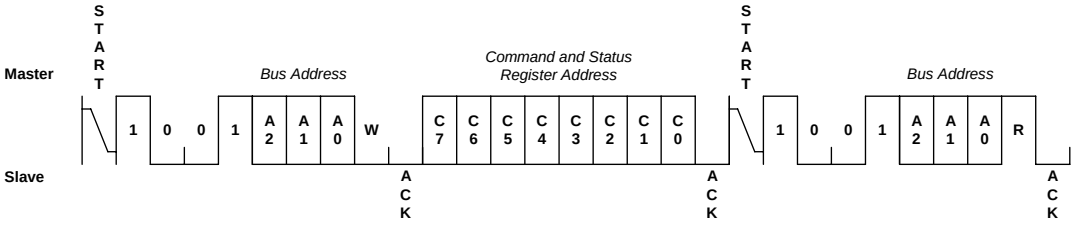


Figure 20 – Command and Status Register Write



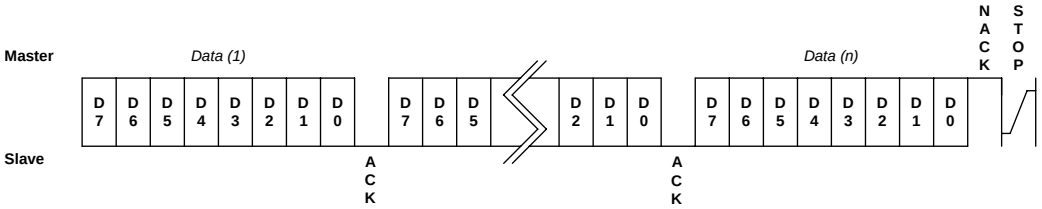


Figure 21 – Command and Status Register Read

DEFAULT CONFIGURATION REGISTER SETTINGS – SMM605FC-890

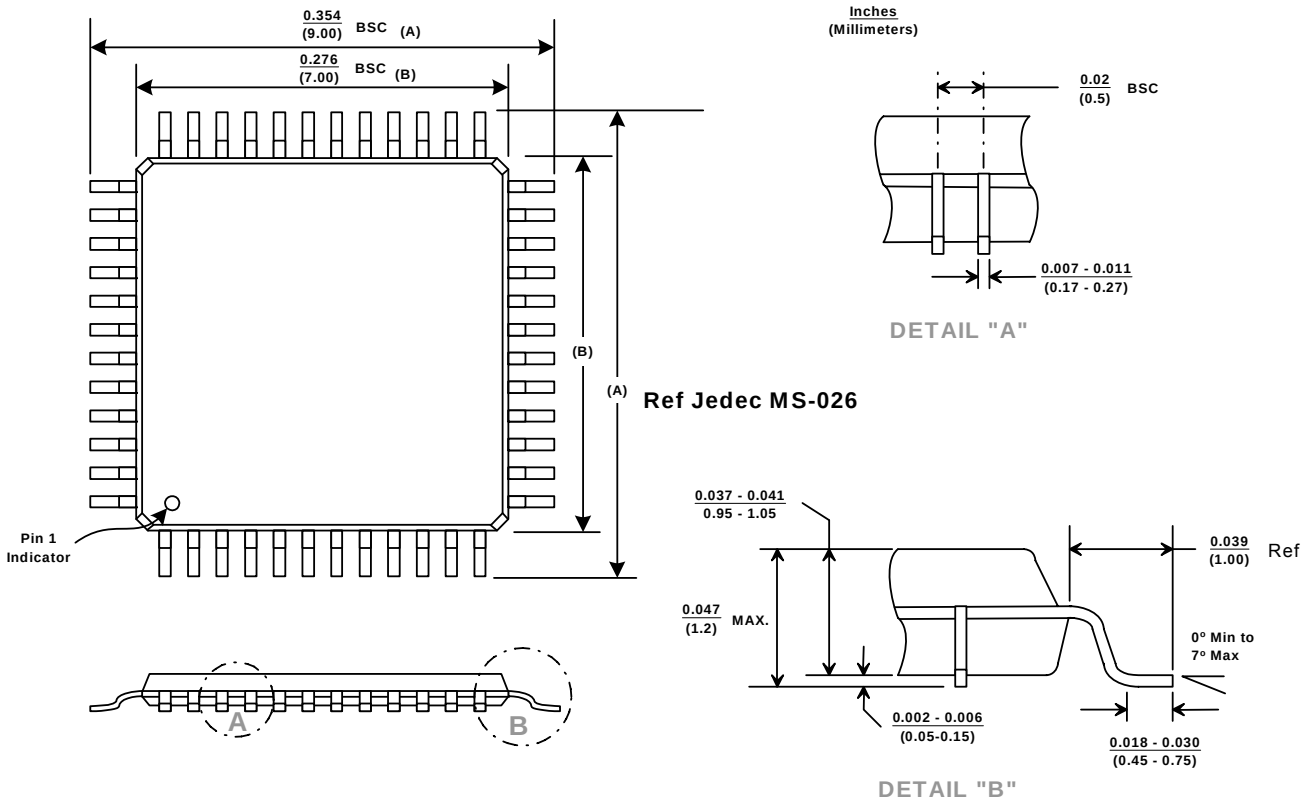
Register	Contents	Register	Contents	Register	Contents
R00	0D	R18	00	R40	0D
R01	84	R19	00	R41	AB
R02	0E	R30	0D	R42	0E
R03	00	R31	64	R43	2D
R04	0E	R32	0D	R44	0E
R05	80	R33	DA	R45	C7
R06	0E	R34	0E	R46	0E
R07	C7	R35	46	R47	F1
R08	0F	R36	0E	R48	0F
R09	55	R37	A2	R49	92
R0A	0B	R38	0F	R4A	0B
R0B	27	R39	20	R4B	70
R0C	7F	R3A	0F	R83	00
R0D	3F	R3B	D9	R84	03
R0E	04	R3C	00	R86	03
R0F	00	R3D	12	R87	FF
		R3E	50		

RC1

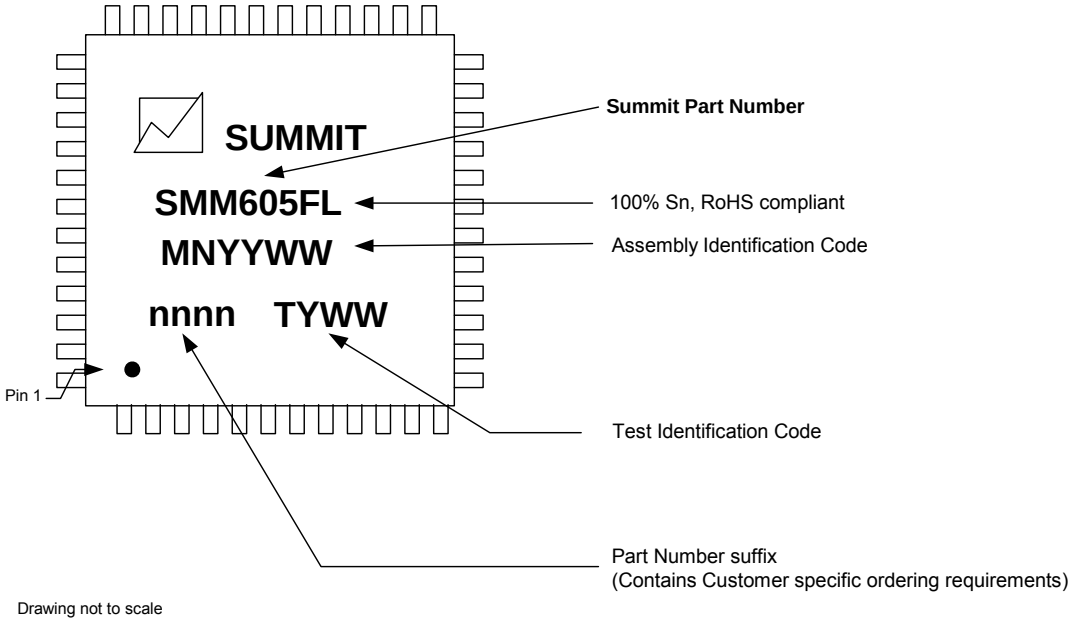
The default device ordering number is SMM605FC-890, is programmed as described above and tested over the commercial temperature range. Application Note 40 contains a complete description of the Windows GUI and the default settings of each of the 48 individual Configuration Registers.

PACKAGE

48 PIN TQFP PACKAGE

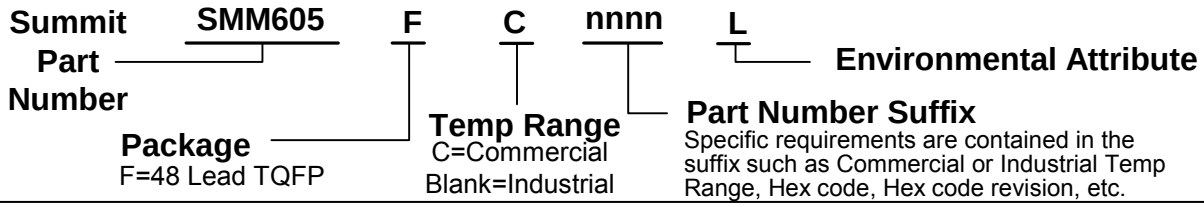


PART MARKING



Drawing not to scale

ORDERING INFORMATION



NOTICE

NOTE 1 - This is a ***Preliminary Information*** data sheet that describes a Summit product currently in pre-production with limited characterization.

Revision 2.1 - This document supersedes all previous versions. Please check the Summit Microelectronics Inc. web site at www.summitmicro.com for data sheet updates.