National Semiconductor

PRELIMINARY

microCMOS

MM54HC169/MM74HC169 4-Bit Up/Down Synchronous Binary Counter

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to achieve high performance. These devices retain the low power and high noise immunity of CMOS logic, while offering the high speed operation and large output drive typically associated with bipolar circuits.

These counters are incremented or decremented on the rising edge of the CLK, clock, input if ENT and ENP are held low. The counters increment when the U/D input is at a logic "1", and will decrement when U/D is low. The ENT input is fed forward to enable the carry output. RCO, ripple carry output, once enabled, will produce a low level pulse while the count is 0 (down count mode) or when the count is all 1s (up mode).

These counters are presettable, that is, they may be loaded when LOAD is taken low and a rising edge appears on the CLK input.

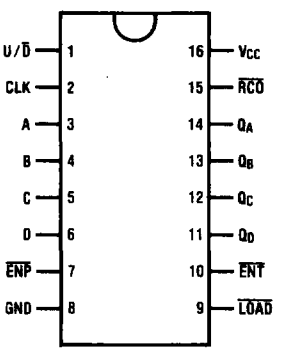
The MM54HC169/MM74HC169 are functional, speed and pin equivalent to the equivalent LS-TTL circuit. Its inputs are protected from damage due to electrostatic discharge by diodes from V_{CC} to ground.

Features

- Wide power supply range: 2.0V to 6.0V
- High input noise immunity
- Wide operating frequency range: 30 MHz
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HC)

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5771-1

Logic Diagram