NTB90N02, NTP90N02

Power MOSFET
90 Amps, 24 Volts
N−Channel D^{2}PAK and TO−220

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Pb−Free Packages are Available

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	24	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±20	Vdc
Drain Current − Continuous @ T_A = 25°C − Single Pulse (t_p = 10 μs)	I_D I_{DM}	90* 200	A A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	85 0.66	W W/°C
Operating and Storage Temperature	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 28 Vdc, V_{GS} = 10 Vdc, L = 5.0 mH, $I_{L(pk)}$ = 17 A, RG = 25 Ω)	E_{AS}	733	mJ
Thermal Resistance Junction−to−Case Junction−to−Ambient (Note 1)	$R_{\theta JC}$ $R_{\theta JA}$	1.55 70	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in^2).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in^2).

*Chip current capability limited by package.

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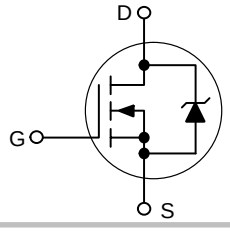
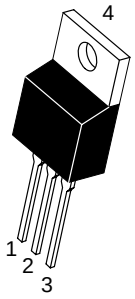
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
24 V	5.0 mΩ @ 10 V	90 A
	7.5 mΩ @ 4.5 V	

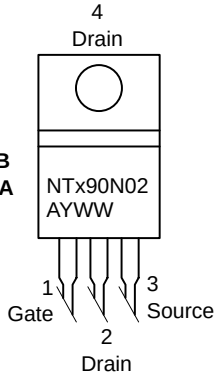
N−Channel

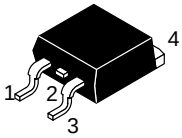


MARKING DIAGRAMS

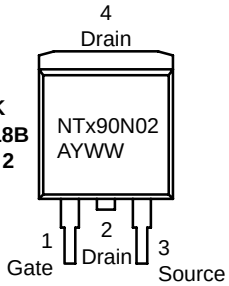


TO−220AB CASE 221A STYLE 5





D^{2}PAK CASE 418B STYLE 2



NTx90N02	= Device Code
x	= P or B
A	= Assembly Location
Y	= Year
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 24 −	 27 25	 − −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 24 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 − −	 − −	 1.0 10	μAdc
Gate−Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 −	 1.9 −3.8	 3.0 −	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 10 Vdc, I_D = 90 Adc) (V_{GS} = 4.5 Vdc, I_D = 40 Adc) (V_{GS} = 10 Vdc, I_D = 20 Adc) (V_{GS} = 4.5 Vdc, I_D = 20 Adc)		$R_{DS(on)}$	 − − − −	 5.0 7.5 5.0 7.5	 5.8 9.0 5.8 9.0	mΩ
Forward Transconductance (Note 3) (V_{DS} = 15 Vdc, I_D = 10 Adc)		g_{FS}	−	25	−	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	2120	−	pF
Output Capacitance		C_{oss}	−	900	−	
Transfer Capacitance		C_{rss}	−	360	−	
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{DD} = 20 Vdc, I_D = 20 Adc, V_{GS} = 4.5 Vdc, R_G = 2.5 Ω)	$t_{d(on)}$	−	16	−	ns
Rise Time		t_r	−	90	−	
Turn−Off Delay Time		$t_{d(off)}$	−	28	−	
Fall Time		t_f	−	60	−	
Gate Charge	(V_{DS} = 20 Vdc, I_D = 20 Adc, V_{GS} = 4.5 Vdc) (Note 3)	Q_T	−	29	−	nC
		Q_1	−	8.0	−	
		Q_2	−	20	−	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 2.3 Adc, V_{GS} = 0 Vdc) (I_S = 40 Adc, V_{GS} = 0 Vdc) (Note 3) (I_S = 2.3 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	 − −	 0.75 1.2 0.65	 1.0 − −	Vdc
Reverse Recovery Time	(I_S = 2.3 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	−	40	−	ns
		t_a	−	21	−	
		t_b	−	18	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.036	−	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

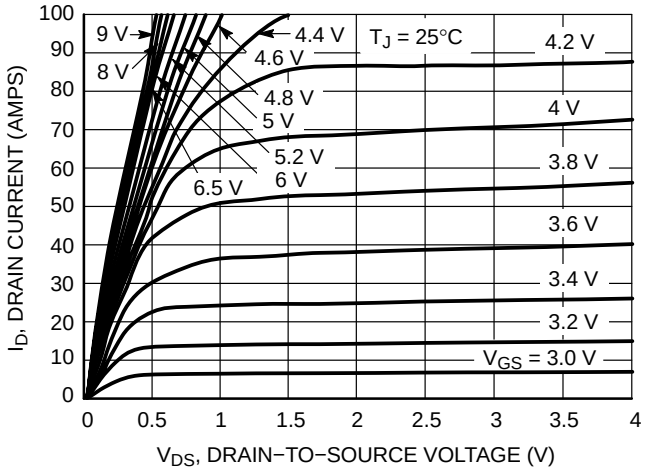


Figure 1. On−Region Characteristics

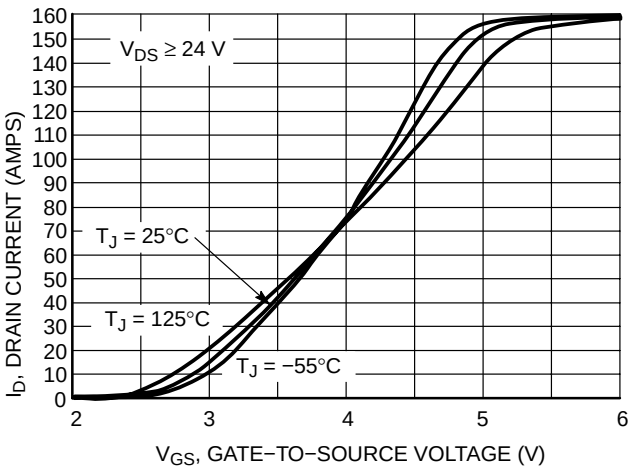


Figure 2. Transfer Characteristics

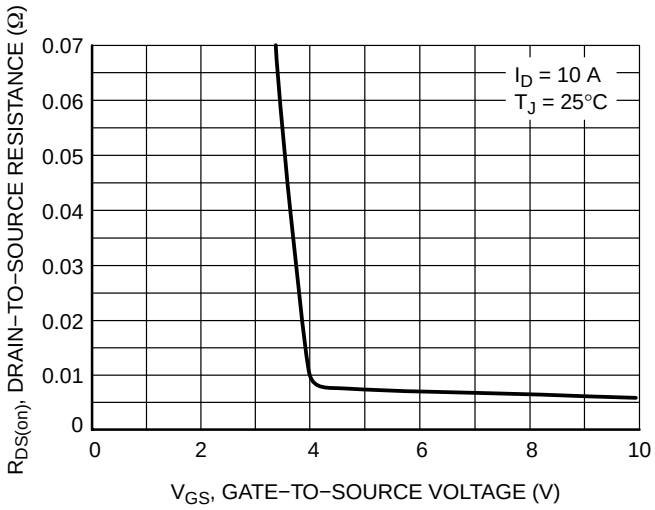


Figure 3. On−Resistance versus Gate−To−Source Voltage

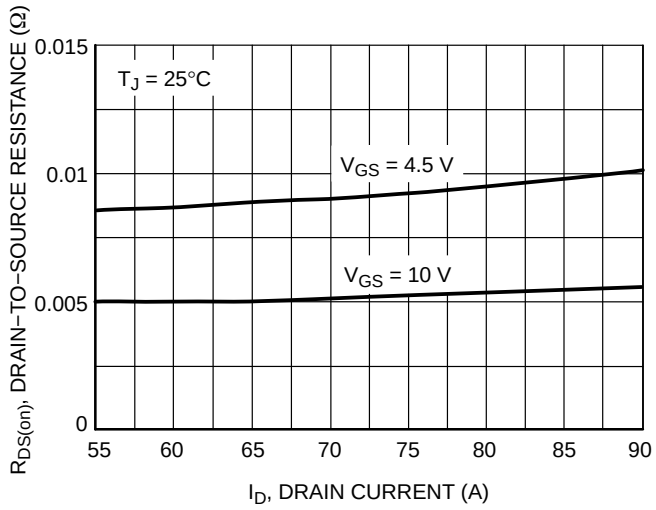


Figure 4. On−Resistance versus Drain Current and Gate Voltage

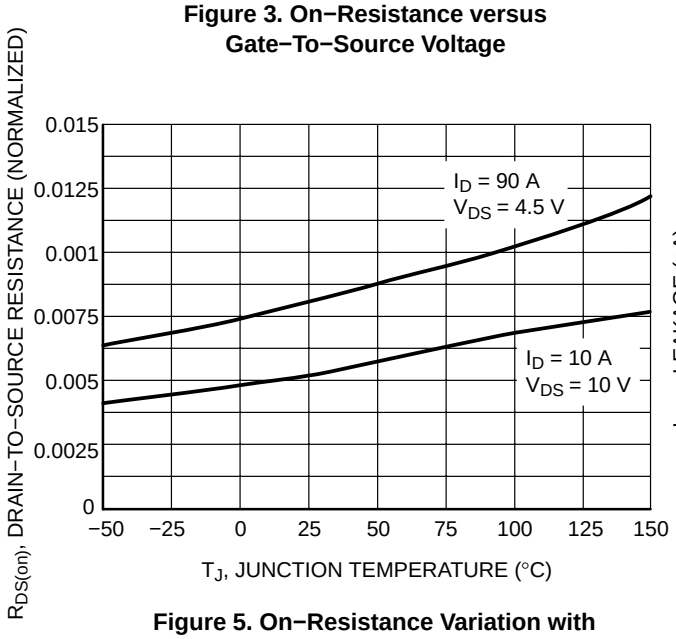


Figure 5. On−Resistance Variation with Temperature

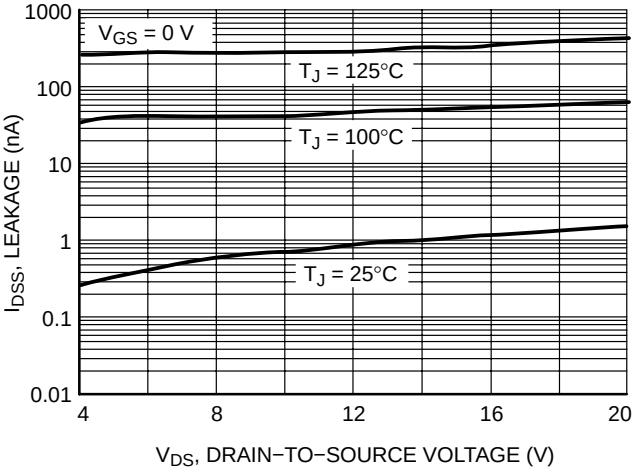


Figure 6. Drain−To−Source Leakage Current versus Voltage

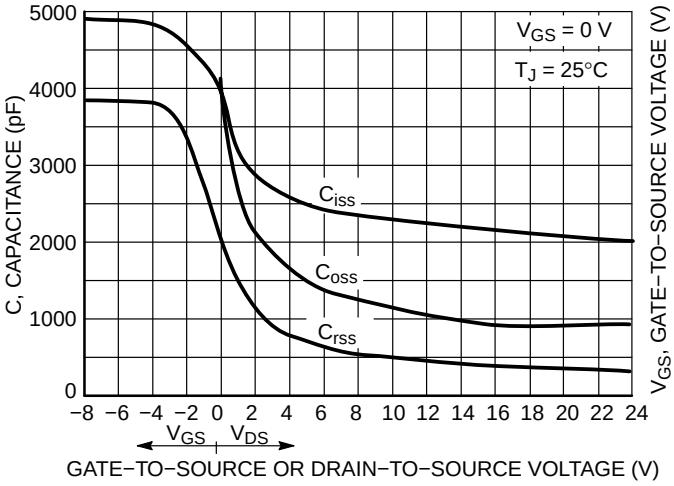


Figure 7. Capacitance Variation

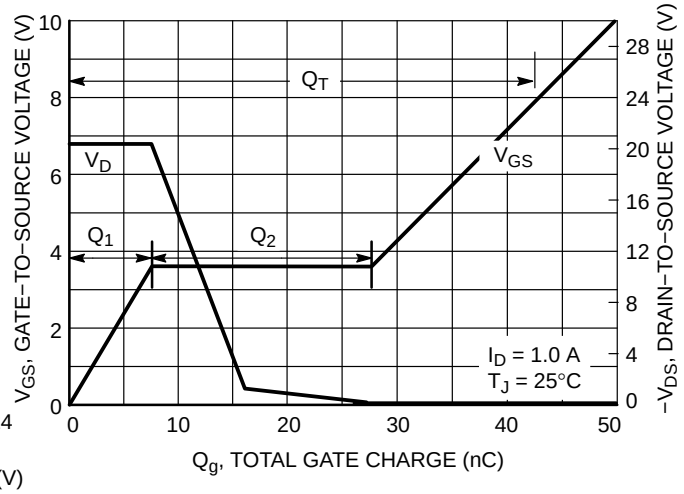


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

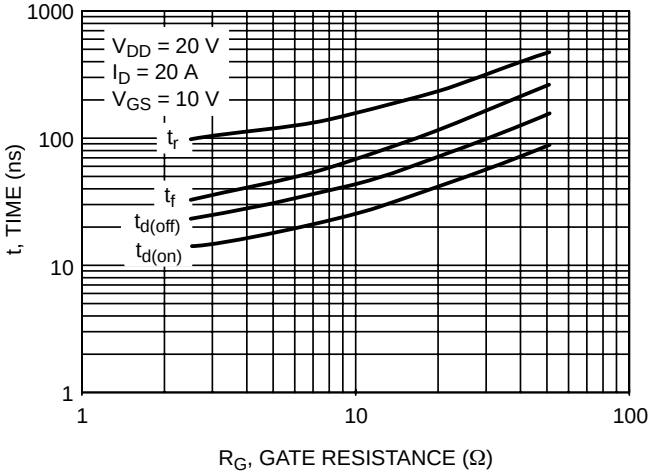


Figure 9. Resistive Switching Time Variation versus Gate Resistance

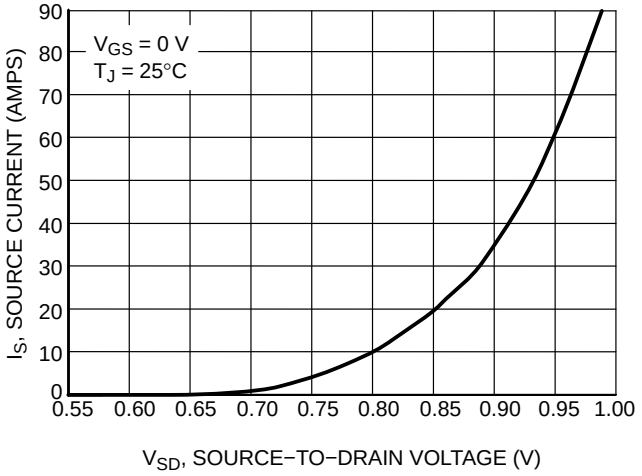


Figure 10. Diode Forward Voltage versus Current

ORDERING INFORMATION

Device	Package	Shipping†
NTP90N02	TO−220AB	50 Units / Rail
NTP90N02G	TO−220AB (Pb−Free)	50 Units / Rail
NTB90N02	D^2PAK	50 Units / Rail
NTB90N02G	D^2PAK (Pb−Free)	50 Units / Rail
NTB90N02T4	D^2PAK	800 Tape & Reel
NTB90N02T4G	D^2PAK (Pb−Free)	800 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_2/10(V_{GG} - V_{GSP})$$

$$t_f = Q_2 \times R_2/V_{GSP}$$

where:

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network.

The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$$

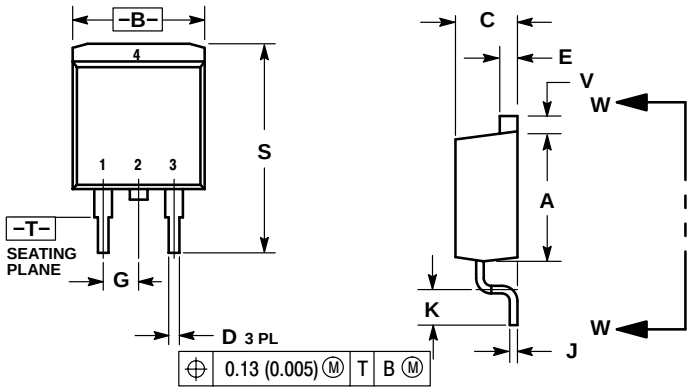
The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

PACKAGE DIMENSIONS

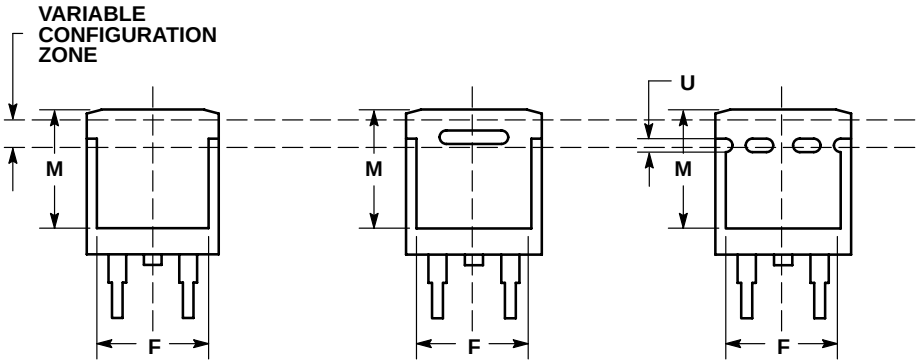
D²PAK
CASE 418AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

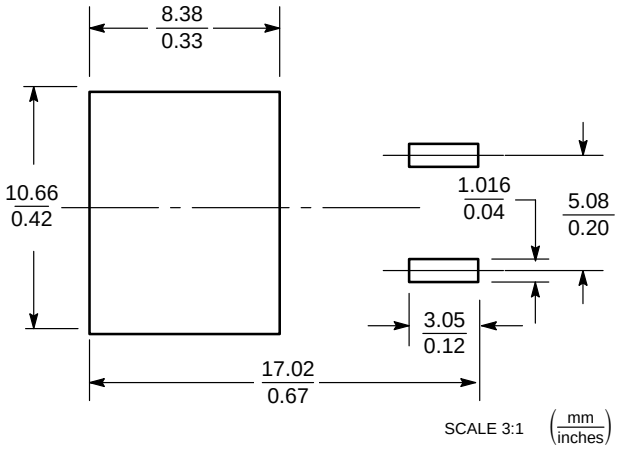
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.036	0.51	0.92
E	0.045	0.055	1.14	1.40
F	0.310	−−−	7.87	−−−
G	0.100 BSC		2.54 BSC	
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
M	0.280	−−−	7.11	−−−
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



VIEW W−W 1 | VIEW W−W 2 | VIEW W−W 3

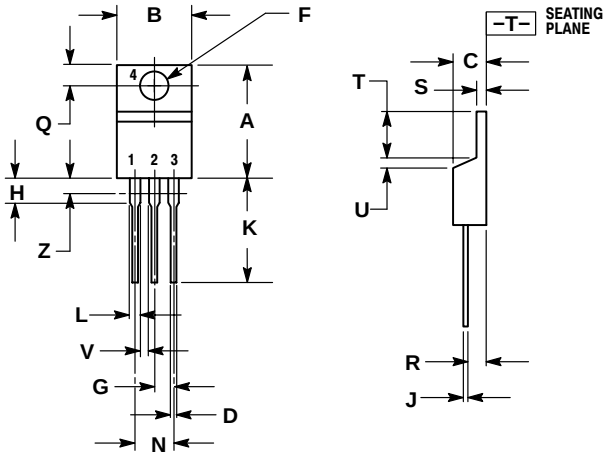
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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Order Literature: http://www.onsemi.com/litorder

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NTB90N02/D