EPSON

SED1220 Series

Dot Matrix LCD Controller Driver

- 12 chara x 3 line (5 x 8 dot)
- Built-in Character Generator ROM and RAM
- Built-in Power Supply Circuit for LCD

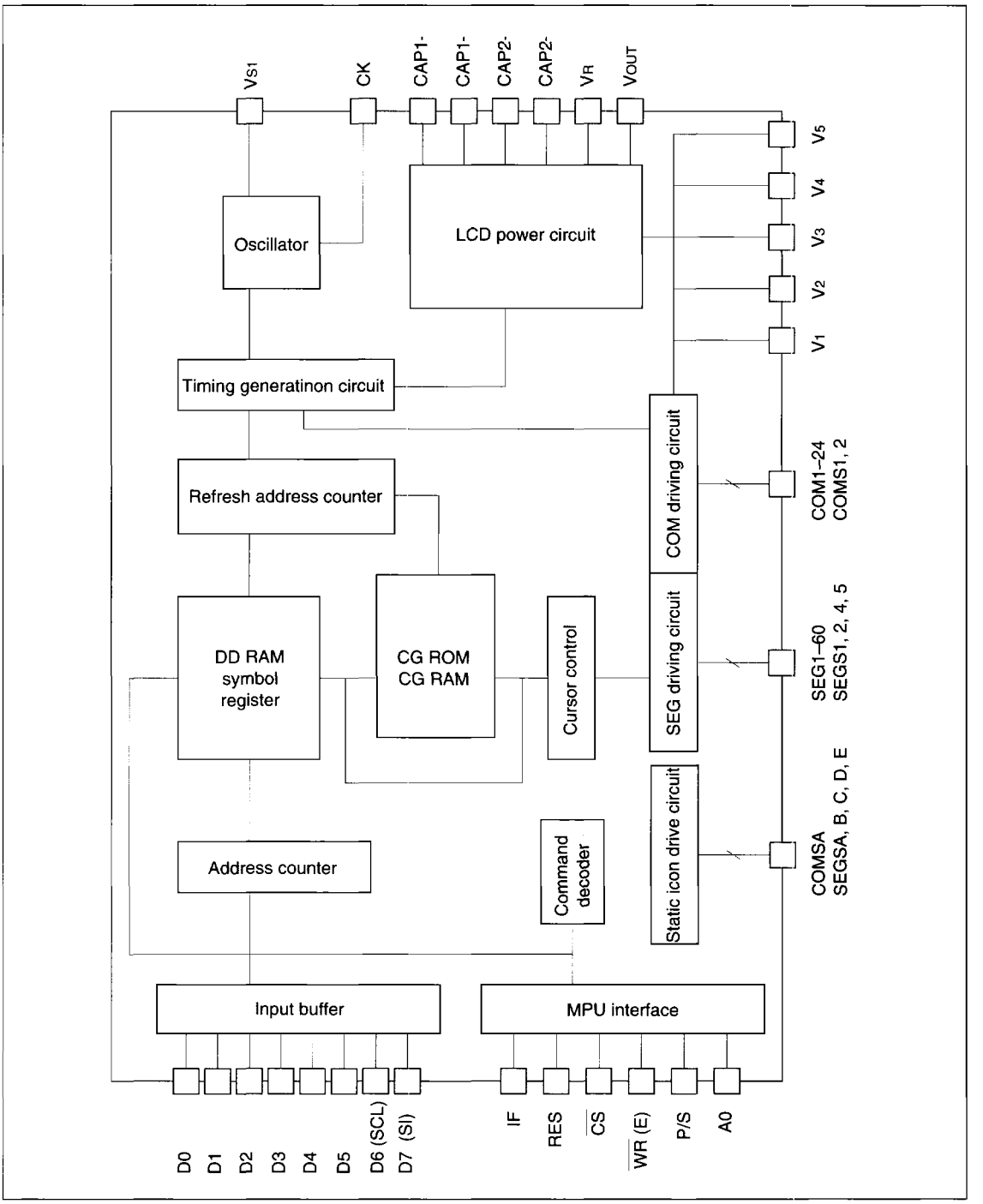
■ OVERVIEW

SED1220 is a dot matrix LCD controller/driver for character display. Using 4bits data, 8bits data or serial data being provided from the micro computer, it displays up to 24 characters, 4 user defined characters and up to 120 symbols. Up to 256 types of built-in character generator ROMs are prepared. Each character font is consisted of 5 × 8 dots. It also contains the RAM for displaying 4 user defined characters each font consisting of 5 × 8 dots. It is symbol register allows character display with high degree of freedom. This handy equipment can be operated with minimum power consumption with its low power consumption design, standby and sleeping mode.

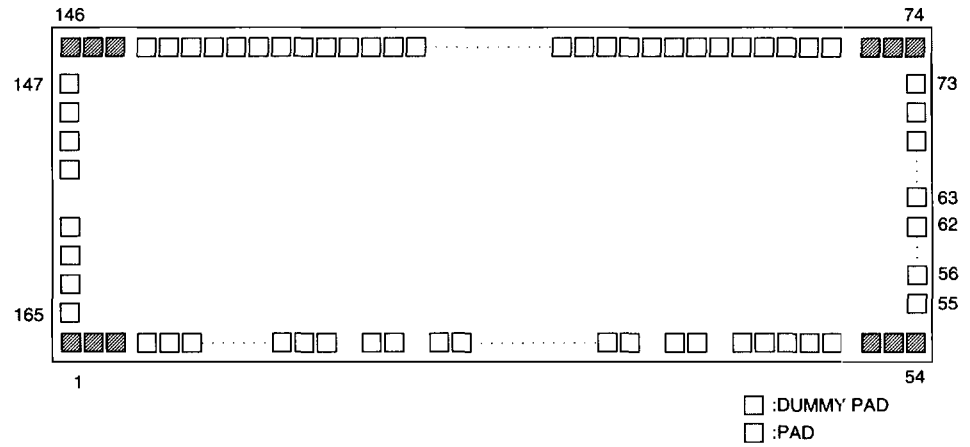
■ FEATURES

- Built-in data display RAM – 36 characters + 4 user defined characters + 120 symbols.
- CG ROM (For up to 256 characters), CG RAM (for 4 characters) and symbol register (for 120 symbols).
- No. of display digit and lines
  < In normal mode >
  (1) (12 digits + 4 segments for signal) × 3 lines + 120 symbols + 5 static symbols (SED1220D**)
  (2) (12 digits + 4 segments for signal) × 2 lines + 120 symbols + 5 static symbols (SED1221D**)
  (3) 12 digits × 2 lines + 120 symbols + 5 static symbols (SED1222D*A)
  (4) 12 digits × 2 lines + 120 symbols + 10 static symbols (SED122AD*B)
  < In standby mode >
  (1) 5 static symbols
  (2) 5 static symbols
- Built-in CR oscillation circuit (C and R contained)
- Accepts external clock input
- High-speed MPU interface
  Affords interface with both 68/80 system MPUs
  Affords interface through 4 bits and 8 bits
- Affords serial interface
- Character font consists of 5 × 8 dots
- Duty ratio (1) 1/26
  (2) 1/18
- Simplified command setting
- Built-in power circuit for driving liquid crystal
  Power amplifier circuit, power regulation circuit and voltage followers × 4
- Built-in electronic volume function
- Low power consumption
  80 µA max. (In normal operation, including operating current of the power supply).
  TBD µA max. (In standby mode for displaying static icon).
  TBD µA max. (In sleeping mode when display is turned off).
- Power supply
  V_{DD} - V_{SS} –2.4 V to –3.6 V
  V_{DD} - V_5 –4.0 V to –6.0 V
- Temperature range for wide range operation
  Ta = –30 to 85°C
- CMOS process
- Shipping style
  Chip (Al pad product) SED1222D*A
  Chip (Au bump product) SED122*D*B
  TCP SED122*T**
- This unit does not employ radiation protection design

■ BLOCK DIAGRAM



■ CHIP SPECIFICATION (SED1220D**, SED1221D**, SED122AD**)



SED122*D**
↑
Digits prepared for CGROM pattern changes

Chip size:	7.70 × 2.77 mm	
Pad pitch:	100 µm (Minimum)	
Chip thickness (for reference):	625 ± 25 µm	(SED122*D*A)
		(SED122*D*B)

1) A1 pad specifications

Pad size on Y side:	75 µm × 135 µm
Pad size on X side:	135 µm × 75 µm

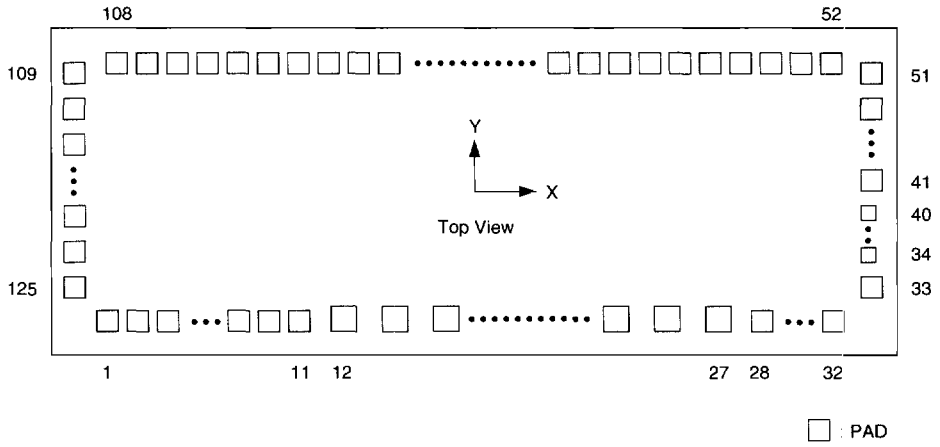
2) Au bump specifications

Bump size on Y side:	69 µm × 129 µm
Bump size on X side:	129 µm × 69 µm
Bump height (for reference)	22.5 µm ± 5.5 µm

<Fuse Pines>

1) Al pad. pad size 86 µm × 75 µm
2) Au bump
   Bump size 80 µm × 69 µm

SED1222D**



SED1222D**
↑
Digits prepared for CGROM pattern changes

Chip size:	7.70 × 2.77 mm
Pad pitch:	124 µm (Min.)
Chip thickness (for reference):	625 ± 50 µm (SED1222D*A)

1) A1 pad specifications

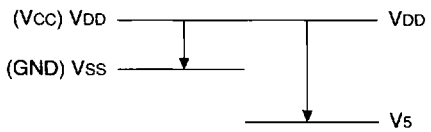
Pad size on Y side:	90 µm × 96 µm
Pad size on X side:	96 µm × 90 µm (PAD. NO 1–11, 28–32, 52–108)
	175 µm × 135 µm (PAD. NO 12–27)

<Fuse Pines>

1) Al pad. pad size 86 µm × 75 µm

■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Power supply voltage (1)		V_{SS}	–6.0 to +0.3	V
Power supply voltage (2)		V_5, V_{out}	–6.0 to +0.3	V
Power supply voltage (3)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Operating temperature		T_{opr}	–30 to +85	°C
Storage temperature	TCP	T_{str}	–55 to +100	°C
	Bare chip		–65 to +125	



Notes: 1. All the voltage values are based on V_{DD} = 0 V.
2. For voltages of V_1, V_2, V_3 and V_4, keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ at all times.
3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction. In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

■ DC CHARACTERISTICS

(V_{DD} = 0 V, V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified.)

Item		Symbol	Condition	min	typ	max	Unit	Applicable pin
Power supply voltage (1)	Recommended operation	V_{SS}		–3.6	–3.0	–2.4	V	V_{SS}
	Operatable			–5.5	–3.0	–2.4		*1
	Data retain voltage			–5.5		–2.0		
Power supply voltage (2)	Recommended operation	V_5		–6.0		–4.0	V	V_5
	Operatable			–6.5		–4.0		*2
	Operatable	V_1, V_2		0.6×V_5		V_{DD}	V	V_1, V_2
	Operatable	V_3, V_4		V_{DD}		0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHC}		0.2×V_{SS}		V_{DD}	V	*3
Low-level input voltage		V_{ILC}		V_{SS}		0.8×V_{SS}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0		1.0	µA	*3
LC driver ON resistance		R_{ON}	Ta=25°C V_5=–7.0V ΔV=0.1V		20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}			0.1	5.0	µA	V_{DD}
Dynamic current consumption	I_{DD}	Display State	V_5 = –6 V without load			80	µA	V_{DD} *5
		Sleep state	Oscillation OFF, Power OFF			5	µA	V_{DD}
		Access state	f_{cyc}=200KHz			500	µA	V_{DD} *6
Input pin capacity		C_{IN}	Ta=25°C f=1MHz		5.0	8.0	pF	*3

Frame frequency	f_{FR}	Ta=25°C V_{SS}=–3.0V	70	100	130	Hz	*10
External clock frequency	f_{ck}	Display of 2 lines		23.4		KHz	*10 *11
	f_{ck}	Display of 3 lines		33.8		KHz	*10 *11

Reset time	t_R		1.0			µs	*7
Reset pulse width	t_{RW}		10			µs	*8
Reset start time	t_{RES}		50			ns	*8

Dynamic system

Built-in power supply	Input voltage	VS1			–2.1		V	*9
	Amplified voltage output voltage	V_{OUT}	When voltage is doubled	–6.0			V	V_{OUT}
	Voltage follower operating voltage	V_5		–6.0		–3.5	V	
	Reference voltage	V_{REG}	Ta = 25°C		–2.0		V	

*1: A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

*2: When the voltage is Tripled, care must be paid to supply the voltage V_{SS} so that operating voltage of V_{OUT} and V_5 may not be exceeded.

*3: D0 to D5, D6 (SCL), D7 (SI), A0, RES, $\overline{CS}$ $\overline{WR}$ (E), P/S, IF

*4: This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V_1, V_2, V_3 or V_4). It is specified in the range of operating voltage (2).

R_{ON} = 0.1 V / ΔI

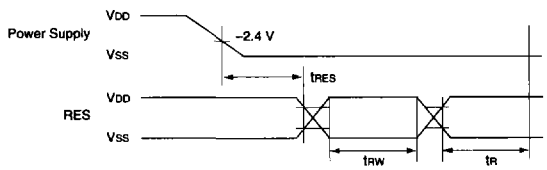
(ΔI: Current flowing when 0.1 V is applied between the power and output)

*5: Character "  " display. This is applicable to the case where no access is made from the MPU and the built-in power circuit and oscillating circuit are in operation.

*6: Current consumption when data is always written by f_{cyc}. The current consumption in the access state is almost proportional to the access frequency (f_{cyc}). When no access is made, only I_{DD} (I) occurs.

*7: t_R (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the SED1220 usually enters the operating state after t_R.

*8: Specifies the minimum pulse width of the RES signal. It is reset when a signal having the pulse width greater than t_{RW} is entered.



All signal timings are based on 20% and 80% of V_{SS} signals.

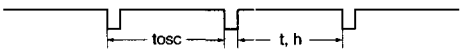
*9: When operating the boosting circuit, the power supply V_{SS} must be used within the input voltage range.

*10: The f_{OSC} frequency of the oscillator circuit for internal circuit drive may differ from the f_{BST} boosting clock on some models. The following provides the relationship between the f_{OSC} frequency, f_{BST} boosting clock, and f_{FR} frame frequency.

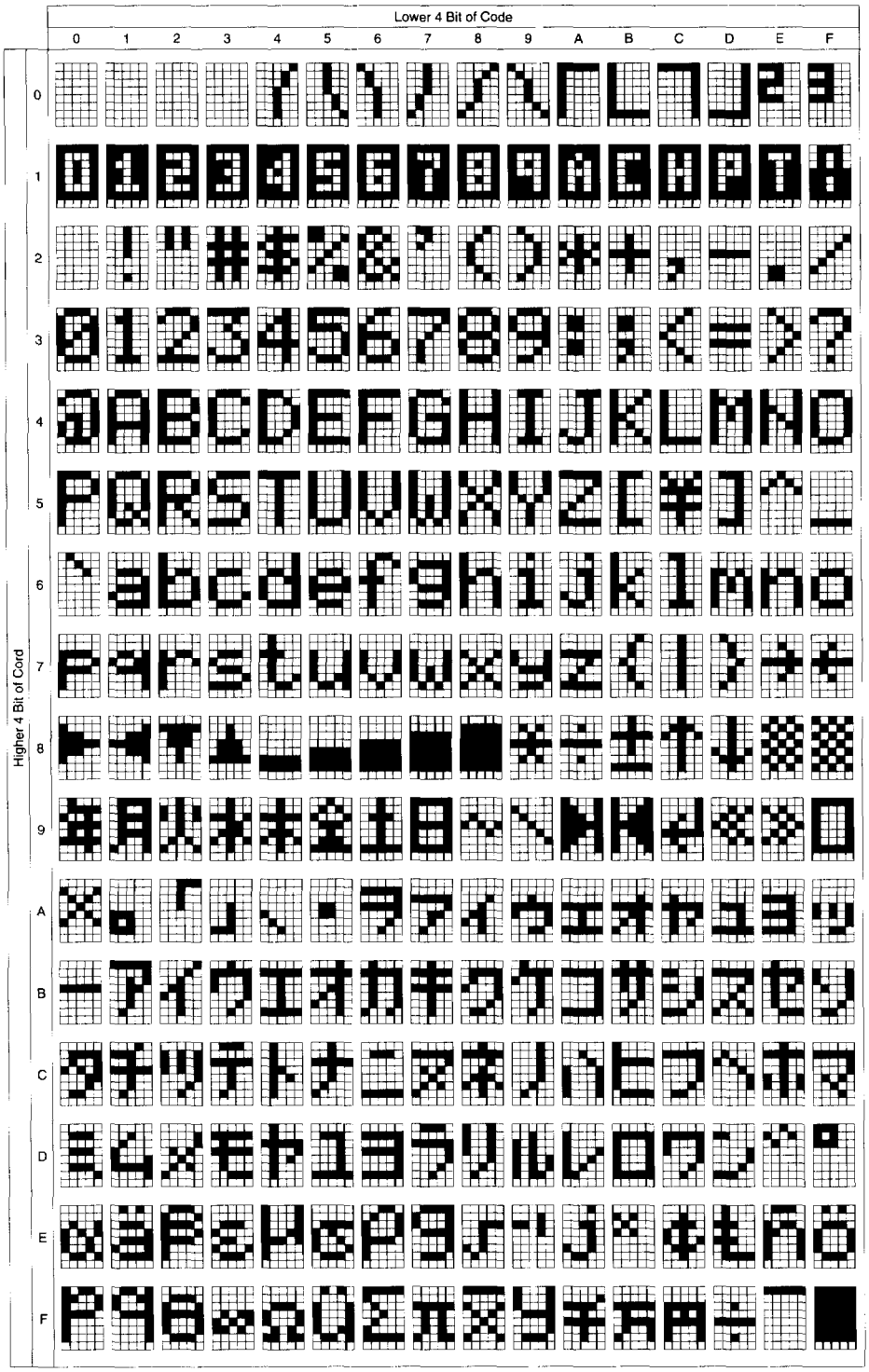
f_{OSC} = (No. of digits) × (1/Duty) × f_{FR}
f_{BST} = (1/2) × (1/No. of digits) × f_{OSC}

*11: When operations are performed using the external clock instead of the buit-in oscillation circuit, following waveforms must be entered.

- Duty = (th/t_{OSC}) × 100 = 70-80%
- f_{OSC} = 1/t_{OSC}



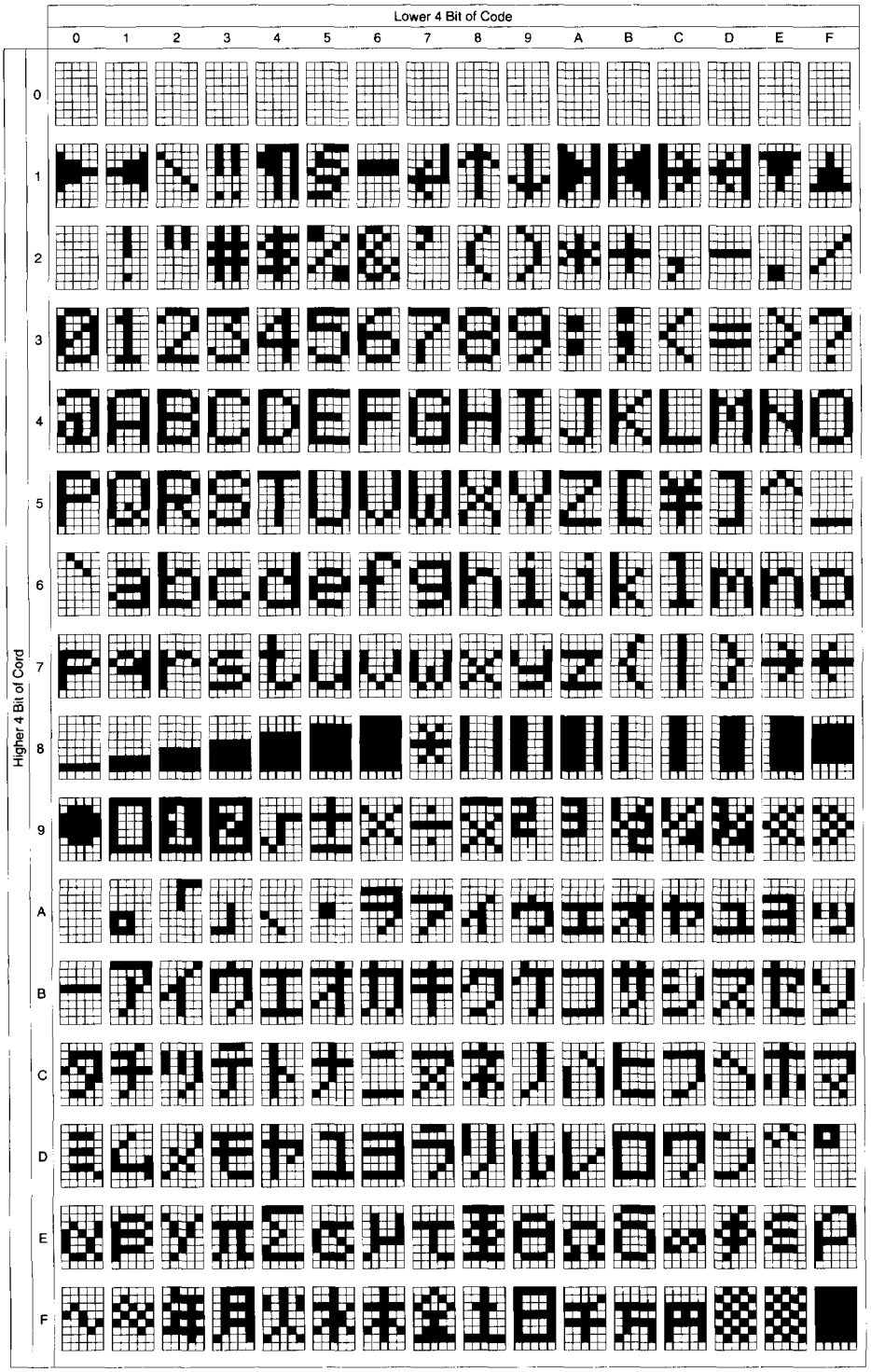
SED122*DA*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

SED122*DB*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

SED122*DG*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F