INTEGRATED CIRCUITS

DATA SHEET

TDA8577

Dual common-mode rejection differential line receiver

Preliminary specification
File under Integrated Circuits, IC01

September 1995

Philips Semiconductors

PHILIPS

FEATURES

- Excellent common-mode rejection, up to high frequencies
- Elimination of source resistance dependency in the common-mode rejection
- Few external components
- High supply voltage ripple rejection
- Low noise
- Low distortion
- All pins protected against electrostatic discharge
- AC and DC short-circuit safe to ground and V_{CC}
- Fast DC settling.

GENERAL DESCRIPTION

The TDA8577 is a two channel differential amplifier with 0 dB gain and low distortion. The device has been primarily developed for car radio applications where long connections between signal sources and amplifiers (or boosters) are necessary and where ground noise has to be eliminated. The device is intended to be used to receive line inputs in audio applications that require a high level of common-mode rejection. The device is contained in a 9-pin single in-line package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current	V_{CC} = 8.5	–	11	14	mA
G_v	voltage gain		–0.5	0	+0.5	dB
SVRR	supply voltage ripple rejection		55	60	–	dB
V_{no}	noise output voltage		–	3.7	5.0	μV
$\|Z_i\|$	input impedance		100	240	–	kΩ
CMRR	common-mode rejection ratio	R_s = 0 Ω	–	80	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8577	9	SIL9	plastic	SOT142

BLOCK DIAGRAM

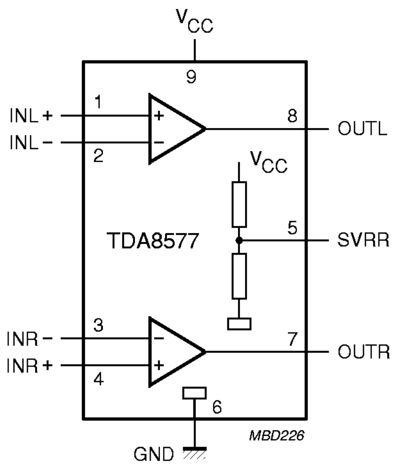


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA8577 contains two identical differential amplifiers with a voltage gain of 0 dB. The device is intended to receive line input signals for audio applications. The TDA8577 has a very high level of common-mode rejection and thus eliminates ground noise. The common-mode rejection remains constant up to high frequencies (the amplifier gain is fixed at 0 dB). The inputs have a high input impedance. The output stage is a class AB stage with a low output impedance. For a large common-mode rejection, also at low frequencies, an electrolytic capacitor connected to the negative input is advised. Because the input impedance is relatively high, this results in a large settling time of the DC input voltage. Therefore a quick-charge circuit is included to charge the input capacitor within 0.2 seconds.

All input and output pins are protected against high electrostatic discharge conditions (4000 V, 150 pF, 150 Ω).

PINNING

SYMBOL	PIN	DESCRIPTION
INL+	1	positive input left
INL−	2	negative input left
INR−	3	negative input right
INR+	4	positive input right
SVRR	5	half supply voltage
GND	6	ground
OUTR	7	output right
OUTL	8	output left
V_{CC}	9	supply voltage

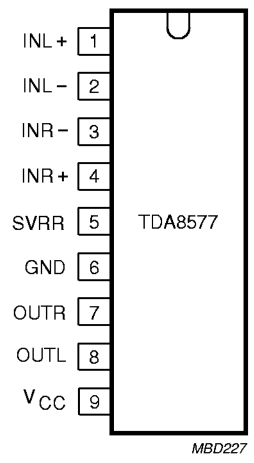


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	–	18	V
I_{ORM}	repetitive peak output current		–	40	mA
V_{sc}	AC and DC short-circuit safe voltage		–	18	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_j	maximum junction temperature		–	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	80 K/W

CHARACTERISTICS

V_{CC} = 8.5 V; T_{amb} = 25 °C; f = 1 kHz; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current		–	11	14	mA
V_O	DC output voltage	note 1	–	4.3	–	V
t_{set}	DC input voltage settling time		–	0.2	–	s
G_v	voltage gain		–0.5	0	+0.5	dB
α_{cs}	channel separation	R_s = 5 kΩ	70	80	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	0.5	dB
f_L	low frequency roll-off	–1 dB; note 2	20	–	–	Hz
f_H	high frequency roll-off	–1 dB	20	–	–	kHz
$\|Z_i\|$	input impedance		100	240	–	kΩ
$\|Z_o\|$	output impedance		–	–	10	Ω
$V_{i(max)}$	maximum input voltage	THD = 1%	–	2	–	V
V_{no}	noise output voltage	R_s = 0 Ω; note 3	–	3.7	5.0	µV
$V_{CM(rms)}$	common-mode input voltage (RMS value)		–	–	1	V
CMRR	common-mode rejection ratio	R_s = 5 kΩ	66	70	–	dB
		R_s = 0 Ω; note 4	–	80	–	dB
SVRR	supply voltage ripple rejection	note 5	55	65	–	dB
		note 6	–	60	–	dB
THD	total harmonic distortion	V_i = 1 V;	–	0.02	–	%
		V_i = 1 V; f = 20 Hz to 20 kHz	–	–	0.1	%
THD_{max}	total harmonic distortion at maximum output current	V_i = 1 V; R_L = 150 Ω	–	–	1	%

Notes

1. The DC output voltage with respect to ground is approximately $0.5V_{CC}$.
2. The frequency response is externally fixed by the input coupling capacitors.
3. The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz (unweighted).
4. The common-mode rejection ratio is measured at the output with a voltage source of 1 V (RMS) in accordance with the test circuit (see Fig.3) while V_{INL} and V_{INR} are shorted-circuited. Frequencies between 100 Hz and 100 kHz.
5. The ripple rejection is measured at the output, with R_s = 2 kΩ, f = 1 kHz and a ripple amplitude of 2 V (p-p).
6. The ripple rejection is measured at the output, with R_s = 0 to 2 kΩ, f = 100 Hz to 20 kHz and a maximum ripple amplitude of 2 V (p-p).

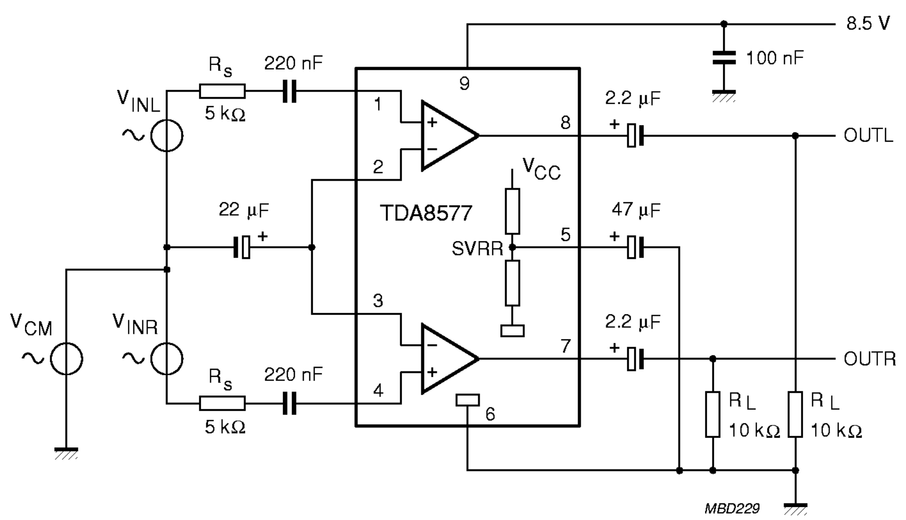


Fig.3 Test circuit.

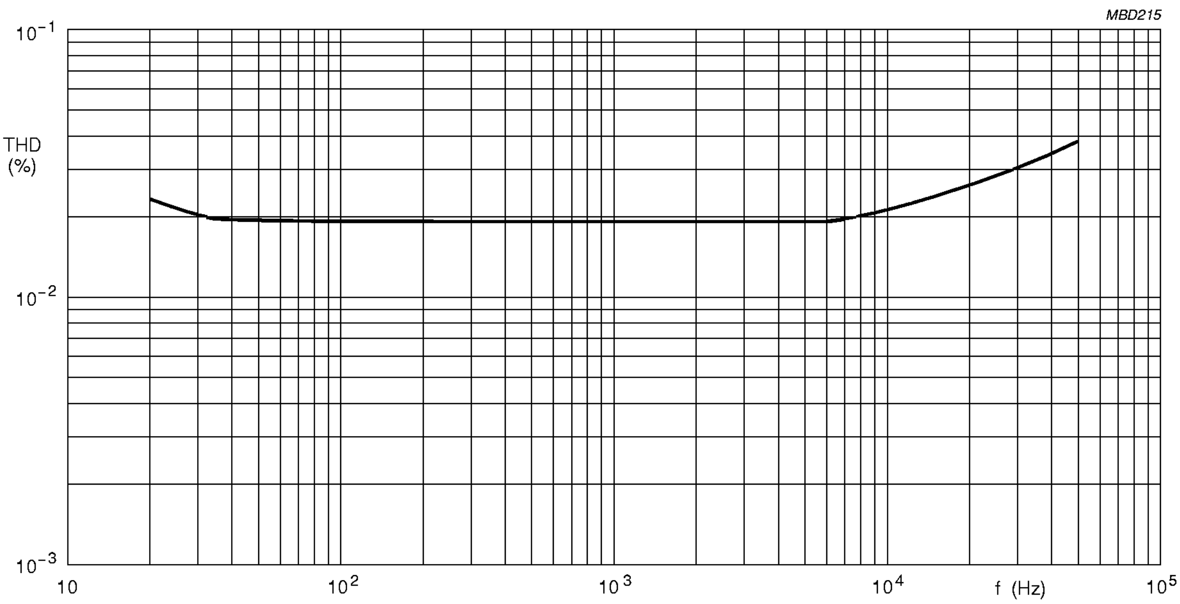
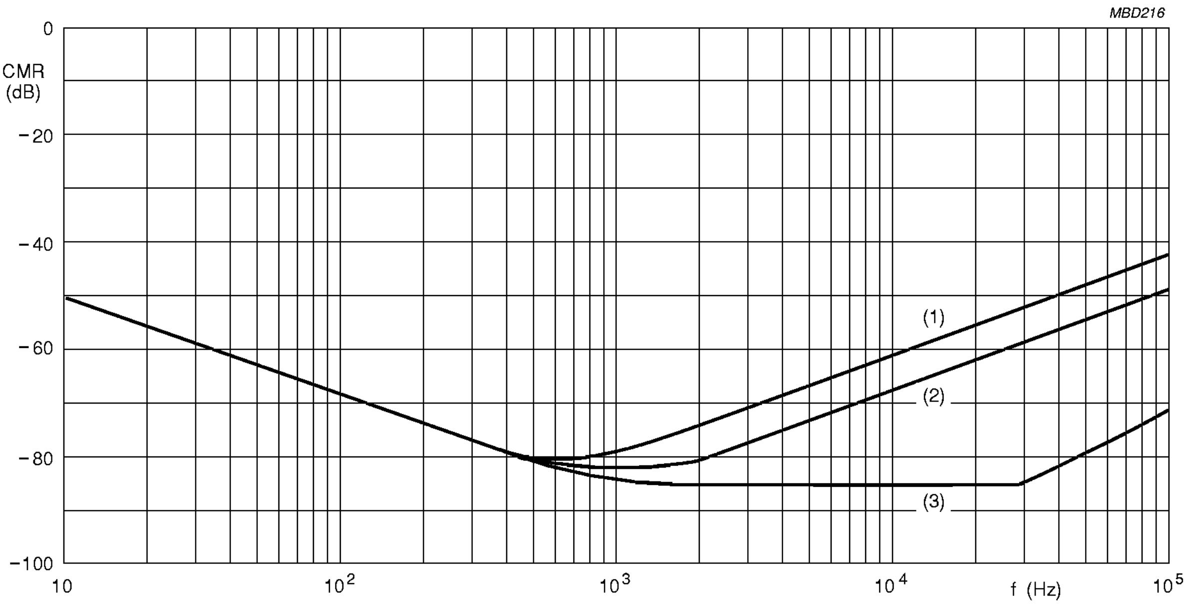


Fig.4 Total harmonic distortion as a function of frequency; V_i = 1V (RMS).



(1) R_s = 5 kΩ
(2) R_s = 2 kΩ
(3) R_s = 0 kΩ

Fig.5 Common-mode rejection ratio as a function of frequency; V_{CM} = 1 V (RMS).

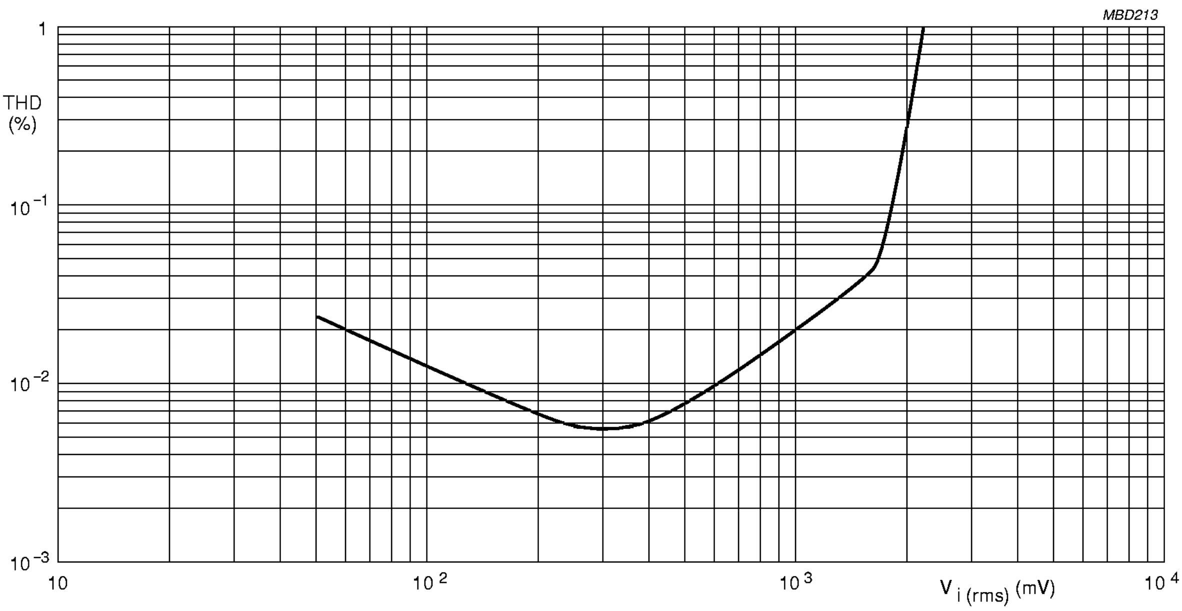


Fig.6 Total harmonic distortion as a function of input voltage; f = 1 kHz.

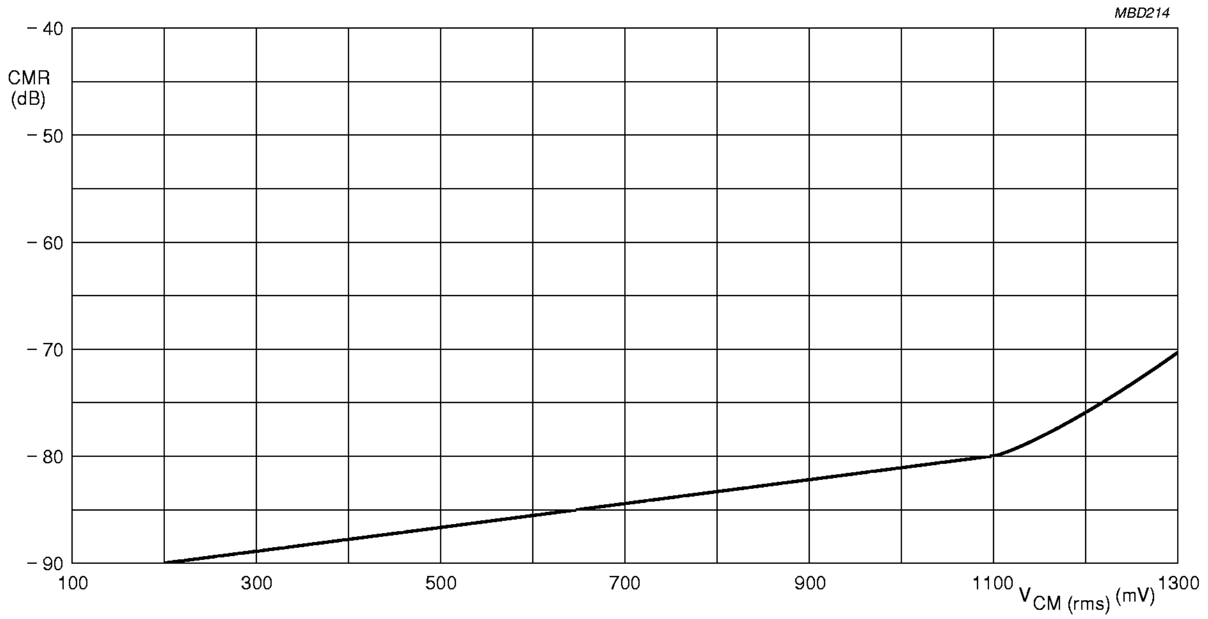
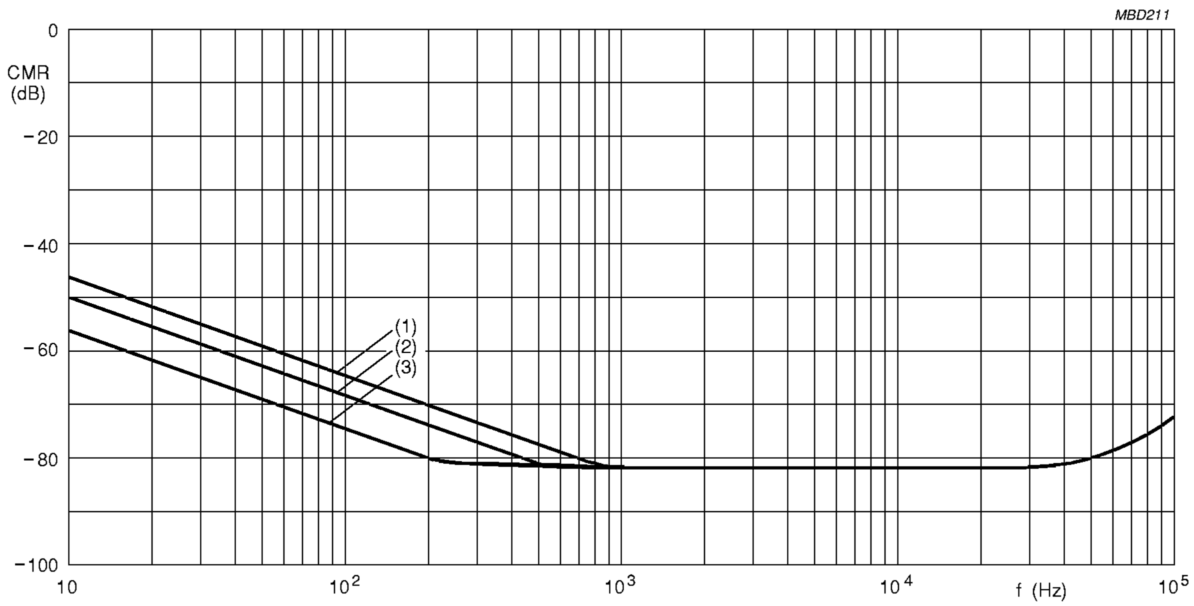


Fig.7 Common-mode rejection ratio as a function of input voltage; f = 1 kHz.



(1) C2 = 22 μF
(2) C2 = 47 μF
(3) C2 = 100 μF

Fig.8 Common-mode rejection ratio as a function of frequency; V_{CM} = 1 V (RMS).

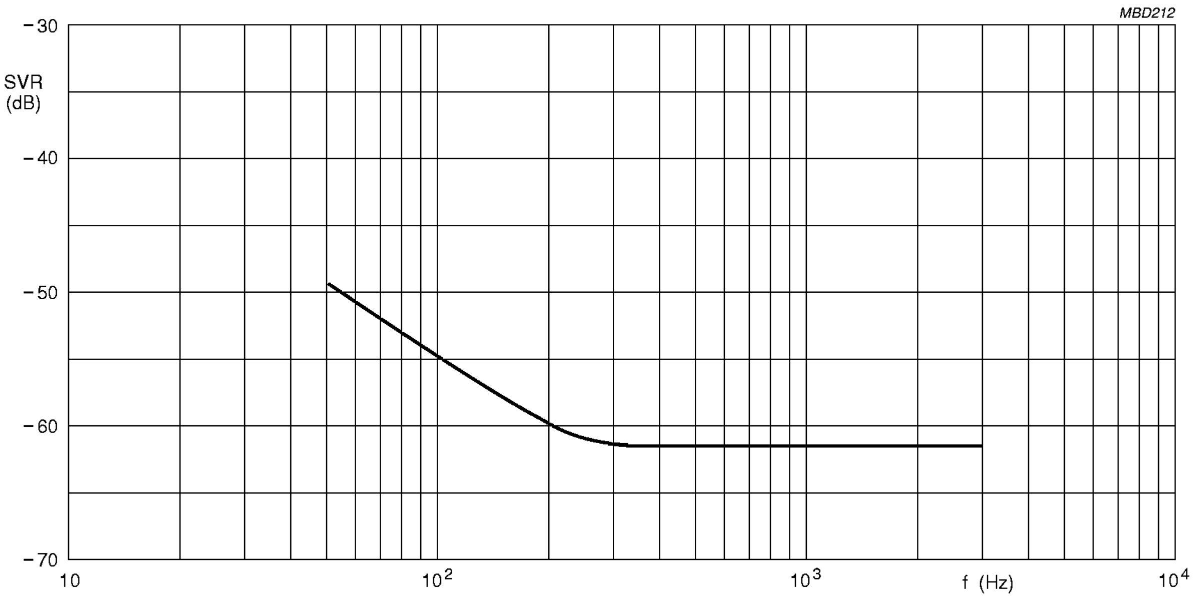


Fig.9 Supply voltage ripple rejection as a function of frequency; V_{ripple} = 2 V (p-p), R_s = 2 kΩ.

APPLICATION INFORMATION

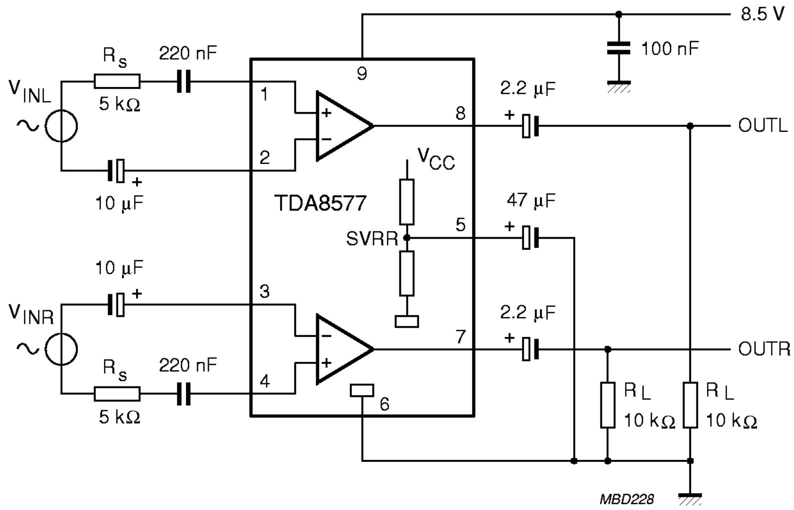
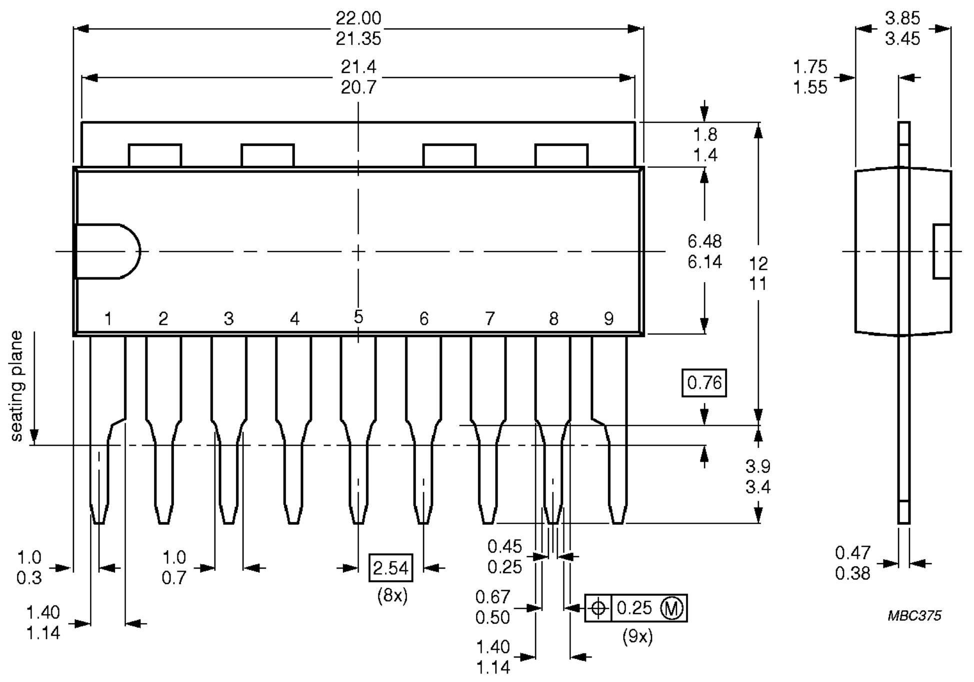


Fig.10 Application circuit with balanced signal source

PACKAGE OUTLINE



Dimensions in mm.

Fig.11 9-lead single in-line; plastic (SOT142).

SOLDERING

Plastic single in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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