DRAM MODULE

512K x 32, 1 MEG x 16

FAST-PAGE-MODE (MT16D(T)51232)
LOW POWER,
EXTENDED REFRESH (MT16D(T)51232 L)

FEATURES

- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 48mW (4.8mW L-version) standby; 1,424mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Multiple RAS lines offer x16 or x32 widths
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- FAST-PAGE-MODE access cycle
- Low CMOS standby current, 3.2µA maximum (L-version)
- Thin outline using TSOP version

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Components
  - SOJ — D
  - TSOP — DT
- Packages
  - Leadless 72-pin SIMM — M
  - Leadless 72-pin SIMM (gold) — G
- Power/Refresh
  - Normal Power/8ms — Blank
  - Low Power/64ms — L
- Part Number Example: MT16DT51232GL-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-10) SOJ Version
(DE-25) TSOP Version

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	RAS3	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

GENERAL DESCRIPTION

The MT16D(T)51232 is a randomly accessed solid-state memory containing 524,288 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

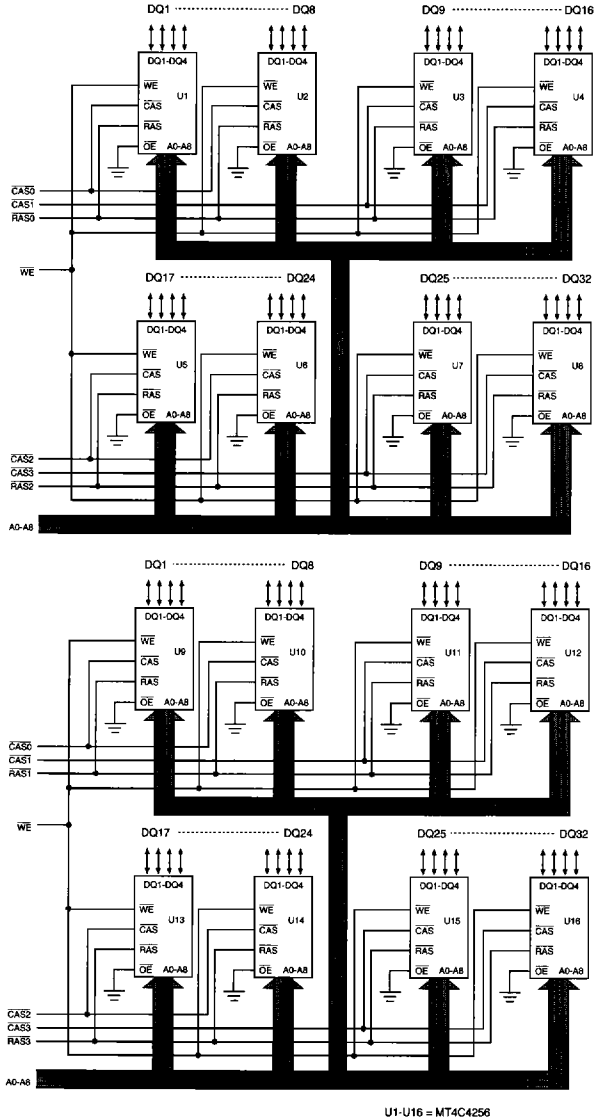
FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A8) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST-PAGE-MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its

correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

For x16 applications, the corresponding DQ and $\overline{CAS}$ pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the x16 memory organization.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4256
U1-U16 = MT4C4256 L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA-IN/OUT
					^tR	^tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY-WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data-Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data-In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	X	X	X	High-Z
BATTERY BACKUP (BBU) REFRESH (L-version)		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-8	8	µA	
Any input 0V ≤ V_{IN} ≤ 6.5V	A0-A8, $\overline{WE}$	I_{I2}	-32	32	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$-$\overline{RAS3}$	I_{I3}	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ1-DQ32	I_{OZ}	-20	20	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	32	32	32	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	16	16	16	mA	
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		3.2	3.2	3.2	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	736	656	576	mA	2, 22
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		684	604	524	mA	2,22,24
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current	I_{CC4}	576	496	416	mA	2, 22
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])		524	444	364	mA	2,22,24
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	736	656	576	mA	2
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		684	604	524	mA	2, 24
REFRESH CURRENT: CBR Average power supply current	I_{CC6}	736	656	576	mA	2, 19
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		684	604	524	mA	2,19,24
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A8 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	3.2	3.2	3.2	mA	24

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		95	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		127	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$, $\overline{RAS0}$-$\overline{RAS3}$	C_{I4}		32	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		18	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST-PAGE-MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	15		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

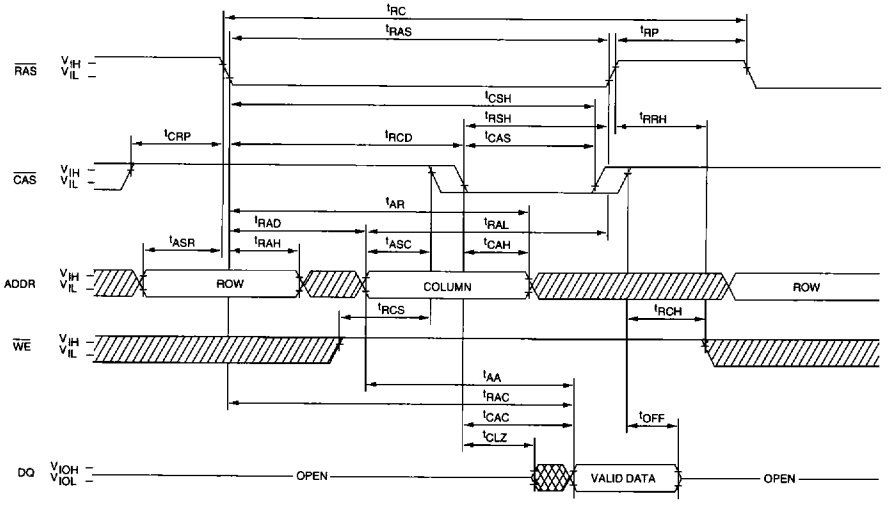
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	3	20	3	20	3	20	ns	12, 25
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8/64		8/64		8/64	ms	3/24
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		15		15		ns	19

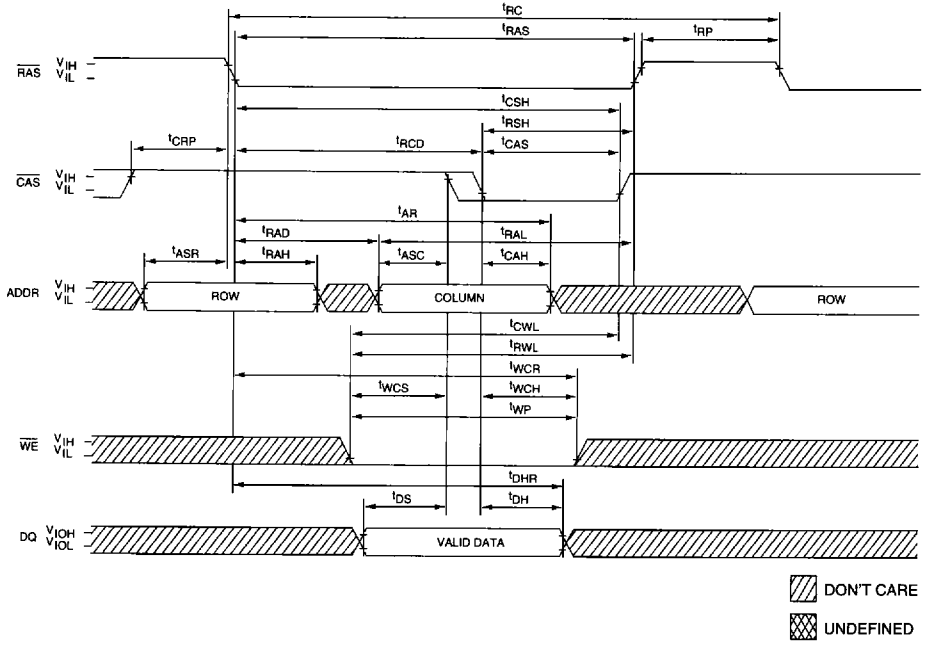
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U16.
22. Icc is dependent on cycle rates.
23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
24. Applies to L-version only.
25. The 3ns minimum is a parameter guaranteed by design.

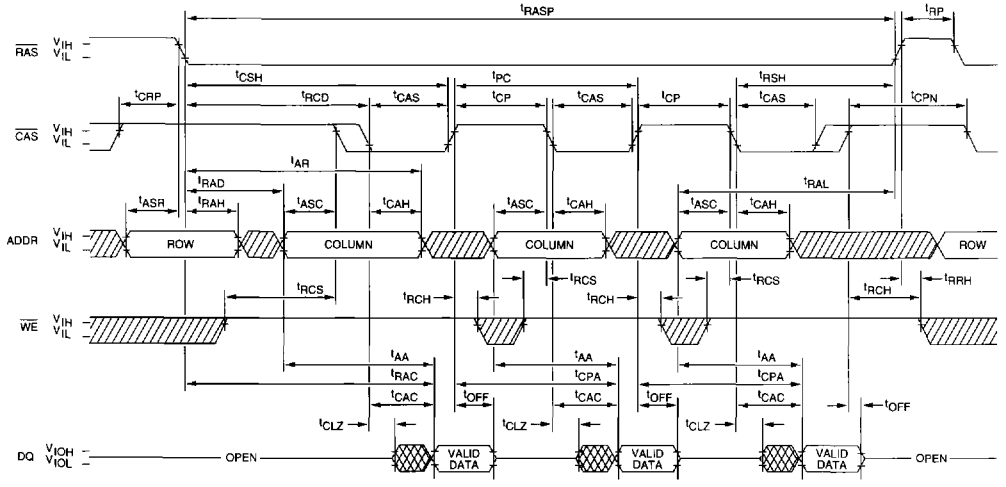
READ CYCLE



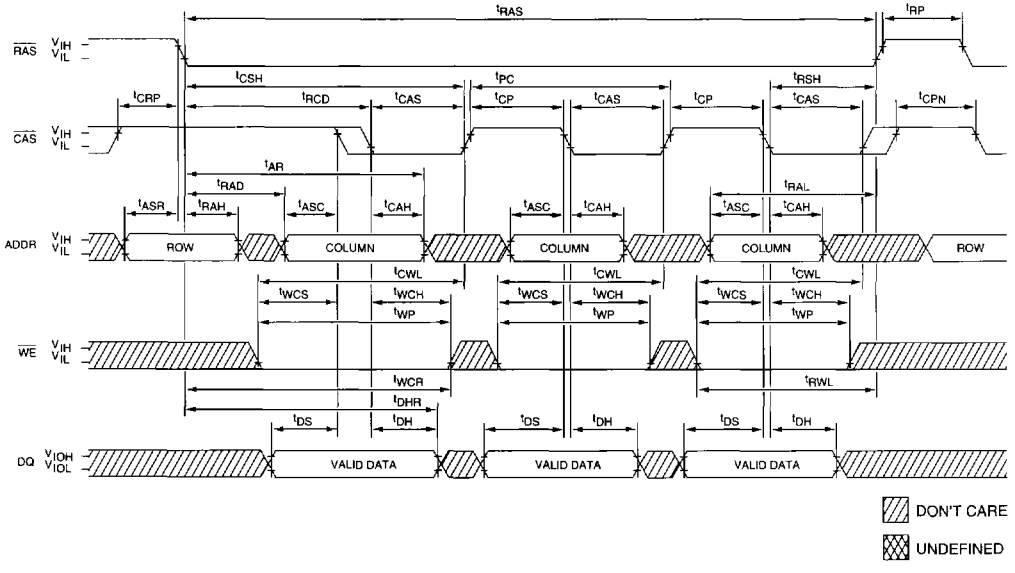
EARLY-WRITE CYCLE



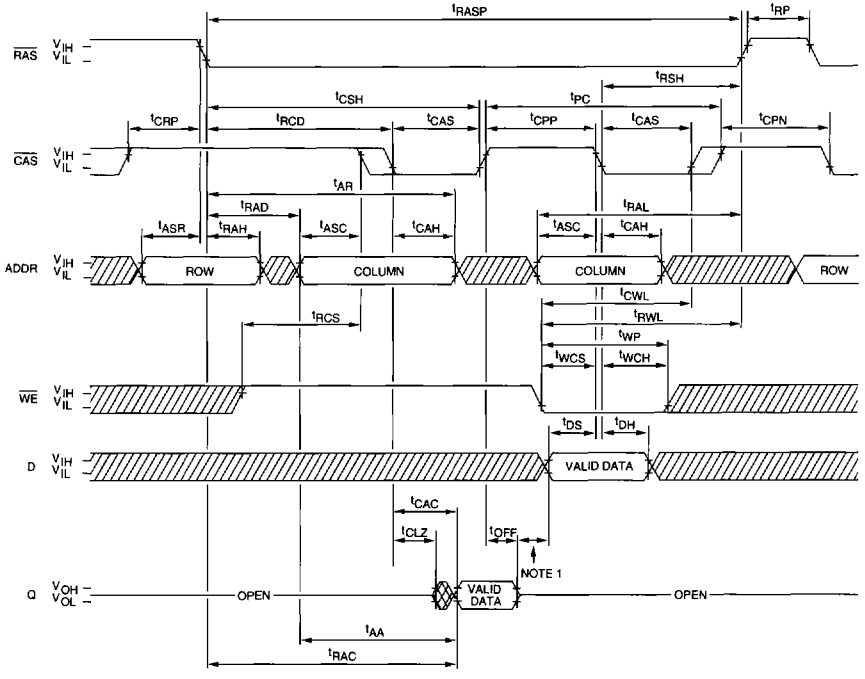
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

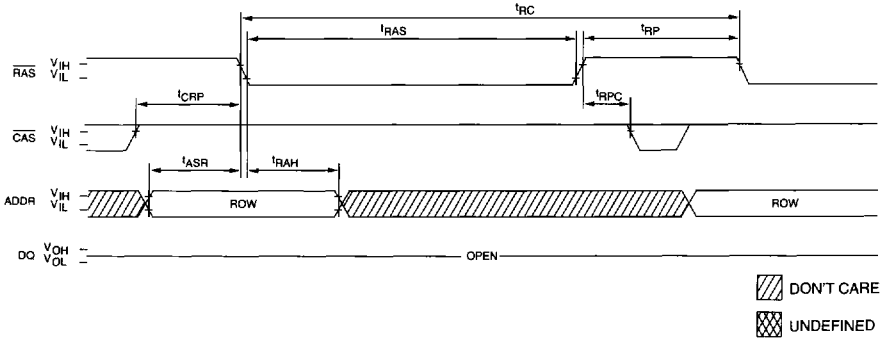


FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

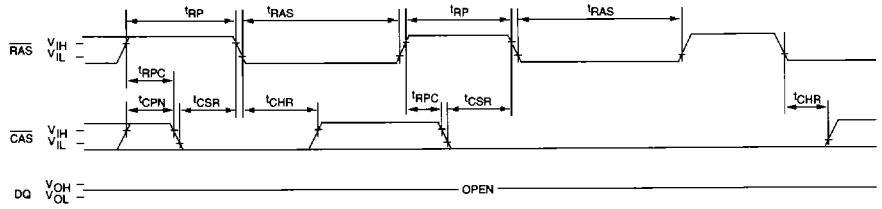


NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

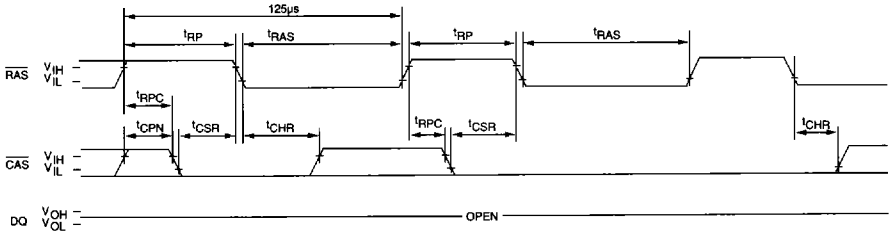
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A7; A8 and WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A8, $\overline{WE}$ = DON'T CARE)



BBU REFRESH CYCLE [24]
(A0-A8, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)