MAX5316

16-Bit, ±1 LSB Accuracy Voltage Output DAC with SPI Interface

General Description

The MAX5316 is a high-accuracy, 16-bit, serial SPI input, buffered voltage output digital-to-analog converter (DAC) in a 4mm x 5mm, 24-lead TQFN package. The device features ±1 LSB INL (max) accuracy and a ±0.25 LSB DNL (typ) accuracy over the temperature range of -40°C to +105°C.

The DAC voltage output is buffered with a fast settling time of 3µs and a low offset and gain drift of ±0.6ppm/°C of FSR (typ). The force-sense output (OUT) maintains accuracy while driving loads with long lead lengths. A separate AVSS supply pin is provided to permit the output amplifier to go to 0V (GND) to maintain full linearity performance near ground.

At power-up, the device resets its outputs to zero or midscale.

The wide 2.7V to 5.5V supply voltage range and integrated low-drift, low-noise reference buffer make for ease of use. The MAX5316 features a 50MHz 3-wire SPI interface. For an I²C interface, use the MAX5317.

The MAX5316 is available in a 24-lead TQFN-EP package and operates over the -40°C to +105°C temperature range.

Applications

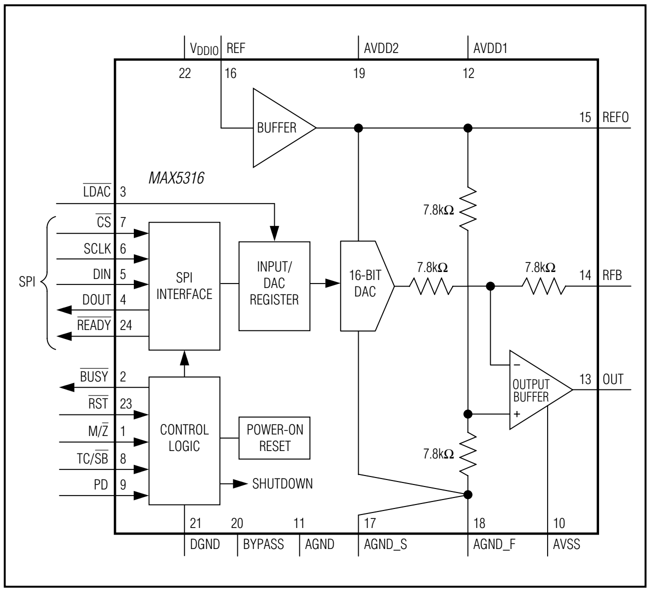
- Test and Measurement
- Automatic Test Equipment
- Gain and Offset Adjustment
- Data-Acquisition Systems
- Process Control and Servo Loops
- Programmable Voltage and Current Sources
- Automatic Calibration
- Communication Systems
- Medical Equipment

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- **Ideal for ATE and High-Precision Instruments**
  - **INL Accuracy Guaranteed with ±1 LSB (Max) Over Temperature**
- **Fast Settling Time (3µs) with 10kΩ || 100pF Load**
- **Safe Power-Up-Reset to Zero or Midscale DAC Output (Pin-Selectable)**
  - **Predetermined Output Device State in Power-Up and Reset in System Design**
- **Negative Supply (AVSS) Option Allows Full INL and DNL Performance to 0V**
- **SPI Interface Compatible with 1.7V to 5.5V Logic**
- **High Integration Reduces Development Time and PCB Area**
  - **Buffered Voltage Output Directly Drives 2kΩ Load Rail-to-Rail**
  - **Integrated Reference Buffer**
  - **No External Amplifiers Required**
- **Small 4mm x 5mm, 24-Pin TQFN Package**

Functional Diagram



For related parts and recommended products to use with this part, refer to www.maxim-ic.com/MAX5316.related.

ABSOLUTE MAXIMUM RATINGS

AGND to DGND ....-0.3V to +0.3V
AGND_F, AGND_S to AGND ....-0.3V to +0.3V
AGND_F, AGND_S to DGND ....-0.3V to +0.3V
AVDD_ to AGND ....-0.3V to +6V
AVDD_ to REF ....-0.3V to +6V
AVSS to AGND ....-2V to +0.3V
V_{DDIO} to DGND...-0.3V to +6V
BYPASS to DGND ....-0.3V to the lower of ($V_{AVDD\_}$ or V_{DDIO} + 0.3V) and +6V
OUT, REFO, RFB to AGND ....-0.3V to the lower of ($V_{AVDD\_}$ + 0.3V) and +6V
REF to AGND ....-0.3V to the lower of V_{AVDD} and +6V
SCLK, DIN, $\overline{CS}$, $\overline{BUSY}$, $\overline{LDAC}$, $\overline{READY}$, M/$\overline{Z}$, TC/$\overline{SB}$, $\overline{RST}$, PD, DOUT to DGND.......-0.3V to the lower of (V_{DDIO} + 0.3V) and +6V
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 28.6mW/°C above +70°C)...............2285.7mW
Operating Temperature Range........................ -40°C to +105°C
Maximum Junction Temperature....................................+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Case Thermal Resistance (θ_{JA}) ....1.8°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....35°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

($V_{AVDD\_}$ = V_{DDIO} = **4.5V to 5.5V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		16			Bits
Integral Nonlinearity (Note 3)	INL	DIN = 0x0000 to 0xFFFF (binary mode), DIN = 0x8000 to 0x7FFF (two's complement mode)	-1	±0.25	+1	LSB
		DIN = 0x0640 to 0xFFFF (binary mode), DIN = 0x8280 to 0x7FFF (two's complement mode), V_{AVSS} = 0V				
Differential Nonlinearity (Note 3)	DNL		-1	±0.25	+1	LSB
Zero Code Error	OE	DIN = 0, T_A = +25°C	-19	±1	+19	LSB
		DIN = 0, T_A = -40°C to +105°C		±6		
Zero Code Error Drift		DIN = 0	-2.5	±0.4	+2.5	ppm/°C
Gain Error	GE	T_A = +25°C	-4	±0.25	+4	LSB
		T_A = -40°C to +105°C		±3		
Gain Error Temperature Coefficient	TCGE		-2.75	±0.6	+2.75	ppm/°C of FSR

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD\_}$ = V_{DDIO} = **4.5V to 5.5V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Range				0		V_{AVDD} - 0.1	V
Reset Voltage Output	$V_{OUT-RESET}$	$\overline{RST}$ = pulse low	M/$\overline{Z}$ = DGND		75		µV
			M/$\overline{Z}$ = V_{DDIO}		2.048		V
		$\overline{RST}$ = pulse low, V_{AVSS} = 0V	M/$\overline{Z}$ = DGND		10		mV
			M/$\overline{Z}$ = V_{DDIO}		2.048		V
		$\overline{RST}$ = DGND	M/$\overline{Z}$ = DGND		-40		mV
			M/$\overline{Z}$ = V_{DDIO}		2.037		V
		$\overline{RST}$ = DGND, V_{AVSS} = 0V	M/$\overline{Z}$ = DGND		10		mV
			M/$\overline{Z}$ = V_{DDIO}		2.037		V
DC Output Impedance (Normal Mode)	R_{OUT}	Closed-loop connection (RFB connected to OUT)			4		mΩ
Output Resistance (Power-Down Mode)		PD = V_{DDIO}			2		kΩ
Output Current	I_{OUT}	Source/sink within 100mV of the supply rails			±4		mA
		Source/sink within 800mV of the supply rails			±25		
Load Capacitance to GND	C_L					200	pF
Load Resistance to GND	R_L	For specified performance		2			kΩ
Short-Circuit Current	I_{SC}	OUT shorted to AGND or AVDD			±60		mA
		REFO shorted to AGND or AVDD			±65		
		BYPASS shorted to AGND or AVDD			±48		
Short-Circuit Duration	T_{SC}	Short to AGND or AVDD		Indefinite			s
DC Power-Supply Rejection	DC PSRR	V_{OUT} at full scale, V_{AVDD} = 4.5V to 5.5V		-1	±0.05	+1	LSB/V
		V_{AVSS} = -1.5V to -0.5V		-1	±0.003	+1	
STATIC PERFORMANCE—VOLTAGE REFERENCE INPUT SECTION							
Reference High Input Range	V_{REF}			2.4		V_{AVDD} - 0.1	V
Reference Input Capacitance	C_{REF}				10		pF
Reference Input Resistance	R_{REF}				10		MΩ
Reference Input Current	I_B				±0.05		µA
STATIC PERFORMANCE—VOLTAGE REFERENCE OUTPUT SECTION							
Reference High Output Range				2.4		V_{AVDD} - 0.1	V
Reference High Output Load Regulation					500		ppm/mA
Reference Output Capacitor		R_{ESR} < 5Ω			0.1	0.15	nF

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD\_}$ = V_{DDIO} = **4.5V to 5.5V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—V_{BYPASS} OUT SECTION						
Output Voltage	V_{BYPASS}		2.3	2.4	2.5	V
Load Capacitance to GND	C_L	Required for stability, R_{ESR} = 0.1Ω (typ)	1		10	µF
POWER-SUPPLY REQUIREMENTS						
Positive Analog Power-Supply Range	V_{AVDD}		4.5		5.5	V
Digital Interface Power-Supply Range	V_{DDIO}		1.7		V_{AVDD}	V
Negative Analog Power-Supply Range	V_{AVSS}		-1.5	-1.25	0	V
Positive Analog Power-Supply Current	I_{AVDD}	No load, external reference, output at zero scale		5.5	7.5	mA
Negative Analog Power-Supply Current	I_{AVSS}	No load, external reference, output at zero scale	-1.75	-1.0		mA
Interface Power-Supply Current	I_{VDDIO}	Digital inputs at V_{DDIO} or DGND		1	10	µA
Positive Analog Power-Supply Power-Down Current		PD = V_{DDIO}, power-down mode		20	50	µA
Negative Analog Power-Supply Power-Down Current		PD = V_{DDIO}, power-down mode	-10	-3		µA
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR	From 10% to 90% full scale, positive and negative transitions		4.9		V/µs
Voltage Output Settling Time	t_S	From falling edge of LDAC to within 0.003% FS, R_L = 10kΩ, DIN = 1000h (6.25% FS) to F000h (93.75% FS)		3		µs
Busy Time	t_{BUSY}	(Note 4)		1.9		µs
DAC Glitch Impulse		Major code transition (1FFFh to 8000h), R_L = 10kΩ, C_L = 50pF		4		nVs
Digital Feed Through		CSB = V_{DDIO}, f_{SCLK} = 1kHz, all digital inputs from 0V to V_{DDIO}		1		nVs
Output Voltage-Noise Spectral Density		At f = 1kHz to 10kHz, without reference noise, code = 8000h		26		$nV/\sqrt{Hz}$
Output Voltage Noise		At f = 0.1Hz to 10Hz, without reference noise, code = 8000h		1.55		$µV_{P-P}$
Wake-Up Time		From power-down mode		75		µs
Power-Up Time		From power-off		1		ms

ELECTRICAL CHARACTERISTICS

($V_{AVDD\_}$ = V_{DDIO} = **2.7V to 3.3V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 2.5V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		16			Bits
Integral Nonlinearity (Note 3)	INL	DIN = 0x0000 to 0xFFFF (binary mode), DIN = 0x8000 to 0x7FFF (two's complement mode); DIN = 0x0640 to 0xFFFF (binary mode), DIN = 0x8280 to 0x7FFF (two's complement mode), V_{AVSS} = 0V	-1.0	±0.20	+1.0	LSB
Differential Nonlinearity (Note 3)	DNL		-1.0	±0.10	+1.0	LSB
Zero Code Error	OE	DIN = 0, T_A = +25°C	-20	+1.5	+20	LSB
		DIN = 0, T_A = -40°C to +105°C		±4		
Zero Code Error Drift (Note 2)		DIN = 0	-3	±0.35	+3	ppm/°C
Gain Error	GE	T_A = +25°C	-4	±0.65	+4	LSB
		T_A = -40°C to +105°C		±3		
Gain Error Temperature Coefficient (Note 2)	TCGE		-3		+3	ppm/°C of FSR
Output Voltage Range			0		V_{AVDD} - 0.1	V
Reset Voltage Output	$V_{OUT-RESET}$	$\overline{RST}$ = pulse low, M/$\overline{Z}$ = DGND		75		µV
		$\overline{RST}$ = pulse low, M/$\overline{Z}$ = V_{DDIO}		1.25		V
		$\overline{RST}$ = pulse low, V_{AVSS} = 0V, M/$\overline{Z}$ = DGND		10		mV
		$\overline{RST}$ = pulse low, V_{AVSS} = 0V, M/$\overline{Z}$ = V_{DDIO}		1.25		V
		$\overline{RST}$ = DGND, M/$\overline{Z}$ = DGND		-40		mV
		$\overline{RST}$ = DGND, M/$\overline{Z}$ = V_{DDIO}		1.25		V
		$\overline{RST}$ = DGND, V_{AVSS} = 0V, M/$\overline{Z}$ = DGND		10		mV
		$\overline{RST}$ = DGND, V_{AVSS} = 0V, M/$\overline{Z}$ = V_{DDIO}		1.24		V
DC Output Impedance	R_{OUT}	Closed-loop connection, RFB connected to OUT		4		mΩ
Output Current	I_{OUT}	Source/sink within 100mV of the supply rails		±4		mA
		Source/sink within 800mV of the supply rails		±25		
Load Capacitance to GND	C_L				200	pF
Load Resistance to GND	R_L	For specified performance	2			kΩ
Short-Circuit Current	ISC	OUT shorted to AGND or AVDD		±60		mA
		REFO shorted to AGND or AVDD		±65		
		BYPASS shorted to AGND or AVDD		±48		
Short-Circuit Duration	TSC	Short to AGND or AVDD	Indefinite			s
DC Power-Supply Rejection	DCPSRR	V_{OUT} at full scale, V_{AVDD} = 2.7V to 3.3V	-1	±0.1	+1	LSB/V
		V_{AVSS} = -1.5V to -0.5V	-1	±0.01	+1	

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD\_}$ = V_{DDIO} = **2.7V to 3.3V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 2.5V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—VOLTAGE REFERENCE INPUT SECTION						
Reference High Input Range	V_{REF}		2.4		V_{AVDD} - 0.1	V
Reference Input Capacitance	C_{REF}			10		pF
Reference Input Resistance	R_{REF}			10		MΩ
Reference Input Current	IB			±0.05		µA
STATIC PERFORMANCE—VOLTAGE REFERENCE OUTPUT SECTION						
Reference High Output Range			2.4		V_{AVDD} - 0.1	V
Reference High Output Load Regulation				500		ppm/mA
Reference Output Capacitor		R_{ESR} < 5Ω		0.1	0.15	nF
STATIC PERFORMANCE—V_{BYPASS} OUT SECTION						
Output Voltage	V_{BYPASS}		2.3	2.4	2.5	V
Load Capacitance to GND	C_L	Required for stability, R_{ESR} = 0.1Ω (typ)	1		10	µF
POWER-SUPPLY REQUIREMENTS						
Positive Analog Power-Supply Range	V_{AVDD}		2.7		3.3	V
Interface Power-Supply Range	V_{DDIO}		1.7		V_{AVDD}	V
Negative Analog Power-Supply Range	V_{AVSS}		-1.5	-1.25	0	V
Positive Analog Power-Supply Current	I_{AVDD}	No load, external reference, output at zero scale		4	6.5	mA
Negative Analog Power-Supply Current	I_{AVSS}	No load, external reference, output at zero scale	-1.5	-0.8		mA
Interface Power-Supply Current	I_{VDDIO}	Digital inputs at V_{DDIO} or DGND		1	10	µA
Positive Analog Power-Supply Power-Down Current		PD = V_{DDIO}, power-down mode		20	50	µA
Negative Analog Power-Supply Power-Down Current		PD = V_{DDIO}, power-down mode	-10	-3		µA
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR	From 10% to 90% full scale, positive and negative transitions		4.9		V/µs
Voltage Output Settling Time	t_S	From falling edge of LDAC to within 0.003% FS, R_L = 10kΩ, DIN = 1000h (6.25% FS) to F000h (93.75% FS)		3		µs

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD\_}$ = V_{DDIO} = **2.7V to 3.3V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 2.5V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Busy Time	t_{BUSY}	(Note 4)		1.9		µs
DAC Glitch Impulse		Major code transition (7FFFh to 8000h), R_L = 10kΩ, C_L = 50pF		2.5		nVs
Digital Feedthrough		CSB = V_{DDIO}, f_{SCLK} = 1kHz, all digital inputs from 0V to V_{DDIO}		1		nVs
Output Voltage-Noise Spectral Density		At f = 1kHZ to 10kHz, without reference noise, code = 8000h		26		nV/$\sqrt{Hz}$
Output Voltage Noise		At f = 0.1Hz to 10Hz, without reference noise, code = 8000h		1.55		µV_{P-P}
Wake-Up Time		From power-down mode		75		µs
Power-Up Time		From power-off		1		ms

Note 2: All devices are 100% tested at T_A = +25°C and T_A = +105°C. Limits at T_A = -40°C are guaranteed by design.
Note 3: Linearity is tested from V_{REFO} to AGND.
Note 4: The total analog throughput time from DIN to V_{OUT} is the sum of t_S and t_{BUSY} (4.9µs, typ).

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

($V_{AVDD\_}$ = 5V, V_{DDIO} = **2.7V to 5.5V**, V_{AVSS} = -1.25V, V_{REF} = 4.096V, R_L = 10kΩ, TC/$\overline{SB}$ = M/$\overline{Z}$, C_{REFO} = 100pF, C_L = 100pF, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{LDAC}$)						
Input High Voltage	V_{IH}		0.7 x V_{DDIO}			V
Input Low Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Hysteresis	V_{IHYST}		200	300		mV
Input Leakage Current	I_{IN}	Input = 0V of V_{DDIO}		±0.1	±1	µA
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUT CHARACTERISTICS (DOUT, $\overline{READY}$, $\overline{BUSY}$)						
Output Low Voltage	V_{OL}	I_{SOURCE} = 5.0mA			0.25	V
Output High Voltage	V_{OH}	I_{SINK} = 5.0mA, except for $\overline{BUSY}$	V_{DDIO} - 0.25			
Output Three-State Leakage	I_{OZ}	DOUT only		±0.1	±1	µA
Output Three-State Capacitance	C_{OZ}	DOUT only		15		pF
Output Short-Circuit Current	I_{OSS}	V_{DDIO} = 5.5V		±150		mA

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD\_}$ = 5V, V_{DDIO} = **2.7V to 5.5V**, V_{AVSS} = -1.25V, V_{REF} = 4.096V, R_L = 10kΩ, TC/$\overline{SB}$ = M/$\overline{Z}$, C_{REFO} = 100pF, C_L = 100pF, C_{BYPASS} = 1μF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
Serial Clock Frequency	f_{SCLK}	Stand-alone, write mode			50	MHz
		Stand-alone read mode and daisy-chained read and write modes (Note 5)			12.5	
SCLK Period	t_{CP}	Stand-alone, write mode	20			ns
		Stand-alone read mode and daisy-chained read and write modes	80			
SCLK Pulse Width High	t_{CH}	40% duty cycle	8			ns
SCLK Pulse Width Low	t_{CL}	40% duty cycle	8			ns
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSSO}	First SCLK falling edge: Stand-alone, write mode	8			ns
		First SCLK falling edge: Stand-alone read mode and daisy-chained read and write modes	28			
$\overline{CS}$ Fall to SCLK Fall Hold Time	t_{CSH0}	Inactive falling edge preceding first falling edge	0			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}	24th falling edge	2			ns
DIN to SCLK Fall Setup Time	t_{DS}		5			ns
DIN to SCLK Fall Hold Time	t_{DH}		4.5			ns
SCLK Rise to DOUT Settle Time	t_{DOT}	C_L = 20pF (Note 6)			32	ns
SCLK Rise to DOUT Hold Time	t_{DOH}	C_L = 0pF (Note 6)	2			ns
SCLK Fall to DOUT Disable Time	t_{DOZ}	24th active edge deassertion	2		30	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	Asynchronous assertion	2		30	ns
$\overline{CS}$ Rise to DOUT Disable	t_{CSDOZ}	Stand-alone, aborted sequence			35	ns
		Daisy-chained, aborted sequence	20			
SCLK Fall to $\overline{READY}$ Fall	t_{CRF}	24th falling-edge assertion, C_L = 20pF			30	ns
SCLK Fall to $\overline{READY}$ Hold	t_{CRH}	24th falling-edge assertion, C_L = 0pF	2			ns
SCLK Fall to $\overline{BUSY}$ Fall	t_{CBF}	$\overline{BUSY}$ assertion		5		ns
$\overline{CS}$ Rise to $\overline{READY}$ Rise	t_{CSR}	C_L = 20pF			35	ns
$\overline{CS}$ Rise to SCLK Fall	t_{CSA}	24th falling edge, aborted sequence	20			ns
$\overline{CS}$ Pulse Width High	t_{CSPW}	Stand alone	20			ns
SCLK Fall to $\overline{CS}$ Fall	t_{CSF}	24th falling edge	100			ns
$\overline{LDAC}$ Pulse Width	t_{LDPW}		20			ns
$\overline{LDAC}$ Fall to SCLK Fall Hold	t_{LDH}	Last active falling edge	20			ns
$\overline{RST}$ Pulse Width	t_{RSTPW}		20			ns

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD\_}$ = 5V, V_{DDIO} = **1.8V to 2.7V**, V_{AVSS} = -1.25V, V_{REF} = 4.096V, R_L = 10kΩ, TC/$\overline{SB}$ = M/$\overline{Z}$, C_{REFO} = 100pF, C_L = 100pF, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{LDAC}$)							
Input High Voltage	V_{IH}			0.8 x V_{DDIO}			V
Input Low Voltage	V_{IL}					0.2 x V_{DDIO}	V
Input Hysteresis	V_{IHYST}			200	300		mV
Input Leakage Current	I_{IN}	Input = 0V or V_{DDIO}			±0.1	±1	µA
Input Capacitance	C_{IN}				10		pF
DIGITAL OUTPUT CHARACTERISTICS (DOUT, $\overline{READY}$, $\overline{BUSY}$)							
Output Low Voltage	V_{OL}	I_{SOURCE} = 1.0mA				0.2	V
Output High Voltage	V_{OH}	I_{SINK} = 1.0mA, except for $\overline{BUSY}$		V_{DDIO} - 0.2			V
Output Three-State Leakage	I_{OZ}	DOUT only			±0.1	±1	µA
Output Three-State Capacitance	C_{OZ}	DOUT only			15		pF
Output Short-Circuit Current	I_{OSS}	V_{DDIO} = 2.7V			±150		mA
TIMING CHARACTERISTICS							
Serial Clock Frequency	f_{SCLK}	Stand-alone, write mode				50	MHz
		Stand-alone read mode and daisy chained read and write modes (Note 5)				8	
SCLK Period	t_{CP}	Stand-alone, write mode		20			ns
		Stand-alone read mode and daisy-chained read and write modes		125			
SCLK Pulse Width High	t_{CH}	40% duty cycle		12			ns
SCLK Pulse Width Low	t_{CL}	40% duty cycle		12			ns
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSSO}	First SCLK falling edge	Stand-alone, read mode	12			ns
			Stand-alone read mode and daisy-chained read and write modes	36			
$\overline{CS}$ Fall to SCLK Fall Hold Time	t_{CSH0}	Inactive falling edge preceding first falling edge		0			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}	24th falling edge		4			ns
DIN to SCLK Fall Setup Time	t_{DS}			8			ns
DIN to SCLK Fall Hold Time	t_{DH}			8			ns

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD\_}$ = 5V, V_{DDIO} = **1.8V to 2.7V**, V_{AVSS} = -1.25V, V_{REF} = 4.096V, R_L = 10kΩ, TC/$\overline{SB}$ = M/$\overline{Z}$, C_{REFO} = 100pF, C_L = 100pF, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Rise to DOUT Settle Time	t_{DOT}	C_L = 20pF (Note 6)			60	ns
SCLK Rise to DOUT Hold Time	t_{DOH}	C_L = 0pF (Note 6)	2			ns
SCLK Fall to DOUT Disable Time	t_{DOZ}	24th active edge deassertion	2		40	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	Asynchronous assertion	2		50	ns
$\overline{CS}$ Rise to DOUT Disable	t_{CSDOZ}	Stand-alone, aborted sequence			70	ns
		Daisy-chained, aborted sequence			130	
SCLK Fall to $\overline{READY}$ Fall	t_{CRF}	24th falling edge assertion, C_L = 20pF			60	ns
SCLK Fall to $\overline{READY}$ Hold	t_{CRH}	24th falling edge assertion, C_L = 0pF	2			ns
SCLK Fall to $\overline{BUSY}$ Fall	t_{CBF}	$\overline{BUSY}$ assertion		5		ns
$\overline{CS}$ Rise to $\overline{READY}$ Rise	t_{CSR}	C_L = 20pF			60	ns
$\overline{CS}$ Rise to SCLK Fall	t_{CSA}	24th falling edge, aborted sequence	20			ns
$\overline{CS}$ Pulse Width High	t_{CSPW}	Stand alone	20			ns
SCLK Fall to $\overline{CS}$ Fall	t_{CSF}	24th falling edge	100			ns
$\overline{LDAC}$ Pulse Width	t_{LDPW}		20			ns
$\overline{LDAC}$ Fall to SCLK Fall Hold	t_{LDH}	Last active falling edge	20			ns
$\overline{RST}$ Pulse Width	t_{RSTPW}		20			ns

Note 5: Daisy-chain speed is relaxed to accommodate (t_{CRF} + t_{CSS0}).
Note 6: DOUT speed limits overall SPI speed. 50MHz is only specified without DOUT functionality.

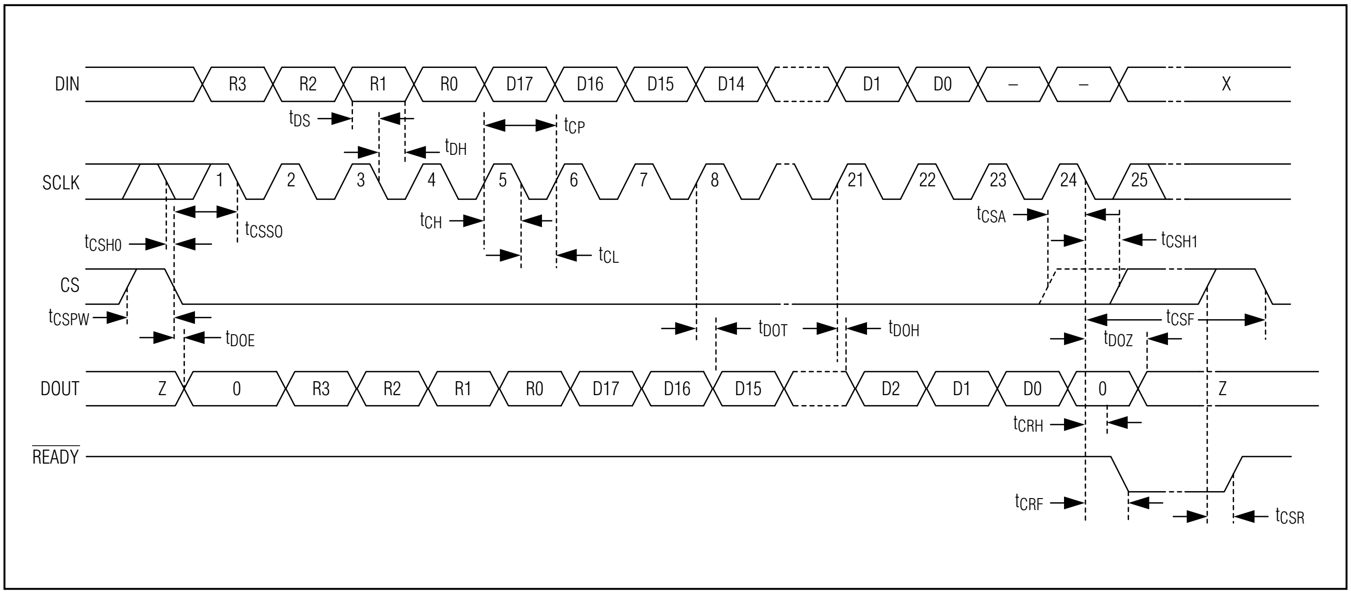
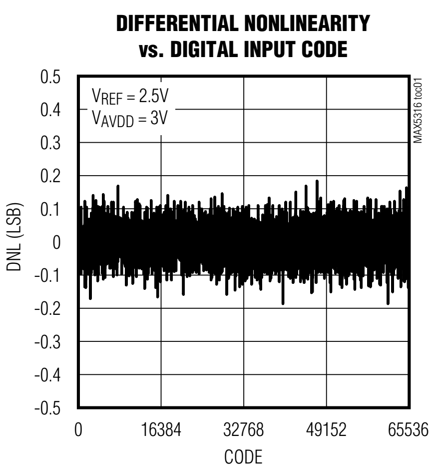
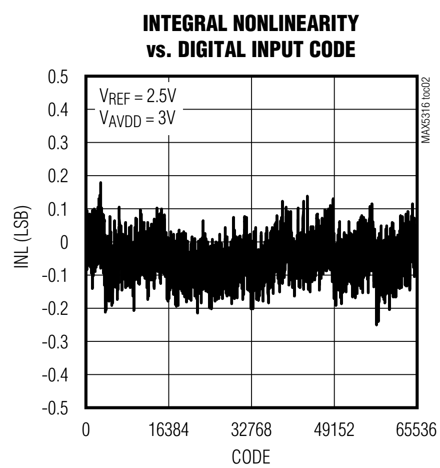


Figure 1. Serial Interface Timing Diagram, Stand-Alone Operation

Typical Operating Characteristics

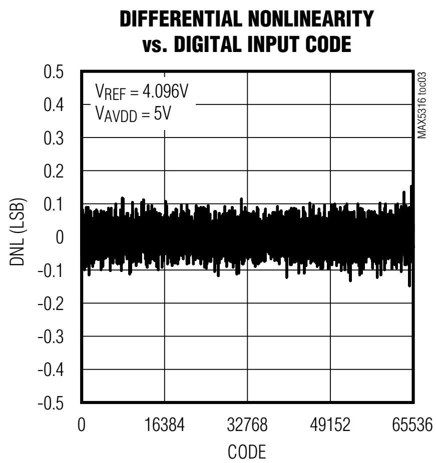
($V_{AVDD\_} = V_{DDIO}$ = 5V, V_{AVSS} = -1.25V, $V_{AGND} = V_{DGND} = V_{AGND\_F} = V_{AGND\_S}$ = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST} = V_{DDIO}$, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1μF, T_A = +25°C, unless otherwise noted.)

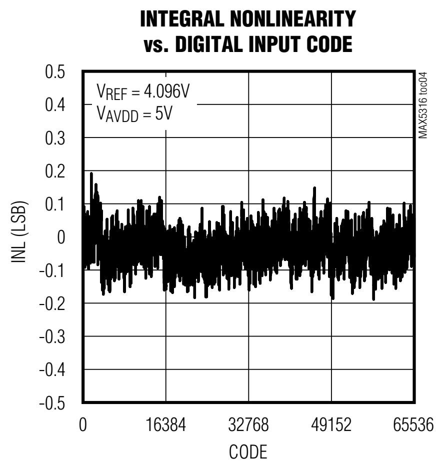


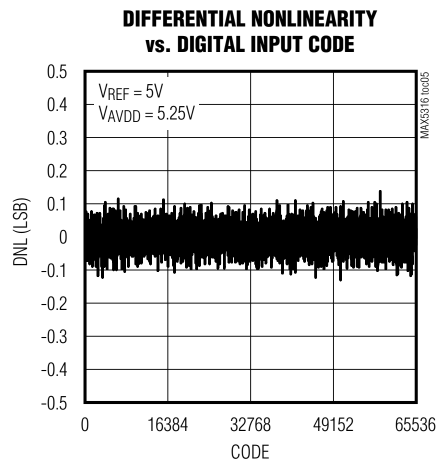


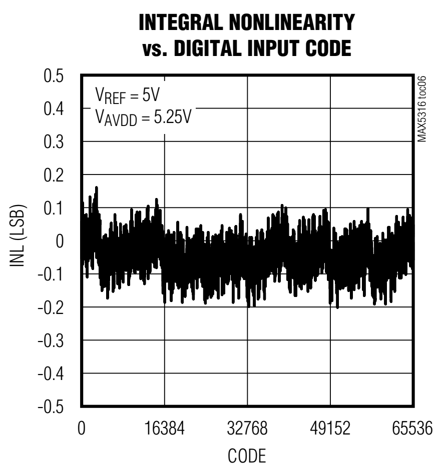
Typical Operating Characteristics (continued)

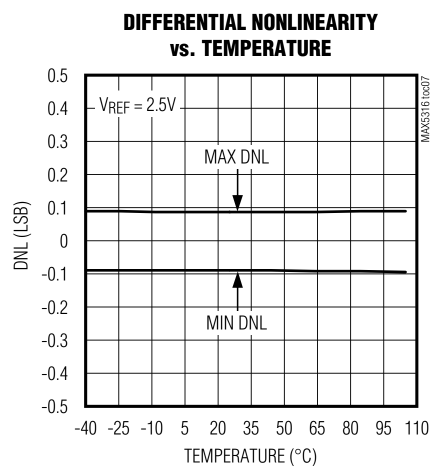
($V_{AVDD\_}$ = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

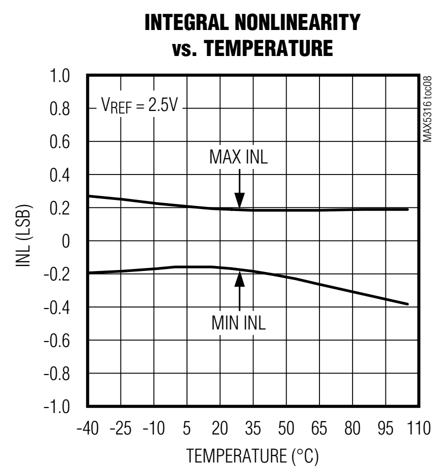








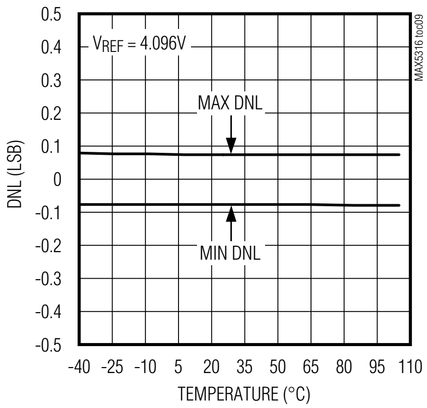




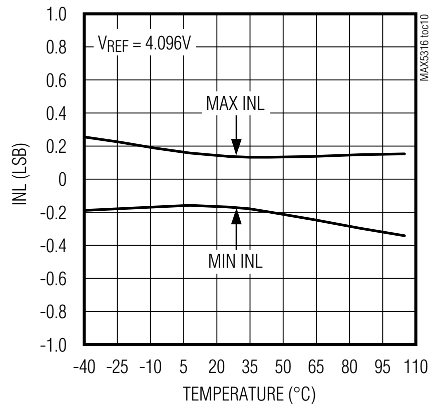
Typical Operating Characteristics (continued)

($V_{AVDD\_}$ = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1μF, T_A = +25°C, unless otherwise noted.)

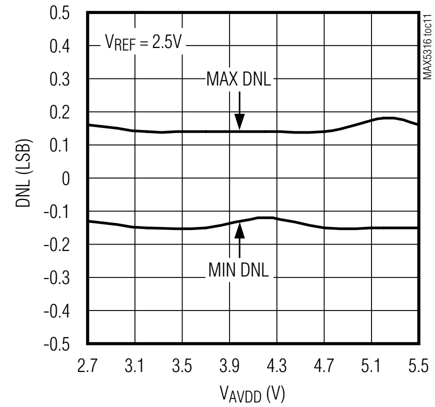
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. TEMPERATURE



DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE



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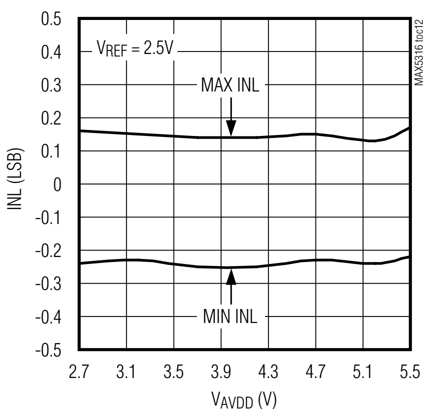
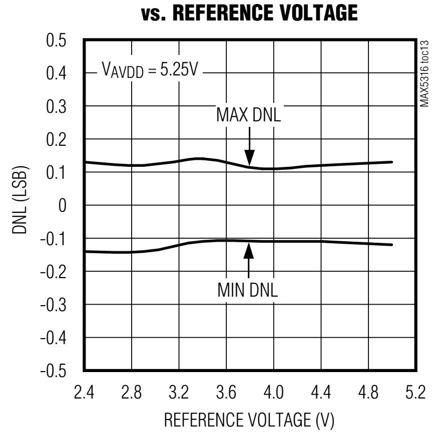
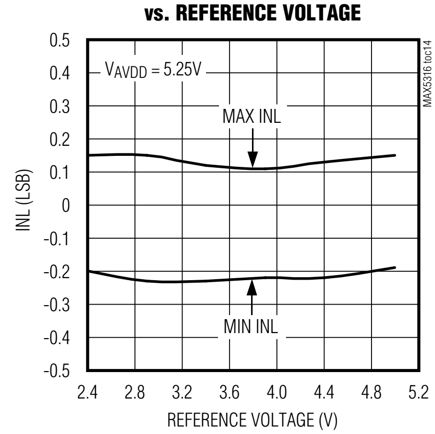


DIFFERENTIAL NONLINEARITY vs. REFERENCE VOLTAGE

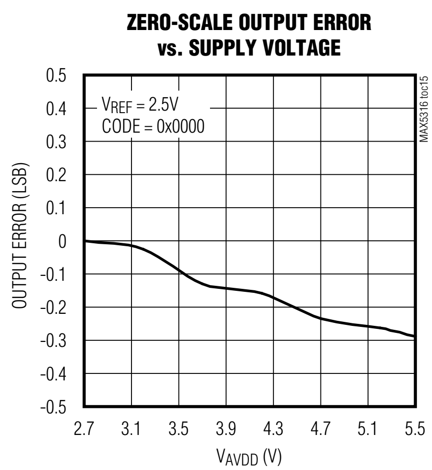


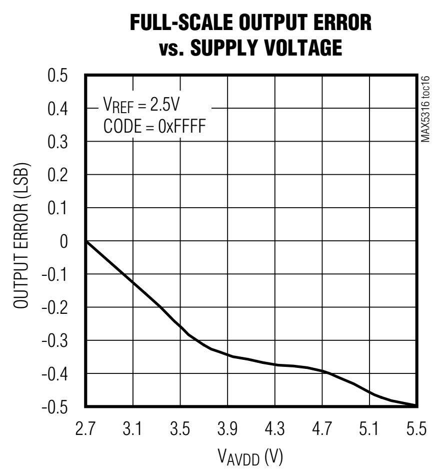
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE

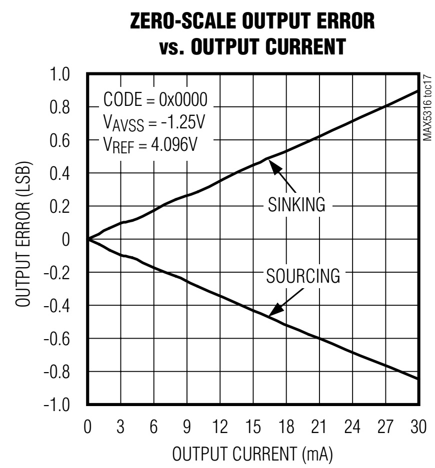


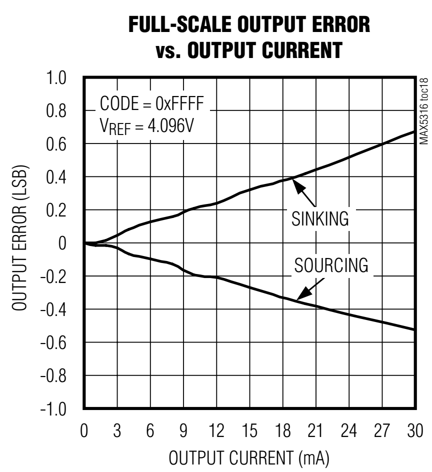
Typical Operating Characteristics (continued)

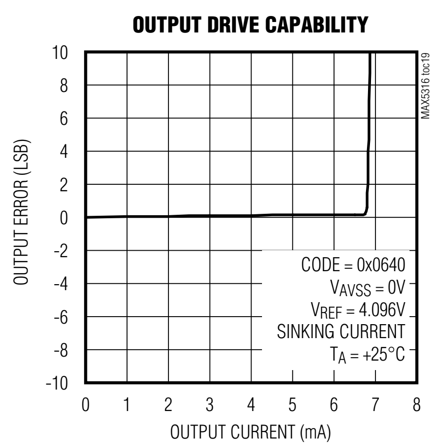
($V_{AVDD\_} = V_{DDIO}$ = 5V, V_{AVSS} = -1.25V, $V_{AGND} = V_{DGND} = V_{AGND\_F} = V_{AGND\_S}$ = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST} = V_{DDIO}$, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

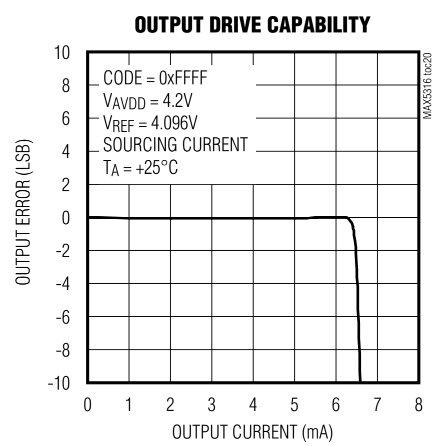






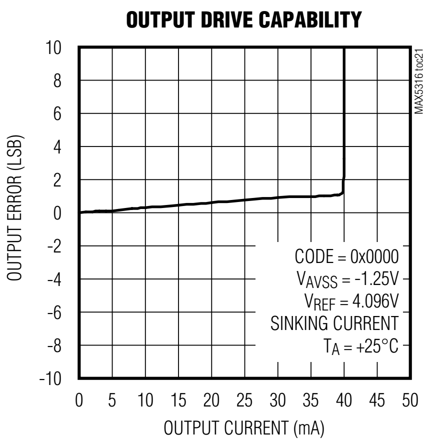


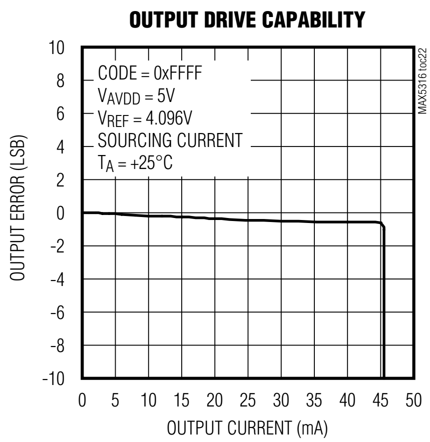


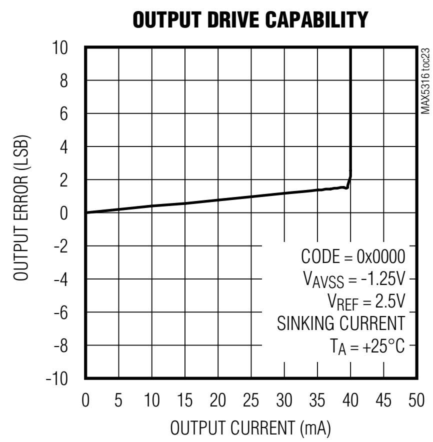


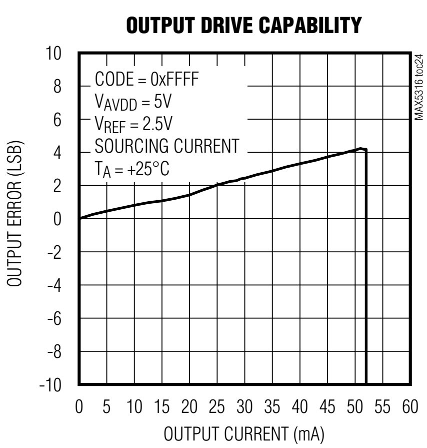
Typical Operating Characteristics (continued)

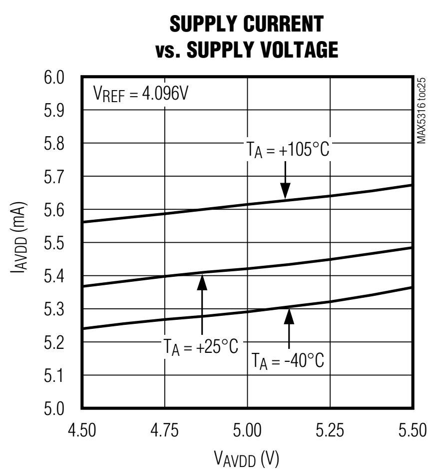
($V_{AVDD\_}$ = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1μF, T_A = +25°C, unless otherwise noted.)

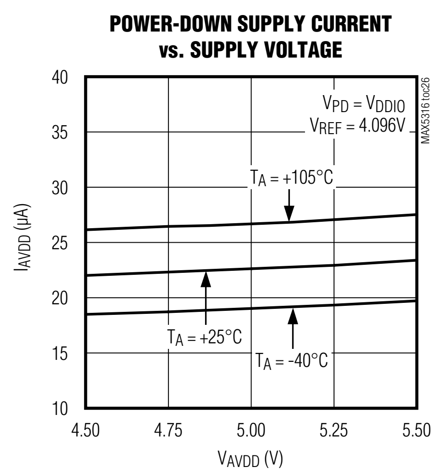








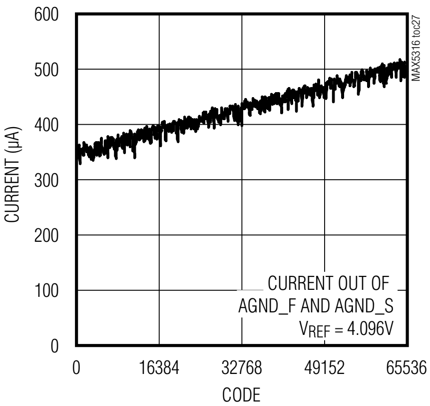




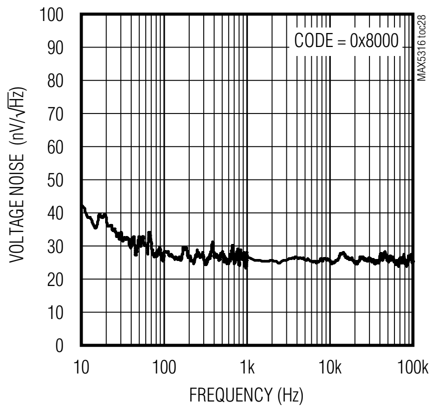
Typical Operating Characteristics (continued)

($V_{AVDD\_}$ = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

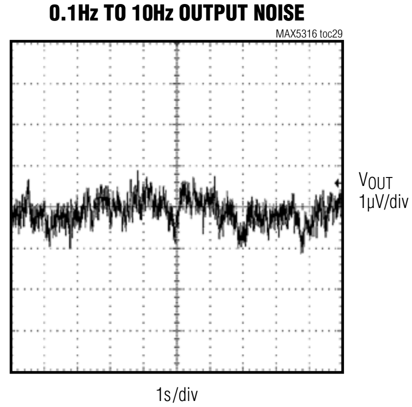
GROUND CURRENT vs. CODE



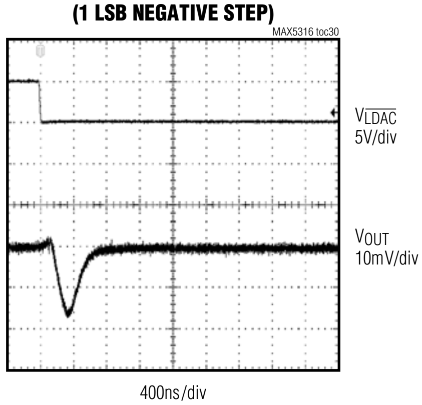
OUTPUT NOISE DENSITY



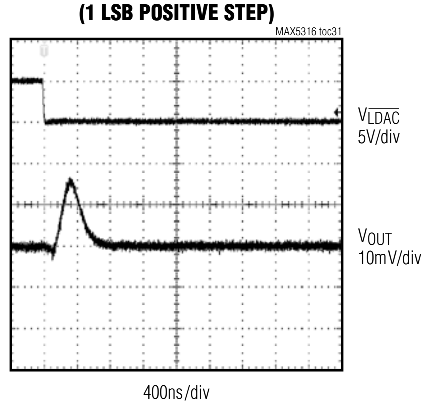
0.1Hz TO 10Hz OUTPUT NOISE



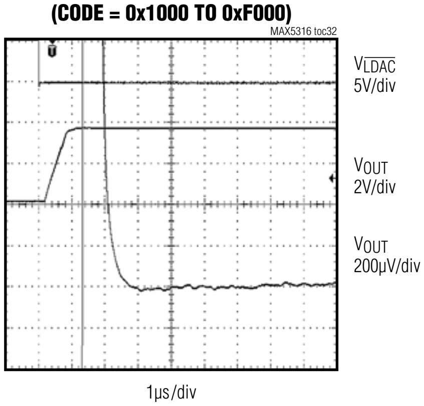
MAJOR CARRY GLITCH (1 LSB NEGATIVE STEP)



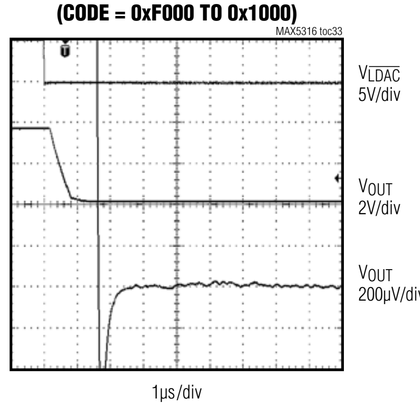
MAJOR CARRY GLITCH (1 LSB POSITIVE STEP)



SETTLING TIME (CODE = 0x1000 TO 0xF000)



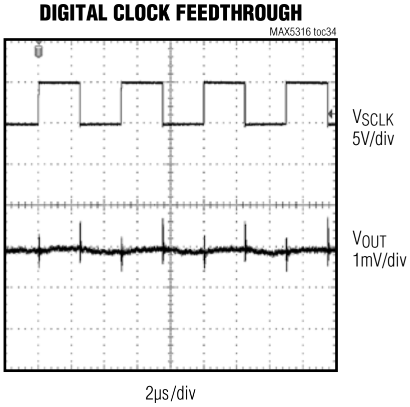
SETTLING TIME (CODE = 0xF000 TO 0x1000)



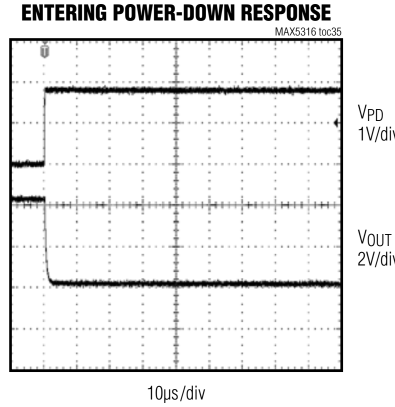
Typical Operating Characteristics (continued)

($V_{AVDD\_}$ = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

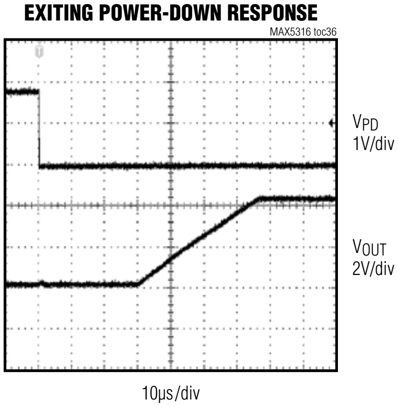
DIGITAL CLOCK FEEDTHROUGH



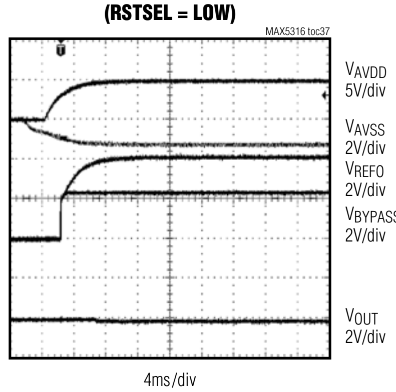
ENTERING POWER-DOWN RESPONSE



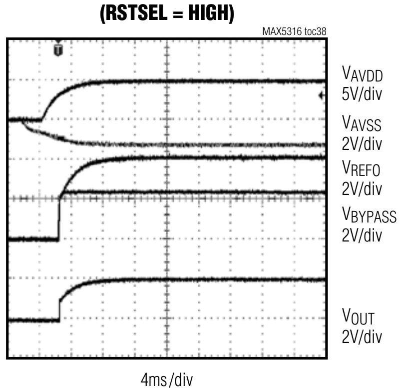
EXITING POWER-DOWN RESPONSE



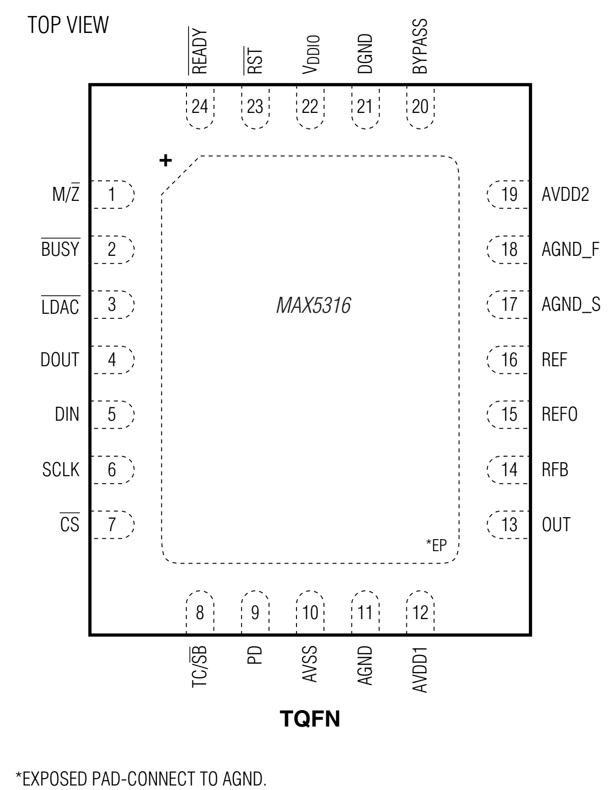
SLOW POWER-UP RESPONSE (RSTSEL = LOW)



SLOW POWER-UP RESPONSE (RSTSEL = HIGH)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	M/$\overline{Z}$	Reset Select Input. M/$\overline{Z}$ selects the default state of the analog output (OUT) after power-on or hardware or software reset. Connect M/$\overline{Z}$ to V_{DDIO} to set the default output voltage to midscale or to DGND to set the default output voltage to zero scale.
2	$\overline{BUSY}$	Digital Input/Open-Drain Output. Connect a 5.1kΩ pullup resistor from $\overline{BUSY}$ to V_{DDIO}. $\overline{BUSY}$ goes low immediately after writing to the DIN register. During this time, the user can continue writing new data to the DIN register, but no further updates to the DAC register and DAC output can take place. If $\overline{LDAC}$ is asserted low while $\overline{BUSY}$ is low, this event is stored. $\overline{BUSY}$ is bidirectional, and can be asserted low externally to delay $\overline{LDAC}$ action. $\overline{BUSY}$ also goes low during power-on reset, when $\overline{RST}$ is low, or when software reset is activated.
3	$\overline{LDAC}$	Active-Low Load DAC Logic Input. If $\overline{LDAC}$ is taken low while $\overline{BUSY}$ is inactive (high), the contents of the input registers are transferred to the DAC register and the DAC output is updated. If $\overline{LDAC}$ is taken low while $\overline{BUSY}$ is asserted low, the $\overline{LDAC}$ event is stored and the DAC register update is delayed until $\overline{BUSY}$ deasserts. Any event on $\overline{LDAC}$ during power-on reset or when $\overline{RST}$ is low is ignored.
4	DOUT	SPI Bus Serial Data Output. See the *Serial Interface* section for details.

Pin Description (continued)

PIN	NAME	FUNCTION
5	DIN	SPI Bus Serial Data Input. See the *Serial Interface* section for details.
6	SCLK	SPI Bus Serial Clock Input. See the *Serial Interface* section for details.
7	$\overline{\text{CS}}$	SPI Bus Active-Low Chip-Select Input. See the *Serial Interface* section for details.
8	TC/$\overline{\text{SB}}$	DIN Format Select Input. Connect TC/$\overline{\text{SB}}$ to DGND to set the data input format to straight binary or to VDDIO to set it to two's complement.
9	PD	Active-High Power-Down Input. Connect PD to DGND for normal operation. Connect PD to VDDIO to place the device in power-down. In power-down, OUT (analog voltage output) is connected to AGND through a 2kΩ resistor, but the contents of the input registers and the DAC latch do not change. The SPI interface remains active in power-down.
10	AVSS	Negative Analog Power-Supply Input. Connect to AGND or a negative supply voltage. When connected to the negative supply voltage, bypass AVSS with a 0.1µF capacitor to AGND.
11	AGND	Analog Ground. Connect to the analog ground plane.
12, 19	AVDD1	Positive Analog Power-Supply Input. Bypass each AVDD_ locally with a 0.1µF and 10µF capacitor to AGND (analog ground plane). Connect AVDD1 and AVDD2 together.
13	OUT	Buffered Analog Voltage Output. Connect OUT to RFB externally to close the output buffer feedback loop. The buffered output is capable of directly driving a 10kΩ load. The state of M/$\overline{\text{Z}}$ sets the power-on reset state of OUT (zero or midscale). In power-down, OUT is connected to AGND through a 2kΩ pulldown resistor.
14	RFB	Feedback Resistor Input. RFB is connected through the internal feedback resistor to the inverting input of the analog output buffer. Externally connect RFB to OUT to close the output buffer feedback loop.
15	REFO	Voltage Reference Buffered Output. Bypass with a 100pF capacitor to AGND.
16	REF	High-Impedance 10MΩ Voltage Reference Input
17	AGND_S	DAC Analog Ground Sense
18	AGND_F	DAC Analog Ground Force. Connect to the analog ground plane.
19	AVDD2	Positive Analog Power-Supply Input. AVDD2 supplies power to the internal digital linear regulator. Bypass AVDD2 locally to AGND with 0.1µF and 10µF capacitors. Connect AVDD2 and AVDD1 together.
20	BYPASS	Internal Bypass Connection. Connect BYPASS to DGND with 0.01µF and 1µF capacitors.
21	DGND	Digital Ground
22	V_{DDIO}	Digital Interface Power-Supply Input. Connect to a 1.7V to 5.5V logic-level supply. Bypass V_{DDIO} with a 0.1µF capacitor to DGND. The supply voltage at V_{DDIO} sets the logic-level for the digital interface.
23	$\overline{\text{RST}}$	Active-Low Reset Input. Drive $\overline{\text{RST}}$ low to DGND to put the device into a reset state. A reset state sets all SPI input registers to their default power-on reset states as defined by the state of inputs M/$\overline{\text{Z}}$ and TC/$\overline{\text{SB}}$. Set $\overline{\text{RST}}$ high to V_{DDIO}, the DAC output remains at the state defined by M/$\overline{\text{Z}}$ until $\overline{\text{LDAC}}$ is taken low.
24	$\overline{\text{READY}}$	SPI Active-Low Ready Output. $\overline{\text{READY}}$ asserts low when the device successfully completes processing an SPI data frame. $\overline{\text{READY}}$ asserts high at the next rising edge of $\overline{\text{CS}}$. In daisy-chain applications, the $\overline{\text{READY}}$ output typically drives the $\overline{\text{CS}}$ input of the next device in the chain or a GPIO of a microcontroller.
—	EP	Exposed Pad. EP is internally connected to AGND. Connect to the analog ground plane.

Detailed Description

The MAX5316 is a high-accuracy, 16-bit, serial SPI input, buffered voltage output digital-to-analog converter (DAC) in a 4mm x 5mm, 24-lead TQFN package. The device features ±1 LSB INL (max) accuracy and a ±1 LSB DNL (max) accuracy over the -40°C to +105°C temperature range.

The DAC voltage output is buffered with a fast settling time of 3µs and a low offset and gain drift of ±0.6ppm/°C of FSR (typ). The force-sense output (OUT) maintains accuracy while driving loads with long lead lengths. A separate AVSS supply allows the output amplifier to go to 0V (GND) while maintaining full linearity performance.

At power-up, the device resets its outputs to zero or midscale, providing additional safety for applications which drive valves or other transducers that need to be off on power-up. This is selected by the state of the M/$\overline{Z}$ input on power-up.

The wide supply voltage range of 2.7V to 5.5V and integrated low-drift, low-noise reference buffer amplifier makes for ease of use. Since the reference buffer input has a high input resistance, an external buffer is not required. The device accepts an external reference between 2.4V and V_{AVDD} - 0.1V for maximum flexibility.

The MAX5316 features a 50MHz, 3-wire SPI, QSPI, MICROWIRE, and DSP-compatible serial interface. The separate digital interface supply voltage input (V_{DDIO}) is compatible with a wide range of digital logic levels from 1.7V to 5.5V, eliminating the need for separate voltage translators.

DAC Reference Buffer

The external reference input has a high input (REF) impedance of 10MΩ ll 10pF and accepts an input voltage from +2.4V to V_{AVDD} - 0.1V. Connect an external reference supply between REF and AGND. Bypass the reference buffer output REFO to AGND with a 100pF capacitor. Connect the anode of an external Schottky diode to REF and the cathode to AVDD1 to prevent internal ESD diode conduction in the event that the reference voltage comes up before AVDD at power up. Follow the recommendations described in the *Power-Supply Sequencing* section.

Visit **www.maxim-ic.com/products/references** for a list of available external voltage-reference devices.

Output Amplifier (OUT)

The MAX5316 includes an internal buffer for the DAC output. The internal buffer provides improved load regulation for the DAC output. The output buffer slews at 5V/µs and can drive up to 2kΩ in parallel with 200pF. The buffer has a rail-to-rail output capable of swinging to within 100mV of AVDD_ and AVSS.

The positive analog supply voltage (AVDD_) determines the maximum output voltage of the device as AVDD_ powers the output buffer.

The output is diode clamped to ground, preventing negative voltage excursions beyond approximately -0.6V.

Negative Supply Voltage (AVSS)

The negative supply voltage (AVSS) determines the minmum output voltage. If AVSS is connected to ground, the output voltage can be set to as low as 100mV without degrading linearity. For operation down to 0V, connect AVSS to a negative supply voltage between -0.1V and -1.25V. The MAX1735 is recommended for generating -1.25V from a -5V supply.

Force/Sense

The MAX5316 uses force/sense techniques to ensure that the load is regulated to the desired output voltage despite line drops due to long lead lengths. Since AGND_F and AGND_S have code dependent ground currents, a ground impedance less than 13mΩ ensures that the INL will not degrade by more than 0.1 LSB. Form a star ground connection (Figure 2a) near the device with AGND_F, AGND_S, and AGND tied together. Always refer remote DAC loads to this system ground for best performance. Figure 2b shows how to configure the device and an external op amp for proper force/sense operation. The amplifier provides as much drive as needed to force the sensed voltage (measured between RFB and AGND_S) to equal the desired voltage.

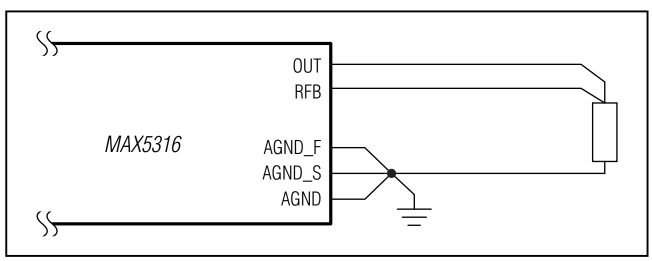


Figure 2a. Star Ground Connection

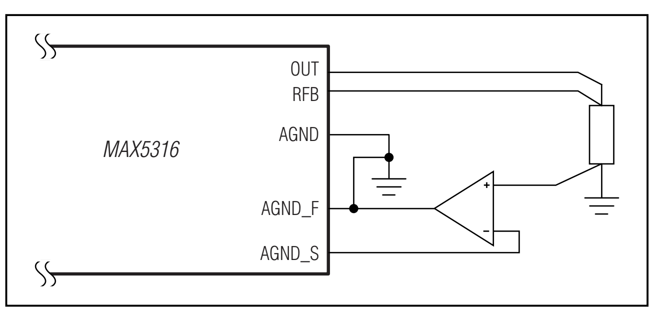


Figure 2b. Force/Sense Connection

16-Bit Ideal Transfer Function

The transfer function for the MAX5316 is given by:

$$V_{OUT} = V_{REF} \times \frac{CODE}{2^{16}}$$

(DIN code from 0x0000 to 0xFFFF)

For the simple binary case and:

$$V_{OUT} = V_{REF} \times \frac{(CODE - 0x8000)}{2^{16}}$$

(DIN code from 0x8000 to 0xFFFF)

$$V_{OUT} = V_{REF} \times \frac{CODE}{2^{16}} + \frac{V_{REF}}{2}$$

(DIN code from 0x0000 to 0xFFFF)

For the two's complement case.

Straight Binary vs. Two's Complement

Table 1 and Table 2 show the math necessary to convert the DIN code into V_{OUT} for the 16-bit DAC. 1 LSB is equal to $V_{REF}/2^{16}$.

Input Range

The range of DIN is summarized in Table 3 and Table 4. Also shown are the range values for the MAX5316 with a 4.096V reference. Note that V_{REF} is the reference voltage applied to REF and 1 LSB is equal to $V_{REF}/2^{16}$.

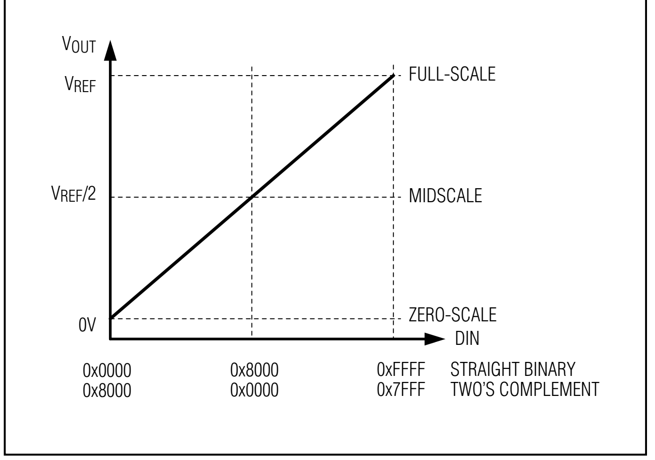


Figure 3. DIN to V_{OUT} Transfer Curve

Table 1. Straight Binary Mode

DIN CODE	EQUATION FOR V_{OUT}	RANGE
0x0000 to 0xFFFF	$V_{OUT} = V_{REF} \times \frac{CODE}{2^{16}}$	0V to (V_{REF} - 1 LSB)

Table 2. Two's Complement Mode

DIN CODE	EQUATION FOR V_{OUT}	RANGE
0x8000 to 0xFFFF	$V_{OUT} = V_{REF} \times \left(\frac{CODE - 0x8000}{2^{16}}\right)$	0V to (V_{REF}/2 -1 LSB)
0x0000 to 0x7FFF	$V_{OUT} = V_{REF} \times \frac{CODE}{2^{16}} + \frac{V_{REF}}{2}$	V_{REF}/2 to (V_{REF} - 1 LSB)

Table 3. DIN Range (Straight Binary Mode)

RANGE	DIN CODE	V_{OUT} (V)	MAX5316 VALUE (V)
Minimum	0x0000	0	0
Maximum	0xFFFF	(V_{REF} - 1 LSB)	4.095938

Table 4. DIN Range (Two's Complement Mode)

RANGE	DIN CODE	V_{OUT} (V)	MAX5316 VALUE (V)
Minimum	0x8000	0	0
Maximum	0x7FFF	(V_{REF} - 1 LSB)	4.095938

Reset

The device is reset upon power-on, hardware reset using $\overline{\text{RST}}$, or software reset using register 0x4, bit 15, command $\overline{\text{RSTSW}}$. After reset, the value of the input register, the DAC latch and the output voltage are set to the values defined by the M/$\overline{\text{Z}}$ input. If a hardware reset occurs during a SPI programming frame, anything before and after the reset for the frame will be ignored. A software reset initiated through the SPI interface takes effect after the end of the valid frame.

Output State Upon Reset

The output voltage can be set to either zero or midscale upon power-up, or a hardware or software reset, depending on the state of the M/$\overline{\text{Z}}$ input. After power-up, if the device detects that this input is low, the output voltage is set to zero scale. If M/$\overline{\text{Z}}$ is high, the output voltage is set to midscale.

Note that during reset, when $\overline{\text{RST}}$ is low or $\overline{\text{RSTSW}}$ is set to 0, the output voltage is set slightly lower than the value after coming out of reset. During reset, the output voltage is set to the values shown for the $V_{OUT\text{-}RESET}$ specification in the *Electrical Characteristics*.

Power-Down

The device can be powered down by either hardware (pulling PD high) or software (setting the PD_SW bit in either the 0x4 or 0xC registers). Note that the hardware and software inputs are ORed. Asserting either is enough to place the device in power-down mode.

In order to restore normal operation to the device, satisfy both of these conditions:

1) Pull PD low.
2) Set the bits PD_SW's (in both 0x4 and 0xC registers) to 0.

In power-down, the output is internally connected to AGND through a 2kΩ resistor. The SPI interface remains active and the DAC register content remains unchanged.

Data Format Selection (Straight Binary vs. Two's Complement)

The MAX5316 interprets the data code input (DIN) as either straight binary or two's complement. To choose the straight binary format, set the TC/$\overline{\text{SB}}$ input low. For two's complement, set the input high.

$\overline{\text{LDAC}}$ and $\overline{\text{BUSY}}$ Interaction

The $\overline{\text{BUSY}}$ line is open drain and is normally pulled up by an external resistor. It is software-configurable to be bidirectional and can be pulled down externally. Whenever the DIN register is changed, the device transfers the value to the DAC register. To indicate to the host processor that the device is busy transferring, the device pulls the $\overline{\text{BUSY}}$ output low. Once transfer is complete, the device releases $\overline{\text{BUSY}}$ and the host processor can load the DAC by toggling the $\overline{\text{LDAC}}$ input. If $\overline{\text{LDAC}}$ is set low while $\overline{\text{BUSY}}$ is low, the $\overline{\text{LDAC}}$ event is latched and implemented when the transfer is complete and $\overline{\text{BUSY}}$ rises.

There are four ways in which the $\overline{\text{LDAC}}$ and $\overline{\text{BUSY}}$ outputs can be used. This is shown graphically in Figure 4.

1) The host sends a new command. The device sets $\overline{\text{BUSY}}$ low. The host monitors $\overline{\text{BUSY}}$ to determine when it goes high. The device then pulses $\overline{\text{LDAC}}$ low to update the DAC.
2) The host sends a new command. The device sets $\overline{\text{BUSY}}$ low. The host toggles $\overline{\text{LDAC}}$ low then high before $\overline{\text{BUSY}}$ goes high. The device latches the $\overline{\text{LDAC}}$ event but does not implement it until processing is complete. Then, $\overline{\text{BUSY}}$ goes high and the device updates the DAC.
3) $\overline{\text{LDAC}}$ is held low. The host sends a new command and the device sets $\overline{\text{BUSY}}$ low. The device updates the DAC when the processing is complete and $\overline{\text{BUSY}}$ goes high.
4) $\overline{\text{BUSY}}$ is pulled down externally to delay DAC update. The $\overline{\text{BUSY}}$ pin is bidirectional. To use $\overline{\text{BUSY}}$ as an input, set the $\overline{\text{NO\_BUSY}}$ bit to 1 using the 0x4 or 0xC command. When configured as an input, pulling $\overline{\text{BUSY}}$ low at least 50ns before the device releases the line delays DAC update. DAC update occurs only after $\overline{\text{BUSY}}$ is released and goes high. If used as an input, drive $\overline{\text{BUSY}}$ with an open-drain output with a pullup to V_{DDIO}.

If the DAC must be updated at a precise time with the least amount of jitter, use option 1.

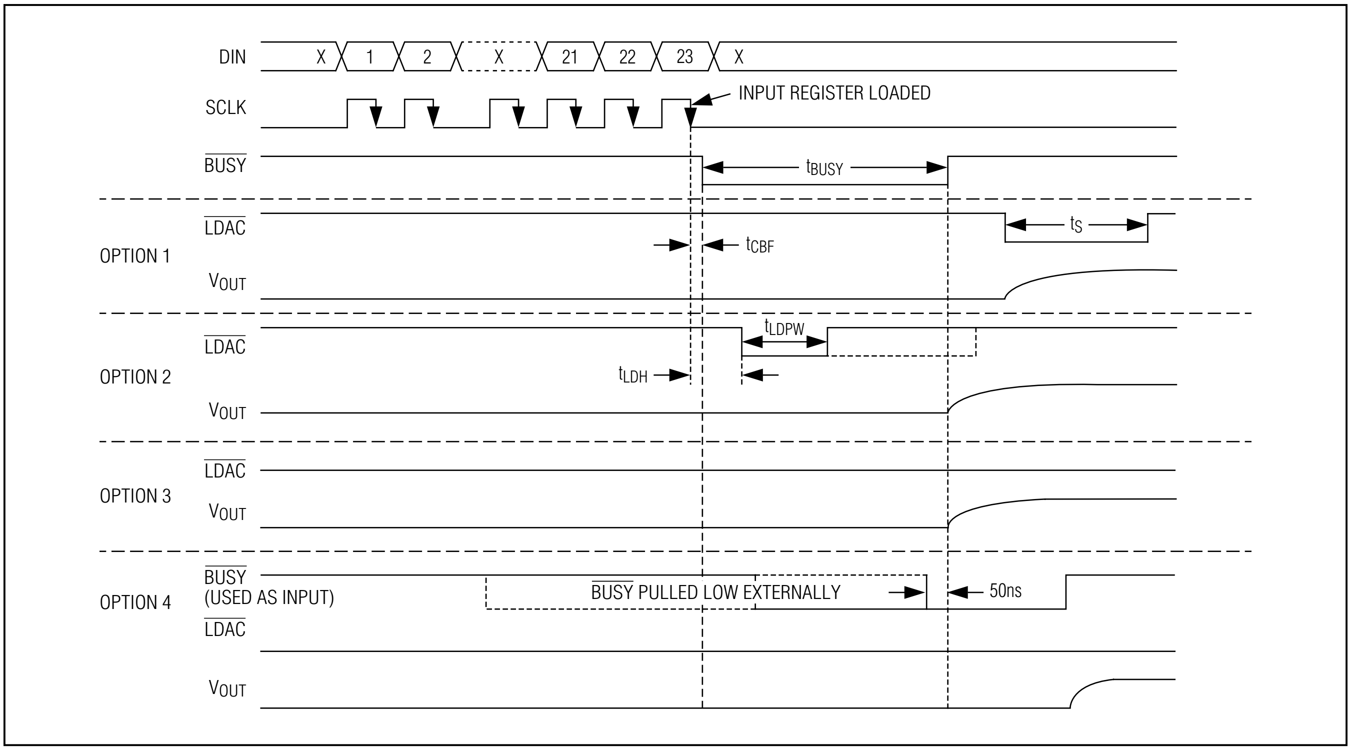


Figure 4. BUSY and LDAC Timing

Serial Interface

Overview

The SPI interface supports speeds up to 50MHz. When CS is high, the remaining interface inputs are disabled to reduce transient currents. The interface supports daisy chaining to enable multiple device to be controlled on the same SPI bus.

The device has a double-buffered interface consisting of two register banks: the input register and the DAC register. The input register for DIN is connected directly to the 24-bit SPI input shift register. The DAC latch contains the DAC code and is loaded as defined in the *LDAC and BUSY Interaction* section.

A valid SPI frame is 24-bit wide with 4-bit command R3 to R0, 16-bit data D15 to D0, and 4 unused LSBs. A full 24-bit SPI command sequence is required for all SPI command operations, regardless of the number of data bits actually used for the command. Any commands terminating with less than a full 24-bit sequence will be aborted without impacting the operation of the part (subject to t_{CSA} timing requirements). Data is not written into the SPI input register or DAC and it continues to hold the preceding valid data. If a command sequence with more than 24 bits is provided, the command will be executed on the 24th SCLK falling edge and the remainder of the command will be ignored.

All SPI commands result in the device assuming control of the DOUT line from the first SCLK edge through the 24th SCLK edge. After relinquishing the DOUT line, the MAX5316 will return to a high-impedance state. An optional bus hold circuit can be engaged to hold DOUT at its last bit value while not interfering with other devices on the bus.

DOUT is disabled at power-up and must be enabled through the SPI interface. When enabled, DOUT echoes the 4-bit command plus 16-bit data, which is being programmed. During readback, DOUT echoes the 4-bit command followed by the true readback data depending upon the type of read command. Table 4 shows the bit positions for DOUT and DIN within the 24-bit SPI frame.

The device is designed such that SCLK idles low, and DIN and DOUT change on the rising clock edge and get latched on the falling clock edge. The SPI host controller should be set accordingly.

Daisy-Chain SPI Operation Using $\overline{\text{READY}}$ Output

The $\overline{\text{READY}}$ pulse appears 24 clock cycles after the negative edge of $\overline{\text{CS}}$ as shown in Figure 5 and can therefore be used as the $\overline{\text{CS}}$ line for the next device in the daisy chain. Since the device looks at the first 24 bits of the transmission following the falling edge of $\overline{\text{CS}}$, it is possible to daisy-chain the device with different command word lengths. $\overline{\text{READY}}$ goes high after $\overline{\text{CS}}$ is driven high.

To perform a daisy-chain write operation, drive $\overline{\text{CS}}$ low and output the data serially to DIN. The propagation of the $\overline{\text{READY}}$ signal then controls how the data is read by the device. As the data propagates through the daisy chain, each individual command in the chain is executed on the 24th falling clock edge following the falling edge of the respective $\overline{\text{CS}}$ input. To update just one device in a daisy chain, send the no-op command to the other device in the chain. To update the first device in the chain, raise the $\overline{\text{CS}}$ input after writing to that device.

Because daisy-chain operation requires paralleling the DOUTs of all the MAX5316 in the chain, the NO_HOLDEN bit in register 0x4 or 0xC should be set to 1 for all devices. Doing so ensures that DOUT goes into high-impedance after the SPI frame is complete (i.e. after the 24th clock cycle) as shown in Figure 6.

Table 5. SPI Command and Data Mapping with Clock Falling Edges

CLOCK EDGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
DIN	R3	R2	R1	R0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
DOUT	0	R3	R2	R1	R0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X

Note that 'X' is don't care.

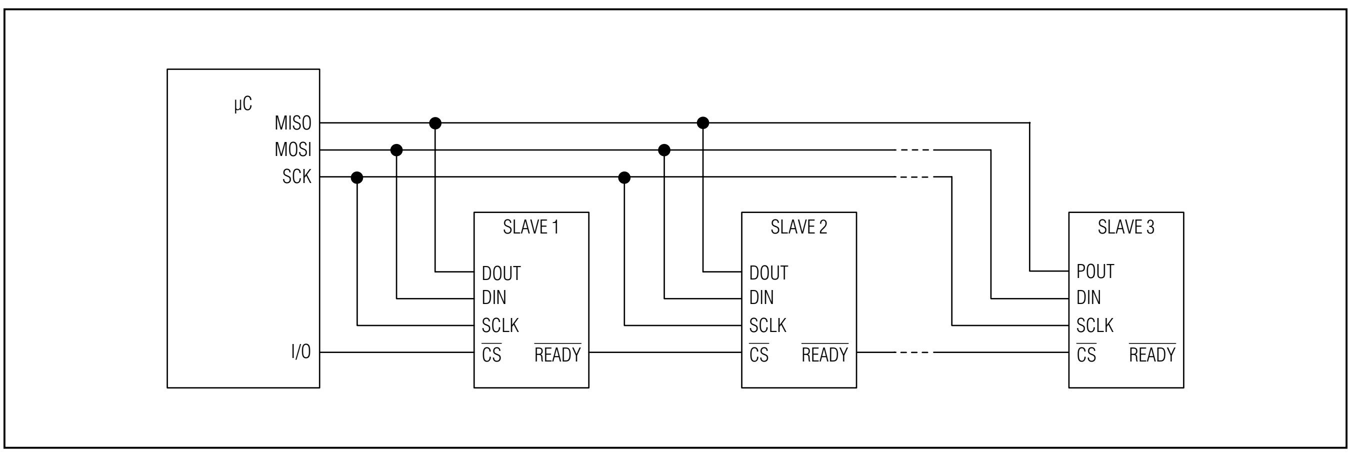


Figure 5. Daisy-Chain SPI Connection Terminating with a Standard SPI Device

Stand-Alone Operation

The diagram in Figure 7 shows a stand-alone connection of the MAX5316 in a typical SPI application. If more than one peripheral device shares the DOUT bus, the NO_HOLDEN bit in register 0x4 or 0xC should be set to 1 for the MAX5316. Doing so ensures that DOUT goes into high-impedance after the SPI frame is complete (i.e. after the 24th clock cycle).

Command and Register Map

All command and data registers have read and write functionality. The register selected depends on the command select bits R[3:0]. Each write to the device consists of 4 command select bits (R[3:0]), 16 data bits (which are detailed in Tables 7–11), and 4 don't care LSBs. A summary of the commands is shown in Table 6.

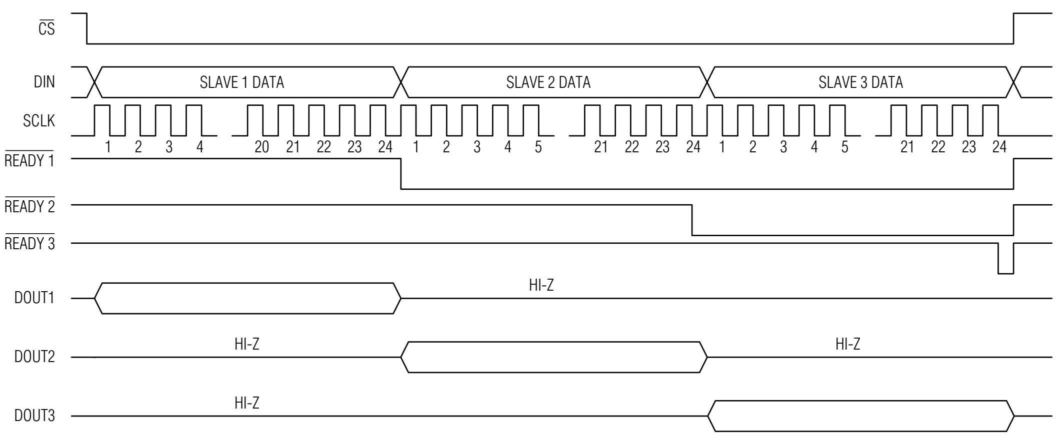


Figure 6. Daisy-Chain SPI Connection Timing

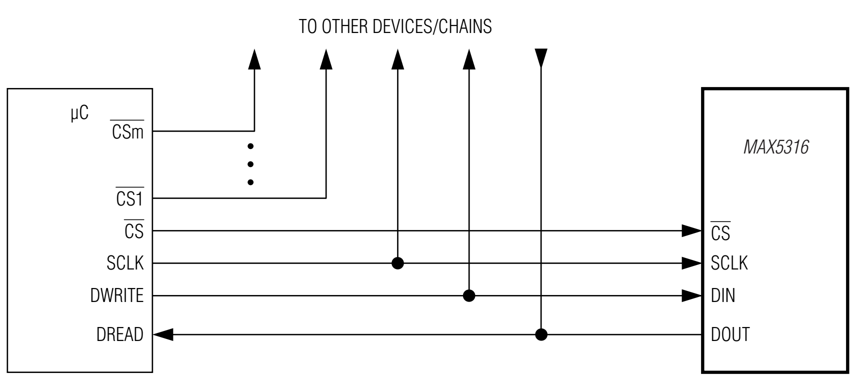


Figure 7. Stand-Alone Operation

Table 6. Register Map Summary

HEX	R3	R2	R1	R0	FUNCTION
0	0	0	0	0	No-op. Used mainly in daisy-chain communications.
1	0	0	0	1	DIN register write
2, 3, 5–8, A, B, D–F	—	—	—	—	Reserved
4	0	1	0	0	Configuration register write
9	1	0	0	1	DIN register read
C	1	1	0	0	Configuration and status register read.

Register Details

Table 7. No-Op Command (0x0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT	NAME	DESCRIPTION
15:0	Don’t care	No action on SPI shift register and DAC input registers. Use for daisy-chain purposes when R[3:0] = 0000.

Table 8a. Straight Binary DIN Write Register ($TC/\overline{SB}$ = 0) (0x1)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DEFAULT	0x0000 when $M\overline{Z}$ = DGND (zero scale) 0x8000 when $M\overline{Z}$ = V_{DDIO} (midscale)															

BIT	NAME	DESCRIPTION
15:0	B[15:0]	16-bit DAC input code in straight binary format. For clarity, a few examples are shown below. 0000 0000 0000 0000 0x0000 zero scale 0100 0000 0000 0000 0x4000 quarter scale 1000 0000 0000 0000 0x8000 midscale 1100 0000 0000 0000 0xC000 three-quarter scale 1111 1111 1111 1111 0xFFFF full scale - 1 LSB

Table 8b. Two's Complement DIN Write Register (TC/$\overline{\text{SB}}$) = 1) (0x1)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DEFAULT	0x8000 when M$\overline{\text{Z}}$ = DGND (zero scale) 0x0000 when M$\overline{\text{Z}}$ = V_{DDIO} (midscale)															

BIT	NAME	DESCRIPTION
15:0	B[15:0]	16-bit DAC input code in two's complement format. For clarity, a few examples are shown below. 1000 0000 0000 0000 0x8000 zero scale 1100 0000 0000 0000 0xC000 quarter scale 1111 1111 1111 1111 0xFFFF midscale – 1 LSB 0000 0000 0000 0000 0x0000 midscale 0000 0000 0000 0001 0x0001 midscale + 1 LSB 0100 0000 0000 0000 0x4000 three-quarter scale 0111 1111 1111 1111 0x7FFF full scale – 1 LSB

Table 9. General Configuration Write Register (0x4)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	PD_SW	NO_HOLDEN	$\overline{\text{RST\_SW}}$	$\overline{\text{NO\_BUSY}}$	DOUT_ON	X	X	X	X	X	X	X	X	X	X	X
DEFAULT	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X

BIT	NAME	DESCRIPTION
15	PD_SW	Software PD (Power-Down). Equivalent to the PD input. 0: Normal mode 1: Power-down mode. OUT is internally connected to AGND using a 2kΩ resistor.
14	NO_HOLDEN	SPI Bus Hold Enable. 0: Bus hold enabled for SPI DOUT output. DOUT stays at its last value after the SPI $\overline{\text{CS}}$ input rises at the end of the SPI frame (i.e. after the 24th clock cycle). 1: Bus hold disabled for SPI DOUT output. DOUT goes high impedance after the SPI $\overline{\text{CS}}$ input rises at the end of the SPI frame (i.e. after the 24th clock cycle).
13	$\overline{\text{RST\_SW}}$	Software Reset. Equivalent to the $\overline{\text{RST}}$ input. 0: Place device in reset 1: Normal operation Set the active low $\overline{\text{RST\_SW}}$ bit low to initiate a software reset (equivalent to pulling $\overline{\text{RST}}$ low)
12	$\overline{\text{NO\_BUSY}}$	$\overline{\text{BUSY}}$ Input Disable. 0: $\overline{\text{BUSY}}$ input is active. 1: $\overline{\text{BUSY}}$ input is disabled. Note that this does not affect the $\overline{\text{BUSY}}$ bit in the General Configuration and Status Register. The $\overline{\text{BUSY}}$ pin is bidirectional. When enabled, it can be pulled down externally to delay DAC updates.
11	DOUT_ON	SPI DOUT Output Disable. DOUT is disabled by default. 0: DOUT output disabled. When DOUT is disabled, the output is pulled low for the duration of the SPI frame. 1: DOUT output enabled.
10:0	—	Don't care. These bits are reserved for the corresponding read command.

Table 10. DIN Read Register (0x9)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
15:0	B[15:0]	16-bit DIN readback value stored in the bits B[15:0].

Table 11. General Configuration and Status Read Register (0xC)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	PD_SW	NO_ HOLDEN	$\overline{\text{RST\_SW}}$	$\overline{\text{NO\_BUSY}}$	DOUT_ON	$\overline{\text{BUSY}}$	X	X	X	X	X	X	REV_ID[3:0]			
DEFAULT	0	0	1	0	0	0	0	0	0	0	0	0	0001			

BIT	NAME	DESCRIPTION
15	PD_SW	Software PD (Power-Down). Equivalent to the PD input. 0: Normal mode. 1: Power-down mode. OUT is internally connected to AGND using a 2kΩ resistor.
14	NO_HOLDEN	SPI Bus Hold Enable. 0: Bus hold enabled for SPI DOUT output. DOUT stays at its final value after the SPI $\overline{\text{CS}}$ input rises at the end of the SPI frame. 1: Bus hold disabled for SPI DOUT output. DOUT goes high impedance after the SPI $\overline{\text{CS}}$ input rises at the end of the SPI frame.
13	$\overline{\text{RST\_SW}}$	Software Reset. Equivalent to the $\overline{\text{RST}}$ input. 0: Place device in reset. 1: Normal operation. Set the active low $\overline{\text{RST\_SW}}$ bit low to initiate a software reset (equivalent to pulling $\overline{\text{RST}}$ low).
12	$\overline{\text{NO\_BUSY}}$	$\overline{\text{BUSY}}$ Input Disable. 0: $\overline{\text{BUSY}}$ input is active. 1: $\overline{\text{BUSY}}$ input is disabled. Note that this does not affect the $\overline{\text{BUSY}}$ bit in the General Configuration and Status Register. The $\overline{\text{BUSY}}$ pin is bidirectional. When enabled, it can be pulled down externally to delay DAC updates.
11	DOUT_ON	SPI DOUT Output Disable. DOUT is disabled by default. 0: DOUT output disabled. When DOUT is disabled, the output is pulled low for the duration of the SPI frame. 1: DOUT output enabled.
10	$\overline{\text{BUSY}}$	Global $\overline{\text{BUSY}}$ status readback. 0: Device is busy transferring DIN code to the DAC register. 1: Device is not busy.
9:4	—	Reserved. Will read back 0.
3:0	REV_ID[3:0]	Device revision

Applications Information

Power-On Reset (POR)

Upon power-on, the output is set to either zero-scale (if $M/\overline{Z}$ is low) or midscale (if $M/\overline{Z}$ is high). The entire register map is set to their default values as shown in Tables 7–11.

Power Supplies and Bypassing Considerations

For best performance, use a separate supply for the MAX5316. Bypass V_{DDIO}, AVDD_, and AVSS with high-quality ceramic capacitors to a low-impedance ground as close as possible to the device. A typical high-quality X7R 10µF capacitor can become self resonant at 2MHz. Therefore, it is actually an inductor above 2MHz and is useless for decoupling signals above 2MHz. It is therefore recommended that several capacitors of different values are connected in parallel (e.g. 0.1µF II 10µF). Figure 8 shows the magnitude of impedance of typical 1µF, 100nF, and 10nF X7R capacitors. As the capacitance reduces, the self-resonant frequency increases. In addition, the parallel combination of all three is shown and exhibits a significant improvement over a single capacitor. These plots do not include any PCB trace inductance.

Minimize lead lengths to reduce lead inductance. Adding just 2nH trace inductance to each of the typical capacitors above produces the effects shown in Figure 9. This shows significant reduction in the self-resonant frequencies of the capacitors.

Internal Linear Regulator (BYPASS)

BYPASS is the output of an internal linear regulator and is used to power digital circuitry. Connect BYPASS to DGND with a ceramic capacitor in the range of 1µF to 10µF with ESR in the range of 100mΩ to 20mΩ to ensure stability.

Power-Supply Sequencing

During power-up, ensure that AVDD_ comes up before the reference does. If this is not possible, connect a Schottky diode between the REF and AVDD_ such as the MBR0530T1G. If REF does come up before AVDD_, the diode conducts and clamps REF to AVDD_. Once AVDD_ has come up, the diode no longer conducts. REF should always be below AVDD_ as specified in the *Electrical Characteristics*. AVDD_ and AVDD_ should be connected together and powered from the same supply.

V_{DDIO} and AVSS can be sequenced in any order. Always perform a reset operation after all the supplies are brought up to place the device in a known operating state.

Layout Considerations

Digital and AC transient signals on AGND inputs can create noise at the outputs. Connect both AGND inputs to form the star ground for the DAC system. Refer remote DAC loads to this system ground for the best possible performance (see the *Force/Sense* section).

Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane, or star connect all ground return paths back to AGND. Do not use wire-wrapped boards and sockets. Use ground plane

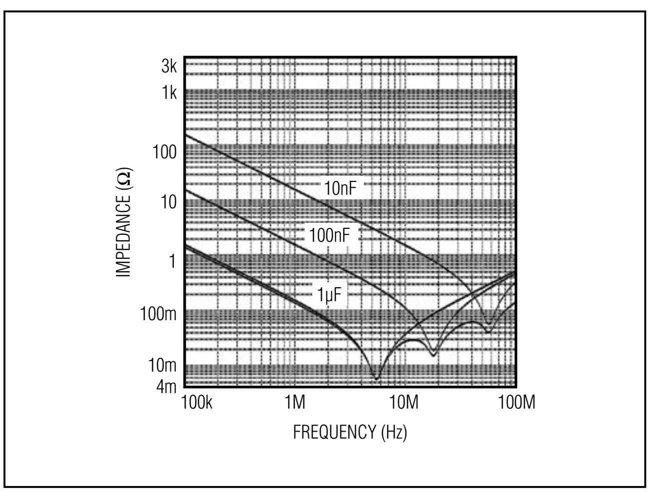


Figure 8. Typical X7R Capacitor Impedance

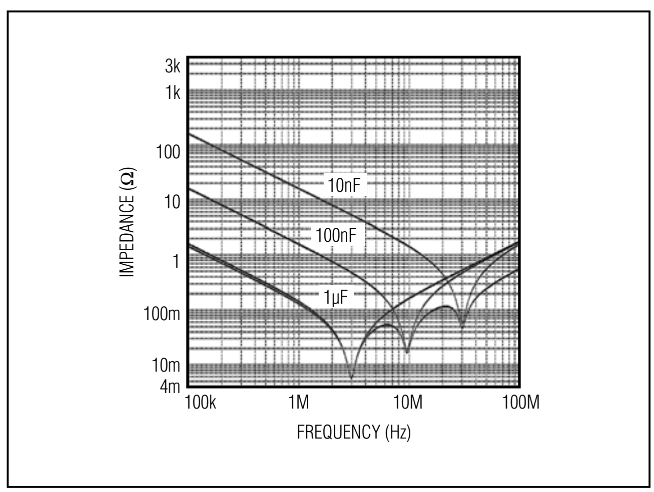


Figure 9. Typical X7R Capacitor Impedance with Additional 2nH PCB Trace Inductance

shielding to improve noise immunity. Do not run analog and digital signals parallel to one another (especially clock signals) and avoid routing digital lines underneath the device package. Connect the exposed pad to AGND (analog ground plane).

For a recommended layout, consult the MAX5316/MAX5318 Evaluation Kit datasheet.

Voltage Reference Selection and Layout

The voltage reference should be placed close to the DAC. The same power-supply decoupling and grounding rules as the DAC should be implemented. Many voltage references require an output capacitor for stability or noise reduction. Provided the trace between the reference device and the DAC is kept short and well shielded, a single capacitor may be used and placed close to the DAC. However, for improved noise immunity, additional capacitors may be used but be careful not to exceed the recommended capacitance range for the voltage reference.

Refer to Applications Note AN4300: *Calculating the Error Budget in Precision Digital-to-Analog Converter (DAC) Applications* for detailed description of voltage reference parameters and trading off the error budget. The MAX6126 is recommended for 16-bit applications.

Optimizing Data Throughput Rate

The *$\overline{\text{LDAC}}$ and $\overline{\text{BUSY}}$ Interaction* section details the timing of data written to the device and how the DAC is updated. Data throughput speed can be increased by overlapping the data load time with the busy period and settling time as shown below in Figure 10. Following the 24th SCLK falling edge, the device holds $\overline{\text{BUSY}}$ low while transferring the value from the DIN register to the DAC register. Providing that the $\overline{\text{LDAC}}$ falling edge arrives before the 24th SCLK falling edge, and assuming the SPI clock frequency is high enough, the throughput period is therefore limited by t_{BUSY} and settling times only. A slight further increase in throughput time can be gained by either toggling $\overline{\text{LDAC}}$ during the busy period or by pulling it low permanently. However, the exact point at which the DAC update occurs is then determined internally as indicated by the $\overline{\text{BUSY}}$ line rising edge. This is not an exact time.

$\overline{\text{BUSY}}$ Line Pullup Resistor Selection

The $\overline{\text{BUSY}}$ pin is an open-drain output. It therefore requires a pullup resistor. A 5.1kΩ value is recommended as a compromise between power and speed. Stray capacitance on this line can easily slow the rise time to an unacceptable level. The $\overline{\text{BUSY}}$ pin can sink up to 5mA. Therefore a resistor as low as V_{DDIO}/0.005 may be used if faster rise times are required.

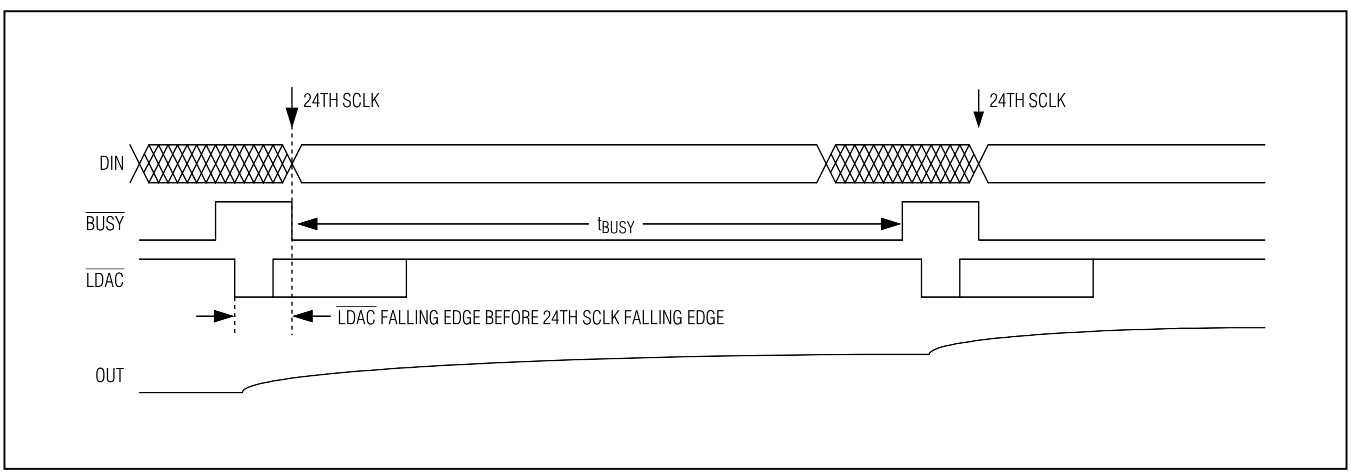


Figure 10. Optimum Throughput with Stable Update Period

Producing Unipolar High-Voltage and Bipolar Outputs

Figure 11 and Figure 12 show how external op amps can be used to produce a unipolar high-voltage output and a bipolar output

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the measured transfer function from a straight line drawn between two codes. This line is drawn between the zero and full-scale codes of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step height and the ideal value of 1 LSB. If the magnitude of the DNL is less than or equal to 1 LSB, the DAC guarantees no missing codes and is monotonic.

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. Typically, the point at which the offset error is specified is at or near the zero-scale point of the transfer function.

Gain Error

Gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after removing the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Settling Time

The settling time is the amount of time required from the start of a $\overline{\text{LDAC}}$ high-to-low transition or $\overline{\text{BUSY}}$ low-to-high transition (whichever occurs last), until the DAC output settles to within 0.003% around the final value.

Digital Feedthrough

Digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

Digital-to-Analog Glitch Impulse

The glitch impulse occurs at the major carry transitions along the segmented bit boundaries. It is specified as the net area of the glitch impulse which appears at the output when the digital input code changes by 1 LSB. The glitch impulse is specified in nanovolts-seconds (nV-s).

Digital-to-Analog Power-Up Glitch Impulse

The digital-to-analog power-up glitch is the net area of the glitch impulse which appears at the output when the device exits power-down mode.

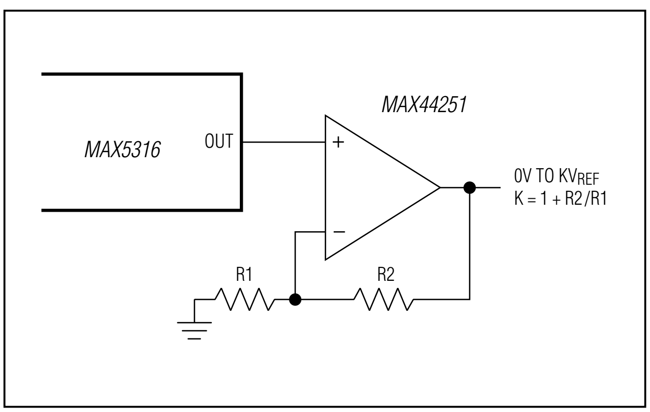


Figure 11. Unipolar High-Voltage Output

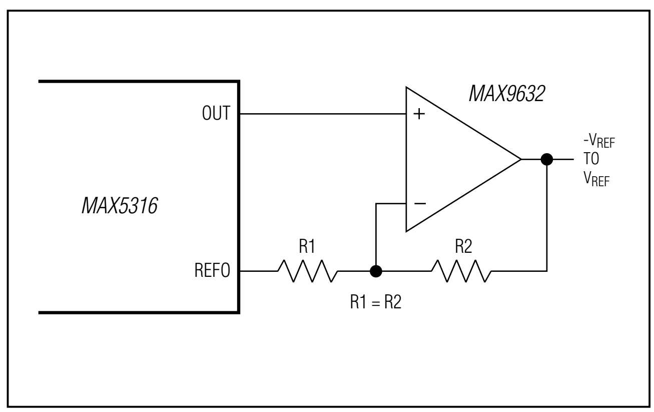
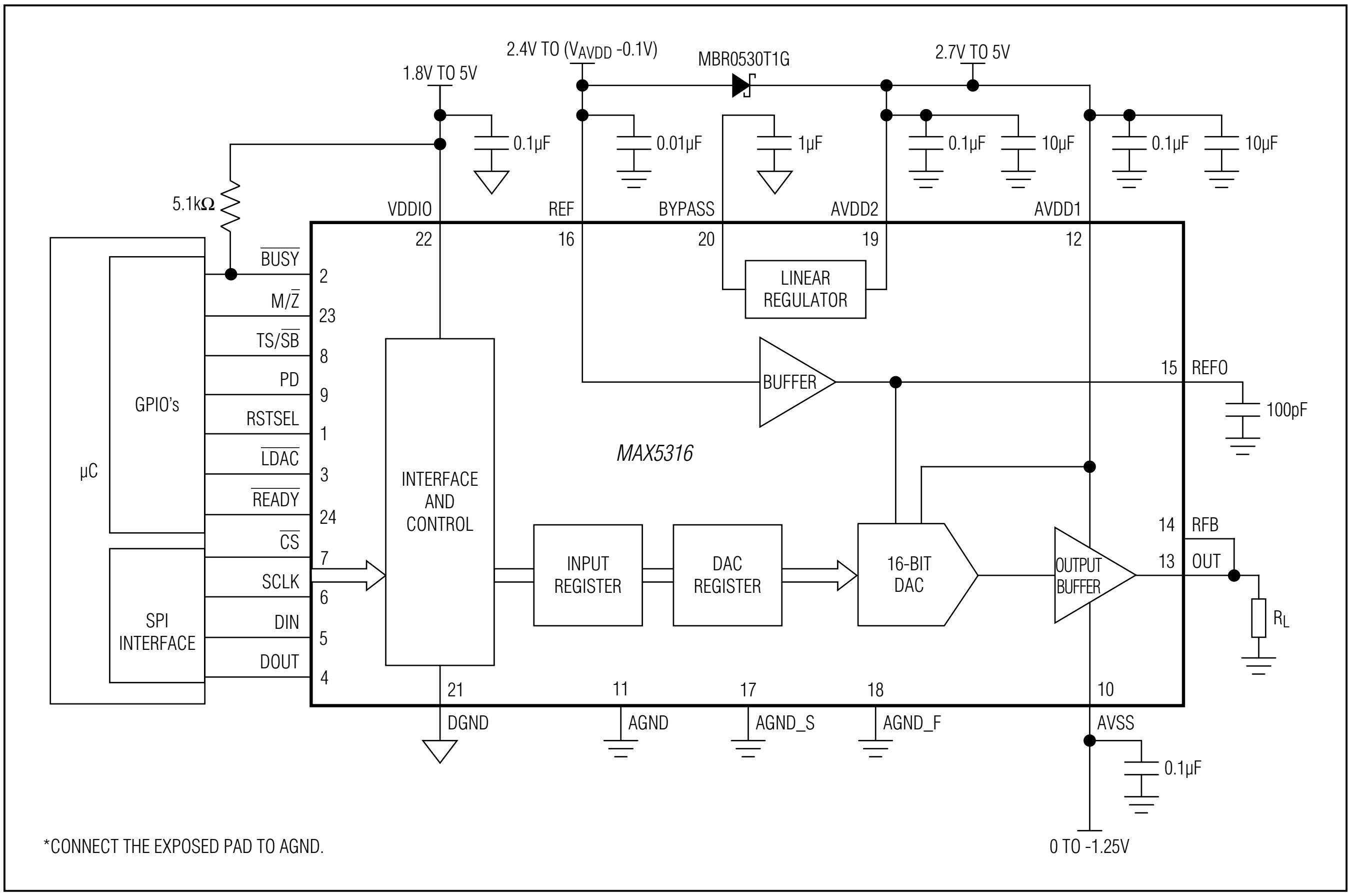


Figure 12. Bipolar Output

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5316GTG+	-40°C to +105°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2445+1	21-0201	90-0083

16-Bit, ±1 LSB Accuracy Voltage Output DAC with SPI Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/12	Initial release	—